Memory Interfacing

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Objectives

> **After completing this module, you will be able to:**

- Identify memory resources for the Zynq SoC
- Describe the various off-chip memory technologies available
- Describe the external memory device interfaces
- Describe the waveform timing for memory device signals
- List some the features of the PS's static memory controller (SMC) in the Zynq SoC
- Configure AXI_EMC
- Describe the operation of dynamic RAM memory

Outline

- *Introduction*
- Static Memory Controllers
- Dynamic Memory Controllers
- Summary

Various Memory Technologies

- **Static**
  - Block RAM
  - LUT (Distributed RAM)
  - Asynchronous static RAM
    - No clock associated; uses Chip Enable (CE), Output Enable (OE), and Write Enable (WE) as control signals
  - Synchronous static RAM
    - Has a clock, uses CE, OE, and WE as enables
- **Flash memory (also older ROM, EPROM, and EEPROM)**
  - Non-volatile, fast read, slow write
- **Dynamic**
  - Requires refresh cycles
    - DRAM, SDRAM
    - DDR, DDR2, DDR3

Memory Interfaces on Zynq

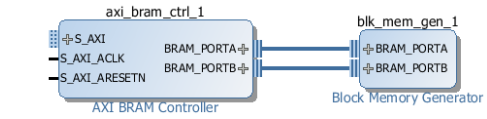
- **On-chip memory (OCM)**
- **Dynamic RAM memory controller (DMC)**
- **Static memory controller (SMC)**
- **Linear Quad SPI flash controller (QSPI) (part of IOP)**
- **SD/SDIO controller (part of IOP)**
- **The above are in addition to the PL memory features**
  - Block RAM
  - LUT RAM
  - Programmable logic-based memory controllers

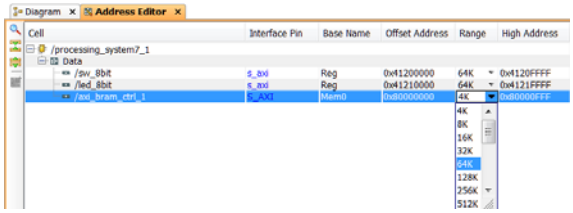
BRAM Controller for Zynq

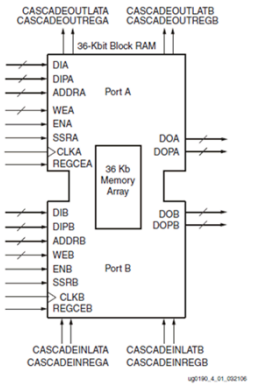
- **axi_bram_ctlr**
  - AXI Interface
  - Memory controller does not include block RAM
  - Must instantiate a block RAM structure
    - bram_block
    - Automatically added if the axi_bram_ctlr is connected to the processor system
- **Size of block RAM block determined in the Addresses tab of the IP Integrator Block Diagram editor**
- **Netlist Generator generates the memory structure accordingly**

AXI BRAM Controller Usage Example

- By default, the controller includes both ports
- By default, when the block RAM is added only one port is included
- Configure the block RAM as True Dual Port RAM
- Size determined in the Addresses tab

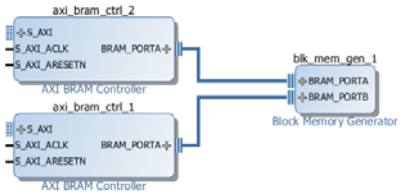


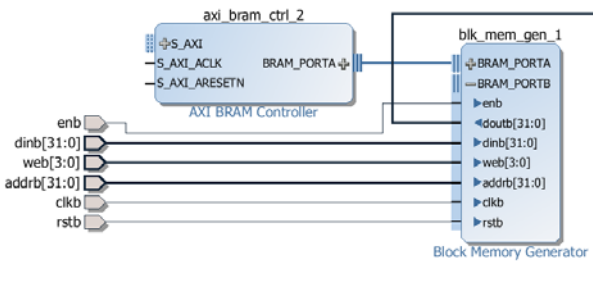




Sharing Block Memory

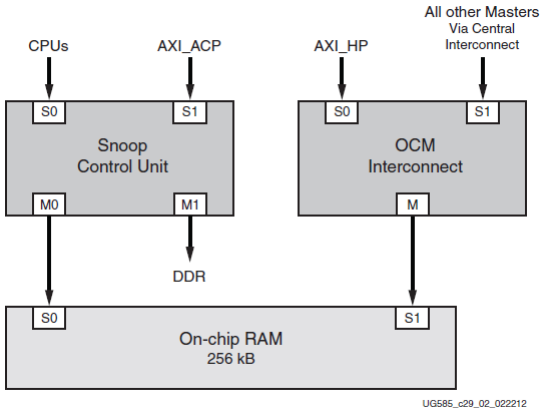
- Two memory controllers can share a block RAM
- Connect in the Block Diagram editor
- Typically used to
  - Share memory between instruction and data side buses
  - Share memory between processors
  - Share memory between a processor and external logic





OCM in Zynq

- **On-chip 256KB RAM**
- **On-chip 128KB ROM (not accessible to user)**
- **Two AXI 3.0, 64-bit slave connections**
  - One dedicated for CPU use via PS central interconnect
  - One for general use by other masters via PS interconnect to PL
- **Low-latency path for CPU reads to OCM**
- **Random access supported to OCM RAM from AXI masters**



OCM in Zynq

- **OCM RAM is divided into four 64KB blocks**
- **Each block is map-able to a specific range in either high or low memory**
  - Selected in SLCR registers
    - 0x0000_0000 to 0x0003_FFFF
    - 0xFFFC_0000 to 0xFFFF_FFFF
    - Movable in 4 independent 64K blocks
    - SLCR register set must be "unlocked" before modifying the specific registers and "locked" after modification
  - Address map "holes" are created depending on how the OCM is mapped
    - Different for Cortex-A9 processor (APU) access vs other masters
- **Linux typically uses DDR in low memory and OCM is moved to high memory**

Static Memory Controllers

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Flash Memory (Non-volatile)

- **Referred to in the industry as** NAND flash
- **Very inexpensive**
- **Include built in controllers to manage the array**
  - Still requires an external controller to operate the protocol
    - External control protocol formats go from simple to complex
  - Serial and parallel protocols
- **Technology includes**
  - Compact flash (CF)
  - SD card
  - USB
  - SPI

Compact Flash

SD Card

USB

SPI

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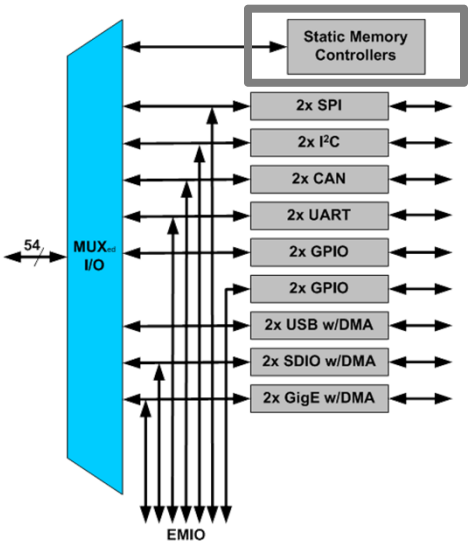
Static Memory Controllers (SMC)

- **The SMC is actually two controllers in one functional block**
  - The NAND memory interface supports NAND flash with multiplexed address and data buses
  - The parallel port interface supports
    - Asynchronous SRAM
    - NOR flash
    - NAND flash devices with an SRAM interface
- **The SMC allows all PS and PL masters to access NAND flash and parallel access-based memories through its AXI slave interface**



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SMC Features

- **Key features of the parallel (SRAM/NOR) interface**
  - Supports 8-bit data width for parallel port interface
  - Supports up to 25 address bits
  - Supports two chip select lines
  - 16-word deep read data and write data FIFO
  - Eight-word deep command FIFO
  - Supports programmable cycle timing per chip select
  - Supports asynchronous mode operation
- **Key features of the NAND flash**
  - Supports 8-bit or 16-bit data width for the NAND interface
  - Single chip select line
  - Meets ONFI (Open NAND Flash Interface) Specification 1.0

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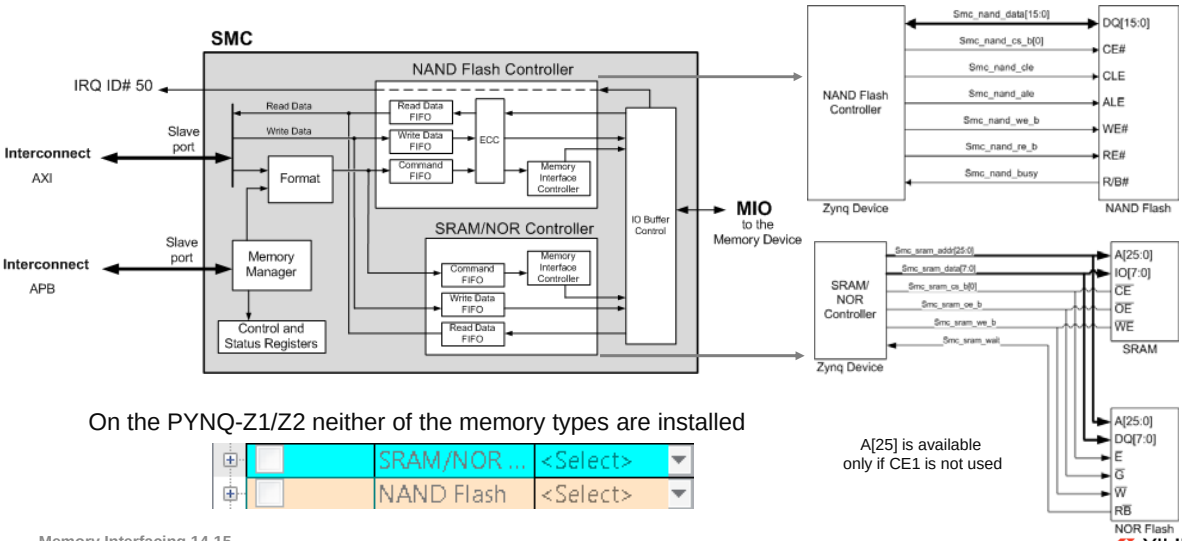
SMC Block Diagram

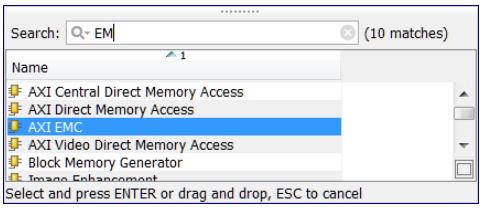


On the PYNQ-Z1/Z2 neither of the memory types are installed

A[25] is available only if CE1 is not used

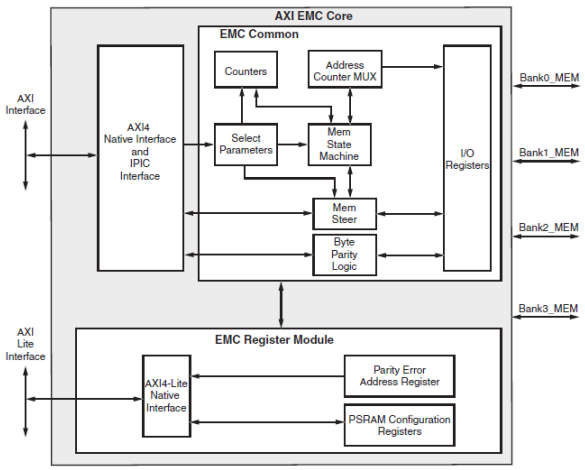
External Memory Controller – AXI_EMC

- **Memory support**
  - Asynchronous or synchronous, static or flash and PSRAM/Cellular RAM
  - Up to four memory banks
  - Memory data widths 8 bit, 16 bit, 32 bit, and 64 bit
  - Programmable memory device timing
- **Interconnect support**
  - 32-bit and 64-bit AXI interface
  - Single beat and burst
  - Narrow and unaligned transfer support
- **AXI4 support**
- **AXI4-Lite support to internal control registers**



AXI_EMC Block Diagram

- **Three main interfaces:**
  - Memory device interface
  - AXI Full Interface
  - AXI Lite Interface



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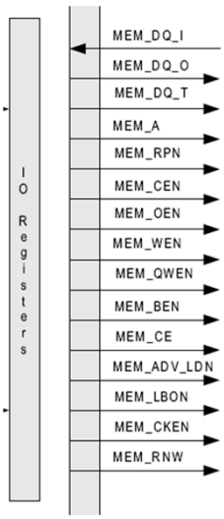
AXI_EMC External Interface

- **All signals are clocked through IOB flops**
  - Optional positive or negative edge
- **The rich signal set will accommodate most memory device interfaces**
  - Byte to quad word data size
  - Up to four banks with multiple devices per bank
  - Multiple byte enables
  - Page mode
  - Synchronous or asynchronous type devices
  - Not all signals need to be used; depends on device needs



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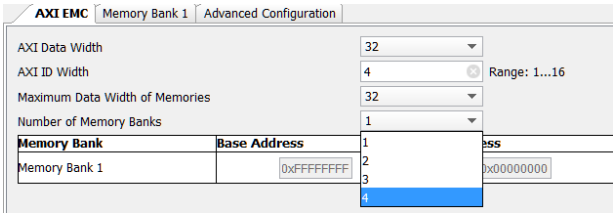
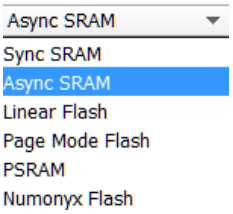
Configuring AXI_EMC

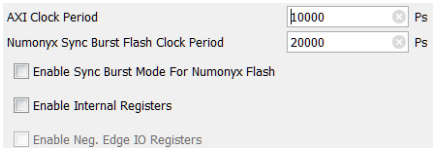
- **Configuration areas**
  - Memory device
    - Number of banks
    - Required signals
    - Waveform timing setup for each bank
  - AXI4 full interface
    - AXI4 full interface for memory access
  - AXI4-Lite interface
    - AXI4-Lite interface, optional for register and control logic
  - Configurable maximum data width
    - 32-bit
    - 64-bit





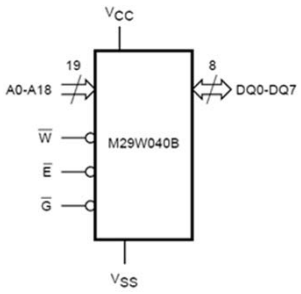
Advanced Configuration Parameters

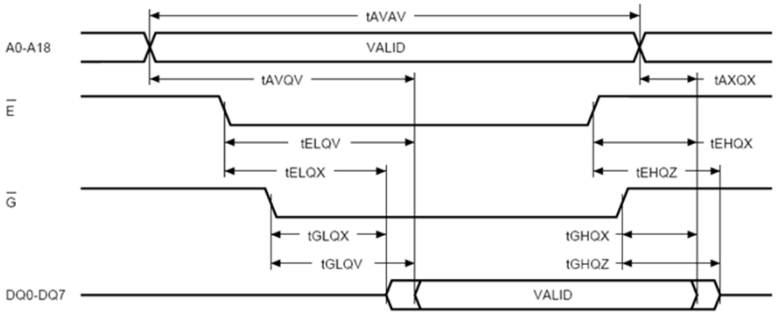
- **Advanced parameters set up**
  - Falling edge I/O uses another pipeline flop; helps with PCB timing
    - Sync SRAM mode
  - Enable optional AXI internal registers over AXI Lite interface
    - SRAM, PSRAM, Linear Flash and Numonyx used in Synch Burst mode



Memory Timing Diagram

- **Most memory devices are parameterized the same**
  - Nomenclature is different among manufacturers
  - This is the source for confusion
- **Careful examination of waveforms is necessary**





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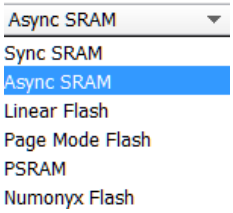
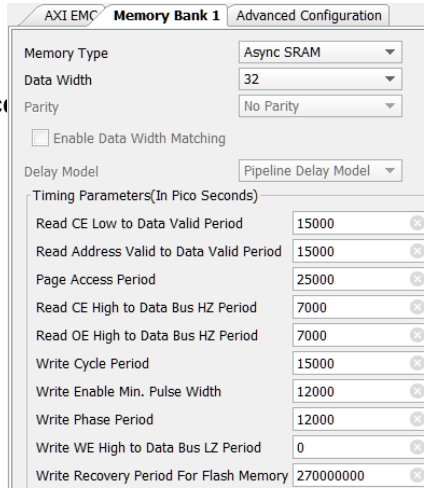
Timing Parameters

- **Each memory bank has its own timing**
  - Allows for different memory device technologies to hang
- **These settings are dependent on the memory devic**
  - Necessary to reference the memory data sheet to setup





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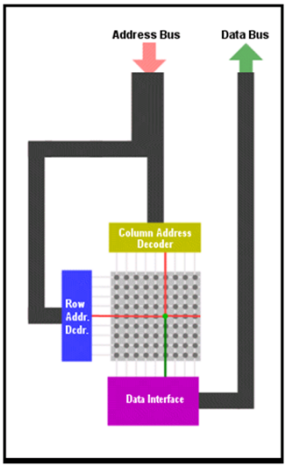
Dynamic Memory Controllers

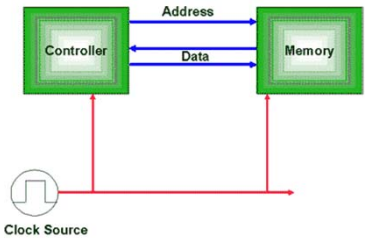
Dynamic RAM

- **Always external**
- **Volatile storage technology only**
  - Requires a periodic refresh to maintain its data
- **Single Data Rate**
  - DRAM, SDRAM
- **Double Data Rate**
  - DDR, DDR2, DDR3
- **The address bus carries both row and column addresses**
  - Identified by RAS and CAS signals
- **Data widths of 8, 16, 32, and 64 bits**
- **Memory size**
  - [(2**(Row Address+Column address)) x # of Banks * Bank data width] bits



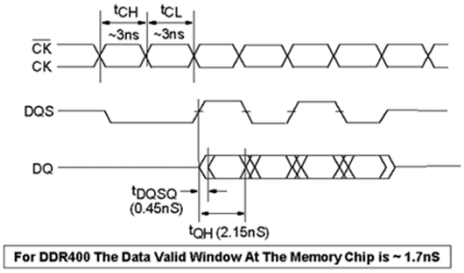
Single Data Rate Dynamic Memory (SDRAM)

- **Introduction of a clock pin to the SRAM**
  - Facilitates design timing considerations
  - Necessary for faster DRAM timing
  - Aids in synchronous design practices
- **Single data rate refers to rising edge clocking**
- **Pipelined memory access**
- **Memory access time is measured with CAS latency in clock cycles**
- **Data mask control (DQM) line**
- **Performance up to 150 MHz**



Double Date Rate Dynamic Memory (DDR)

- **Data is transferred on both clock edges**
  - Twice as fast as equivalent SDRAM
- **DDR clock rates up to 200 MHz**
- **Introduced memory banks**
  - Similar to extended address lines
  - Each bank can have a separate row
  - Facilitates faster access to random addresses
- **DQS signal to strobe data to and from controller**

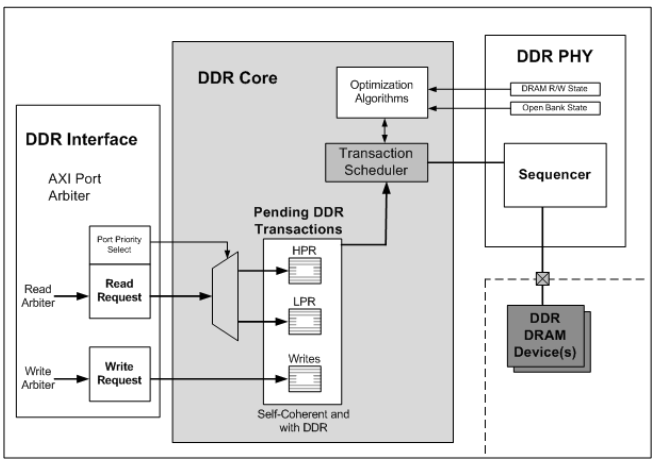


DDR2 and DDR3 Dynamic Memory

- **Faster clocking (data rate is double the clock rate)**
  - 533 MHz for DDR2
  - 800 MHz for DDR3
- **Shortened page size for reduced activation power**
- **Burst lengths of four and eight for improved data bandwidth capability**
  - Minimum read latency of four clock cycles
- **Eight banks in 1-GB densities and above**
- **Intelligent interface for timing calibration**

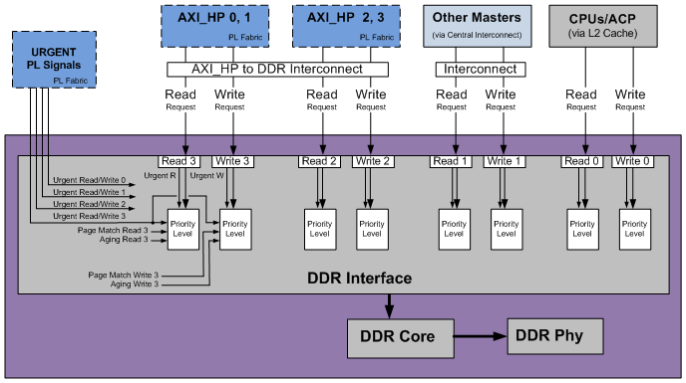
Dynamic Memory Controller (DMC) Block Diagram

- **DDR memory interface of PS**
  - Supports LPDDR2, DDR2, and DDR3
    - Up to 400 MHz for low-power LPDDR2
    - Up to 400 MHz for DDR2
    - Up to 533 MHz for DDR3
  - 73 dedicated pins for the DDR interface
  - Configurable 16-bit and 32-bit external DDR data bus width
  - 64-deep read/write acceptability buffer
  - ECC support for 16-bit data width only
- **Four AXI interfaces**



DMC PS Interface

- **Four ports**
  - One from CPU block
  - One from the Central interconnect
  - Two from the PL AXI HP to DDR interconnect



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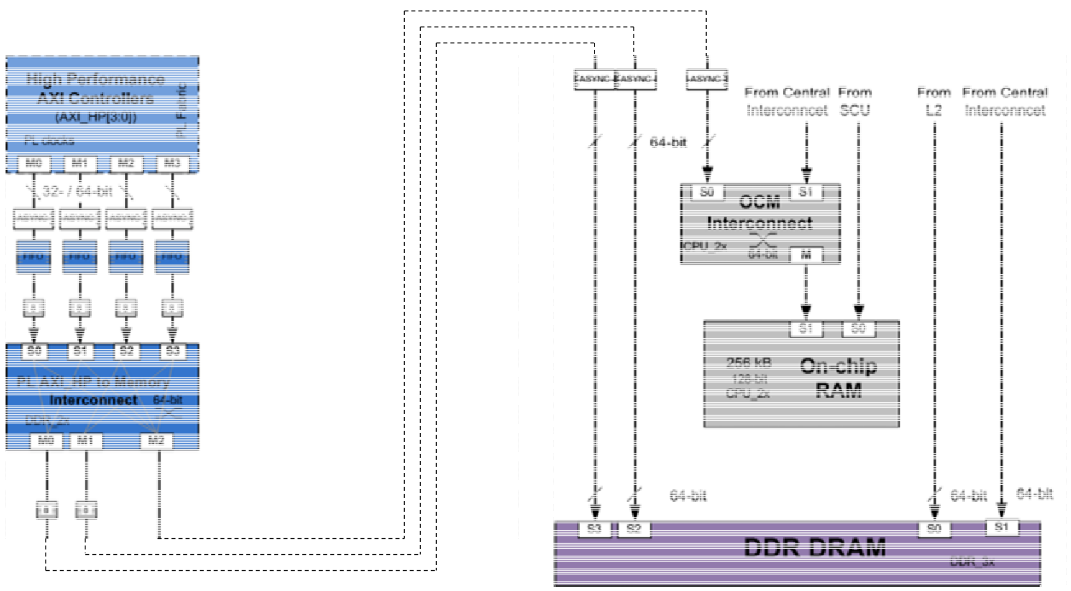
PL Interface to PS Memory Subsystem



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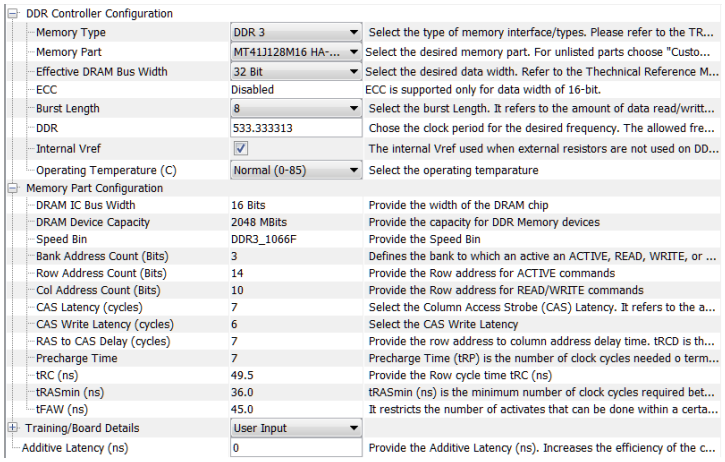
Supported External DDR Memory Types

Tech	Density (Mb)	Width	Speed
LPDDR2	128, 256, 512, 1024	x16, x32	400
DDR2	256, 512, 1024, 2048, 4096	x16, x32	400, 533, 667, 800
DDR3	1024, 2048, 4096, 8192	x16, x32	800, 1066

PS7 DDR Configuration

- **PS7 DDR Configuration**
  - Supports memory types
    - LPDDR2
    - DDR2
    - DDR3
  - Select the memory part or customize
  - Select the DRAM bus width
  - Set the operating frequency (MHz)
  - Advanced configuration: operating temperature, DQS to clock delay (ns), board delay (ns)



Best Case Latencies

- **Processing system**
  - CPU at 667 MHz
  - DDR at 533 MHz
  - Programmable logic is running at 150 MHz
- **Latency in terms of CPU clock cycles**
  - S_AXI_HP at 76 CPU cycles is 17 cycles for the PL (114 ns)

	L1 Cache	L2 Cache	DDR	OCM	IOP Slave	M_AXI_GP0
CPU Pipeline	1	25	67	20	122	86
Peripheral Master	–	–	136	106	–	126
S_AXI_ACP	27	32	89	27	124	–
S_AXI_HP0	–	–	76	46	–	–
S_AXI_GP0	–	–	118	88	144	–

Memory Performance

- **System configuration**

PL AXI	CPU_6x_4x	CPU 2x	DDR_3x	DDR_2x	DDR
150 MHz	675 MHz	225	525	350	DDR3 – 32

- **Memory utilization – 4 HP ports, burst of 16**

Access Type	Address Pattern	Efficiency (%)
Reads	Sequential	97
Reads	Random	92
Writes	Sequential	90
Writes	Random	87
Reads and Writes	Sequential	87
Reads and Writes	Random	78

Summary

Summary

- **There are various kinds of memories in use and Vivado has memory controllers for most of them**
- **Dual-ported block RAM allows sharing of memory between**
  - Two processor buses
  - Processor bus and programmable logic
- **A block RAM port is made accessible to programmable logic by making the one of the ports external to the processing system**
- **On-chip memory (OCM) provides ROM and RAM used for boot operations**
- **The SMC in the PS supports**
  - Asynchronous SRAM
  - NOR flash
  - NAND flash devices

Summary

- **AXI_EMC is used with static or flash memory technologies**
- **Up to four memory banks are supported**
  - Each can be different size (data/address bus) and technology
  - Separate base and high addresses
  - Each bank timing is programmable and independent
- **AXI4 full interface for memory operation and optional AXI4-Lite connection for controller register access**
- **Support for industry-standard static memory devices**
  - Synchronous and asynchronous
  - Page mode
  - Flexible byte enables

Summary

- **Dynamic RAM is the most popular and cost-effective memory technology**
- **The DMC supports 16-bit and 32-bit DDR memory devices**
- **DRAM operational complexity requires a controller**
  - Multiplexed address lines
  - Burst mode support
  - Datapath timing calibration
  - Aggressive timing closure
- **DDR is connected to the dedicated pins hence LOC constraints are required**
- **Four high-performance AXI FIFO interface ports (S_AXI_HPx) facilitate high-performance PL interface to the DDR memory**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