Lab2 Intro
Debugging Using Vivado Logic Analyzer

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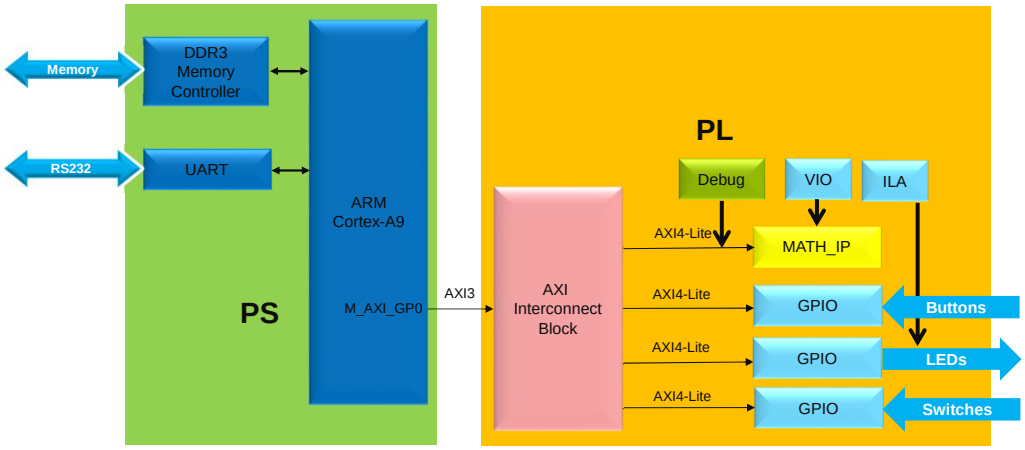
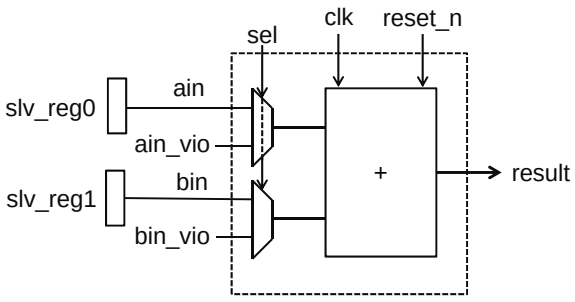
Introduction

- Software and hardware interact with each other in an embedded system.
- The XSDK includes System Debugger as software debugging tool.
- The Vivado logic analyzer tool allows for hardware debugging by providing access to the internal signals, using number of cores, without necessarily bringing them out via the package pins using several types of cores.
- These cores may reside in the programmable logic (PL) portion of the device and can be configured with several modes that can monitor signals within the design.
- Vivado provides capabilities of marking any net at several stages of the design flow. In this lab you will be introduced to various debugging cores.

ARM Cortex-A9 based Embedded System Design Debugging using Logic Analyzer Cores and Mark Debug



The Custom IP – MATH_IP



Procedure

- Open lab1 Vivado project and save as lab2
- Add the provided custom IP
- Add the VIO and ILA cores
- Synthesize the design and assign the S_AXI nets for debugging
- Generate the bitstream
- Generate the application in the XSDK
- Test and debug in design in hardware

Summary

- In this lab, you added a custom core with extra ports so you can debug the design using the VIO core.
- You instantiated the ILA and the VIO cores into the design.
- You used Mark Debug feature of Vivado to debug the AXI transactions on the custom peripheral.
- You then opened the hardware session from Vivado, setup various cores, and verified the design and core functionality using XSDK and the logic analyzer.
- Finally, you carried out cross triggering between hardware and software.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