Low Latency High Bandwidth Transfer

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Objectives

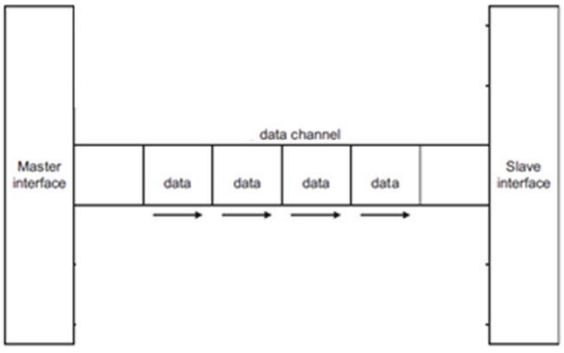
- **After completing this module, you will be able to:**
  - Identify the signals on the AXI streaming interface
  - List some of the features of the AXI FIFO Memory Map to streaming component
  - List the AXI bridge components and describe when to use them
  - Describe the differences between AXI CDMA, DataMover and DMA components
  - List the operational features of the Zynq SoC PS DMAC

Outline

- *Introduction*
- AXI Bridges
- PS DMA
- PL DMA
- Summary

Streaming Concept

- **Data moves in a single direction from a master to a slave**
  - Simplex communication
  - Dual direction would be dual simplex
    - individual channels in each direction
- **Data only**
  - No address bus
  - Minimum control lines
- **Data interpretation**
  - Packet or no packet
  - Master and slave must have prior knowledge of data format
  - Optional use of hardware signaling



AXI Streaming Advantages

- **No need to learn new bus architectures to build a hardware interface**
- **Saves clock cycles—faster than a bus interface**
  - Eliminates bus signaling overhead
    - No arbitration
    - No address decode
    - No acknowledge cycles
  - Decoupled data clock from CPU allows for asynchronous operation
- **Control bits limit need for a complex interrupt structure**
- **AXI port standard promotes design reuse**

AXI Streaming Signals

- **More signals defined than typically required**
- **Required signals**
  - ACLK
  - TDATA
- **Special, user-defined sideband signals consist of TUSER**
- **Other popular and useful signals are**
  - TVALID
  - TREADY
  - TLAST

Signal	Source	Description
ACLK	Clock source	The global clock signal. All signals are sampled on the rising edge of **ACLK**.
ARESETn	Reset source	The global reset signal. **ARESETn** is active-LOW.
TVALID	Master	**TVALID** indicates that the master is driving a valid transfer. A transfer takes place when both **TVALID** and **TREADY** are asserted.
TREADY	Slave	**TREADY** indicates that the slave can accept a transfer in the current cycle.
TDATA[(8n-1):0]	Master	**TDATA** is the primary payload that is used to provide the data that is passing across the interface. The width of the data payload is an integer number of bytes.
TSTRB[(n-1):0]	Master	**TSTRB** is the byte qualifier that indicates whether the content of the associated byte of **TDATA** is processed as a data byte or a position byte.
TKEEP[(n-1):0]	Master	**TKEEP** is the byte qualifier that indicates whether the content of the associated byte of **TDATA** is processed as part of the data stream. Associated bytes that have the **TKEEP** byte qualifier deasserted are null bytes and can be removed from the data stream.
TLAST	Master	**TLAST** indicates the boundary of a packet.
TID[(i-1):0]	Master	**TID** is the data stream identifier that indicates different streams of data.
TDEST[(d-1):0]	Master	**TDEST** provides routing information for the data stream.
TUSER[(u-1):0]	Master	**TUSER** is user defined sideband information that can be transmitted alongside the data stream.

AXI Streaming Interface Design Techniques

- **The datapath should be serial, as opposed to block, of word width to facilitate FIFO usage**
- **Use of pipeline registers to maintain a high clock rate—clock period vs. system latency**
- **Use multiple AXI streaming channels and control bits**
  - AXI streaming data channel
  - TVALID/TREADY as fabric FIFO flags
  - TLAST for framing and packets
- **Consider design reuse for next project**
- **Use AXI streaming exceptions to trap for control operations**

System Considerations

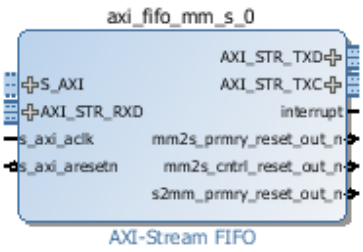
- **Use FIFOing type logic functions**
- **Deterministic hardware/software latency**
  - Control application hardware data rate and software loop timing so that FIFO does not empty or fill
    - A FIFO that empties indicates that the data rate could be increased
    - A FIFO that goes full indicates data overrun and loss—tighten up the software loop code or adjust the data rate
  - Select FIFO size base on the burst nature of data rate; just large enough to ensure that FIFO will not overflow
  - Synchronization between hardware and software
  - Data pipeline, starting up, and ending (fill and flush)

System Considerations

- **Limit interrupt usage—there is high overhead for context switching**
  - Use AXI streaming TLAST signal instead
- **Keep software loop access to AXI streaming tight**
  - Avoid subroutine or device driver calls to AXI streaming instructions
- **Most systems require asynchronous clocking**
  - Xilinx block RAM FIFOs can be used as instruments to cross clock boundaries
- **Consider system latency in both hardware and software when evaluating real-time performance**

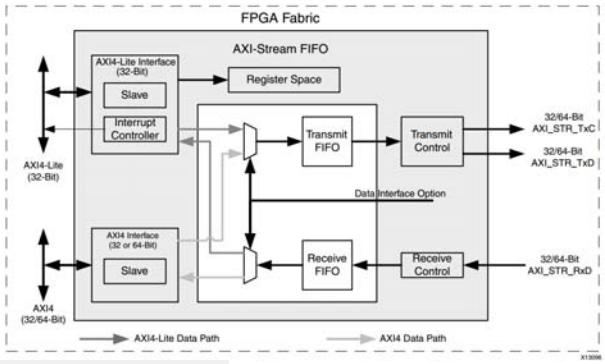
AXI FIFO Memory Map to Streaming

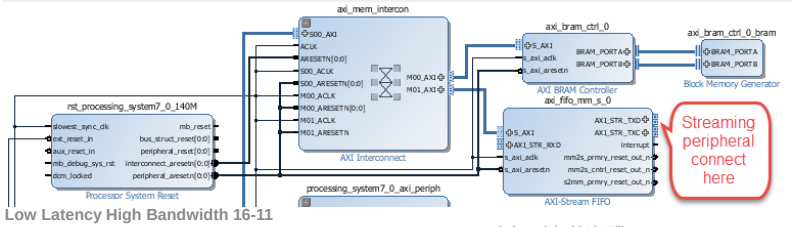
- **General AXI interconnect has no support for the AXI stream interface**
  - axi_fifo_mm_s provides this facility
  - FIFO included
- **Added as all other types of IP from the IP Catalog**
- **Features**
  - AXI4/AXI4-Lite slave interface
  - Independent internal 512B-128KB TX and RX data FIFOs
  - Full duplex operation
  - Supports AXI Ethernet basic mode only



AXI-Stream FIFO
axi_fifo_mm_s

- **Slave AXI connection**
  - RX/TX FIFOs
  - Interrupt controller
  - Control registers
- **Three user-side AXI Stream interfaces**
  - TX data
  - RX data
  - TX control





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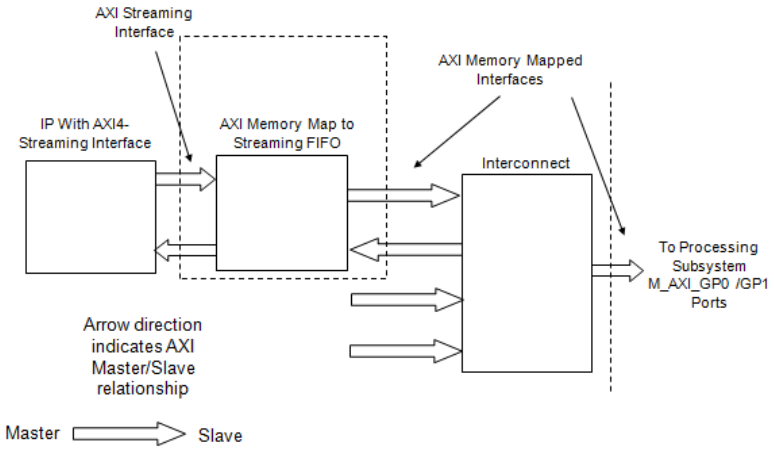
AXI Streaming FIFO Use Case



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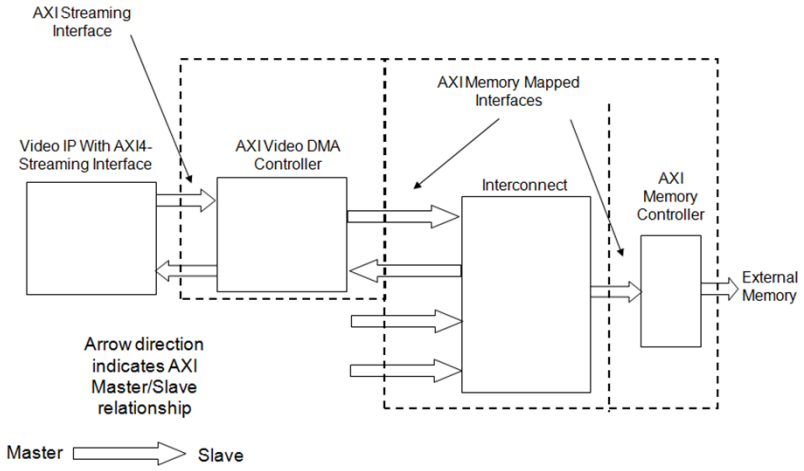
AXI-Streaming Video Solution



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Zynq SoC AXI PS-PL Interfacing

- **In the Zynq SoC, PS-PL interfacing is accomplished with nine AXI ports**
  - Two general-purpose master ports
  - Two general-purpose slave ports
  - Four high-performance slave ports
  - One accelerator coherence port (ACP) slave port
- **An understanding of PS interconnect (switches) operation is necessary for proper design use of the various ports**

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AXI Bridges

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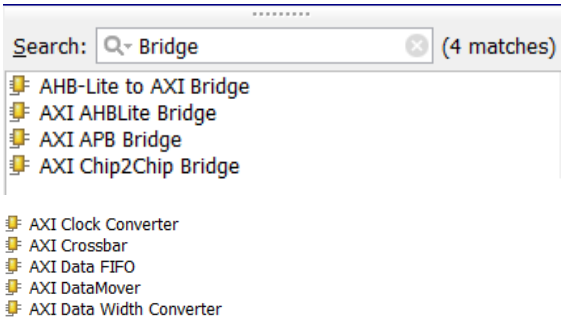
AXI Buses and Bridges

- **Four bridges are available**
  - AHB-Lite to AXI bridge
  - AXI to AHB-Lite bridge
  - AXI to APB bridge
  - AXI Chip2Chip bridge
- **Other AXI IP**
  - AXI Clock Converter
  - AXI Crossbar
  - AXI Data FIFO
  - AXI DataMover
  - AXI Data Width Converter



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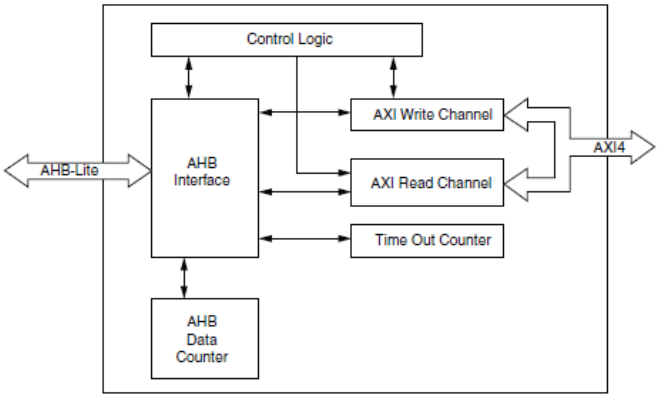
AHB-Lite to AXI Bridge

- Translates AHB-Lite transactions into AXI4 transactions
- Functions as an AHB-Lite slave on the AHB bus and as an AXI master on the AXI bus



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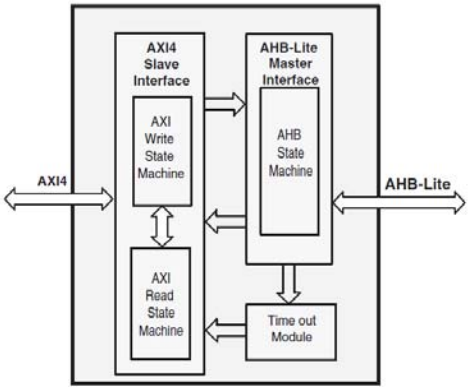
AXI to AHB-Lite Bridge

- Translates AXI4 transactions into AHB Lite transactions
- Functions as a slave on the AXI4 interface and as a master on the AHB-Lite interface



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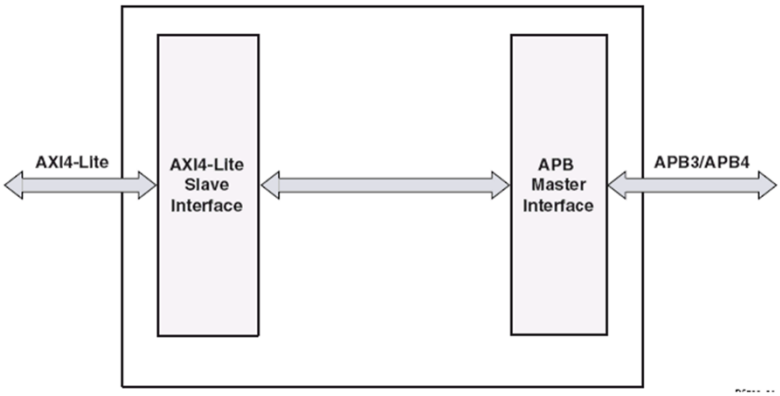
AXI4-Lite to APB Bridge

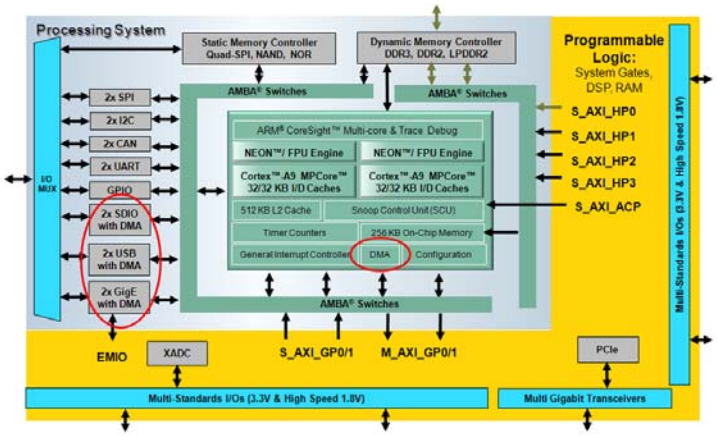
- Translates AXI4-Lite transactions into APB transactions
- Functions as a slave on the AXI4-Lite interface and as a master on the APB interface



PS DMA

Support for PS DMA

- **There is DMA support for USB, Ethernet, and SD-SDIO**

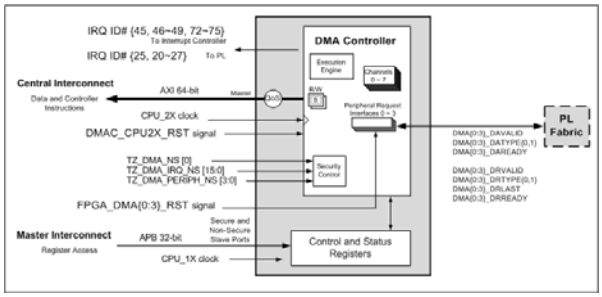


PS DMA Engine

- **Eight concurrent DMA channels**
  - Four for the programmable logic, four for the processing system
- **Support for multiple transfer types**
  - Memory to peripheral
  - Peripheral to memory
  - Scatter gather
  - Programmable logic or processing system peripherals
- **Support for single outstanding cache line access**
- **Eight interrupt lines**
- **64 deep FIFO**
- **Support for both 32-bit and 64-bit transfers**

Programming the PS DMA

- **DMAs are complex and require programming in order to be used**
- **Similar to an assembly language**
  - Variable-length instructions 1-6 bytes
  - Separate program counter for each channel
- **Documented in the *Zynq-7000 SoC Technical Reference Manual* (UG585)**



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PL DMA

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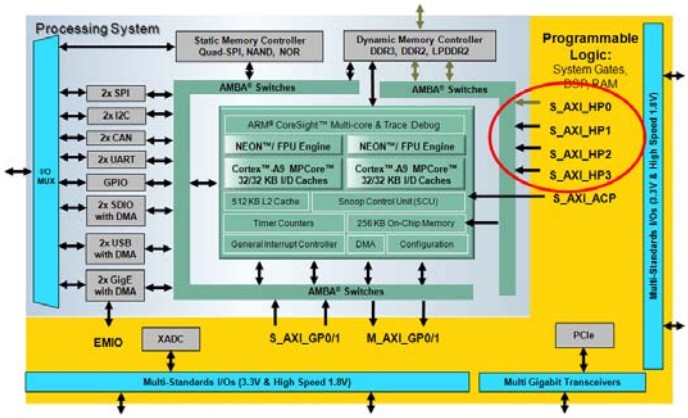
Support for PL DMA

> **PL-based DMA engines are used to transfer data from PL components to DDR and OCM**



AXI DMA

> **Four AXI-based DMA services are provided**
>> Central DMA (CDMA)
- Memory-to-memory operations

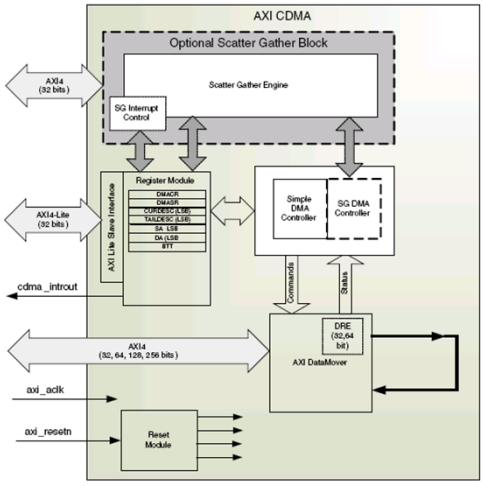
>> DMA
- Memory to/from AXI stream peripherals

>> FIFO Memory Mapped To Streaming
- Streaming AXI interface alternative to traditional DMA

>> Video DMA
- Optimized for streaming video application to/from memory

LogiCORE IP AXI CDMA

- High-bandwidth Direct Memory Access (DMA) between a memory-mapped source address and a memory-mapped destination address
- Optional Scatter Gather (SG)
- Initialization, status, and control registers are accessed through an AXI4-Lite slave interface



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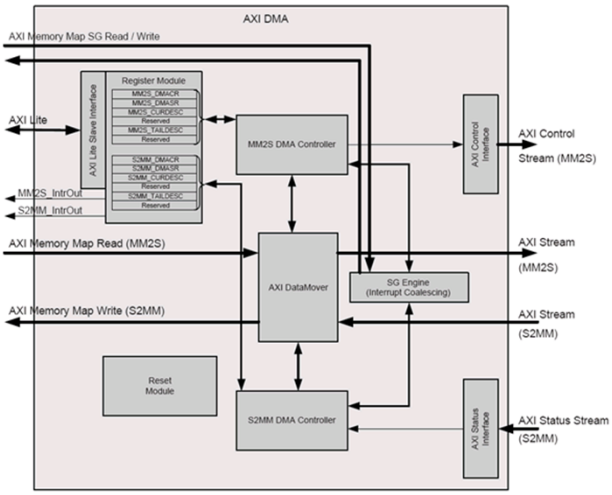
AXI DMA

- The AXI DMA provides high-speed data movement between system memory and AXI stream-based target IP, such as AXI Ethernet
- Movement is between memory and AXI-based IP



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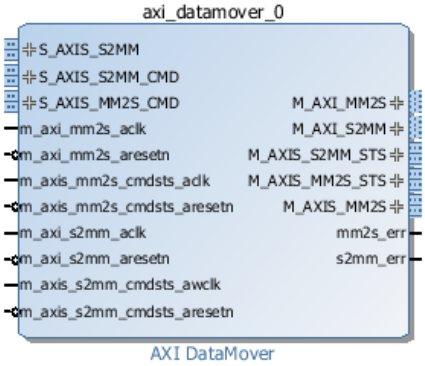
AXI Streaming FIFO with the PS

- Memory-mapped streaming interface
- Alternative to DMA
- Write or read of data packets to or from a device without any concern over the AXI streaming interface

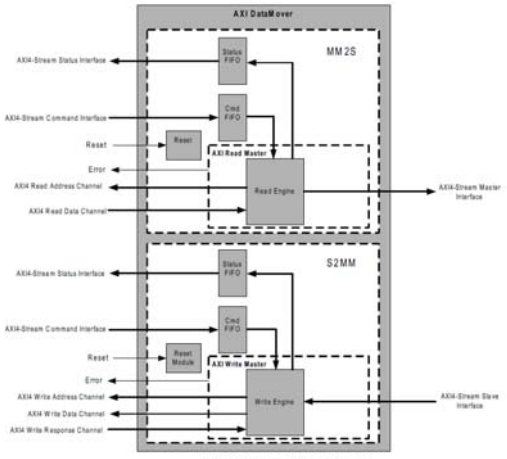
AXI DataMover

- Memory-mapped streaming interface
- Alternative to DMA
- Write/read of data packets to/from AXI streaming interface
- Primary AXI4 data width support of 32, 64, 128, 256, 512, and 1,024 bits
- Parameterized Memory Map Burst Lengths of 2, 4, 8, 16, 32, 64, 128, and 256 data beats
- Byte level realignment



AXI DataMover

- Enables high throughput data transfer between AXI4 memory-mapped domain and AXI4-Stream domain
- MM2S and S2MM AXI4-Stream channels operate independently
- Enables full-duplex operations
- Programmable data widths for both AXI4 Memory Map and AXI4 Stream Map
- Supports optional general-purpose store-and-forward feature



AXI DataMover Block Diagram

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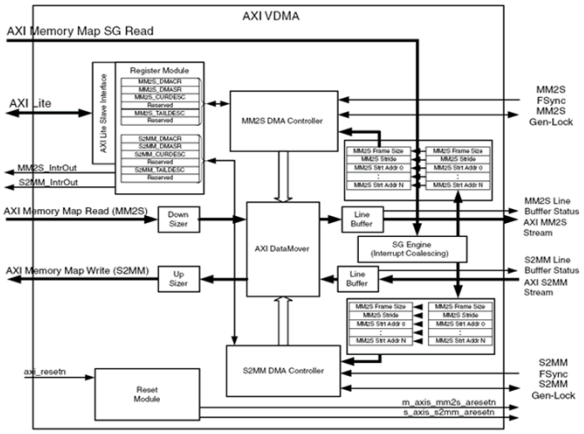
LogiCORE IP AXI Video DMA

- The AXI VDMA provides high-speed data movement between system memory and AXI stream-based target video IP



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Summary

Summary

- **AXI Streaming is a high-speed alternative to a bus-type interface**
- **AXI Streaming has no direct connection to the processor core**
- **The back end in programmable logic fabric appears as a simple AXI Streaming interface**
- **Optional control and user signals can be enabled**
- **The AXI FIFO Memory Map to Streaming component provides**
  - Interface to AXI interconnect
  - Data FIFOs
  - Signal compatibility to other Xilinx cores

Summary

- All Xilinx IP and the whole ecosystem supports the AXI interface
- The AXI CDMA controller allows for memory-to-memory transfer
- The AXI DMA component facilitates memory to/from an AXI interface peripheral
- The AXI Streaming FIFO provides DMA-like streaming services with a lot less logic and complexity
- The AXI Datamover enables high throughput transfer of data between the AXI4 memory mapped domain to AXI4 stream domain
- The AXI Video DMA component services are optimized for video streaming applications

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Intelligent.

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