



High-Level Synthesis with Vitis HLS tool

Course Objectives

- ▶ After completing this course, you will be able to:
 - Describe the High-Level Synthesis flow
 - Describe scheduling and binding phases of the HLS flow
 - Understand the control and datapath extraction
 - Identify the steps to extract RTL from C using the Vitis HLS tool
 - Identify steps involved in validation and verification flows
 - State various directives which can be helpful in improving performance and resource utilization
 - Describe how to use Vitis Vision library functions in the Vitis HLS tool
 - Perform system-level integration of blocks generated by the Vitis tool

Course Outline

Day 1

The course consists of the following modules:

- ▶ Introduction to High-Level Synthesis (HLS)
- ▶ Using Vitis HLS
- ▶ Lab 1: Creating Project and Understanding Reports
- ▶ Improving Performance
- ▶ Lab 2: Optimizing Performance through Pipelining
- ▶ Data Types

Course Outline

Day 2

- ▶ Improving Area and Resources Utilization
- ▶ Lab 3: Improving Area and Resources Utilization
- ▶ Handling Block- and Ports- Level Protocols
- ▶ Coding Considerations
- ▶ Creating a Processor System
- ▶ Lab 4: Creating a Processor System to filter Audio Signal

Prerequisites

- ▶ Basic knowledge with the Vitis/Vivado Design Suite tool set
- ▶ Basic C programming
- ▶ Basic understanding of a processor-based system

Platform Support

- ▶ AMD-Xilinx University board
 - PYNQ-Z2, PYNQ-Z1
- ▶ Vitis Design Suite: Vitis HLS 2021.2, 2022.1, 2022.2
- ▶ Supported Operating Systems
 - Red Hat Enterprise Linux 7.8, 7.9, 8.1, 8.2, 8.3, 8.4 (64 Bit)
 - Cent OS 7.8, 7.9, 8.1, 8.2, 8.3 (64 Bit)
 - Ubuntu Linux 18.04.4 LTS, 18.04.5 LTS, 20.04 LTS, 20.04.1 LTS, 20.04.2 LTS (64 Bit)
 - Amazon Linux 2 AL2 LTS
 - Windows 10 Professional (64-bit)



Thank You

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