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Lab1 Intro
Vitis HLS Design Flow

Objectives

- After completing this lab, you will be able to:
  - Create a project in Vitis HLS
  - Run C-simulation
  - Use debugger
  - Synthesize and implement the design using the default options
  - Use design analysis perspective to see what is going on under the hood
  - Understand and analyze the generated output

The Design

- This lab uses a simple matrix multiplication example to walk you through the Vitis HLS project creation and analysis steps. The design consists of three nested loops. The Product loop is the inner most loop performing the actual elements product. The Col loop is the outer-loop which feeds next column element data with the passed row element data to the Product loop. Finally, Row is the outer-most loop. The res[i][j]=0 (line 79) resets the result every time a new row element is passed and new column element is used

```
67 #include "matrixmul.h"
68
69 void matrixmul(
70       mat_a_t a[MAT_A_ROWS][MAT_A_COLS],
71       mat_b_t b[MAT_B_ROWS][MAT_B_COLS],
72       result_t res[MAT_A_ROWS][MAT_B_COLS])
73 {
74   // Iterate over the rows of the A matrix
75   Row: for(int i = 0; i < MAT_A_ROWS; i++) {
76     // Iterate over the columns of the B matrix
77     Col: for(int j = 0; j < MAT_B_COLS; j++) {
78       // Do the inner product of a row of A and col of B
79       res[i][j] = 0;
80       Product: for(int k = 0; k < MAT_B_ROWS; k++) {
81         res[i][j] += a[i][k] * b[k][j];
82       }
83     }
84   }
85 }
```

Procedure

- Create a project after starting Vitis HLS in GUI mode
- Run C simulation
  - to understand the design behavior
- Run the debugger
  - to see how the top-level module works
- Synthesize the design
- Analyze the generated output using the Analysis perspective
- Run C/RTL co-simulation
  - to perform RTL simulation
- View simulation results in Vitis
  - to understand the IO protocol
- Export RTL in the Evaluate mode and run the implementation

Summary

- Completed the major steps of the high-level synthesis design flow using Vitis HLS.
- Created a project, added source files, synthesized the design, simulated the design, and implemented the design.
- Learned about how to use the Analysis perspective to understand the scheduling.

Thank You

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