Concepts in VLSI Design Laboratory

IT126IU

Instructor: Nguyen Toan Van

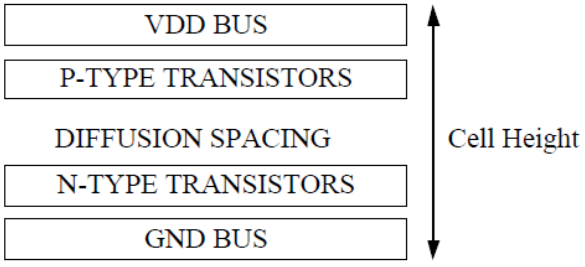
Lab 3
Layout of an Inverter using Virtuoso L

Objectives:

- To create a layout view of the basic inverter circuit from scratch in Virtuoso Layout Editor
- To design the layout keeping basic design rules in mind
- To design cell layout of a constant height for use in hierarchical design

Introduction to Layout, DRC and LVS

- Layout is representation of a circuit in terms of planar geometric shapes (e.g. rectangles, polygons) showing the patterns of metal, polysilicon, oxide, or diffusion layers that make up the components (resistors, inductors, capacitors, transistors) of the integrated circuit.
- When using a standard process (e.g. 45nm, 90nm or 180nm process available in our lab), the behaviour of the final integrated circuit depends significantly on the positions and interconnections of the geometric shapes due to parasitic resistances and capacitances contributed by them. While designing a layout, designer must keep in mind performance (e.g. power-delay product) and size (area occupied by the chip) criterion.
- While designing digital circuits, one usually follows an ASIC design flow, where, the height of standard cells that are used is the same throughout the cell library, but their widths must vary according to their logical functions and drive strengths. The following figure shows a generalized standard cell height concept:



Although we will follow a full-custom IC design flow, we will maintain same cell height throughout our cell library.
The generated layout must pass a series of checks in a process known as physical verification. The most common checks in this verification process are:

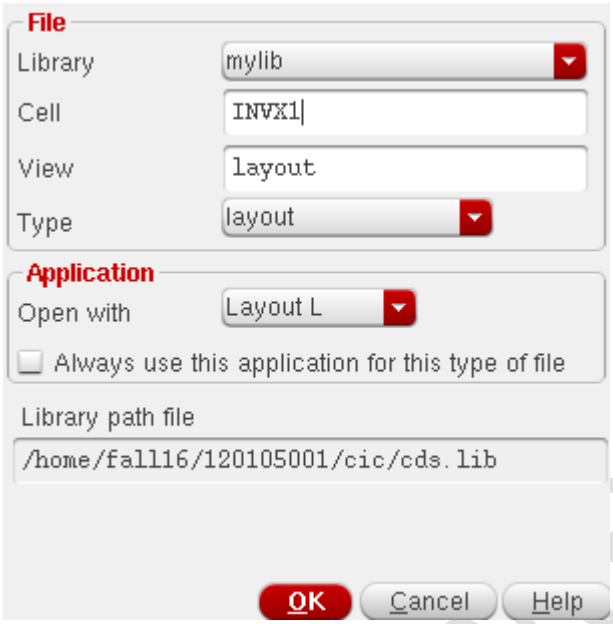
- Design Rule Checking (DRC)
- Layout Versus Schematic (LVS) checking
- Parasitic extraction and post-layout simulation

Design Rule Check (DRC):
Design Rule Checking (DRC) is the process that determines whether the designed layout of a circuit satisfies a rules specified by the process being used.
Design Rules are a series of rules (e.g. area, width, overlap, enclosure, extension, spacing) provided by semiconductor manufacturers which are specific to a particular semiconductor manufacturing process. Design rules specify certain geometric and connectivity restrictions to ensure that the process can fabricate the device properly.

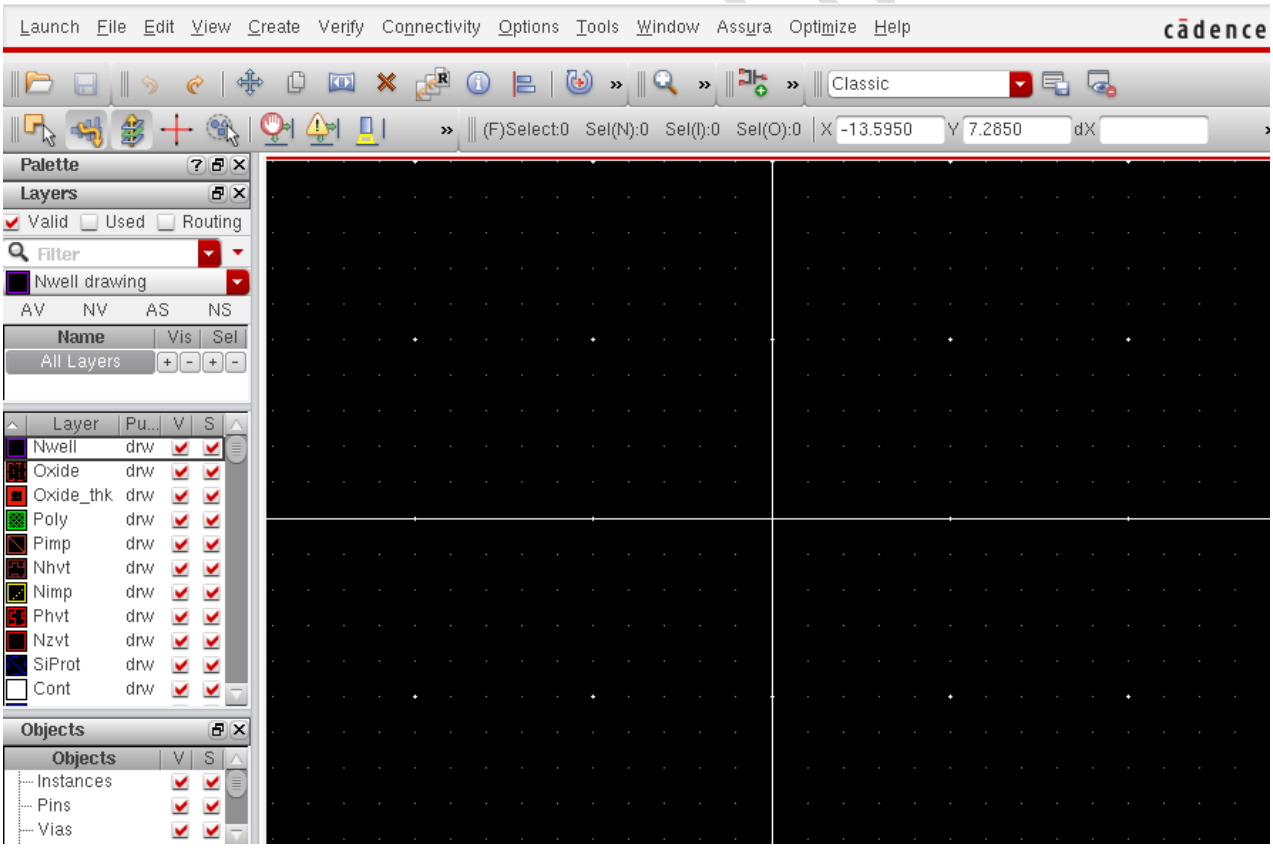
Layout versus Schematic (LVS) Check:
The Layout Versus Schematic (LVS) is the verification step to determine whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design. A successful Design rule check (DRC) ensures that the layout conforms to the rules designed/required for faultless fabrication. However, it does not guarantee if it really represents the circuit we desire to fabricate. This is why an LVS check is used.

Layout design using Virtuoso Layout Suite L Editor

Invoke **Virtuoso Layout Suite L Editor** from the **CIW** by executing ***File*** -> ***New*** -> ***Cellview***. The '**New File**' form appears. Fill it in as shown in the figure below:
Cell: *INVX1*, **View:** *layout*. Click **OK**.



The following window of **Virtuoso Layout Suite L Editor** will appear.

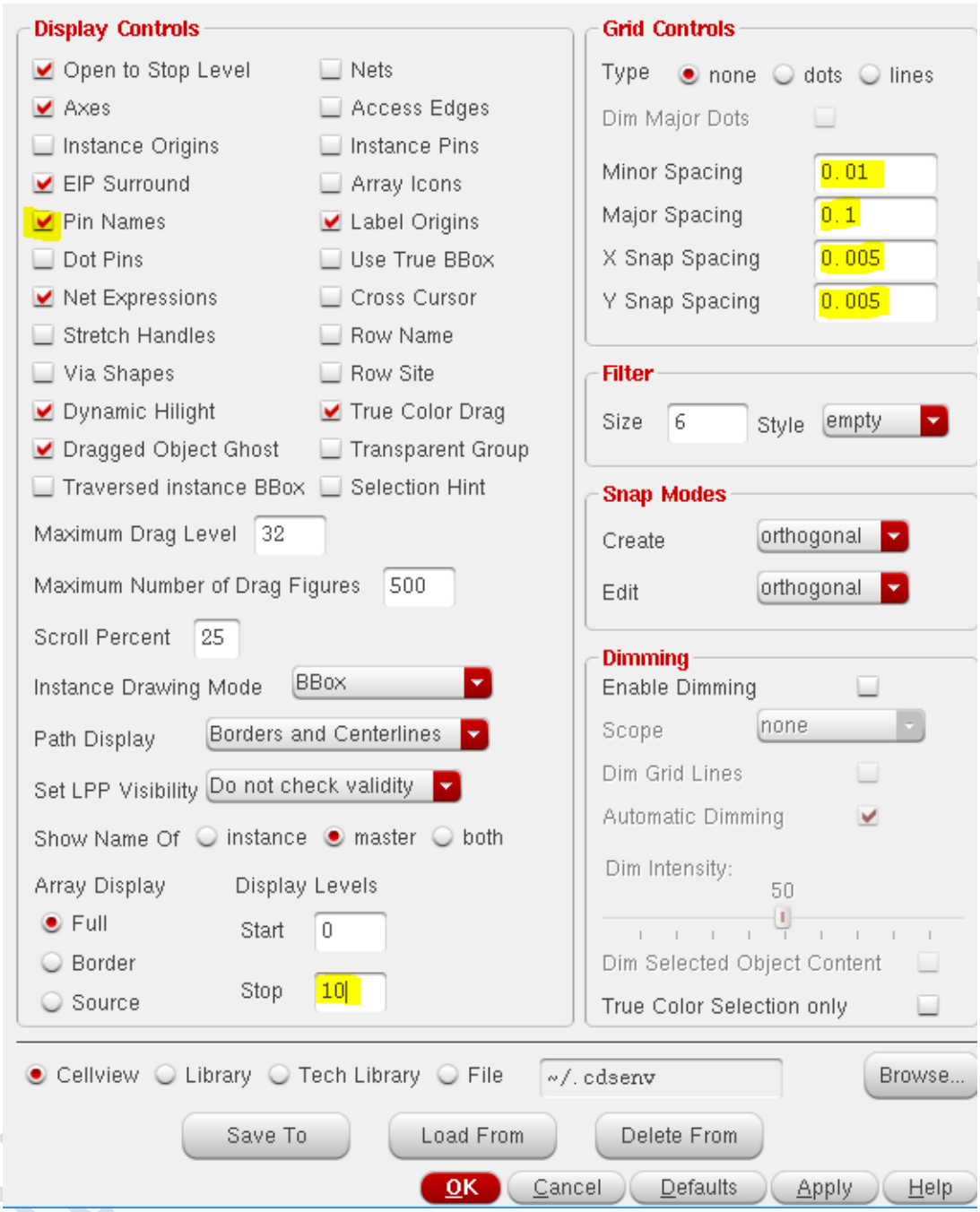


On the left side of the window, you will find a panel called 'Layers'. This panel is divided in three main categories which are: layer color, layer name and layer purpose. The details are described in the table below:

Color	Matches the color in the Editing window. Each layer has its own color and pattern. Each layer has two colors associated with it: a fill color and an outline color. These colors can be changed to fit your taste by editing the technology file.
Name	The type of layer (Nwell, Oxide, Poly, Metal1, etc)
Purpose	In gpdk090 the only purpose classifications are: drw = drawing, slot = slot Drawing is used in layout, slot is used to create a hole for metal stress relief

Verify that the layers display corresponds to the gpdk090 layers shown in the GPDK 90 nm Mixed Signal Process Specification manual (*gpdk090_DRM.pdf*).

3. Before starting to design layout, you need to set the layout display configuration. Execute the following in the Virtuoso Layout Editor***: Options -> Display*** or press '**e**' on keyboard. Configure the form as shown in the figure below: You have to set the following parameters only:

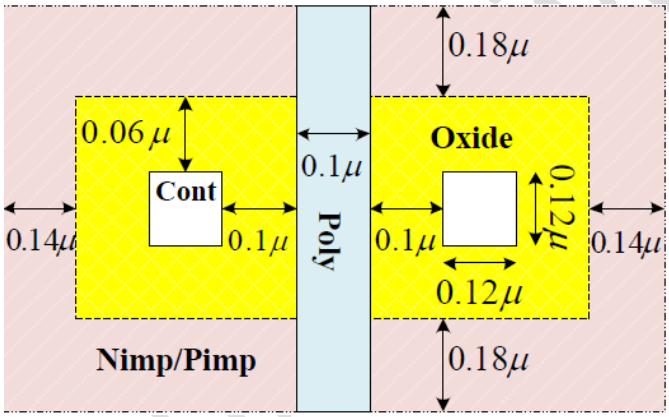


4. Now we are going to build the layout of the inverter. An inverter has an NMOS and a PMOS transistor. First we will build an NMOS transistor.

Layout of NMOS inverter consists of oxide, Nimp, Cont and Poly layers. Study the rules of these layers and calculate the minimum size of the Poly, Cont, Oxide and Nimp layer to create an NMOS transistor.
The rules related to the NMOS transistor can be summarised as follows:

Contact size	0.12 μm × 0.12 μm (Fixed)
Poly width (Minimum)	0.1 μm (Fixed MOS gate length)
Contact to poly spacing (Minimum)	0.1 μm
Contact to oxide enclosure (Minimum)	0.06 μm
Poly/Nimp extending from oxide (Minimum)	0.18 μm (gate side enclosure)
Nimpenclosing oxide (Minimum)	0.14 μm (enclosure other than gate sides)
Minimum Metal 1 width	0.12 μm
Maximum Metal 1 width	12.0 μm
Minimum Metal 1 to Contact enclosure	0.06 μm (on at least two opposite sides)

The following figure illustrates some of the design rules mentioned above:



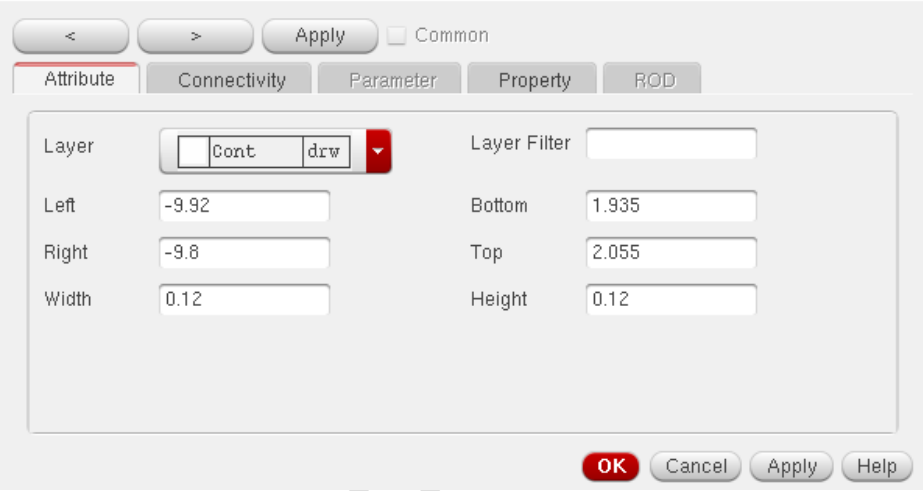
Now study the PMOS transistor structure in the GPDK 90 nm Mixed Signal Process Spec. The PMOS transistor consists of Oxide, Poly, Pimp, Cont and Nwell layer. Study the rules of these layers and calculate the minimum size of Poly, Cont, Oxide, Pimp and Nwell layer to create a PMOS transistor. The rules related to PMOS are same as NMOS except the there is an additional layer, the Nwell, whose rules are as follows:

Minimum Nwell width	0.6 μm
Minimum Nwell spacing to Nwell (same potential)	0.6 μm
Minimum Nwell spacing to Nwell (different potential)	1.2 μm
Minimum Nwell spacing to N+ active area	0.3 μm
Minimum Nwell spacing to P+ active area	0.3 μm
Minimum Nwell enclosure to P+ active area	0.12 μm
Minimum Nwell enclosure to N+ active area	0.12 μm
Minimum N+ Active Area to P+ Active Area Spacing	0.16 μm

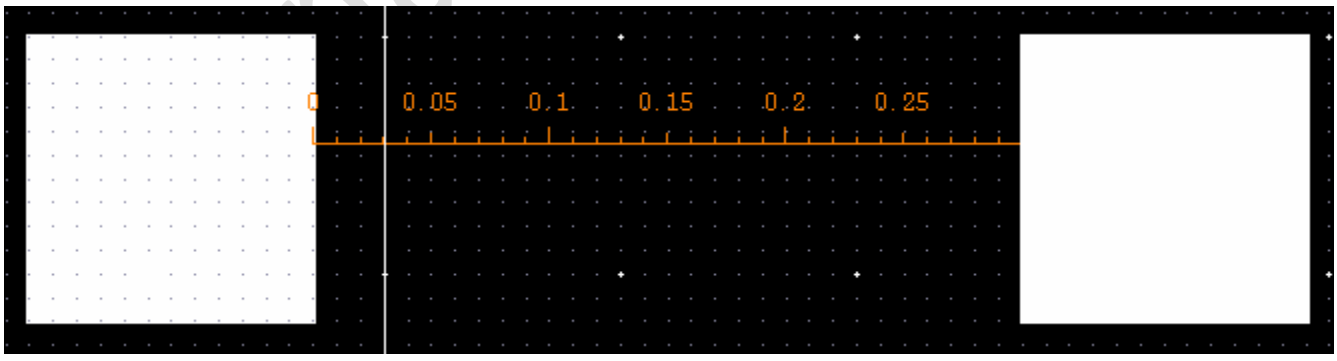
Now we start building the NMOS and PMOS transistor layout. Look at the **LSW** and find the current drawing layer.

5. Click on the following icon in **Virtuoso Layout Suite L Editor** window so that it notifies you anytime you make a violation of any design rule. When clicked, it will show '**DRD Notify ON**'. DRD stands for Design Rule Driven.

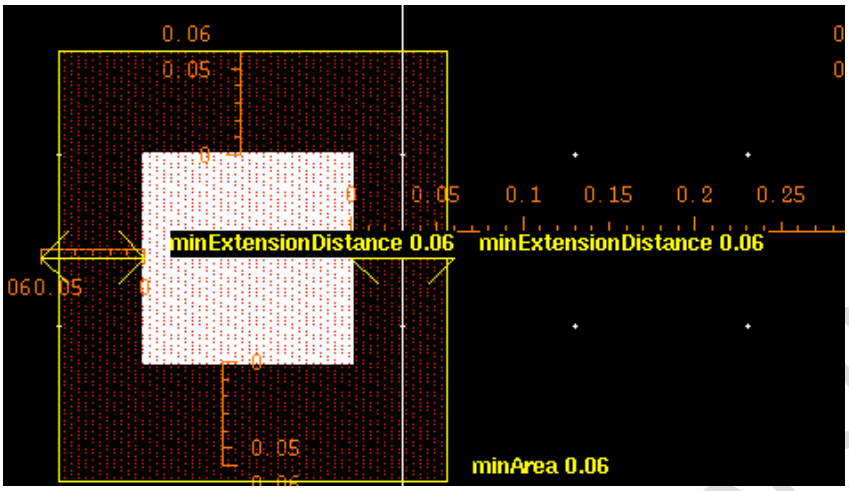
6. Select '**Cont (drw)**' (contact) layer from the '**Layers**' panel and draw a rectangle of '**Cont (drw)**' layer using ***Create*** -> ***Shape*** -> ***Rectangle*** or simple pressing '**r**'. Press '**Esc**' to stop '**create rectangle**' tool. In gpdk090 technology, **Cont** layers must be of dimension **0.12 μm x 0.12 μm**. So, if your rectangle is not of that dimension, click on the rectangle, press '**q**'. In the following window, check if the criterion has been met and change '**Width/Height**' if required.



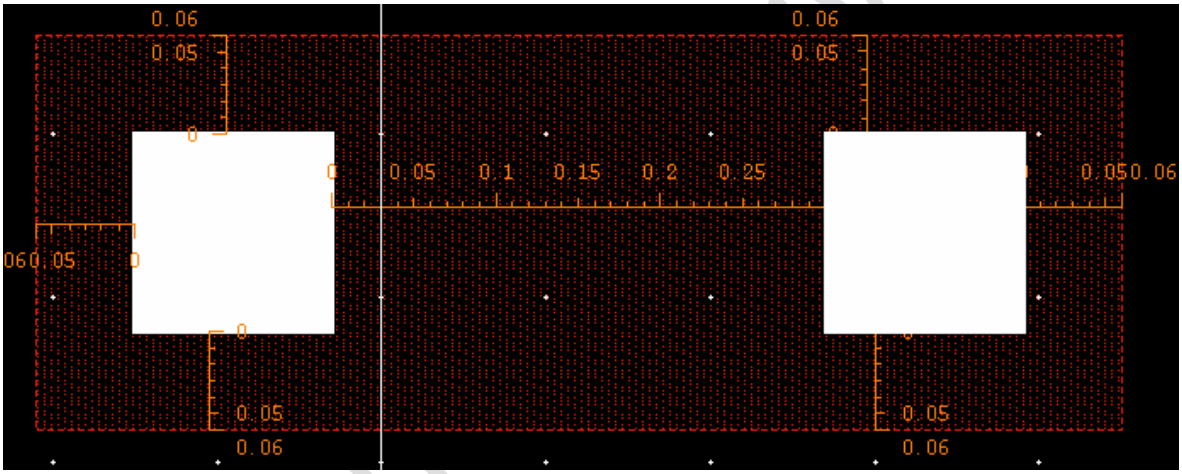
Contact to poly spacing must be **0.1 μm** in this technology and the **channel length** of NMOS/PMOS in our design is **0.1 μm**. So, we need a minimum space of **0.3 μm** between the contacts at source and drain.
7. Press '**k**' to invoke the '**ruler**' tool. Use it to measure lengths whenever needed. To copy, press '**c**'. After placing two contacts, the layout looks like this:



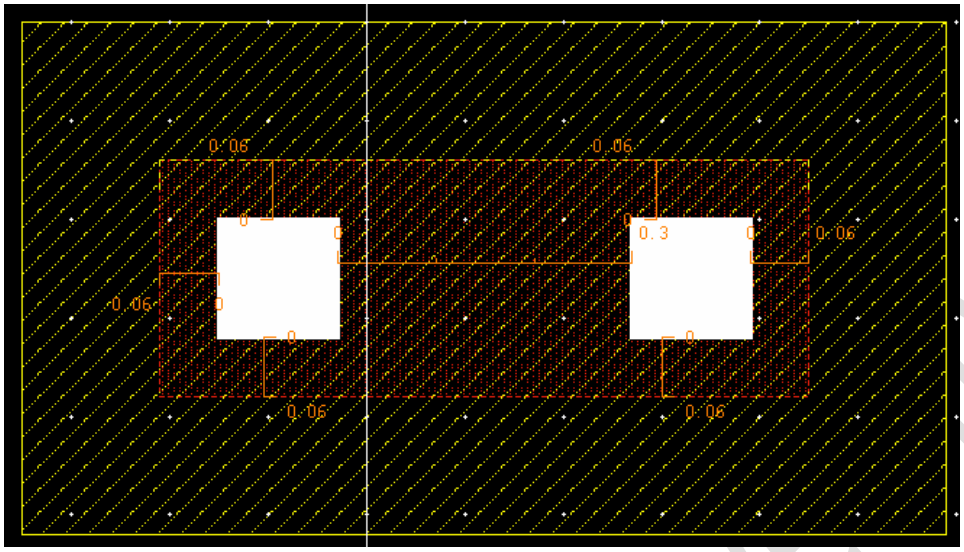
8. Now, **contact to oxide spacing** is minimum **0.06 μm**. So, draw a rectangle of '**Oxide (drw)**' layer so that it covers both the contacts and extends from each side by **0.06 μm**.
While drawing this, you will see Design rule violations when they are committed.



9. After drawing oxide layer, the layout should look like this:

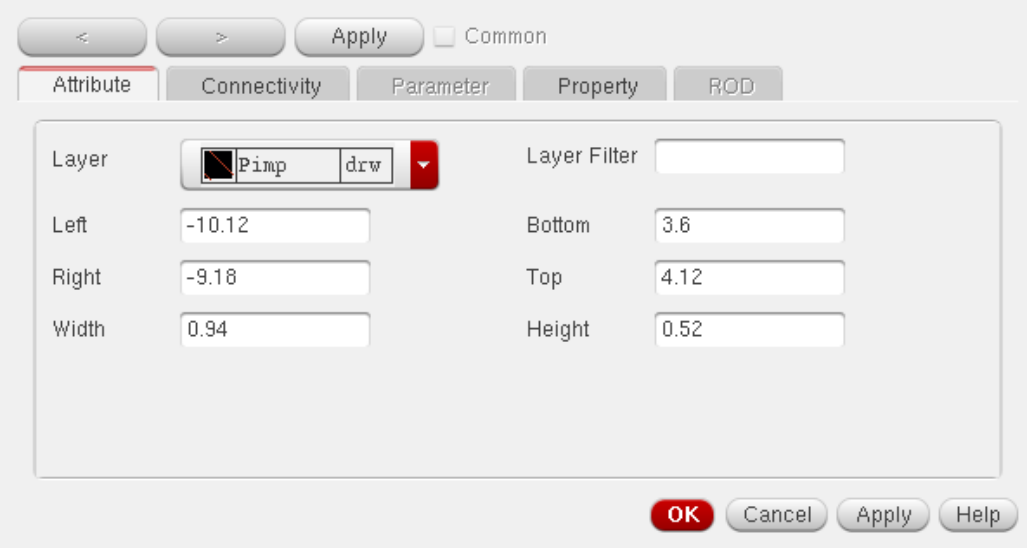


10. Now we will draw '**Nimp (drw)**' layer, which must extend from the oxide layer by a minimum of **0.14 μm**. First, draw a rectangle and then extend it to meet design rules. Use stretch tool by pressing '**s**'. Layout will look like the following:



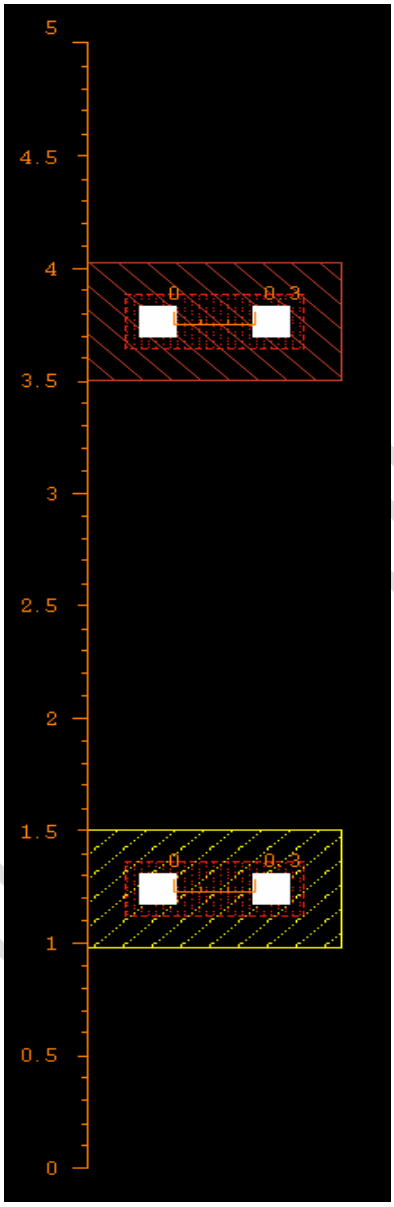
11. Now, copy it and create another copy of all these layers by selecting all and pressing '**c**'.

12. Click on the '**Nimp (drw)**' layer of the copy in the upper portion of the layout and press '**q**' to edit properties. From '**Edit Rectangle Properties**' window, select '**Pimp (drw)**' layer under '**Layer**' option. Click **OK**.

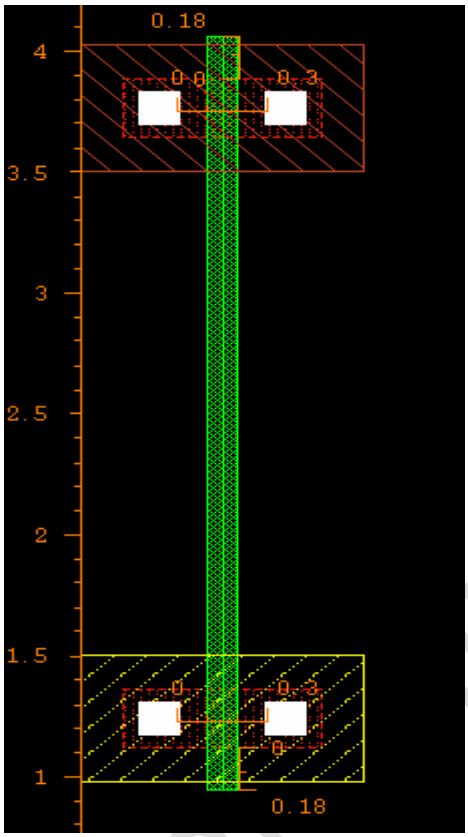


13. With more metal layers available in today's silicon processes, using the routing approach, such as first metal traverse vertically and second metal traverse horizontally, would be advantageous in standar cell physical design. Using this method, the second layer (e.g. Metal2) can be used for power and ground routing over internal standard cell transistors. In standard cell layout, it is preferable to use firt conducting layer, such as Metal1, as much as possible to make internal connections of NMOS and PMOS transitors within the cell. If there is a nedd to use other conducting layers, such as, Metal2, use of such layers must be kept to a minimum. It is desired to use first routing (e.g. Metal1) layer for standard cell ports.

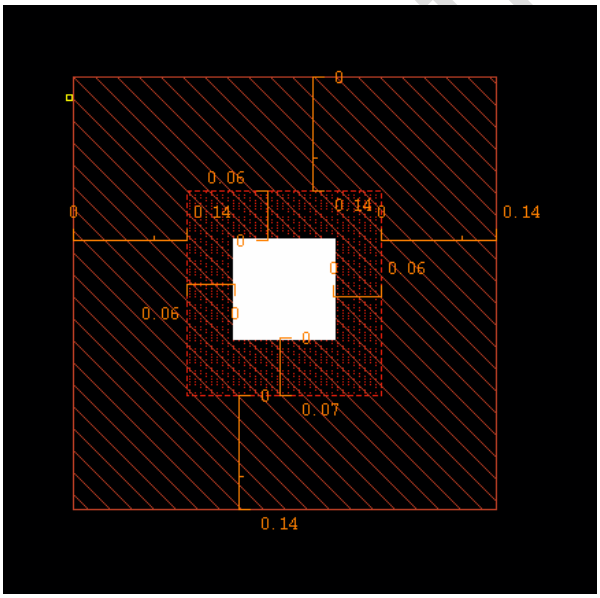
Our cells will have a height of **5 μm**. Place the two parts (NMOS and PMOS) **2 μm** apart, and create a ruler so that the cell height can be checked whenever needed and the separation between the NMOS and PMOS can be maintained properly. Now, the layout will look like the following:

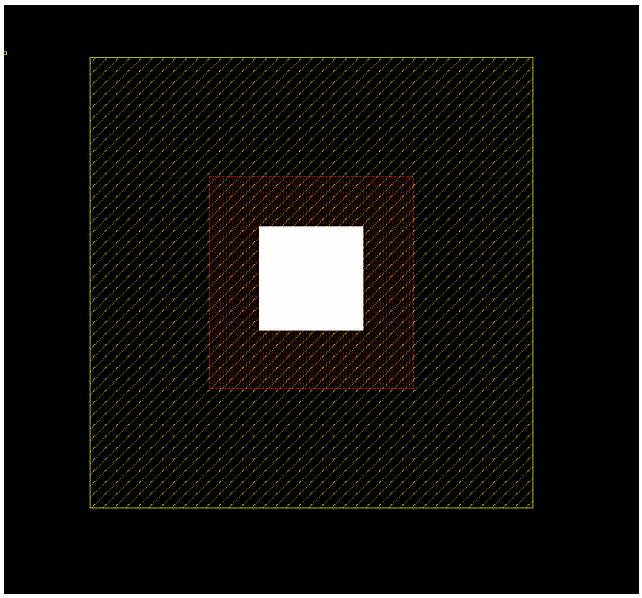


14. Next, draw a '**Poly (drw)**' path by selecting '**Poly**' layer from the '**Layers**' panel and pressing '**p**' to invoke '**create path**' tool. This layer must be of **0.1 μm** in width and in between the two contacts, extending from the oxide layer by **0.18 μm** (at least, on both sides). After placing the '**poly**' gate, the layout will look like the following one:

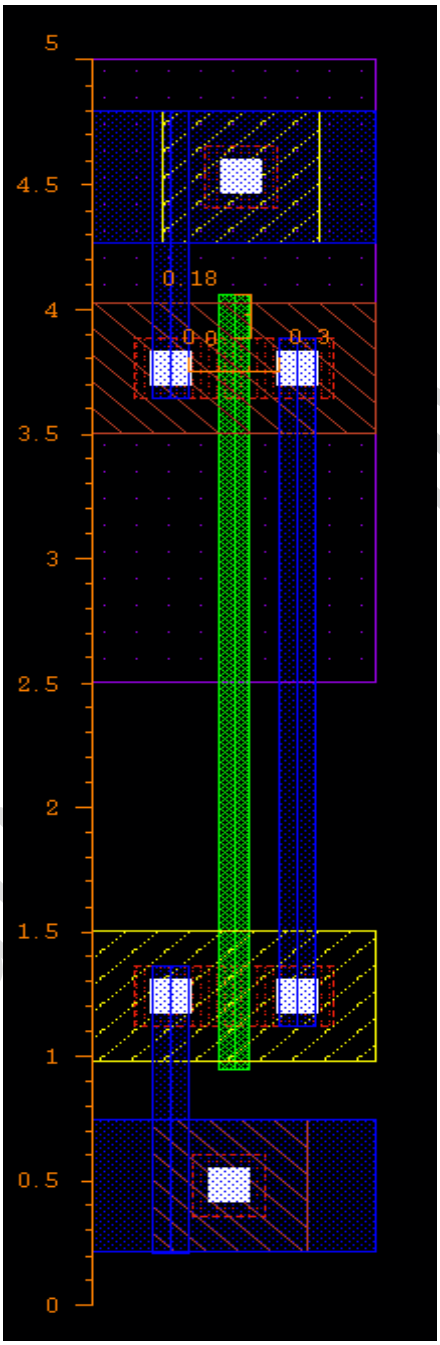


15. Now that you know most of the shortcuts and layers, draw contact for body terminals for NMOS and PMOS. These portions should consist of Cont, Oxide and Nimp (for body of PMOS) or Pimp (for body of NMOS). Check DRD notifications for design rule violations. The following figure shows a Psubstrate and an Nwell contact. The measurement dimensions are shown only on the left one, as they are same for both contacts.

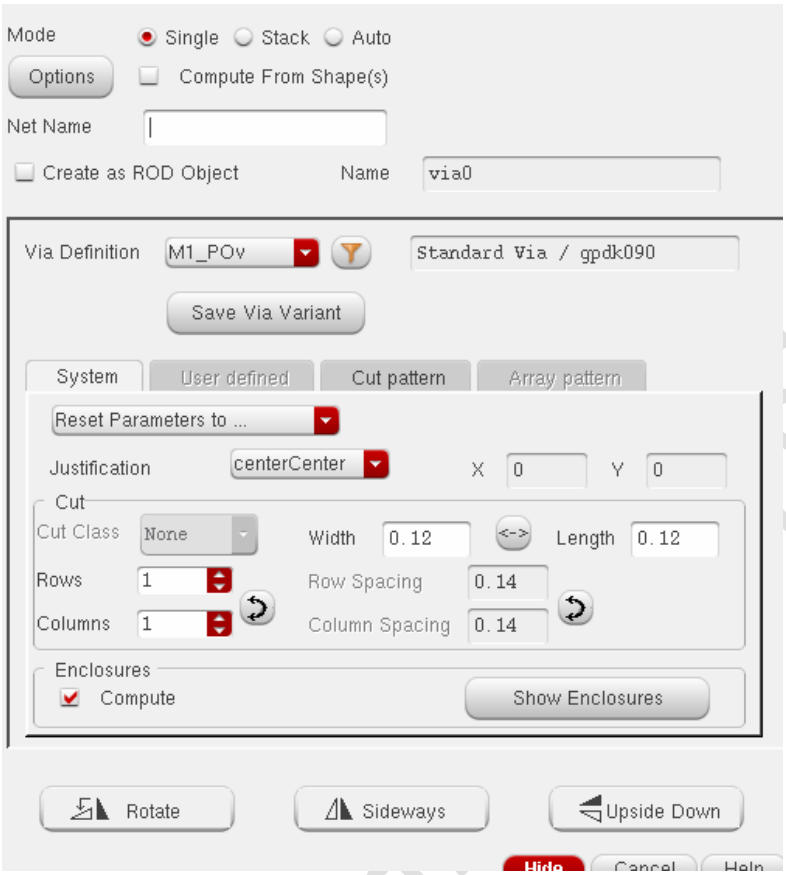




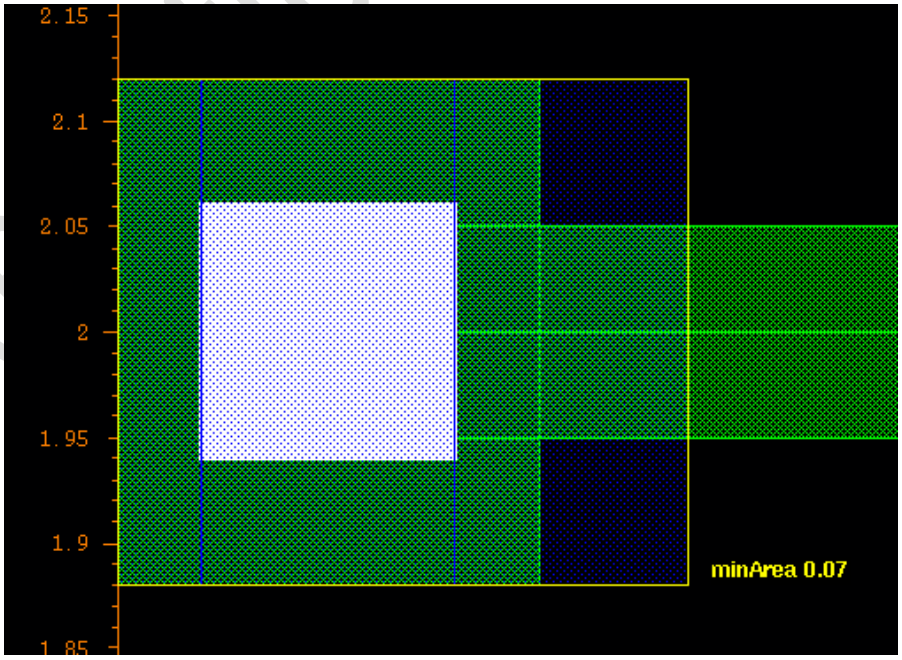
16. Connect the Drain regions of the NMOS and PMOS. Also connect the source of both MOS's to respective body terminals using '**Metal1 (drw)**' layer. Connect the drains of the MOS's using '**Metal1 (drw)**' layer.
17. PMOS should be in '**Nwell (drw)**'. So draw an '**Nwell (drw)**' rectangle surrounding both the PMOS and the body contact for PMOS. The layout will look like the following:



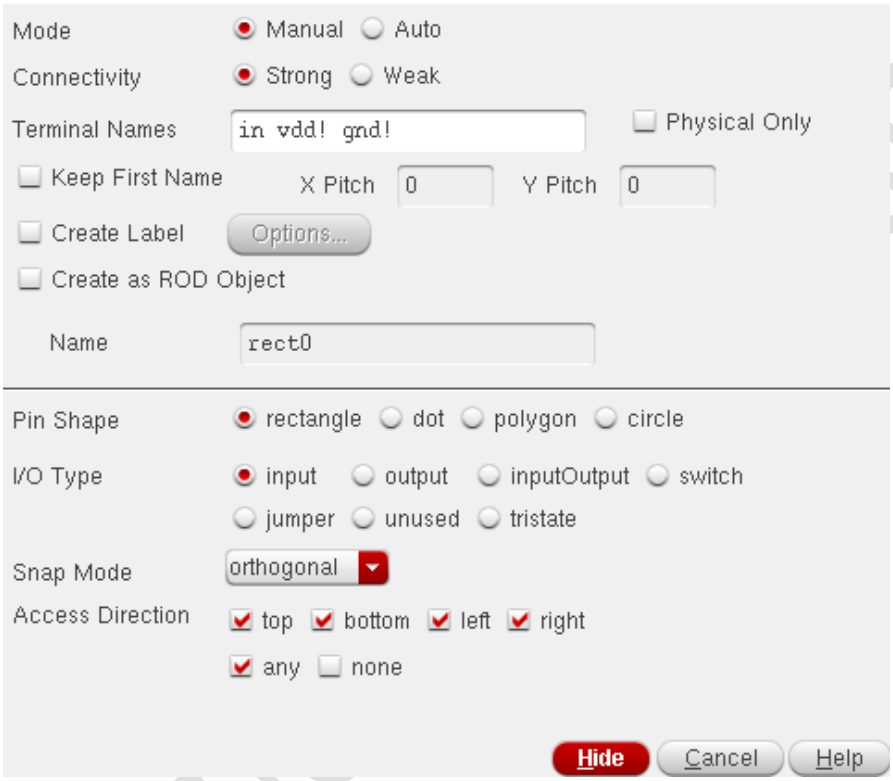
18. Now, we have to place pins. The gate is in '**poly (drw)**' layer. Let's bring it to '**Metal1(drw)**' layer by extending the '**Poly (drw)**' layer, creating a contact between '**Poly**' and '**Metal1**' layer by pressing '**o**' to '**create via**' and selecting '**M1_POv**' under '**via definition**' and placing it on layout.



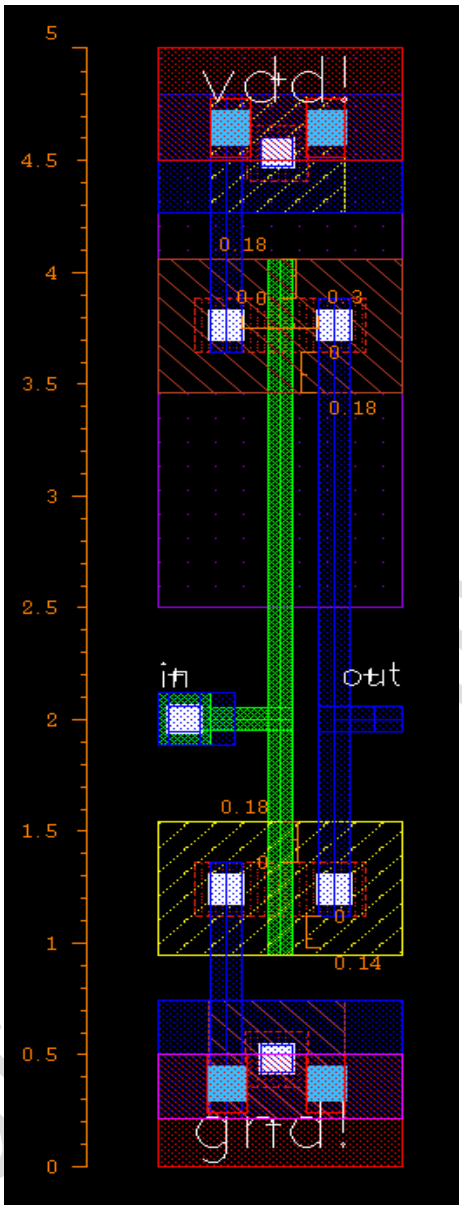
19. Also draw a '**Metal1 (drw)**' rectangle on the via, because the default **Metal1** rectangle area is less than the required minimum.



20. Now, Execute ***Create → Pin*** to create pins for **vdd!**, **gnd!**, **in** and **out**.
For **in**, **vdd!** and **gnd!** select '**input**' as **'I/O type'** and for **out** select '**output**' as **'I/O type'**. Now, draw rectangles on the **Poly-Metal1** via for '**in**' pin, PMOS source-to-body '**Metal1**' connection for '**vdd!**' pin and NMOS source-to-body connection for '**gnd!**' pin. For '**out**' pin, draw the rectangle on the **Metal1** layer connecting the two drains of MOS's.



You may add label to pins.
21. Finally, add **Metal2** paths of **0.5*μ*** width for power rails and connect them to power nets in **Metal1** by using **Metal1 to Metal2** via by invoking '**create via**'.
The final layout will look like the following:



QUESTIONS:

What is layout design? What rules a designer must keep in mind while designing layout? Why does DRC rules are provided by the foundry? What principles in layout designing are best practices for a designer?

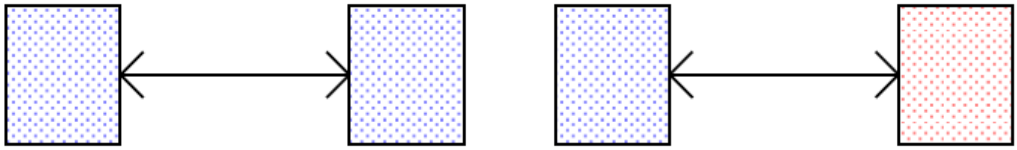
Appendix A (Shortcut keys for Cadence Virtuoso ® Layout Editor L)

Shortcut Key	Tasks performed
f	Fit display to window
r	Draw rectangle
q	Edit property of an object

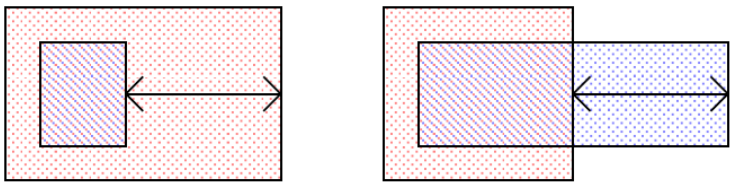
p	Makes a min width path of the layer selected in LSW
Ctrl+a	Select all
Ctrl+d	Deselect all
c	Copy
m	Move
s	Stretch side of a rectangle
k	Invoke ruler tool
Shift+k	Delete all rulers
i	Add an instance
u	Undo
Shift+u	Redo
e	Display options
o	Add via between layers
l	Create a label

Appendix B (gpdk090 Design Rules Guide (Abridged Version for VLSI-I Lab))
Terminology Definitions

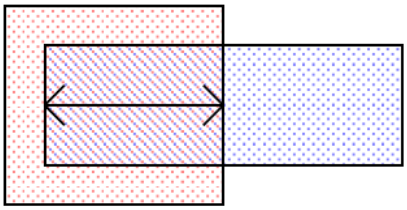
Spacing - distance from the outside of the edge of a shape to the outside of theedge of another shape.



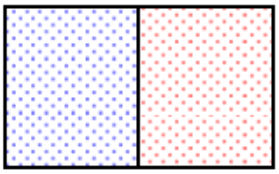
Enclosure - distance from the inside of the edge of a shape to the outside of theedge of another shape.



Overlap - distance from the inside of the edge of a shape to the inside of the edgeof another shape.



Butting - outside of the edge of a shape touching the outside of the edge of anothershape.



Appendix C (Some Most Commonly Violated Design Rules for gpdk090 technology)

Description (For metals k=2 to 6, for vias k=1 to 6)	**Value (µm/µm$_2$) wherever applicable**
Minimum oxide (active) area	0.06
Minimum 1.2V N/P Channel gate length	0.1
Minimum poly interconnect width	0.1
Minimum gate/poly interconnect space	0.12
Minimum N/P-channel gate extension beyond active area	0.18
Minimum poly interconnect to related/unrelated active area space	0.1
Minimum poly interconnect area	0.1
Bent gate is not allowed	
Minimum N+/P+ implant width	0.24
Minimum N+/P+ implant space	0.24
Minimum N+/P+ implant to active area enclosure	0.14
Minimum N+/P+ implant to gate side enclosure	0.18
Minimum N+ to P+ active area (inside Nwell) spacing	0.16
Minimum N+/P+ implant area	0.15
N+ implant is not allowed over P+ implant	
Minimum P+ to N+ active area (outside Nwell) spacing	0.16
Maximum and minimum Contact width/length	0.12
Minimum Contact to Contact spacing	0.14
Minimum Contact on Active Area to gate spacing	0.1
Minimum gate Contact to Active Area spacing	0.12
Minimum Active Area to Contact enclosure	0.06
Minimum Poly to Contact enclosure	0.04
Minimum Poly to Contact enclosure on at least two opposite sides (end of line)	0.06
Contact on gate is not allowed, Contact must be covered by Metal1 and active area/poly	
Minimum Metal 1 width	0.12
Maximum Metal 1 width	12
Minimum Metal 1 to Metal 1 spacing	0.12

Minimum Metal 1 to Contact enclosure	0
Minimum Metal 1 to Contact enclosure on two opposite sides of the Contact	0.06
Minimum Metal1 area	0.07
Minimum Metal k width	0.14
Maximum Metal k width	12
Minimum Metal k enclosure of Via k-1	0.005
Minimum Metal k enclosure of Via k-1on at least two opposite sides	0.06
Minimum Metal k area	0.08
Minimum and maximum Via k width	0.14
Minimum Via k to Via k spacing	0.15
Minimum Metal k to Via k enclosure	0.005
Minimum Metal k to Via k enclosure on at least two opposite sides of Via k	0.06
Minimum of four Via k with spacing <= 0.30µm or nine Via k with spacing <= 0.60µm are required when connecting Metal k and Metal k+1 when one of the Metals has a width > 1.0µm at the connection point	
Minimum Nwell width	0.6
Minimum Nwell spacing to Nwell (same potential)	0.6
Minimum Nwell spacing to Nwell (different potential)	1.2
Minimum Nwell spacing to N+/P+ Active Area	0.3
Minimum Nwell enclosure of N+/P+ Active Area	0.12