Concepts in VLSI Design Laboratory

IT126IU

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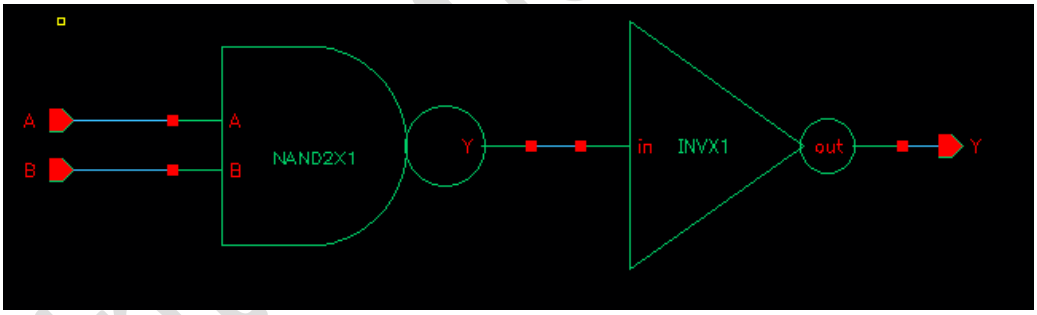
Lab 6:
Introduction to Hierarchical Design (2-input AND gate using 2-input NAND gate and an inverter)

Objectives:

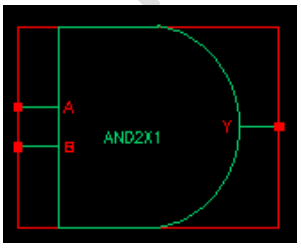
- To be familiar with concept of hierarchical design
- To perform Schematic Level Verification, Layout Design, DRC and LVS check
- To perform post-layout simulation of top level design

Introduction to Hierarchical Design

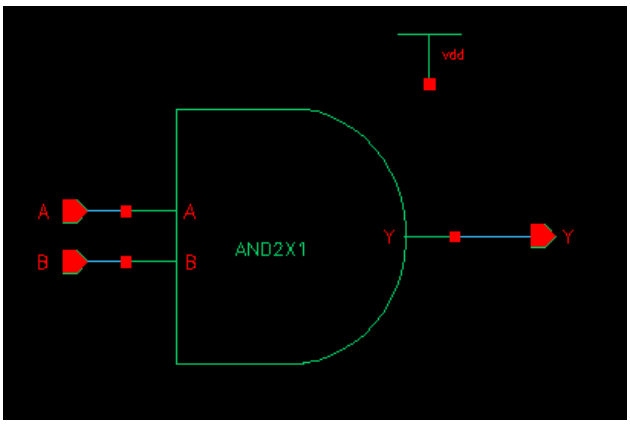
By this time, you should have completed layout of *INVX1* and *NAND2X1*. Now, you will learn how to perform hierarchical design.
1. Create a new cellview of type schematic named *AND2X1*.
2. Instantiate *NAND2X1* and *INVX1* symbol from your library *mylib* in that schematic.
Your final schematic should look something like the following:



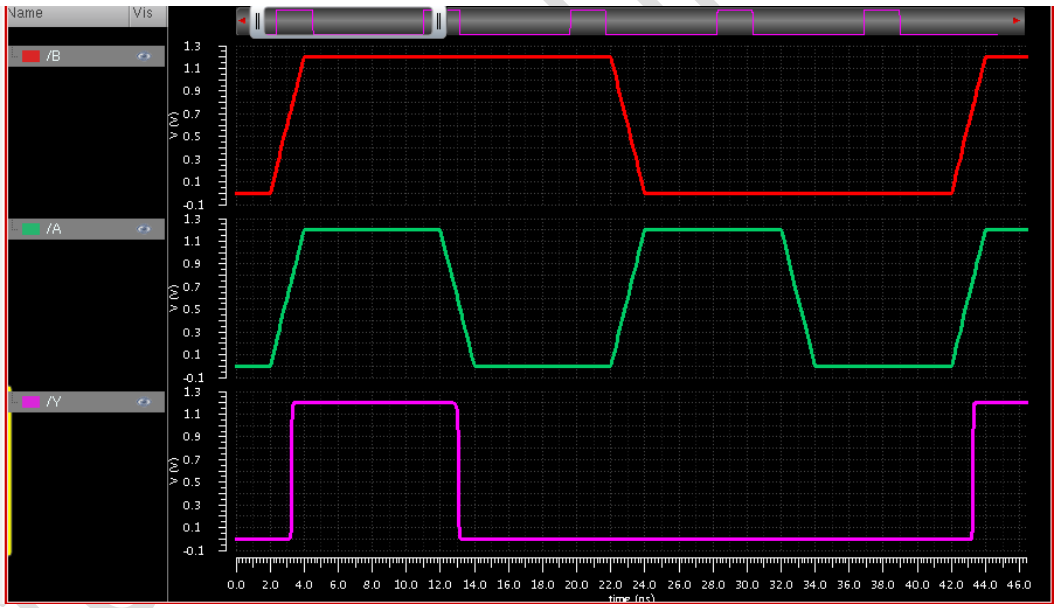
3. Now make a symbol of *AND2X1*.



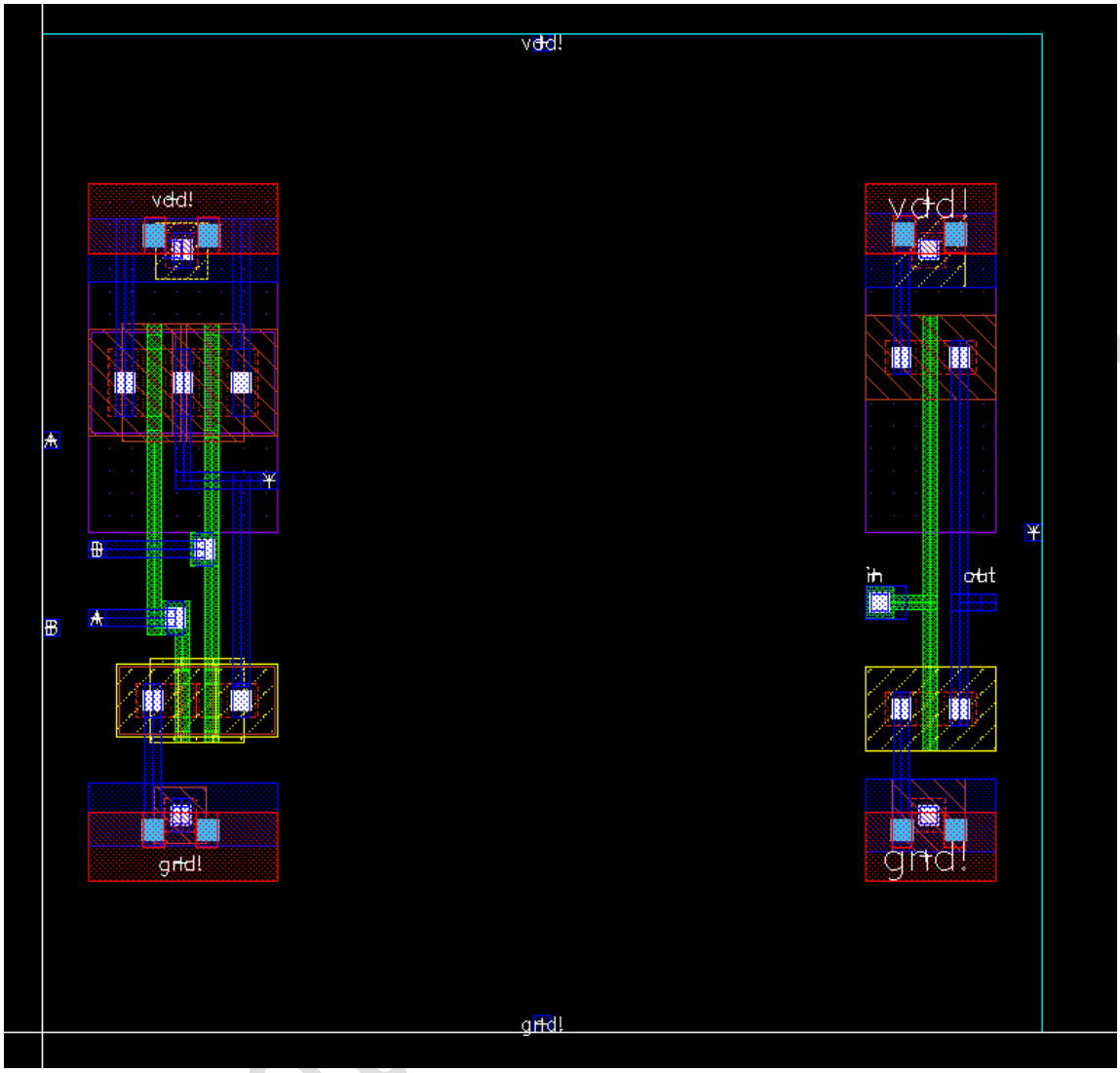
4. Now create a new cellview named *AND2X1_test*, instantiate *AND2X1* and *vdd* in that cell and the final schematic should look like the following:



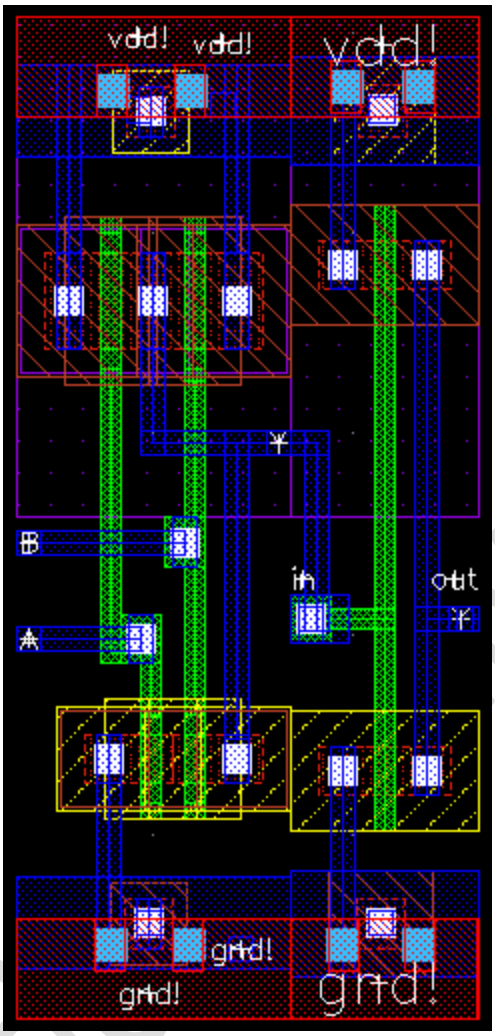
5. Now, launch **ADE L**, setup **Stimuli**, **Model library**, **Analysis** type and **Outputs to be plotted** in the same way as you have done in Lab 5. Run the simulation.



6. If functional verification is okay, then execute ***Launch*** -> ***Layout XL*** from the schematic of **AND2X1**.
7. Follow procedure of Lab 5 to generate instances and set display options. You will get something like the following:



8. Connect them as required and the final layout should look like the following (probably better!):



9. Perform DRC, LVS and QRC as you have done in Lab 4 and Lab 5.

QUESTIONS:

What is hierarchical design? What design principles will make hierarchical layout design easier?