Concepts in VLSI Design Laboratory

IT126IU

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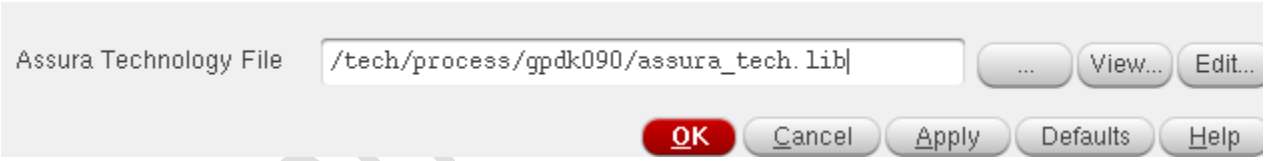
Lab 4
DRC, LVS, RCX and Post-layout simulation of an inverter

Objectives:

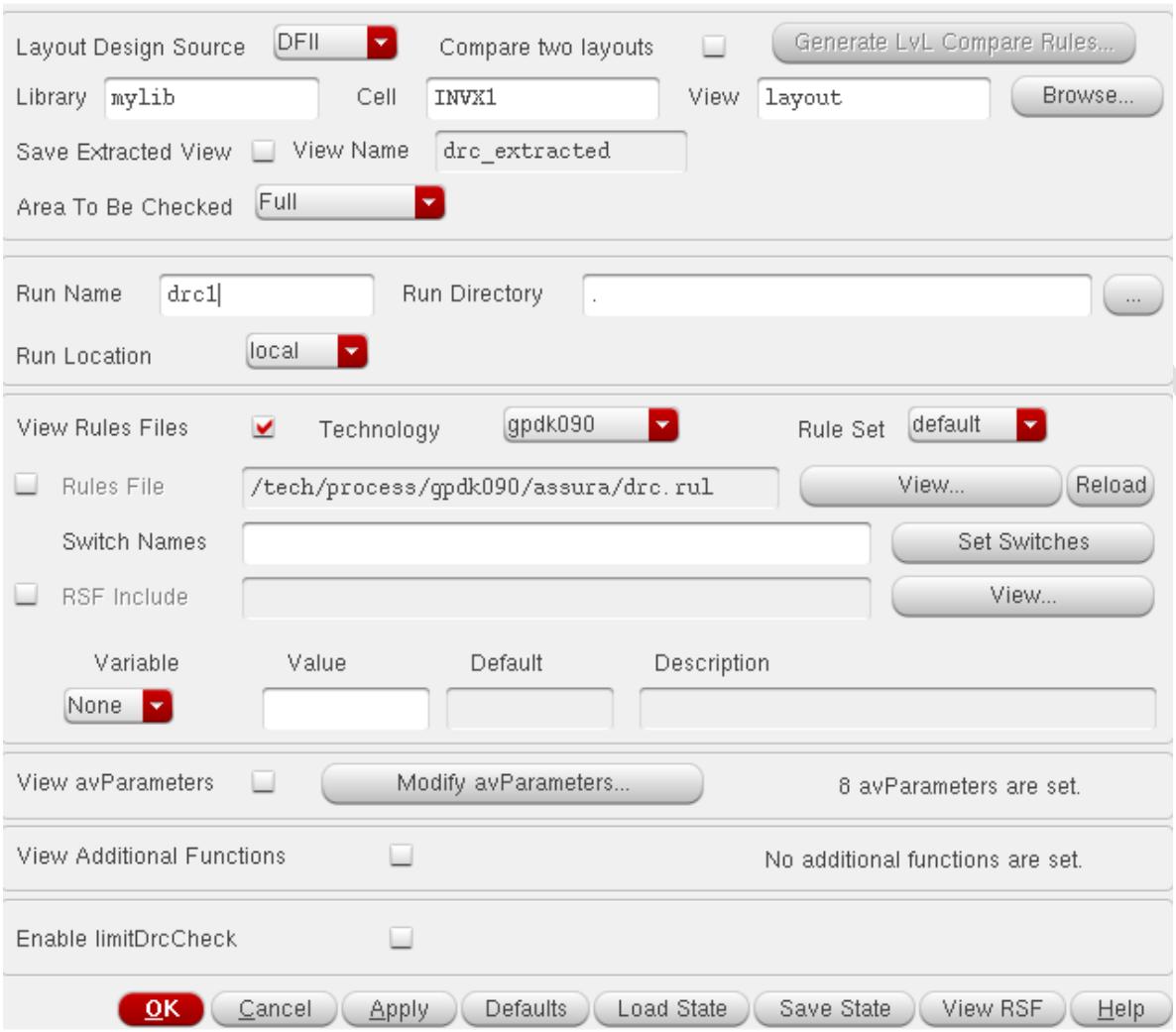
- To perform Design rule check (DRC), Layout vs. Schematic check (LVS) of inverter layout.
- To extract parasitic resistance and capacitance from layout of designed inverter.
- To perform transient simulation of extracted view.
- To create layout views for body ties of NMOS and PMOS for further use.

I. DRC Rules check by Cadence's ASSURA

1. Now we would like to check the DRC rules by ASSURA. Execute ***Assura → Technology***. In the following window, type the path of '**Assura Technolgy File**' as shown. Click **OK**.



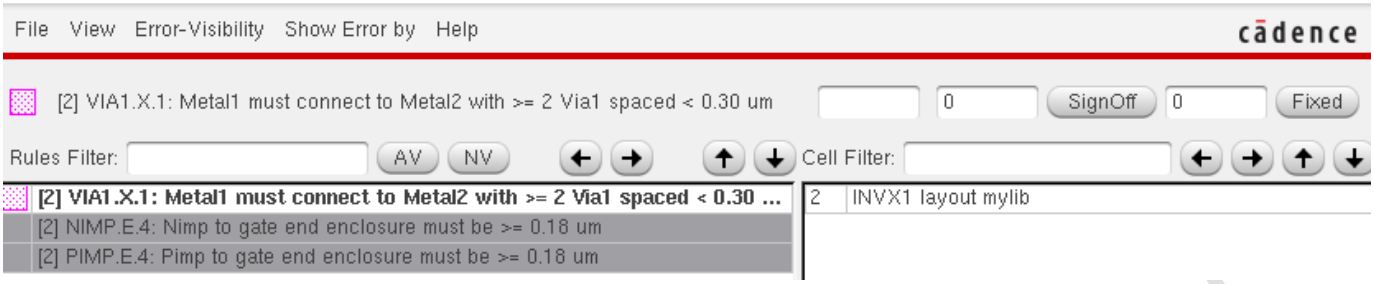
2. Execute ***Assura→Run DRC***. A DRC window appears as shown below. Fill in the form as indicated in the picture.
Give a **Run name**. Select '**gpdk090**' under '**Technology**'. Then click **OK**.



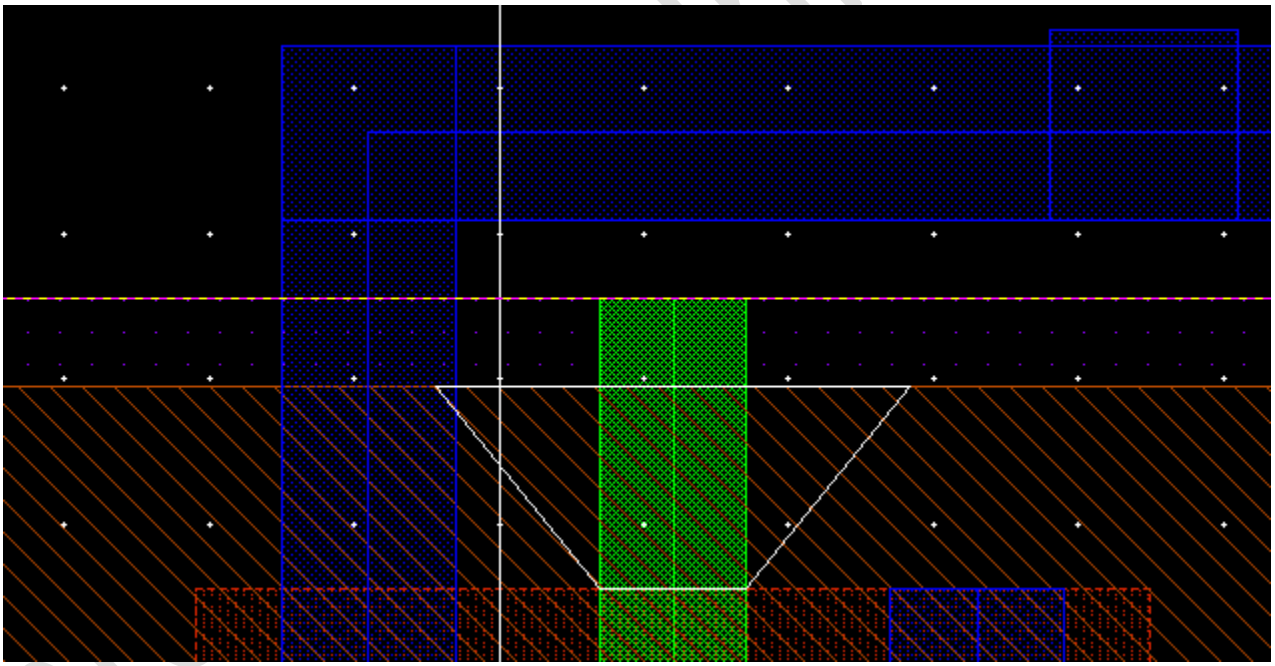
3. A DRC completed window appears as shown below, after completion of DRC run:

Click **Yes**.

4. 'Error layer Window' (ELW) appear as shown below with *INVX1* layout window which shows the errors.

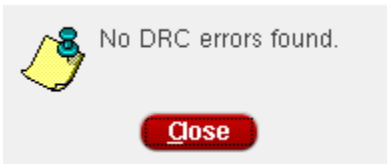


5. To correct the errors, find the error location by clicking on the error and then clicking on the right arrow key on ELW. To hide all the errors, click on '**NV**' (no Layers visible) button.
The particular error in the following figure is due to a lower than 0.18 m enclosure of gate by Pimp (drw) layer. Stretch the Pimp layer to correct it. Similarly, do this for all errors in your layout. No one can list all the errors one may commit, try correcting one after another and be familiar with them by solving them through practice.



After correcting all the errors, run the DRC again.

6. If your design is error free, you should get the following message.

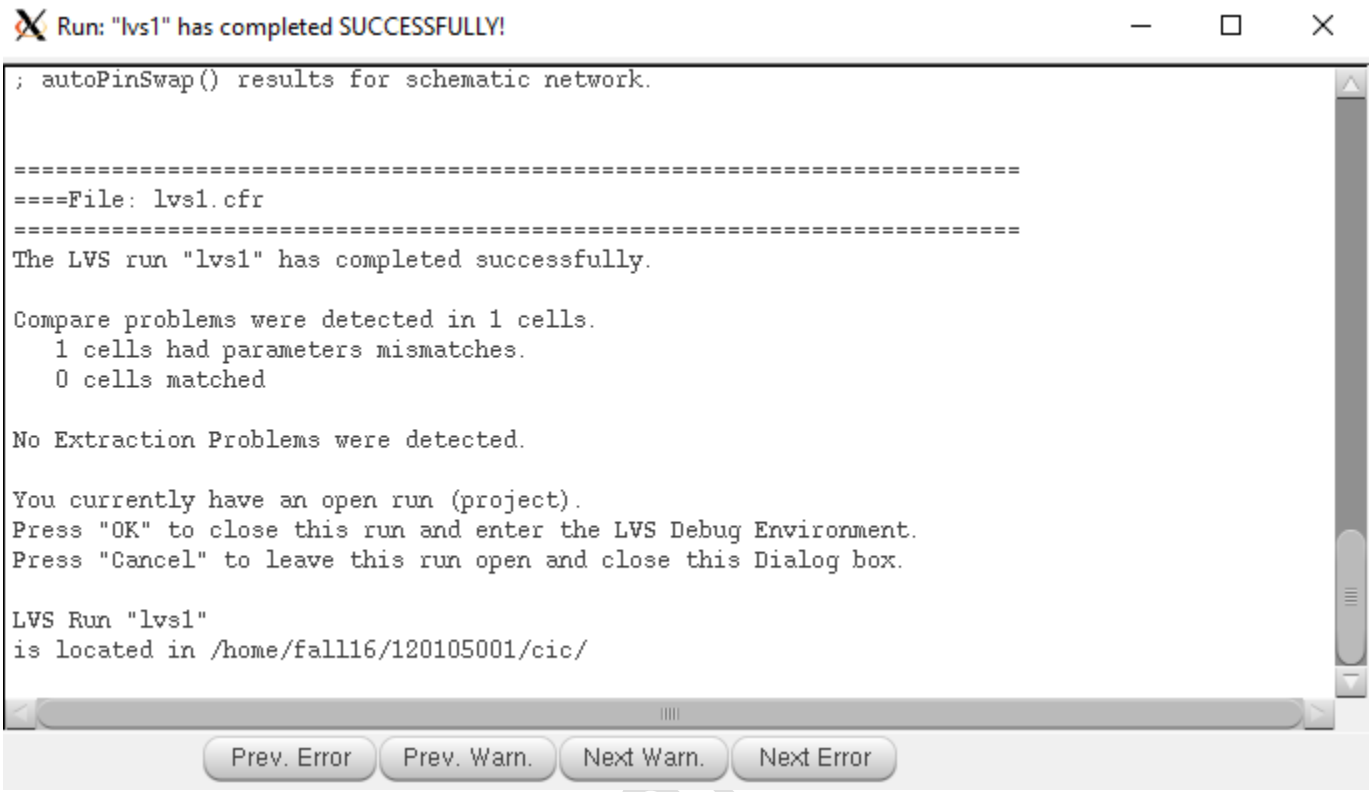


II. LVS check by Cadence's ASSURA

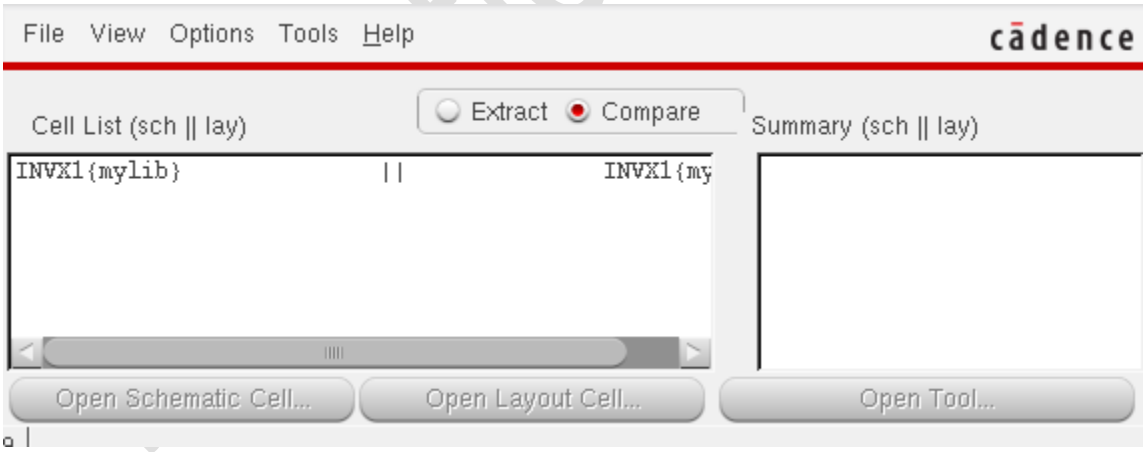
1. Execute ***Assura→Run LVS***. Select gpdk090 and give a **Run name**.

Click OK

2. After completion of lvs run, you will get a result window. If you have done everything right, it will say that Schematic and Layout match.
Suppose that you have made a mistake, your schematic says the PMOS width is 480n where layout says it is 240n. What will happen in LVS report? Let's see.

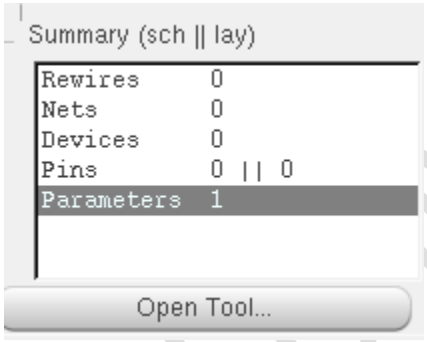


Note that, LVS report says that 1 cell had parameter mismatch. That means one cell had two different dimensions in schematic and layout. Click **OK**. '**LVS Debug**' window will appear:

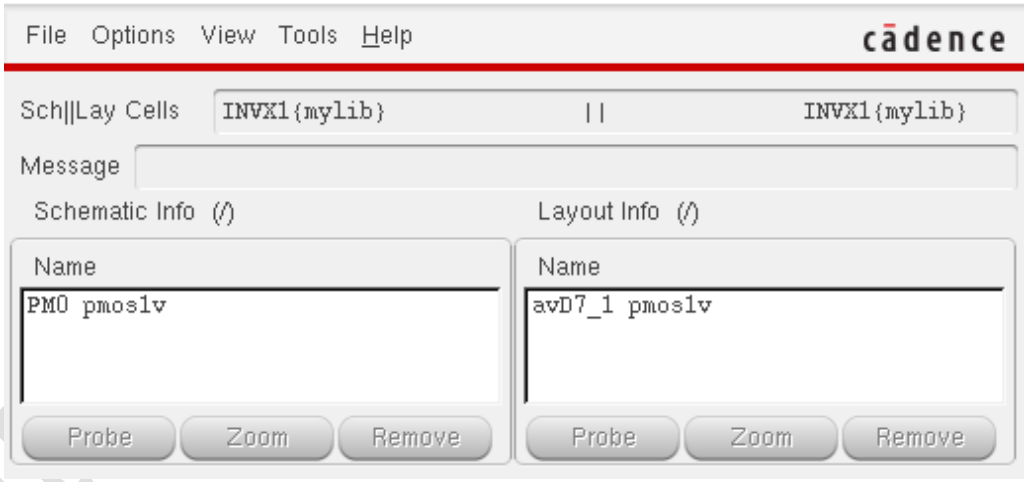


3. Select INVX1 (mylib). Notice that the summary window shows the list of errors.

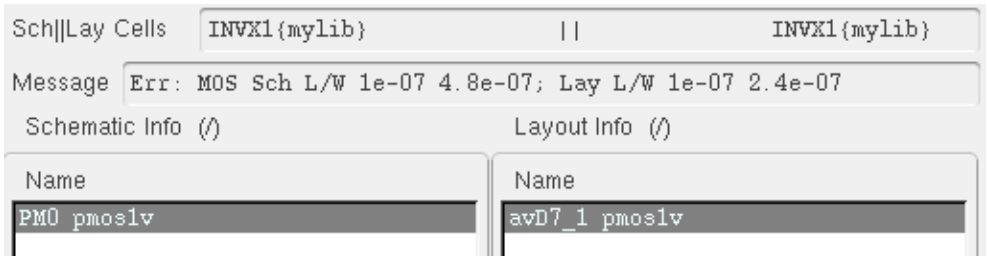
4. Only parameter mismatch has occurred. Click on **Parameters** and **Open Tool**.



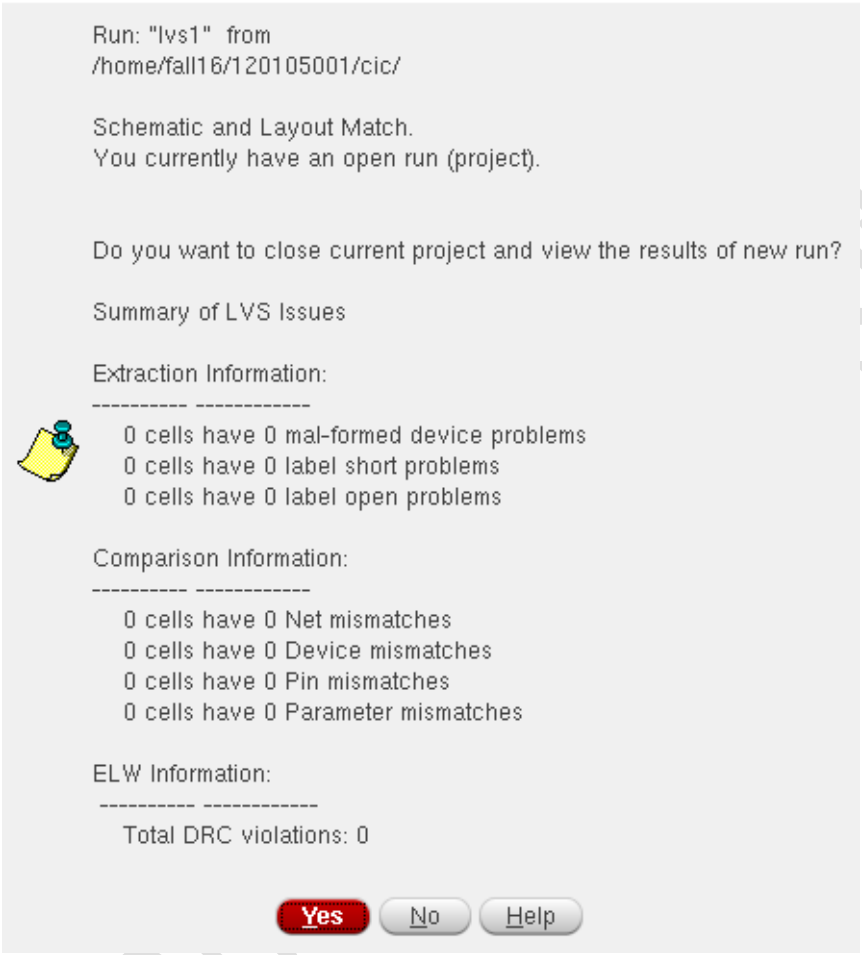
5. '**Parameters mismatch tool**' will open.



6. Select PM0 pmos1v. Now in the **Message** box, you can see the mismatch error.

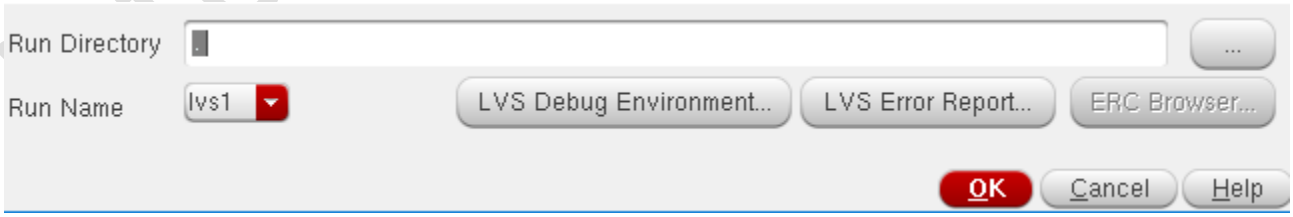


7. Change the width of PMOS to the value of width in layout and run LVS again. This time you will get an LVS match.

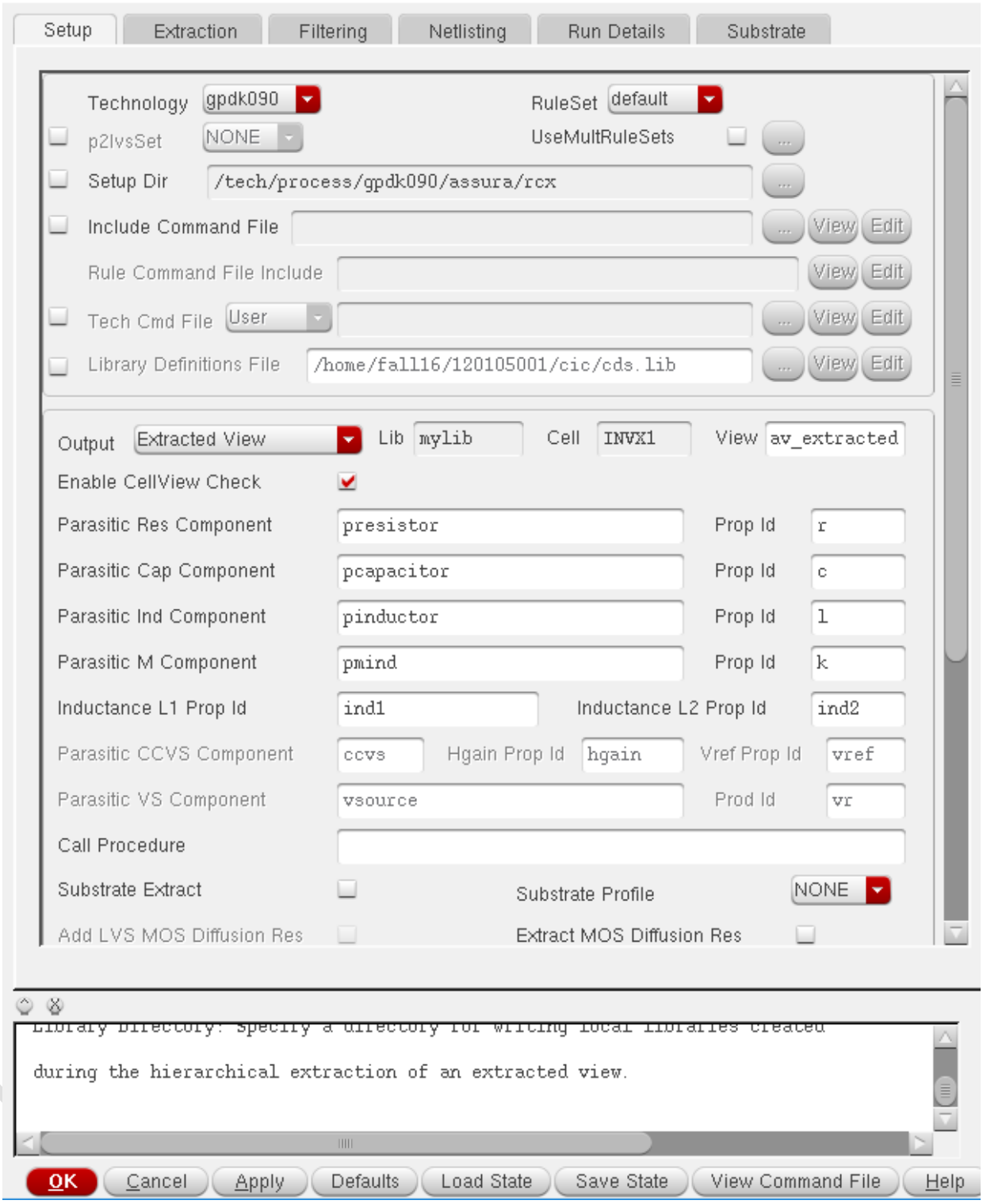


III. Parasitic Extraction by Quantus QRC

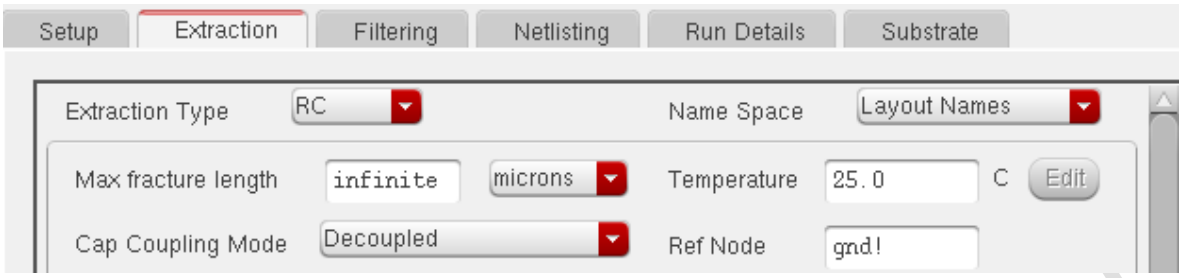
1. Execute ***Assura→Open Run***. Select the final error free lvs run name in the run name field (it automatically loads the last lvs run). Click **OK**.



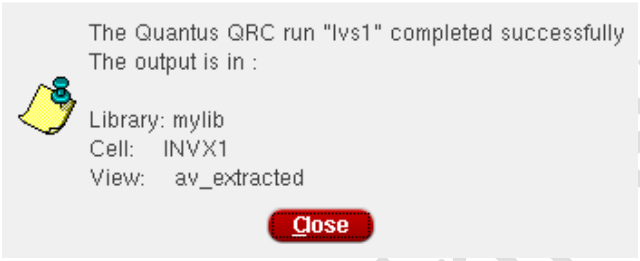
2. Execute ***Assura→Run Quantus QRC***. Select **Extracted View** in the **output** field under **Setup** tab.



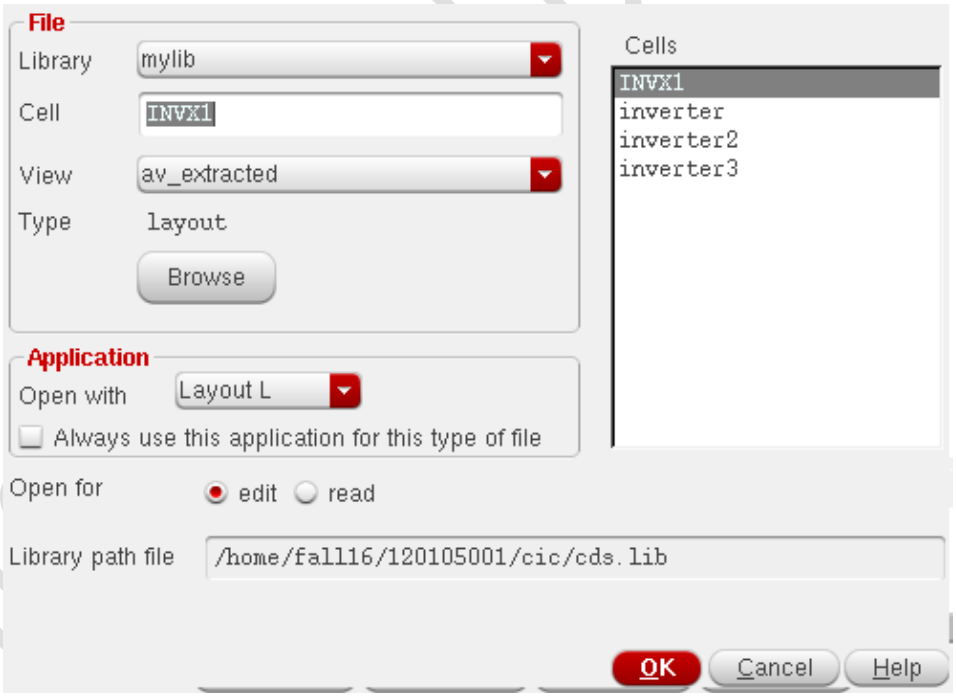
3. Go to **Extraction** tab. Select **RC** as **Extraction type** and put the name of your reference node (**gnd!** in the given case) and click **OK**.



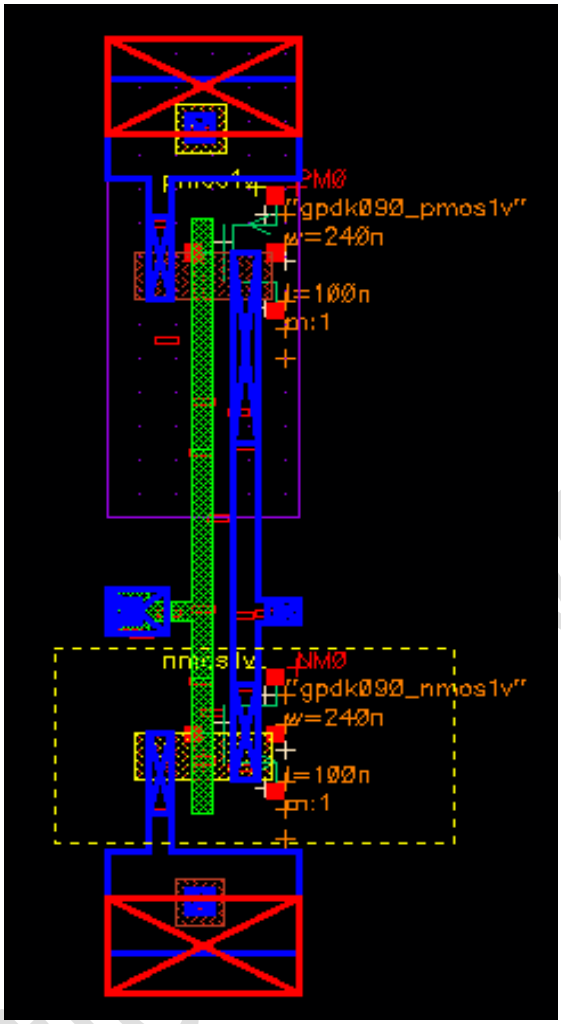
4. After completion of the run, you will get the following message:



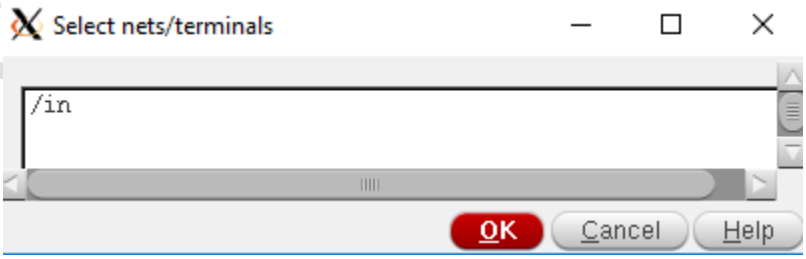
5. Execute ***File→Open*** and fill in the form as follows. Click **OK**.



An extracted view will open.



6. Now Launch ADE L from the **av_extracted** view and setup everything other than outputs to be plotted in the same way as you have done in Lab 1. After setting everything else, execute ***Outputs→To be plotted → Select on design***. Go to **av_extracted** view. Click on the **in** pin location on that view. The following window will appear. Select pin name **in** and click **OK**. Do the same for **out** pin.



Then run the simulation and observe the output waveforms. Then measure power and delay using waveform calculator.

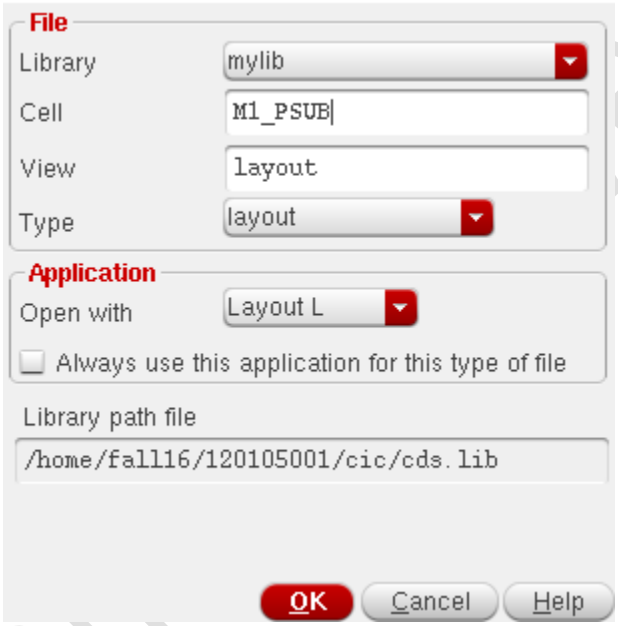
QUESTIONS:

What happens to delay and power consumption after parasitic RC effects are included? And explain why it happens.

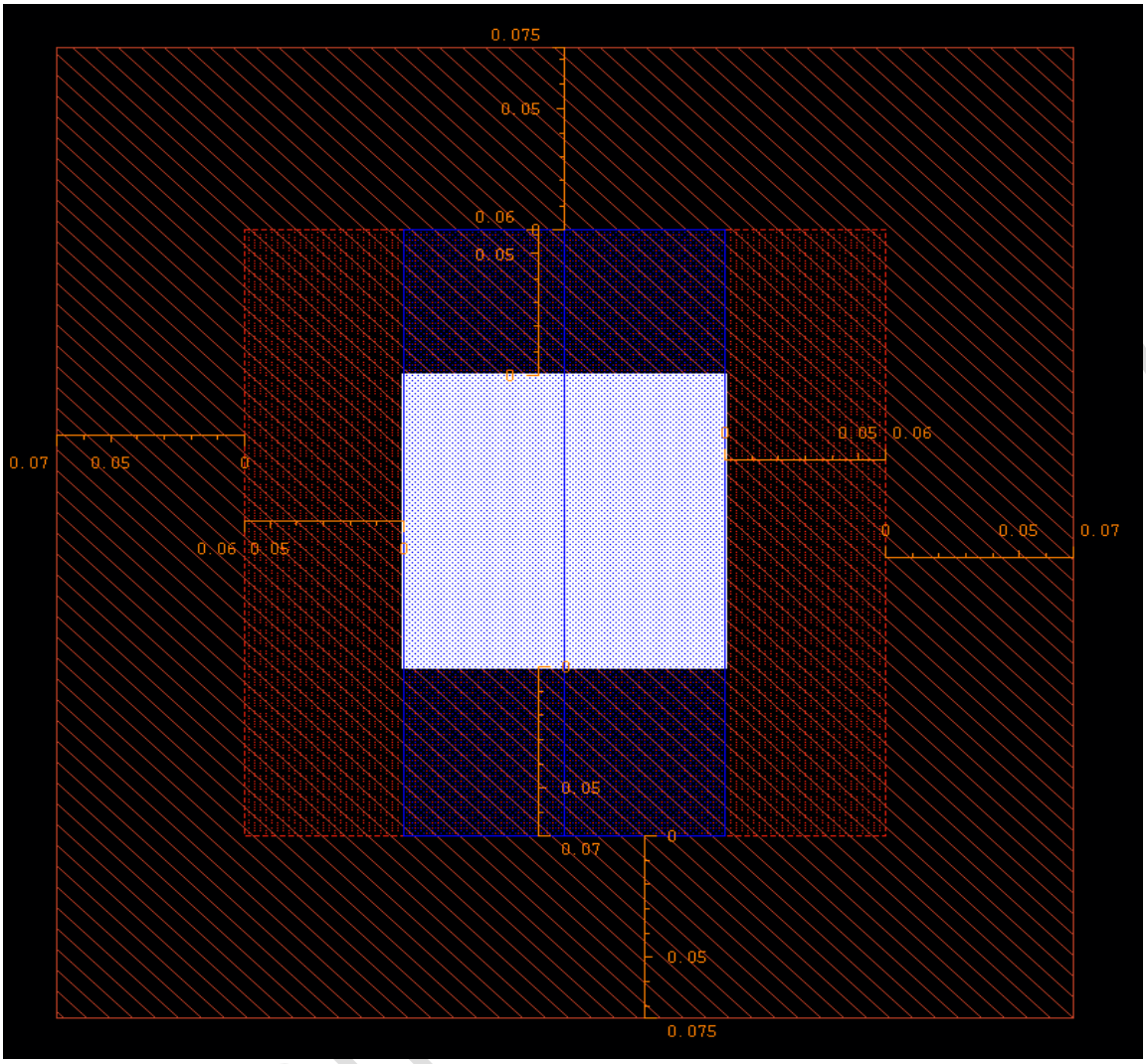
IV. Creating Layout views of Body ties

Now you know what body tie is. We will now make two instances for body ties one for **Psub** and one for **Nwell**.

1. Execute ***File→New→Cellview*** and fill in the New File form as follows. Click **OK**.



2. Draw psubstrate contact in the same way as you have made it in Lab3.



3. Save it and make nwell contact similarly (name it **M1_NWELL**), just change the **Pimp** layer to **Nimp** and everything else is the same.
Save these two for later use.