**International University**

School of Electrical Engineering

**CONCEPTS IN VLSI DESIGN LABORATORY**

**IT126IU**

**LAB 3**

**Layout of an Inverter using Virtuoso L**

**Submitted by**

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**GRADING GUIDELINE FOR LAB REPORT**

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A screenshot of a computer screen

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Figure 2 – PMOS Layout

A screenshot of a computer screen

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Figure 3 – The Final Layout

A diagram of a bus

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Figure 4 – A Generalized Standard Cell Height Concept

A diagram of a complex structure

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Figure 5 – Design Rules

**List of Tables**

Table 1 – Layer color, layer name and layer purpose

|  |  |
| --- | --- |
| **Color** | Matches the color in the Editing window. Each layer has its own color and pattern. Each layer has two colors associated with it: a fill color and an outline color. These colors can be changed to fit your taste by editing the technology file. |
| **Name** | The type of layer (Nwell, Oxide, Poly, Metal1, etc) |
| **Purpose** | In gpdk090 the only purpose classifications are: drw = drawing, slot = slot Drawing is used in layout, slot is used to create a hole for metal stress relief |

Table 2 – The rules related to the NMOS transistor

|  |  |
| --- | --- |
| Contact size | 0.12 **µ**m × 0.12 **µ**m (Fixed) |
| Poly width (Minimum) | 0.1 **µ**m (Fixed MOS gate length) |
| Contact to poly spacing (Minimum) | 0.1 **µ**m |
| Contact to oxide enclosure (Minimum) | 0.06 **µ**m |
| Poly/Nimp extending from oxide (Minimum) | 0.18 **µ**m (gate side enclosure) |
| Nimpenclosing oxide (Minimum) | 0.14 **µ**m (enclosure other than gate sides) |
| Minimum Metal 1 width | 0.12 **µ**m |
| Maximum Metal 1 width | 12.0 **µ**m |
| Minimum Metal 1 to Contact enclosure | 0.06 **µ**m (on at least two opposite sides) |

Table 3 – The rules related to the PMOS transistor

|  |  |
| --- | --- |
| Minimum Nwell width | 0.6 **µ**m |
| Minimum Nwell spacing to Nwell (same potential) | 0.6 **µ**m |
| Minimum Nwell spacing to Nwell (different potential) | 1.2 **µ**m |
| Minimum Nwell spacing to N+ active area | 0.3 **µ**m |
| Minimum Nwell spacing to P+ active area | 0.3 **µ**m |
| Minimum Nwell enclosure to P+ active area | 0.12 **µ**m |
| Minimum Nwell enclosure to N+ active area | 0.12 **µ**m |
| Minimum N+ Active Area to P+ Active Area Spacing | 0.16 **µ**m |

**Nomenclature**

NMOS = N-channel Metal-Oxide Semiconductor

PMOS = P-channel Metal-Oxide Semiconductor

CIW = Command Interpreter Window

GPDK = Generic Process Design Kit

IC = Integrated Circuit

ADE = Analog Design Environment

DRC = Design Rule Check

ERC = Electrical Rule Check

LVS = Layout Versus Schematic

EDA = Electronic Design Automation

FF = Fast-Fast

FS = Fast-Slow

TT = Typical-Typical

VDD = Drain Power Voltage

**Objectives**

* To create a layout view of the basic inverter circuit from scratch in Virtuoso Layout Editor
* To design the layout keeping basic design rules in mind
* To design cell layout of a constant height for use in hierarchical design

**Theoretical Background**

1. **Introduction to Layout, DRC and LVS**

* Layout is representation of a circuit in terms of planar geometric shapes (e.g. rectangles, polygons) showing the patterns of metal, polysilicon, oxide, or diffusion layers that make up the components (resistors, inductors, capacitors, transistors) of the integrated circuit.
* When using a standard process (e.g. 45nm, 90nm or 180nm process available in our lab), the behaviour of the final integrated circuit depends significantly on the positions and interconnections of the geometric shapes due to parasitic resistances and capacitances contributed by them. While designing a layout, designer must keep in mind performance (e.g. power-delay product) and size (area occupied by the chip) criterion.
* While designing digital circuits, one usually follows an ASIC design flow, where, the height of standard cells that are used is the same throughout the cell library, but their widths must vary according to their logical functions and drive strengths. The following figure shows a generalized standard cell height concept:

A diagram of a bus

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Although we will follow a full-custom IC design flow, we will maintain same cell height throughout our cell library.

The generated layout must pass a series of checks in a process known as physical verification. The most common checks in this verification process are:

* Design Rule Checking (DRC)
* Layout Versus Schematic (LVS) checking
* Parasitic extraction and post-layout simulation

**Design Rule Check (DRC):**

Design Rule Checking (DRC) is the process that determines whether the designed layout of a circuit satisfies a rules specified by the process being used.

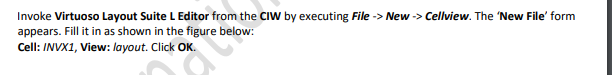
Design Rules are a series of rules (e.g. area, width, overlap, enclosure, extension, spacing) provided by semiconductor manufacturers which are specific to a particular semiconductor manufacturing process. Design rules specify certain geometric and connectivity restrictions to ensure that the process can fabricate the device properly.

**Layout versus Schematic (LVS) Check:**

The Layout Versus Schematic (LVS) is the verification step to determine whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design. A successful Design rule check (DRC) ensures that the layout conforms to the rules designed/required for faultless fabrication. However, it does not guarantee if it really represents the circuit we desire to fabricate. This is why an LVS check is used.

**Experimental Procedure**

1. **Layout design using Virtuoso Layout Suite L Editor**



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A black rectangular object with yellow lines and red squares

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A screenshot of a computer program

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**Discussion**

**What is Layout Design?**

**Layout design** refers to the process of placing and organizing a large number of elements of a design in a specific area. In electronics, **IC layout design** refers to the arrangement of circuit components (like transistors, resistors, etc.) and their connections on a semiconductor die. This process converts a circuit schematic into a physical design that can be fabricated on a chip.

**Rules a Designer Must Keep in Mind While Designing Layout**

1. Alignment and Consistency:

* Ensure components or elements are aligned consistently (grid-based approach is often helpful).
* Maintain uniform spacing between elements.

1. Hierarchy and Flow:

* Design the layout to provide a clear visual hierarchy, leading the user’s eye to the most important elements.
* Maintain a logical flow for readability and usability (e.g., left-to-right, top-to-bottom flow in text).

1. Aesthetic Balance:

* Use white space effectively to avoid clutter and provide breathing space for design elements.
* Maintain proportionate sizes of components for visual harmony.

1. Scalability and Responsiveness (in Web Design):

* Ensure the layout can adjust to different screen sizes and devices.

1. DRC (Design Rule Check) Rules in IC Design:

* Ensure compliance with Design Rule Checks (DRC) specific to the fabrication process, like spacing between components, minimum width of wires, and layer thicknesses.

**Why DRC Rules Are Provided by the Foundry**

In VLSI design, **Design Rule Check (DRC) rules** are a set of constraints provided by the **foundry** (the semiconductor fabrication company) to ensure that the chip can be manufactured reliably and within the tolerances of the fabrication process. These rules are to prevent fabrication errors, improve optimization, process compability and signal integrity and performance

**Best Practices and Principles for Layout Design**

1. Adhere to Foundry DRC Rules:

* Always respect the DRC rules provided by the foundry to ensure that the design is manufacturable and reliable.

1. Minimize Parasitic Effects:

* Parasitic capacitances and resistances can negatively affect the performance of circuits, so ensure minimum parasitic coupling by maintaining adequate spacing between components and reducing unnecessary interconnect lengths.

1. Optimize for Performance and Area:

* The layout should be compact without sacrificing performance. Optimize critical paths for speed by minimizing delays and ensuring robust power distribution.

1. Follow Symmetry (for Analog Design):

* In analog layout design, symmetry is essential to balance noise and improve matching characteristics of transistors.

1. Guard Rings and Shielding:

* Use guard rings and shielding techniques to reduce noise and interference between sensitive analog and digital sections.

1. Layer Management:

* Utilize layers efficiently to avoid congestion in metal routing and to ensure proper connectivity.

1. Plan for Future Scalability:

* Ensure that the layout is flexible enough to accommodate future design modifications, such as design scaling or adding new features.

1. Power Distribution Network (PDN):

* Ensure a robust power grid to avoid IR drop and maintain signal integrity. Power and ground layers should be optimized for minimal resistance and good distribution of power.

1. Electromagnetic Compatibility (EMC) and Signal Integrity:

* Design for minimizing cross-talk, noise, and signal degradation, especially in high-frequency designs.

1. Consider Yield and Manufacturability:

* While performance is critical, designing for manufacturability is also essential to ensure that the chip yields well in mass production.

**Appendix**

Appendix A (Shortcut keys for Cadence Virtuoso ® Layout Editor L)

|  |  |
| --- | --- |
| Shortcut Key | Tasks performed |
| f | Fit display to window |
| r | Draw rectangle |
| q | Edit property of an object |
| p | Makes a min width path of the layer selected in LSW |
| Ctrl+a | Select all |
| Ctrl+d | Deselect all |
| c | Copy |
| m | Move |
| s | Stretch side of a rectangle |
| k | Invoke ruler tool |
| Shift+k | Delete all rulers |
| i | Add an instance |
| u | Undo |
| Shift+u | Redo |
| e | Display options |
| o | Add via between layers |
| l | Create a label |

**Appendix B (gpdk090 Design Rules Guide (Abridged Version for VLSI-I Lab))**

**Terminology Definitions**

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**Appendix C (Some Most Commonly Violated Design Rules for gpdk090 technology)**

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