

AVR084: Replacing ATmega323 by ATmega32

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Introduction

This application note is a guide to assist current ATmega323 users in converting existing designs to the ATmega32. In addition to the functional changes, the electrical characteristics of the ATmega32 are different including an increase in operating frequency because of a change in process technology. Check the data sheet for detailed information.

ATmega323 Errata Corrected in ATmega32

The following items from the Errata Sheets of the ATmega323 do not apply to the ATmega32. Refer to the ATmega323 Errata Sheet for a more detailed description of the errata.

Interrupts Abort TWI Power-down

The TWI Power-down operation is no longer interrupted by other interrupts, and the TWI does not return to its idle state when interrupts occur during Power-down.

TWI Master does not Accept Spikes on Bus Lines

In ATmega32, a digital filter eliminates the problems with spikes triggering a false start condition. In addition, if a start condition is incorrectly received it will now generate the status code Bus Error and set TWINT when the SDA line goes to the idle state. Hence, the previous dead-lock situation has been eliminated.



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Microcontroller

Application Note

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TWCR Write Operation Ignored when Immediately Repeated

In ATmega32 consecutive write operations to the TWCR Register work as expected, and there is no need to insert a NOP in between.

PWM not Phase Correct

All Timers in ATmega32 have been redesigned to generate phase correct PWM.

TWI is Speed Limited in Slave Mode

The speed limit in Slave mode does not apply to ATmega32. In ATmega32, the CPU clock frequency in the slave must be at least 16 times higher than the SCL frequency, as described in the data sheet.

Problems with UBRR Settings

In ATmega32, any change made to the Baud-rate Registers will take effect immediately, so that all following transmissions/receptions are according to the new baud rate setting. Writing to UBRRH does not clear UBRRH. The work around in the Errata Sheet for ATmega323 is upward compatible with ATmega32, even though two out-operations to UBRRH are now redundant.

Missing OverRun Flag and Fake Frame Error in USART

The OverRun Flag in ATmega32 is always associated with the current FIFO stage, and no fake Frame Error is generated on OverRun.

Changes to Names

The following control bits have changed names, but have the same functionality and placement when accessed as in ATmega323:

Table 1. Changed Bit Names

Bit Name in ATmega323	Bit Name in ATmega32	I/O Register (ATmega323)	Comments
PWMn(0)	WGMn0	TCCRn(A)	"A" and "0" in 16-bit timer only
PWMn1	WGMn1	TCCRnA	
CTCn	WGMn2	TCCRn(B)	"B" in 16-bit timer only
ASB	RWWSB	SPMCR	
ASRE	RWWSRE	SPMCR	

The following I/O Register has changed name, but include the same functionality and placement when accessed as in ATmega323:

Table 2. Changed Register Names

Register Name in ATmega323	Register Name in ATmega32	Comments
ADCSR	ADCSRA	

Improvements to Timer/Counters

For details about the improved and additional features, please refer to the data sheet. The following features have been added:

- Variable top value in PWM mode.
- Timer/Counter0 extended with compare function and PWM.
- For Timer/Counter1, Phase and Frequency Correct PWM mode in addition to the Phase Correct PWM mode.

Updating of OCR in PWM mode (Applies to all Timer/Counters)

In PWM mode, the value written to the Output Compare Register is not physically used as compare value until the Timer/Counter reaches the value TOP. The interpretation of this point of time differs between ATmega323 and ATmega32. In ATmega323, the new OCR value is used in the cycle where the Timer/Counter has the value TOP. In ATmega32, the counter value TOP is used to update the compare value, i.e., it is first active in the cycle where the Timer/Counter has the value TOP-1 down-counting.

Improvements to ADC

The ADC in ATmega32 supports differential and amplified measurements.

Changes to Electrical Characteristics

The ATmega32 is produced in a different process than the ATmega323 and electrical characteristics will thus differ between these devices. As an example the I_{CC} during Power Down Sleep Mode for the ATmega323 is $\sim 4\mu A$ while ATmega32 has $\sim 15\mu A$. Please consult the data sheets for further details on electrical characteristics.

Changes to EEPROM Write Timing

In ATmega323, the EEPROM write time takes 2,048 cycles of the calibrated RC Oscillator. In ATmega32, the EEPROM write time takes 8,448 cycles of the calibrated RC Oscillator. This is in both devices regardless of the clock source and frequency of the system clock. The calibrated RC Oscillator is assumed to be calibrated to 1.0 MHz in both devices.

Note: Changing the value in the OSCCAL Register affects the frequency of the calibrated RC Oscillator and hence the EEPROM write time.

Programming Interface

The Parallel Programming algorithm is changed. In Parallel mode, the ATmega32 supports Page Programming of the EEPROM. The timing requirements for Parallel Programming have been changed. See the ATmega32 data sheet for details.

The STK500 supports both In-System Programming and Parallel Programming of the ATmega32.

Fuse Settings

ATmega32 contains more fuses than ATmega323. Table 3 shows the ATmega323 compatible Fuse settings. Some of the Fuses are described further in the following sections.

Table 3. Comparing Fuses in ATmega323 and ATmega32⁽¹⁾

Fuse	Default ATmega323 Setting	Default ATmega32 Setting	ATmega323 Compatible Setting
OCDEN	–	1	1
JTAGEN	0	0	0
SPIEN	0	0	0
CKOPT	–	1	0 ⁽²⁾
EESAVE	1	1	1
BOOTSZ 1	1	0	1
BOOTSZ 0	1	0	1
BOOTRS T	1	1	1
BODLEV EL	1	1	1
BODEN	1	1	1
SUT1	–	1	See note ⁽³⁾
SUT0	–	0	See note ⁽³⁾
CKSEL3	0	0	See note ⁽³⁾
CKSEL2	0	0	See note ⁽³⁾
CKSEL1	1	0	See note ⁽³⁾
CKSEL0	0	1	See note ⁽³⁾

- Notes:
1. A dash indicates that the fuse is not present in ATmega323.
 2. See “Oscillators and Selecting Start-up Delays” on page 4.
 3. The CKSEL Fuses are available in both ATmega323 and ATmega32. However, the SUT and CKSEL setting should be reconsidered when moving to ATmega32. See “Oscillators and Selecting Start-up Delays” on page 4.

Oscillators and Selecting Start-up Delays

In ATmega323, the CKSEL Fuses selects both which Oscillator is active, and the duration of the Start-up delay. In ATmega32, the active Oscillator and its frequency range is selected by the CKSEL Fuses, while the SUT Fuses selects Start-up delay for the given Oscillator. Hence, the CKSEL Fuse setting from ATmega323 must be reconsidered when moving to ATmega32. Follow the guidelines from the section “System Clock and Clock Options” in the ATmega32 data sheet to find appropriate start-up values.

The crystal Oscillator in ATmega323 is capable of driving an addition clock buffer from the XTAL2 output. In ATmega32, this is only possible when the CKOPT Fuse is programmed. In this mode the Oscillator has a rail-to-rail swing at the output, but at the expense of higher power consumption. Hence, do only program this fuse when rail-to-rail swing is required.

Changes to Watchdog Timer

The frequency of the Watchdog Oscillator in ATmega32 is close to 1.0 MHz for all supply voltages. The typical frequency of the Watchdog Oscillator in ATmega323 is close to 1.0 MHz @ 5 V, but the Time-out period increases with decreasing V_{CC} . This means that the selection of Time-out period for the Watchdog Timer (in terms of number of WDT Oscillator cycles) must be reconsidered when porting the design to ATmega32. Refer to the data sheet for ATmega32 for further information.

Improvements to JTAG Interface

Both ATmega323 and ATmega32 support a JTAG TAP interface for On-Chip debugging, Boundary-scan testing, and programming through the JTAG interface.

The number of scan cells in ATmega32 is higher than in ATmega323 to give better support for analog connections. Use the ATMEL provided Boundary-scan Description Language (BSDL) file for the appropriate device when creating the production test for the circuit board, and refer to the data sheet for description of the analog functions. As shown in the BSDL file, also the JTAG Device-ID has been changed from ATmega323 to ATmega32.

JTAG instructions PROG_PAGELOAD and PROG_PAGEREAD have been changed from using a virtual Flash Page Register in ATmega323 to accessing an 8-bit data register in ATmega32. This improvement makes it possible to use JTAG Page Programming regardless of where in the scan chain the AVR is. The improvement comes at an expense of higher number of vectors to program the same amount of flash.

The instruction set is extended by a BREAK instruction that is interpreted by the On-chip Debug system as an additional source of break. This makes the maximum number of Break Points in ATmega32 unlimited, while the number of Break Points in ATmega323 is limited by the number of Break Point comparators.

Self-Programming

Both ATmega32 and ATmega323 supports Self-Programming. In ATmega323 the CPU is halted both during Page Erase and during Page Write. In ATmega32, the CPU is only halted when programming the No-Read-While-Write – NRWW – section of the Flash memory. The SPEN bit in the SPMCR Register will be auto-cleared in both devices. This means that a Boot Loader for ATmega323 can be written without polling for completion of the erase or the write operation. If this is the case, porting the code to ATmega32 requires rewriting the code to poll for SPEN to go low before starting a new Page Erase, Page Write or writing the Lock bits command.

However, the data sheet for ATmega323 recommends this polling operation for compatibility with future devices, so as long as this recommendation is followed, the Boot Loader can be used in ATmega32 without modification.

Other Concerns

The ATmega32 has a signature byte different from the one used in ATmega323. Make sure you are using the signature byte of ATmega32 when porting the design.

Be aware that EEPROM write access must be completed before entering power-down sleep mode. Otherwise the system oscillator will continue to run, drawing additional current.



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