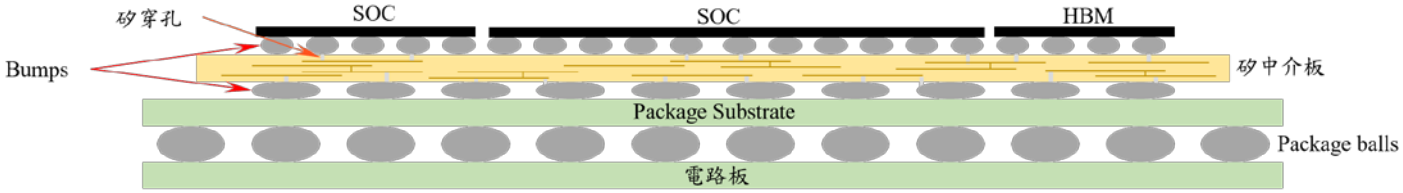
r12522545 吳世瑜

1. (20%) Please answer the following questions. Your answer should contain pictures and texts for a better explanation. A single page of A4 is recommended.
   (a) By using TSMC's CoWoS technology, Nvidia puts computing chip and high-bandwidth memory together and makes H100, its most powerful GPU. Explain what CoWoS is, how it works, what it is different from other packaging technology, and where it can be used. (學號尾數為單號者回答此題)

CoWoS(Chip-on-Wafer-on-Substrate)

台積電獨創的 2.5D 晶圓級多晶片封裝技術，在矽中介層上並排整合多個晶片，以實現更好的互連密度和性能，如下圖各個晶片透過矽中介板上的微凸塊黏合，形成晶圓上晶片 (CoW)。



CoWoS 製程技術，首先從製作一個矽中介層開始。這個中介層實際上就是一個像晶片大小的基板，上面有一堆穿越矽穿孔（TSV）的小孔，這些小孔允許將晶片電性連接在一起。

當中介層製作完成後，會將這些晶片黏貼在中介層上。這個黏貼的過程叫做 WLCSP，是一個高密度的封裝技術，可以在一個晶圓上整合多個晶片。

接著，需要將整個封裝切割成單個獨立的封裝，這些獨立的封裝會被安裝在一個基板上。總結來說，CoWoS 是一個非常適用於需要高頻寬和高度整合的應用領域的高性能封裝技術。

台積電於 2012 年首次開發了用於先進晶片的 CoWoS 封裝，並於 2016 年與 HBM 結合。 聊天機器人和生成式人工智慧的興起產生了對高頻寬記憶體(HBM)的需求，這加劇了對 CoWoS 的需求，目前該晶片封裝已佔總收入的 7%。

- CoWoS 技術允許將**多個晶片整合**在一個封裝中，這些晶片可以包括處理器、記憶體、圖形處理器等，這樣可以提高系統性能。不同種類的晶片可以在同一個封裝內以高度緊湊的方式組合在一起，**減少了晶片之間的距離**，降低了延遲。
- CoWoS 技術還可以**降低功耗**，因為它允許晶片之間的高效通信和散熱，並提供更好的電源管理。
- 由於 CoWoS 技術的使用，晶片可以更加緊湊地堆疊在一起，這樣可以實現更高的集成度，同時**減小占地面積**，這在許多應用中都非常重要，特別是移動設備和高性能計算。
- CoWoS 技術還提供了高頻寬的**晶片內互連**，這有助於實現更快的數據傳輸速度，這對於高性能應用非常關鍵。
- 雖然 CoWoS 技術在技術上較為複雜，但它可以幫助設計更簡單、更**節省成本**的系統，因為它消除了某些傳統封裝技術所需的一些組件和接口。

2. (15%) Please draw the compound gate using only NAND, NOR, and INV gates for the following function

(a) $Y = \overline{(\bar{A} \cdot B)} + \overline{(B \cdot C)}$

(b) $Y = \overline{(A \oplus B)} \cdot \overline{(C + \bar{D})}$

(c) $Y = \overline{(A \oplus (B \cdot C)) + (D \oplus E)}$

NAND

0	0	1
0	1	1
1	0	1
1	1	0

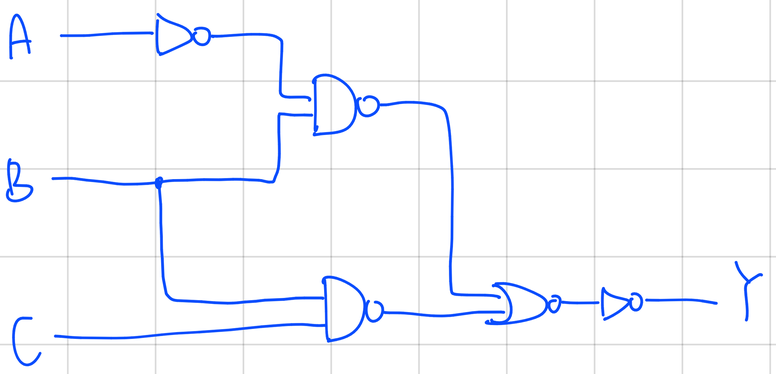
NOR

0	0	1
0	1	0
1	0	0
1	1	0

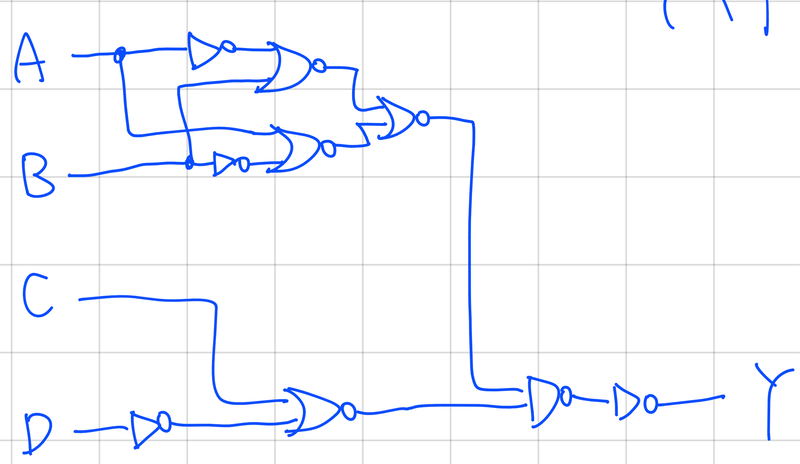
XOR

0	0	0
0	1	1
1	0	1
1	1	0

(a)



(b)



(c)

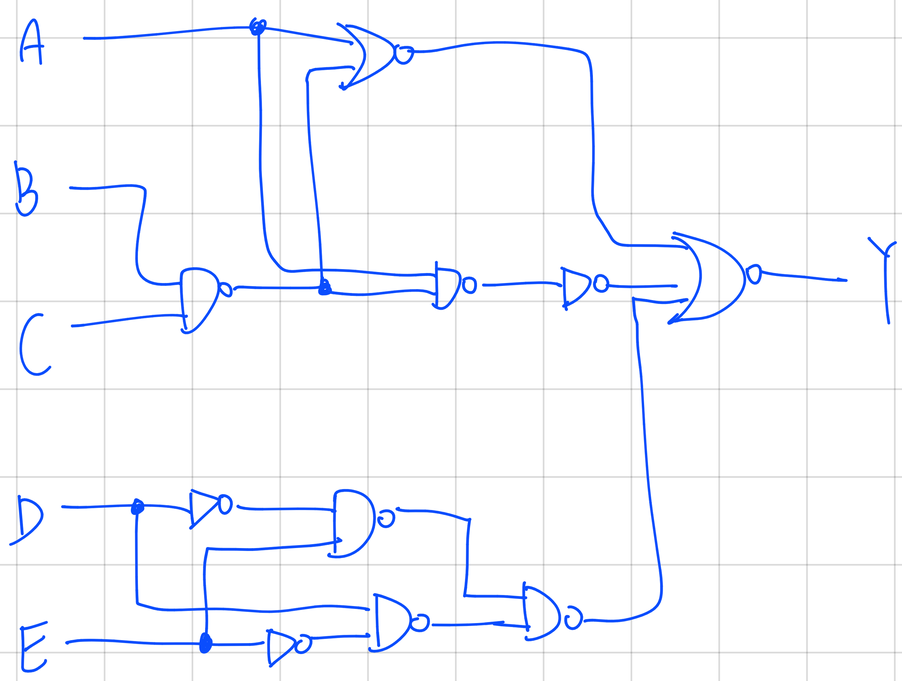
$$Y = \overline{(A \oplus (B \cdot C)) + (D \oplus E)}$$

$$= \overline{(A \oplus (B \cdot C))} \cdot \overline{(D \oplus E)}$$

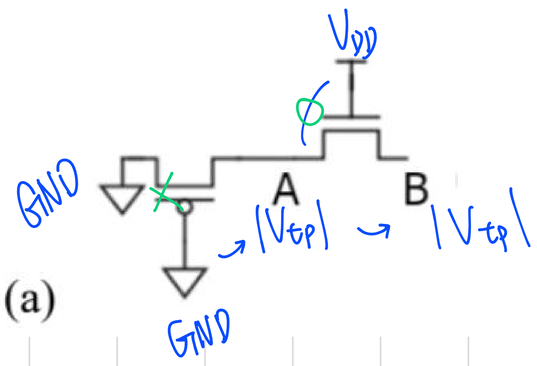
$$= \overline{(\bar{A}(B \cdot C) + A\overline{(B \cdot C)})} \cdot \overline{(\bar{D}E + D\bar{E})}$$

$$= \left[\overline{\bar{A} \cdot (B \cdot C)} \cdot \overline{A \cdot \overline{(B \cdot C)}}\right] \cdot \left(\overline{\bar{D} \cdot E} \cdot \overline{D \cdot \bar{E}}\right)$$

$$= \left[A + \overline{(B \cdot C)}\right] \cdot \left\{\bar{A} + (B \cdot C)\right\} \cdot \overline{(\bar{D} \cdot E)} \cdot \overline{(D \cdot \bar{E})}$$



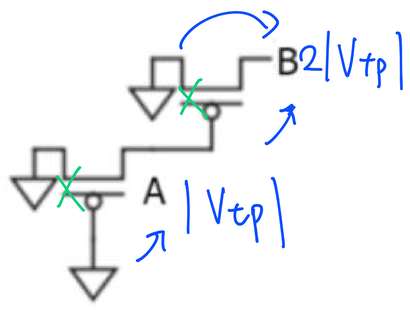
3. (20%) Please express **all the node voltages** in the pass transistor networks shown below (neglect the body effect).
(You can use **V_{DD}, GND, $|V_{tp}|$, or V_{tn}** to express your answer.)
(Assume that every NMOS has the same threshold voltage, and so does the PMOS.)



(a)

A = $|V_{tp}|$

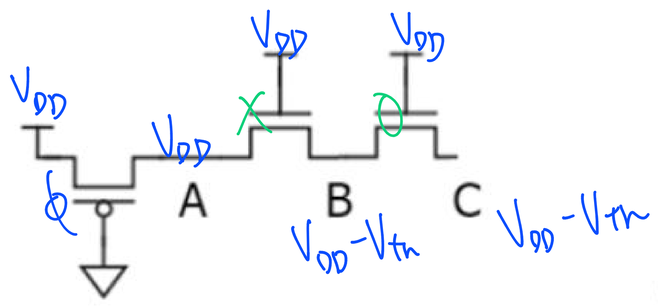
B = $|V_{tp}|$



(b)

A = $|V_{tp}|$

B = $2|V_{tp}|$

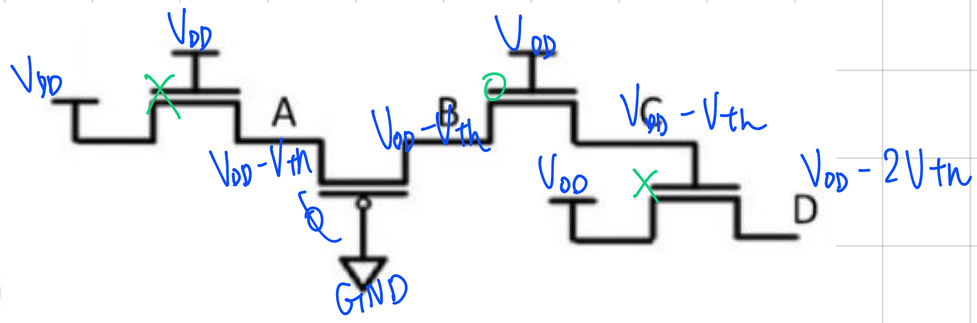


(c)

A = V_{DD}

B = $V_{DD} - V_{tn}$

C = $V_{DD} - V_{tn}$



(d)

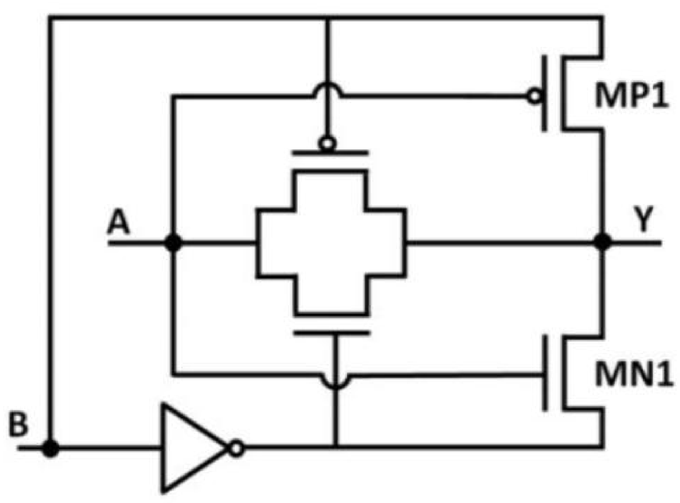
A = $V_{DD} - V_{tn}$

B = $V_{DD} - V_{tn}$

C = $V_{DD} - V_{tn}$

D = $V_{DD} - 2V_{tn}$

4. (20%) For the following transmission-gate circuit,
(a) (10%) Please show the function of this circuit.
Hint: You can use the truth table method to find the function of Y.
(b) (10%) Is there any bad-zero or bad-one problem in this circuit? **Explain why.** (Bad-one means the voltage of logic-1 is only VDD-V_{tn}; bad-zero means the voltage of logic-0 is $|V_{tp}|$)



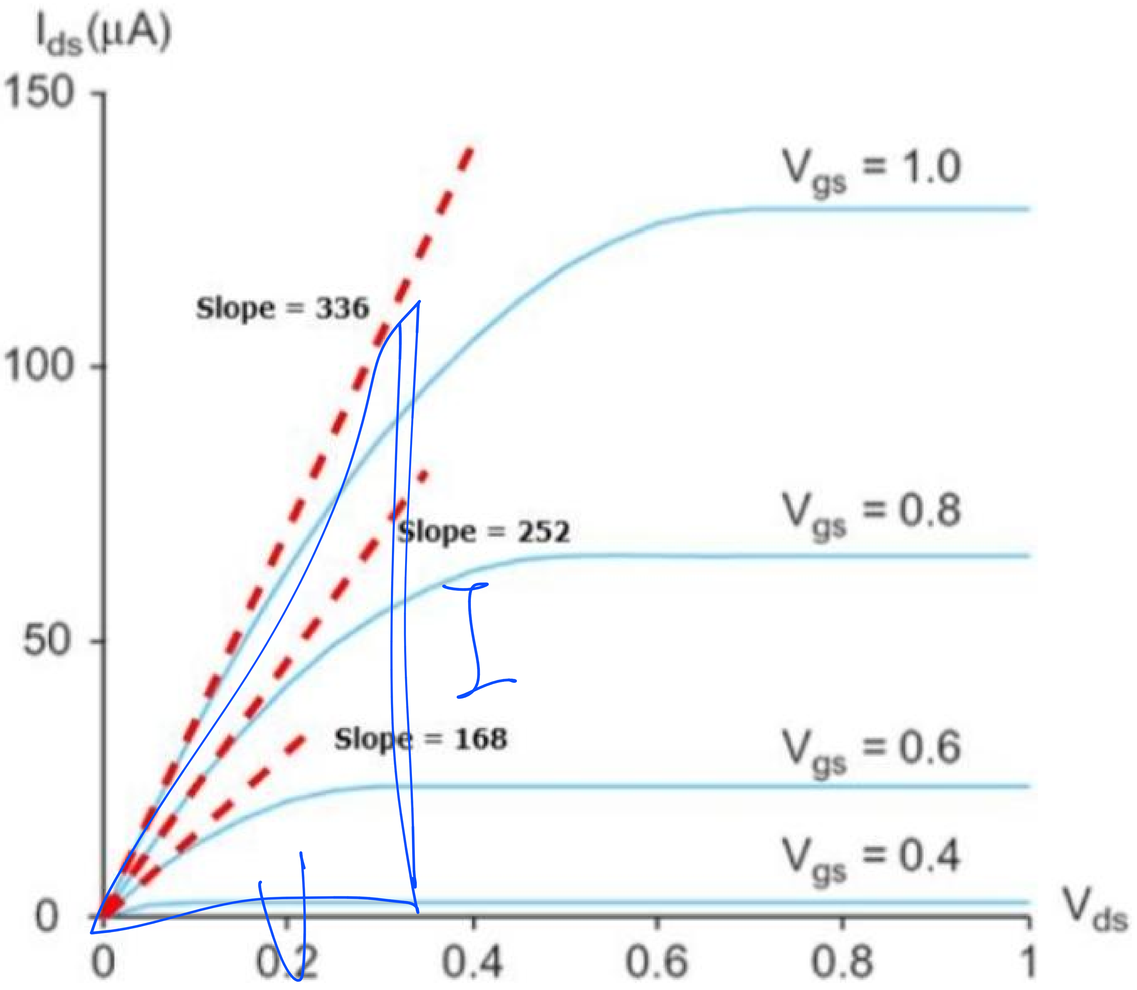
(a)

A	B	Y	
0	0	0	⇒ 中間 MOS 通 ⇒ strong 0
0	1	1	⇒ 1 來自 MP1 ⇒ strong 1
1	0	1	⇒ 中間 MOS 通 ⇒ strong 1
1	1	0	⇒ 0 來自 MN1 ⇒ strong 0

⇒ $Y = A \oplus B$

→ No bad 0 or 1

5. (10%) For the following I-V curves of an NMOS transistor, given the slope at 0 for the top three curves, estimate a precise value of V_t (小數點以下兩位). Explain how you find this value from the three slopes.



$$\text{Slope} = \frac{I_{ds}}{V_{ds}}$$

$$I_{ds} = \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds}$$

$$\frac{I_{ds}}{V_{ds}} = \text{Slope} = \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)$$

(在接近0的地方)

$$336 = \beta(V_{gs1} - V_t)$$

$$252 = \beta(V_{gs2} - V_t)$$

$$168 = \beta(V_{gs3} - V_t)$$

$$\Rightarrow \frac{336}{252} = \frac{1 - V_t}{0.8 - V_t} \Rightarrow V_t = 0.2$$

$$\frac{336}{168} = \frac{1 - V_t}{0.6 - V_t} \Rightarrow V_t = 0.2$$

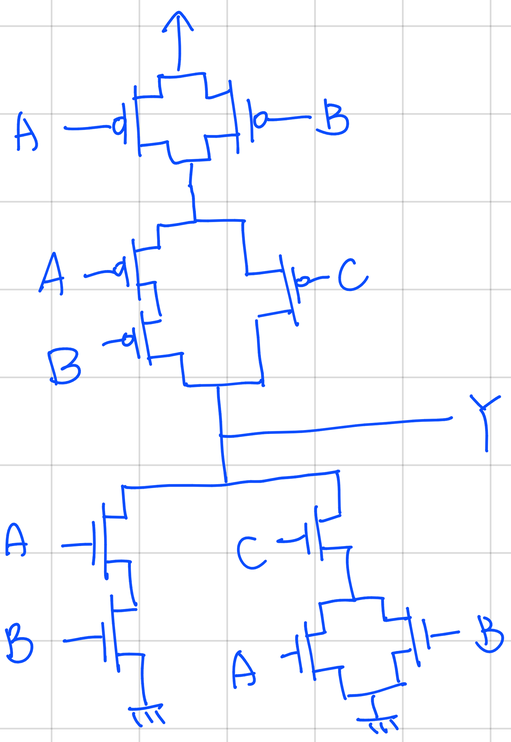
$$\frac{252}{168} = \frac{0.8 - V_t}{0.6 - V_t} \Rightarrow V_t = 0.2$$

$$V_t = 0.2\ \text{V}$$

6. (15%) A 3-input minority gate returns output "**1**" if no more than two of the inputs are "**1**".
   (a) (5%) Sketch a **transistor-level** circuit diagram for a 3-input minority gate using a single stage of CMOS static logic. Please use the least number of transistors. Note that all three inputs and their complements are available for this circuit.
   (b) (10%) Design a 3-input minority gate using CMOS **NANDs**, **NORs,** and **inverters**. Compare the numbers of transistors required in (a) and (b).

(a)

A	B	C	Y
0	0	0	1
1	0	0	1
0	1	0	1
0	0	1	1
1	1	0	0
1	0	1	0
0	1	1	0
1	1	1	0

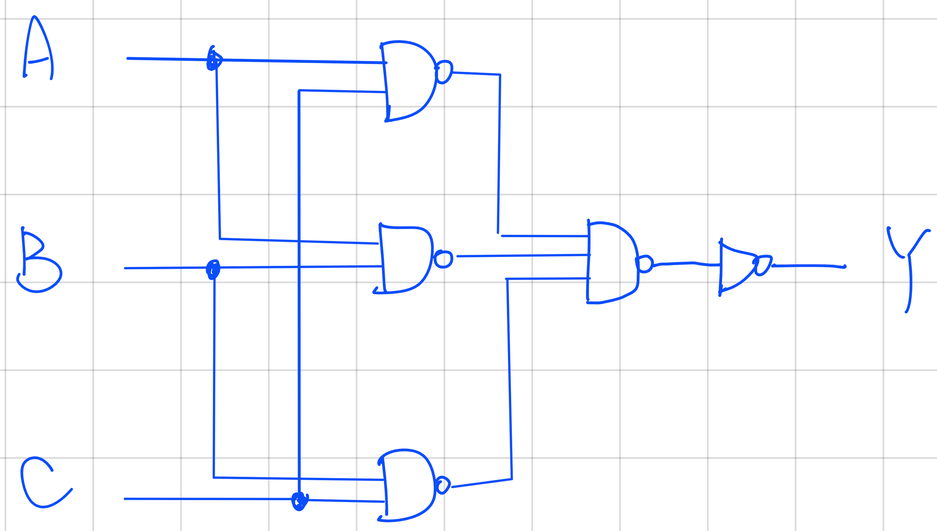


⇒ 10 個 CMOS

$$\overline{(A\cdot B)+(B\cdot C)+(A\cdot C)} = \overline{A\cdot B+(A+B)\cdot C}$$

$$\overline{Y}=(A\cdot B)+(B\cdot C)+(A\cdot C)$$

(b)



⇒ NAND：4 個 CMOS
INV：2 個 CMOS
總 4×4+2=18

⇒ 用 CMOS 組成的較少