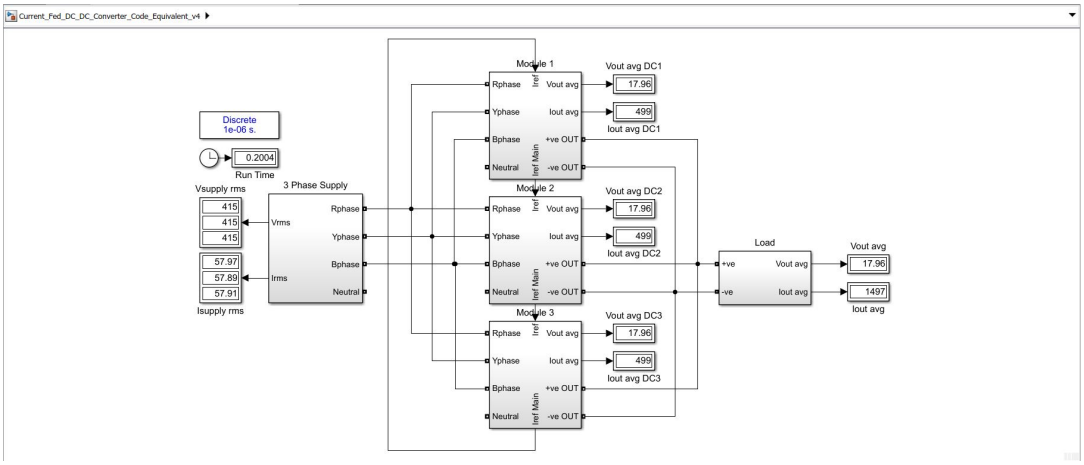
| | | |
|---|---|---|
| **Doc. No.** | | |
| **Equipment Type** | 9 kW SMPS | |
| | | |

**Entire System:**

3 DC-DC Converters of 9kW Power Rating are connected in parallel at the output side. The simulation has been run for 200ms. It has the following parameters:

V_supply = 415Vrms

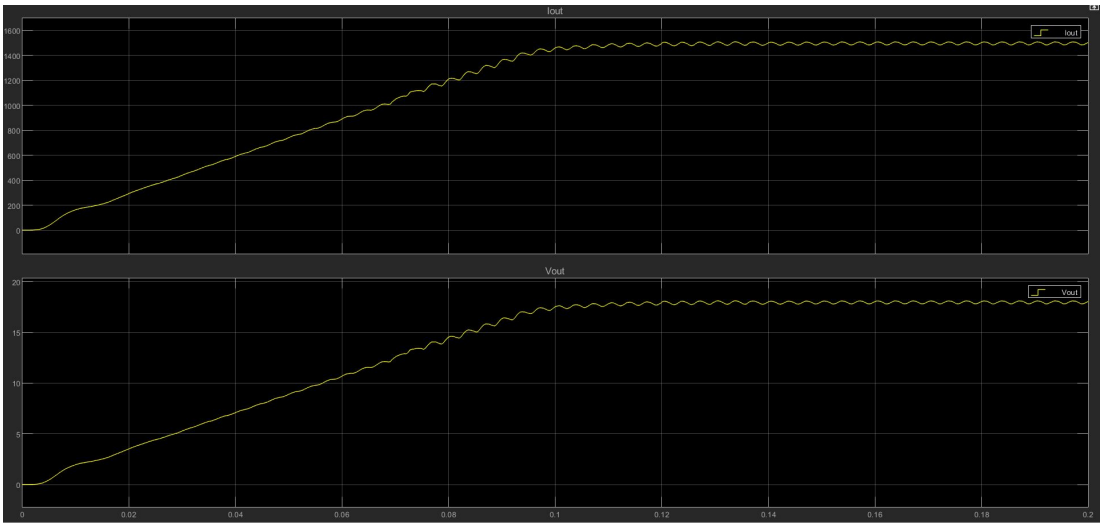
f_supply = 50Hz



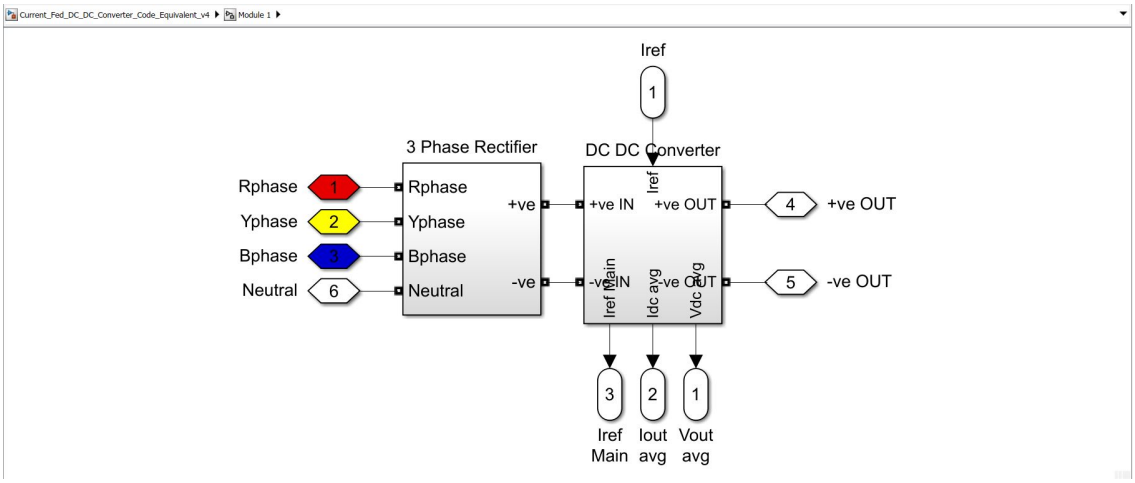

Here, Module 1 is the Master Module, while Module 2 and Module 3 are slave modules (it will be explained later what exactly is meant by “Master” and “Slave” modules). These modules are connected in parallel at both the input side and the output side. Each module regualtes an output voltage of 18V and has the capability of pumping out 500A of current.

**Load Waveforms:**

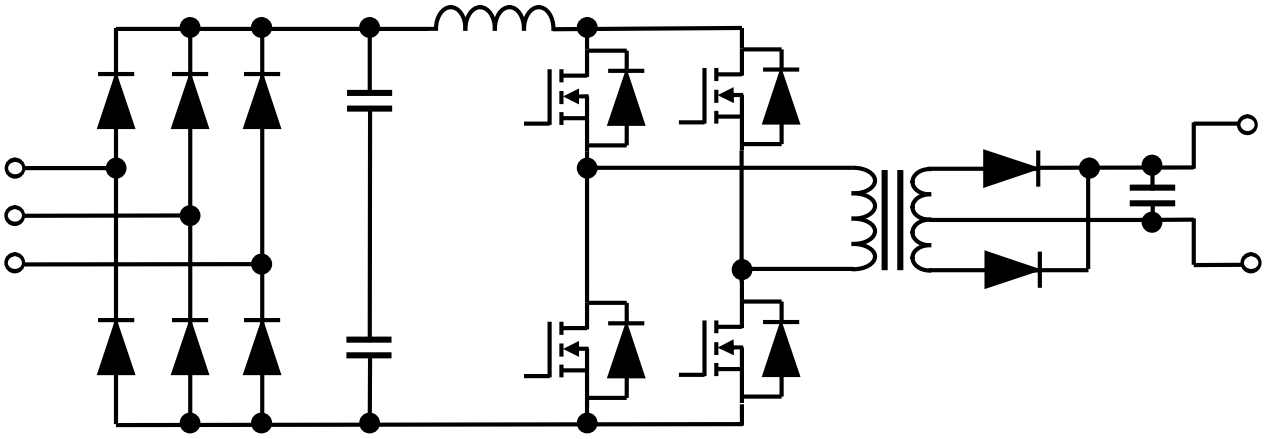
Here, the load voltage is 18V and the load current is 1500A (since 3 modules are connected in parallel). The observed ripple on the voltage waveform has a frequency of 300Hz and peak to peak amplitude of 300mV. Similarly, the observed ripple on the current waveform has a frequency of 300Hz and peak to peak amplitude of 25A.



**Individual module:**




Each unit consists of a 3 Phase Diode Bridge Rectifier followed by a Current fed DC-DC Converter. Currently, the input current THD is not below 5% and hence either the uncontrolled rectifier will be replaced by a controlled recitifer or a PFC will be implemented in the DC Link (However these 2 solutions have not been worked upon yet). The current fed converter is expected to easily be connected in parralel on the output side without implementing any other software based solutions to take care of circulating current.

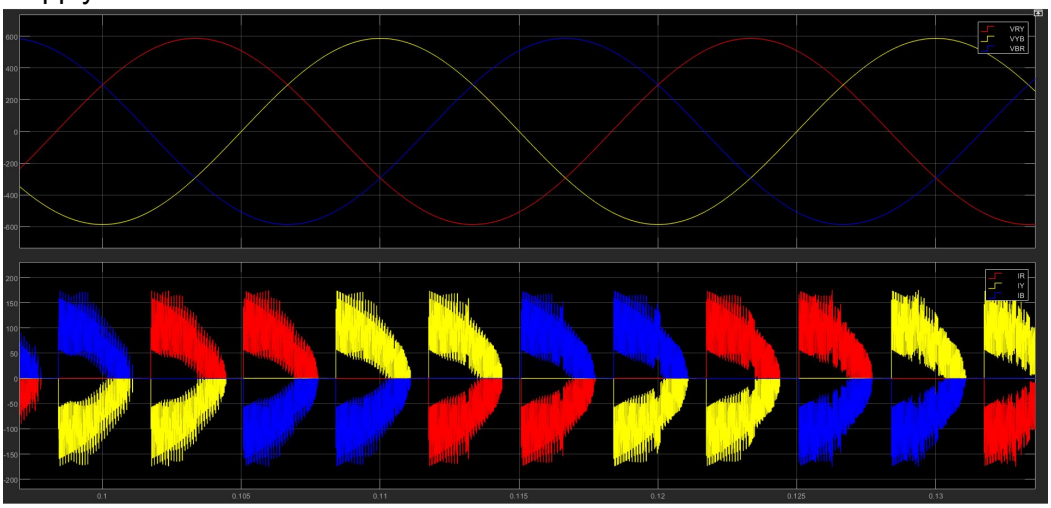


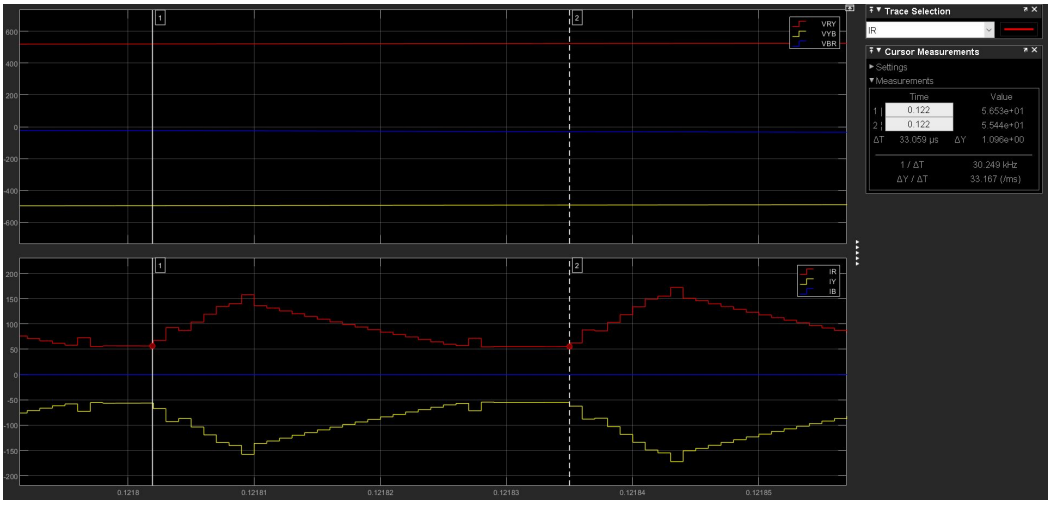
**Supply Waveforms:**

Vsupply = 415V rms

Isupply = 58A rms

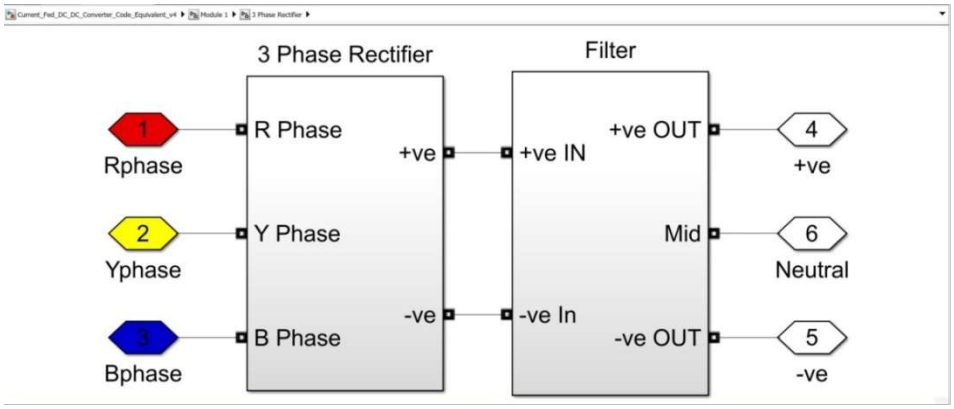
fsupply = 50Hz



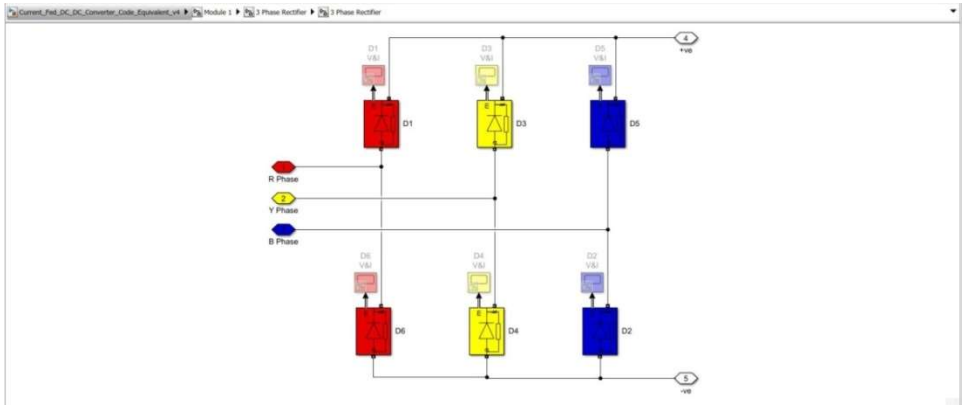

It has been observed that the twice of the high switching frequency of the DC-DC converter (i.e. 2 x fsw = 2 x 15kHz = 30kHz) has reflected back at the supply current waveform.

**First Stage:**



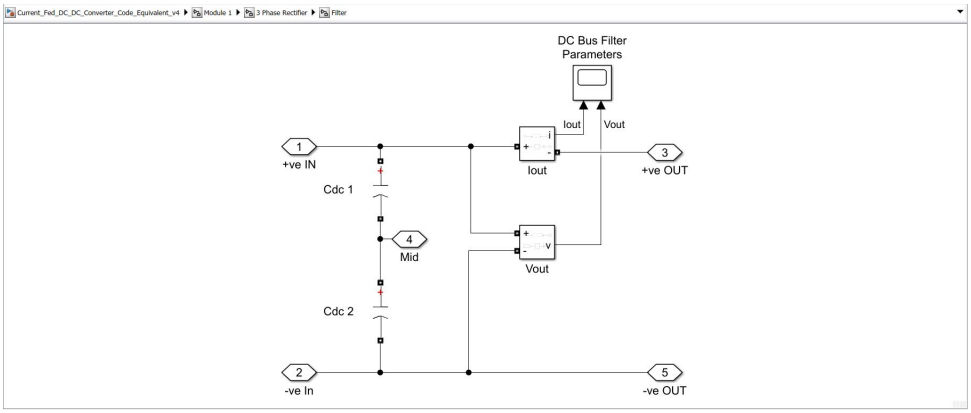

**3 Phase Diode Bridge Rectifiers**:

First Stage consists of a diode based 6 pulse three phase uncontrolled rectifier.

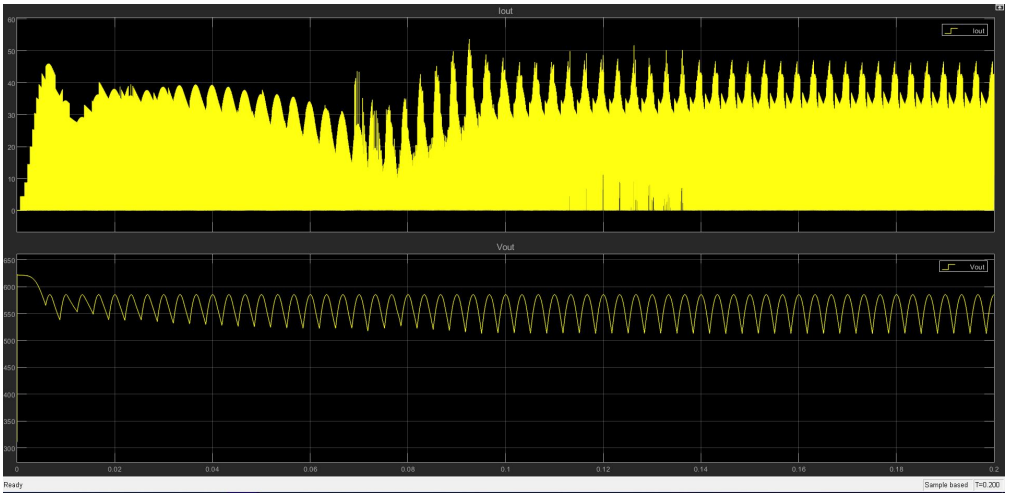


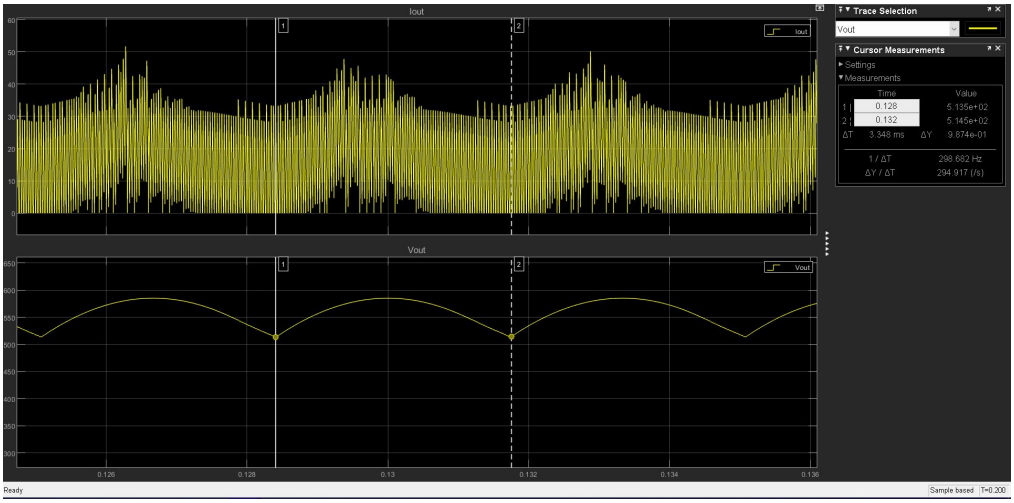

**DC Filter for 3 Phase Rectifier:**

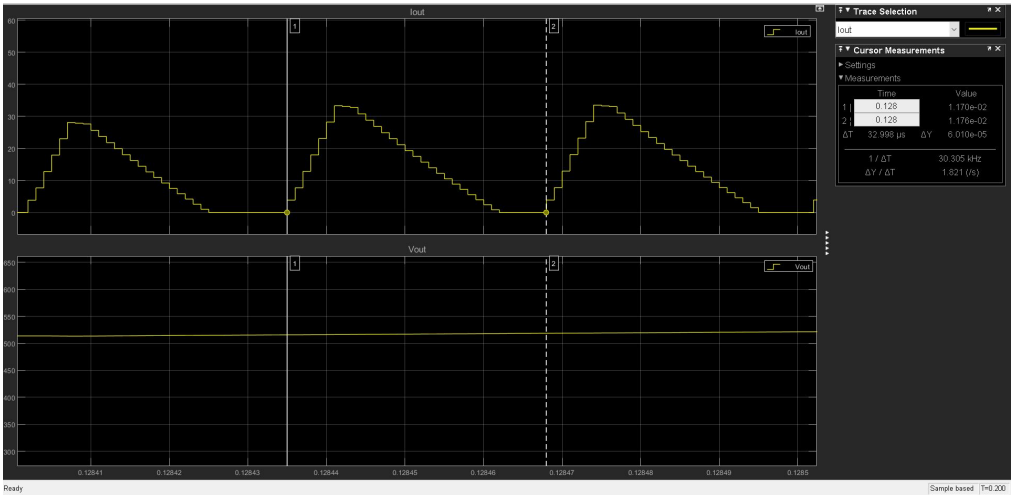
2 series connected filter capacitors of each of the value 220μF has been connected across the DC Link. Thus the equivalent capacitance connected across the DC Link is 110μF. Note: This capacitor is inadequate to filter out the 300Hz ripple created by the 3phase rectifier. It was connected because we were experimenting with the feasibility of connecting a Zig-Zag transformer for mitigating the high input current THD problem, and hence needed a DC midpoint for the same.



## 3 Phase Rectifier Output Waveforms:

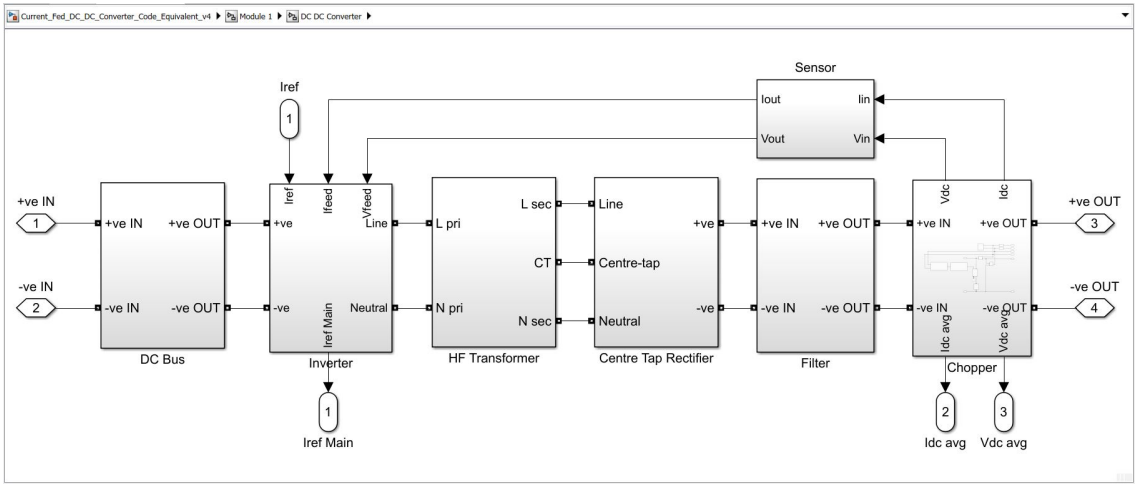


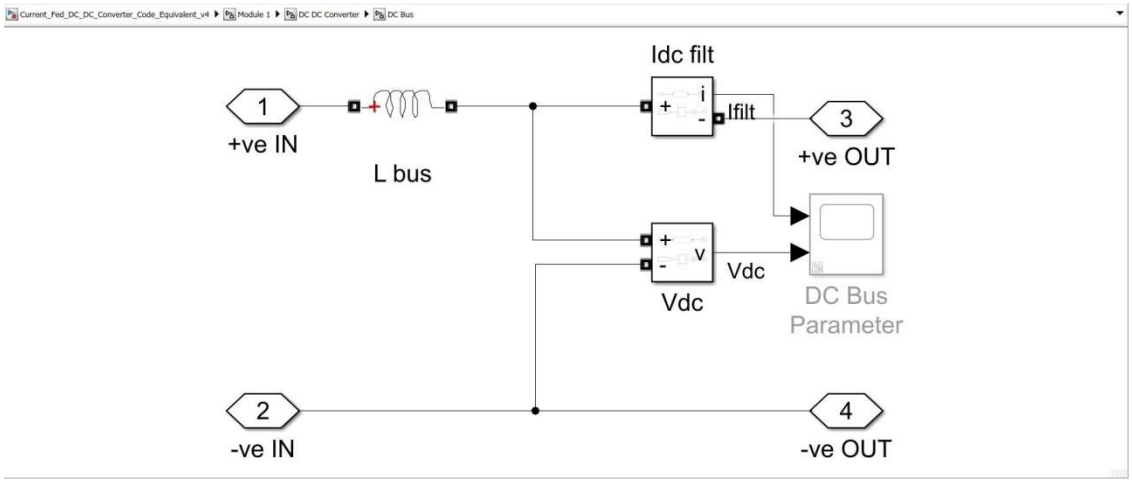
**Second Stage:**

The second stage consists of a current driven DC-DC converter. It is made up of an inductor in the DC link (this inductor stores the energy and then discharges it with the help of the inverter), followed by a full bridge converter, followed by a high frequency transformer, followed by a centre tap full wave rectifier and finally followed by a DC filter.



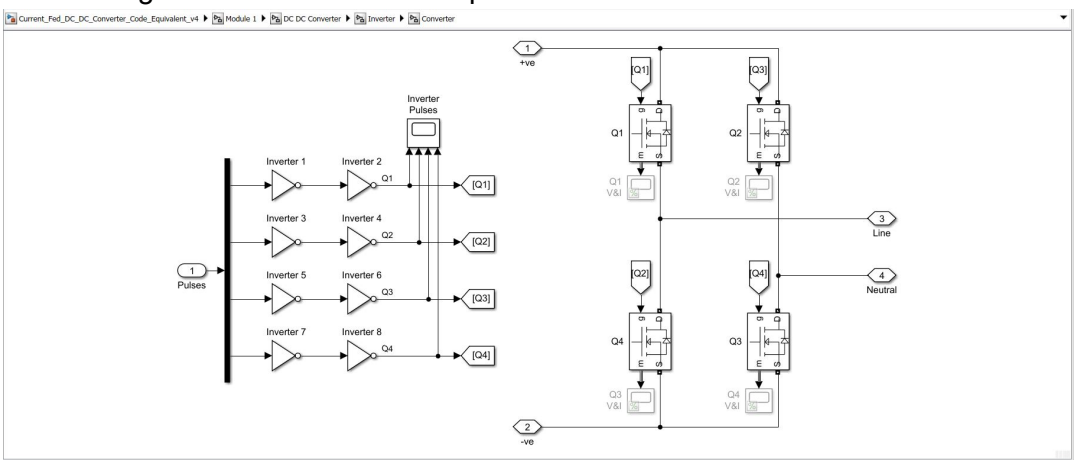

**DC Link**:

At first the DC-DC converter consists of an inductor with a value of 100uH. Note: This value has not been calculated. Ramdas Sir suggested this value from his years of experience to quickly start the simulation and since this value itself, worked it was never calculated. However, if required it can be calculated as it was during the Marine 250kW DC-DC converter application.



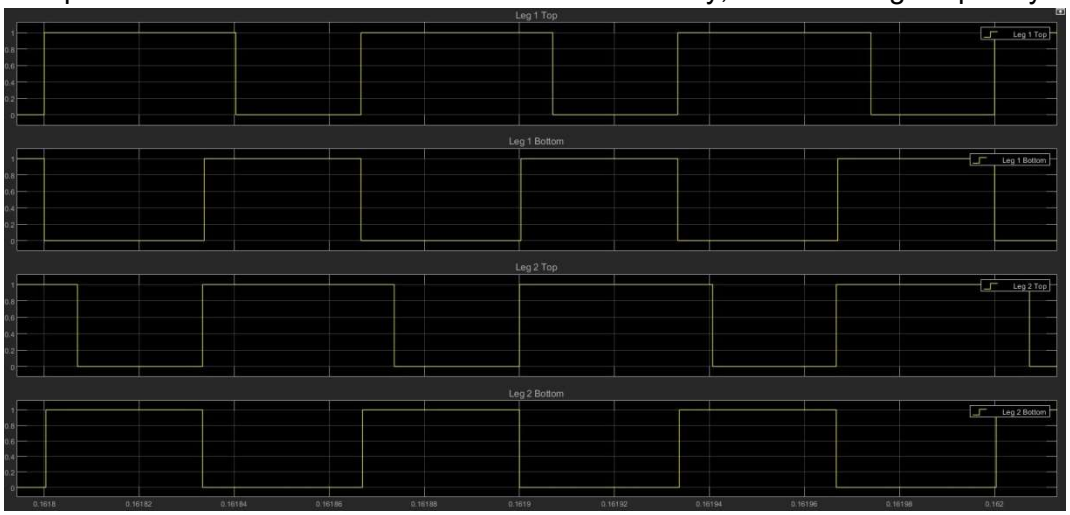
**Inverter of the DC-DC Converter:**

A Full Bridge converter has been implemented



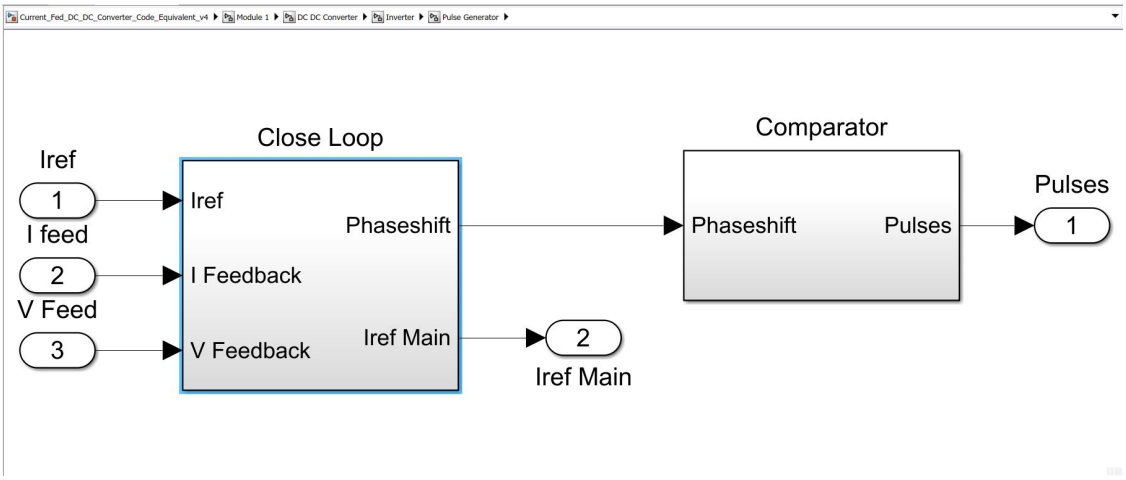

**Firing Pulses of the Inverter of the DC-DC Converter:**

Here, the duty cycle of the bottom switches remain constant at 50% while the duty cycle of the top switches varies between 50% to 75%. Depending upon the amount of duty cycle of the top switches beyond 50%, the top and the bottom switches of the same leg are closed together at that period and the energy is stored in the inductor during this time period. While, it is discharged in the rest of the time period. Thus it acts as a boost converter. Currently, the switching frequency is 15kHz.



**Control Logic:**

The control logic has the close loop which calculates the required duty cycle of top switches and provides it to the comparator which generates the required switching pulses.

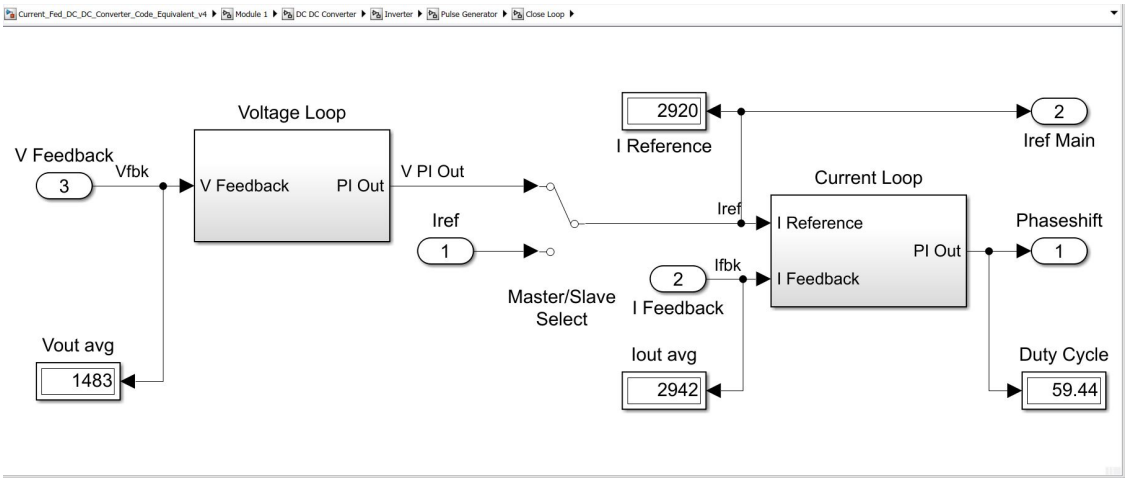


**Close Loop:**

Depending upon the type of module (whether it is master or slave) there are differences in the source of the current reference of the current loop. Each of the close loops has a voltage loop and current loop cascaded to each other. However, only the voltage loop of the master module is active all the time and it provides as a current reference to the current loop of all the modules.

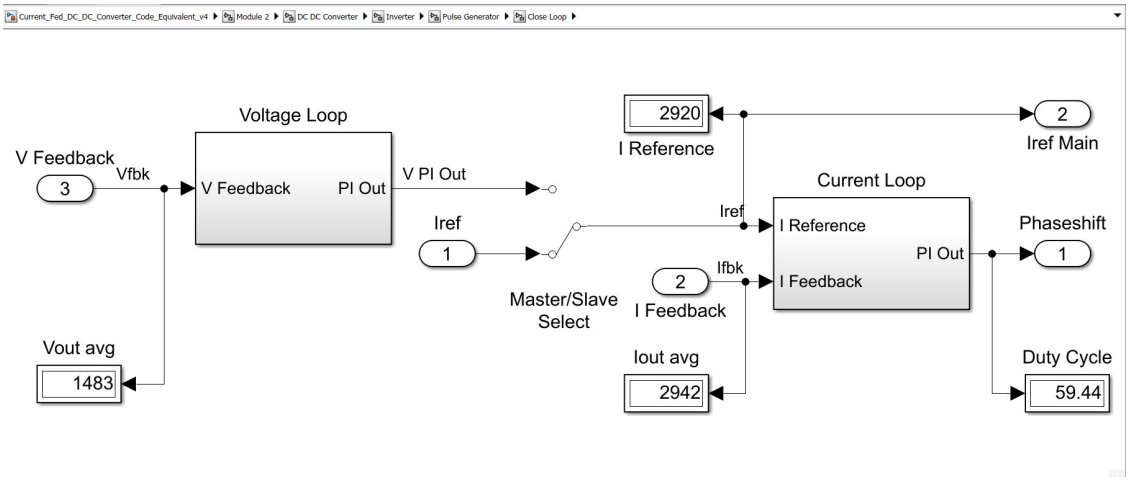
**Master Module:**

The voltage loop of the master module is active and it provides the current reference to all the modules.




**Slave Module:**

The voltage loop of the slave module is inactive and it acquires current reference from the voltage loop of the master module.



**Voltage Loop:**

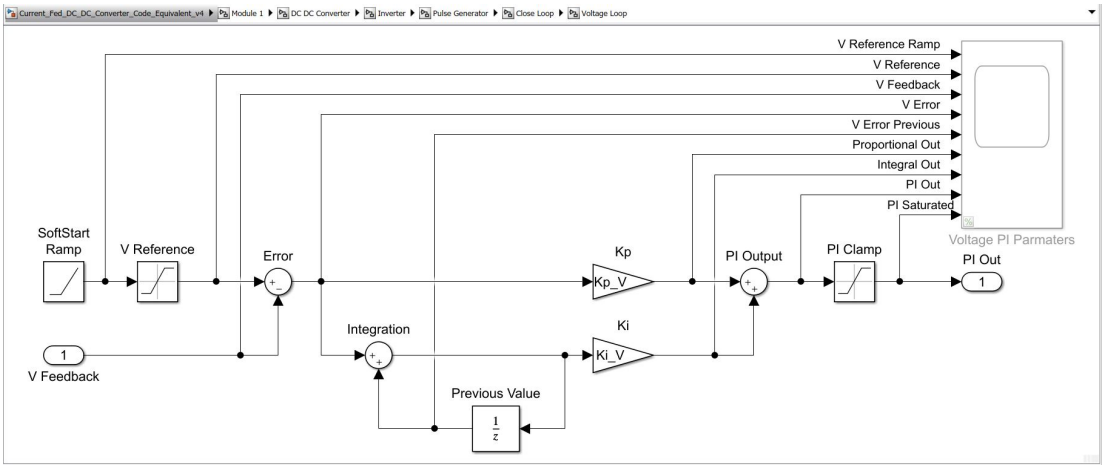
The voltage loop is a conventional PI loop with the proportional path and integral path in parallel to each other. It has the following parameters:

Reference = 1480 (this is 18V equivalent and scaled to a 12 bit ADC accommodating 50V operating range)

Kp = 1 (Proportional constant)

Ki = 0.001 (Integral Constant)

Note: Kp and Ki were tuned by trial and error method.




**Current Loop:**

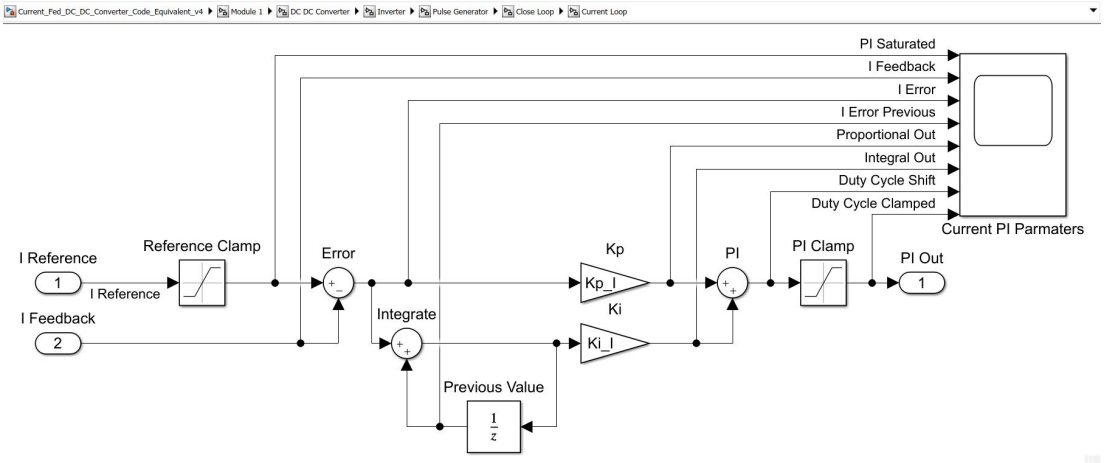
The current loop is a conventional PI loop with the proportional path and integral path in parallel to each other. It has the following parameters:

Reference = 2920 (this is 500A equivalent and scaled to a 12 bit ADC accommodating operating range)

Kp = 0.025 (Proportional constant)

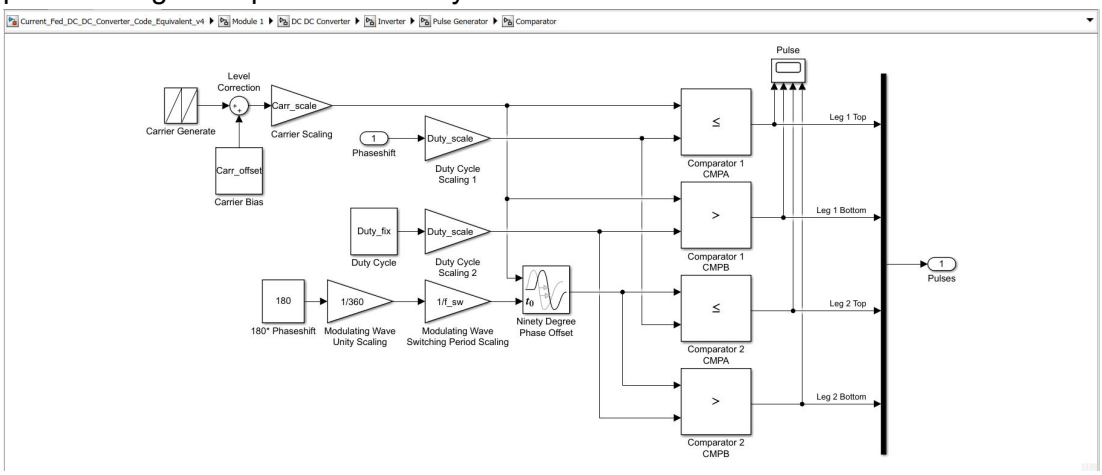
Ki = 0.000001 (Integral Constant)

Note: Kp and Ki were tuned by trial and error method.



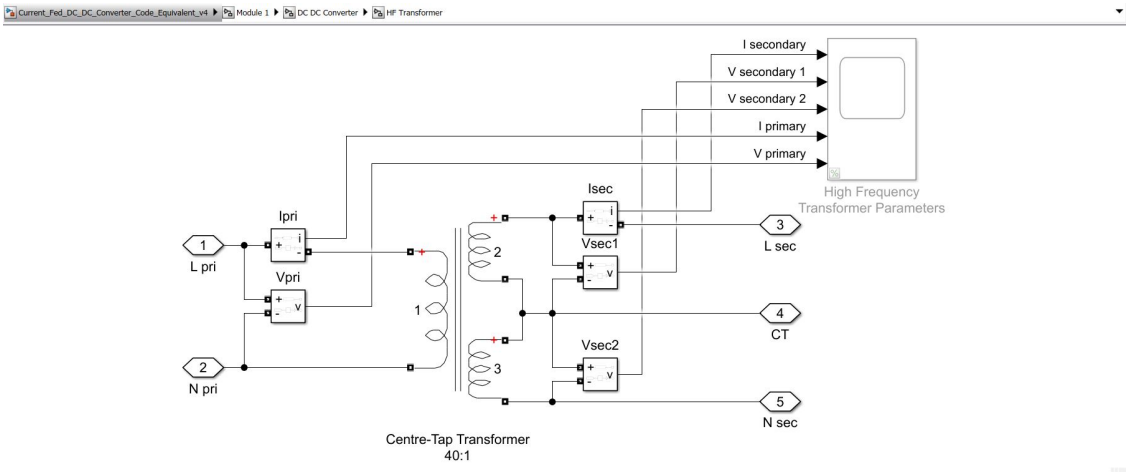
**Pulse Generator:**

A carrier wave of unity amplitude is compared with a constant of 0.5 to produce a fixed 50% duty cycle square wave and this is used as the pulse for the bottom switch of leg 1. The same carrier wave is also compared with the unity scaled duty cycle value provided by the close loop function to produce a varying duty cycle square wave and this is used as the pulse for the top switch of leg 1. The switching frequency is 15kHz. In order to produce the pulses of the switches of leg 2, the respective pulses of leg 1 are phase-shifted by 180°.



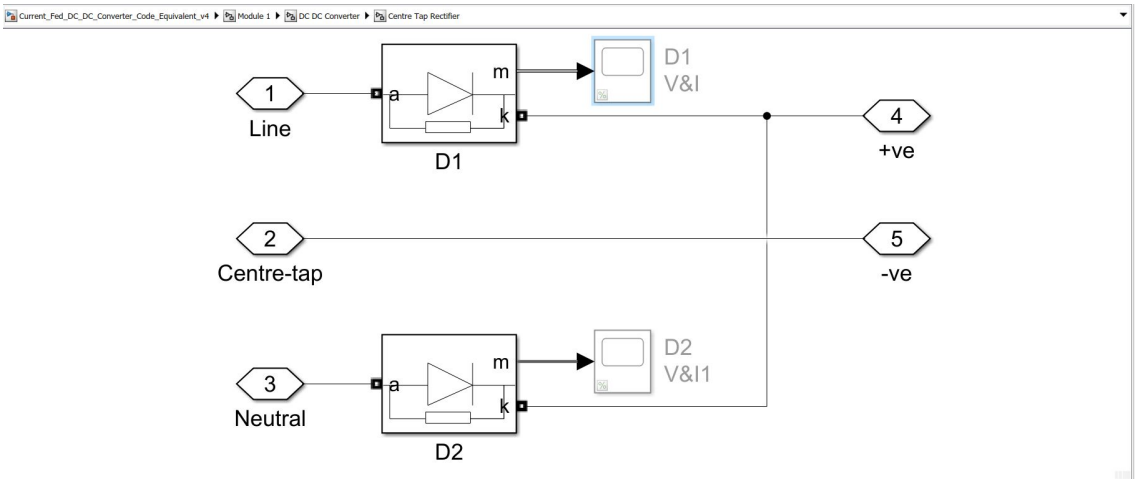

**High Frequency Transformer:**

The high frequency transformer has a transformer ratio of 36:1 to produce the 18V output. This can be changed according to the project requirements. In this simulation the transformer is an ideal transformer with 0 leakage inductance, 0 leakage resistance, ∞ magnetization inductance and ∞ magnetization resistance.



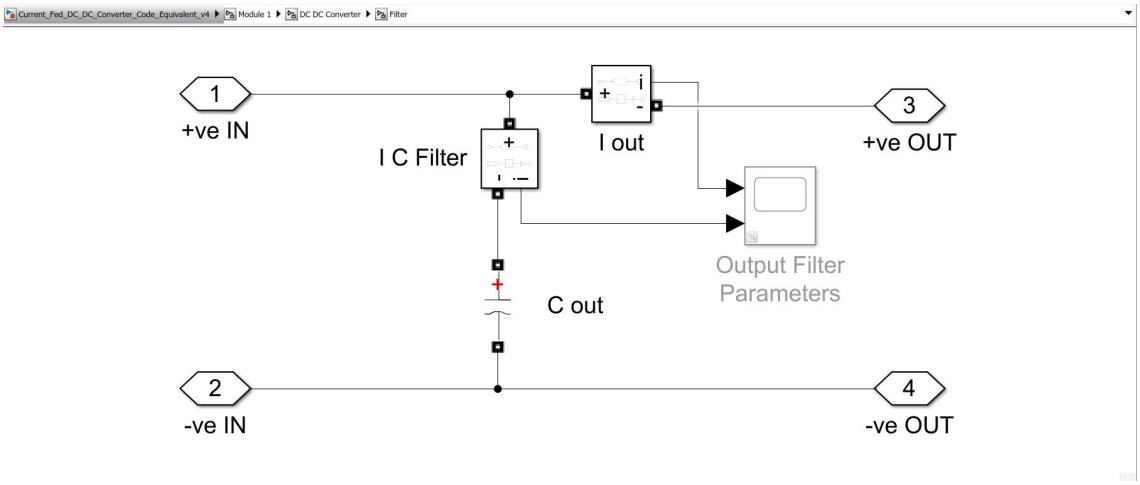
**Rectifier of the DC-DC Converter:**

A centre tap full wave rectifier has been implemented since the current rating is very high and reducing the number of switches on the path from 2 in case of bridge rectifier to 1 in this case is expected to reduce the $I^2R$ losses. Note: The efficiency and losses in this system have not been calculated yet.



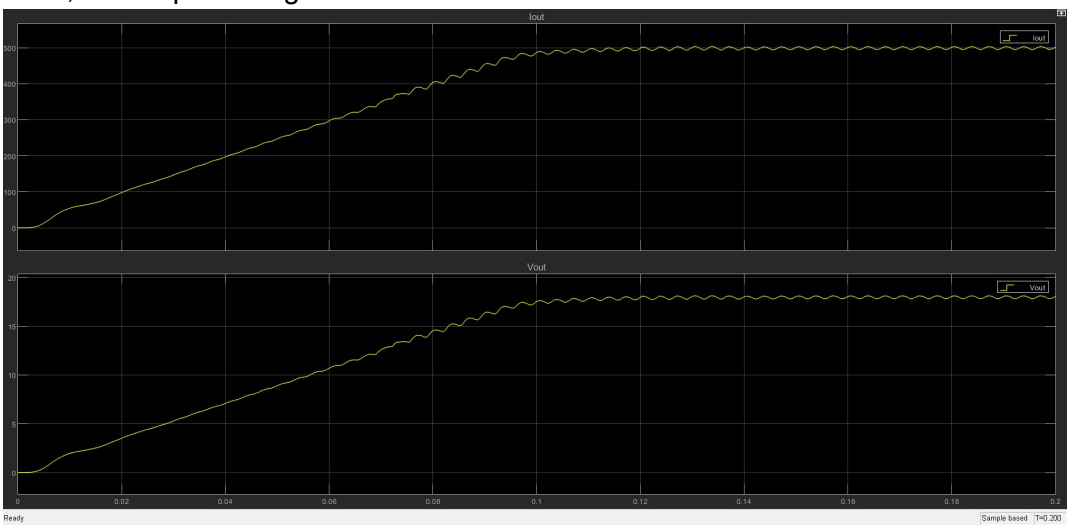

**DC Filter of the DC-DC Converter:**

The output DC filter consists of a capacitor of the value of 560µF.



**Output Waveforms:**

Here, the output voltage is 18V and the load current is 500A.




The observed ripple on the voltage waveform has a frequency of 300Hz and peak to peak amplitude of 300mV. Similarly, the observed ripple on the current waveform has a frequency of 300Hz and peak to peak amplitude of 8.44A.