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Course: EE126

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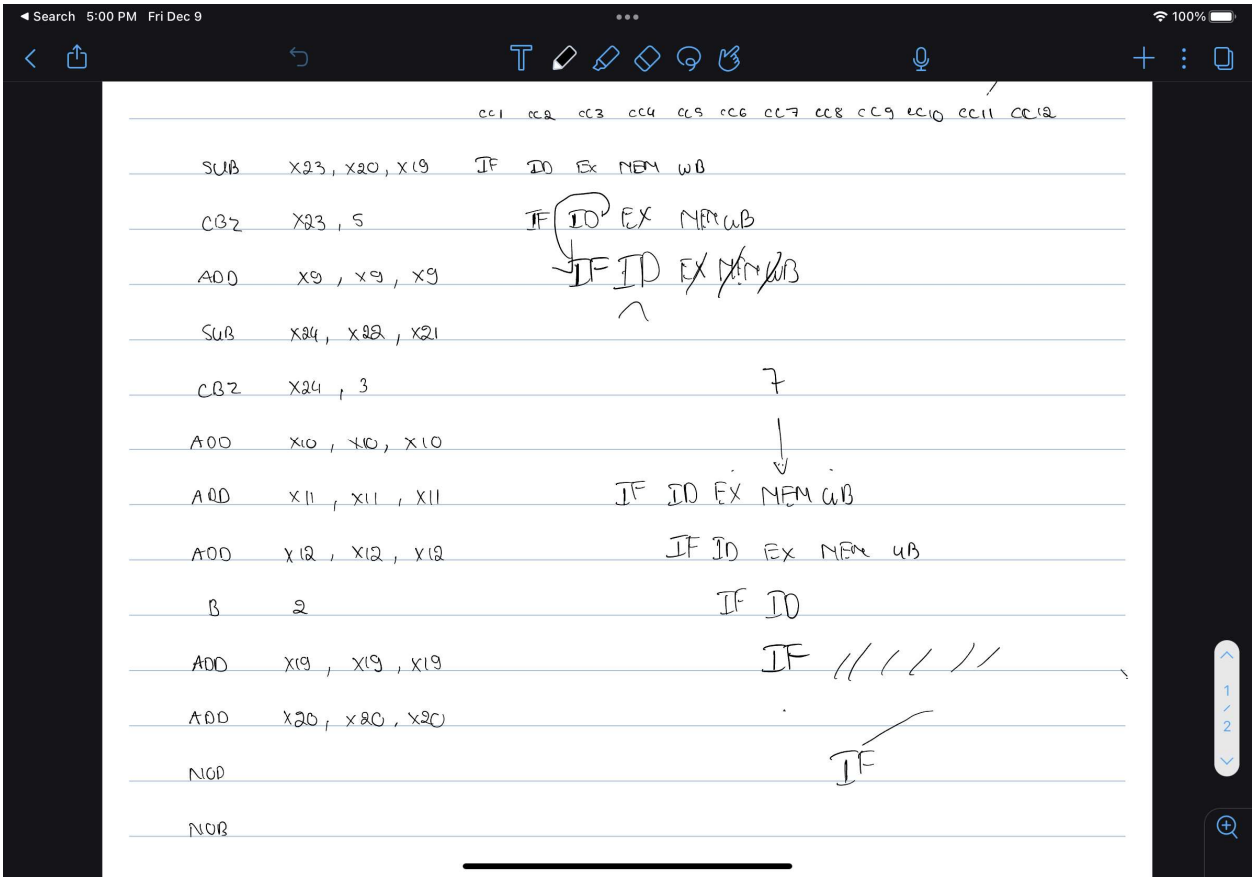
Lab Report 5

I. Introduction:

- The goal of this lab is to overcome data hazard using forwarding and stalling. The main implementation is to install the control unit and the hazard detection unit.

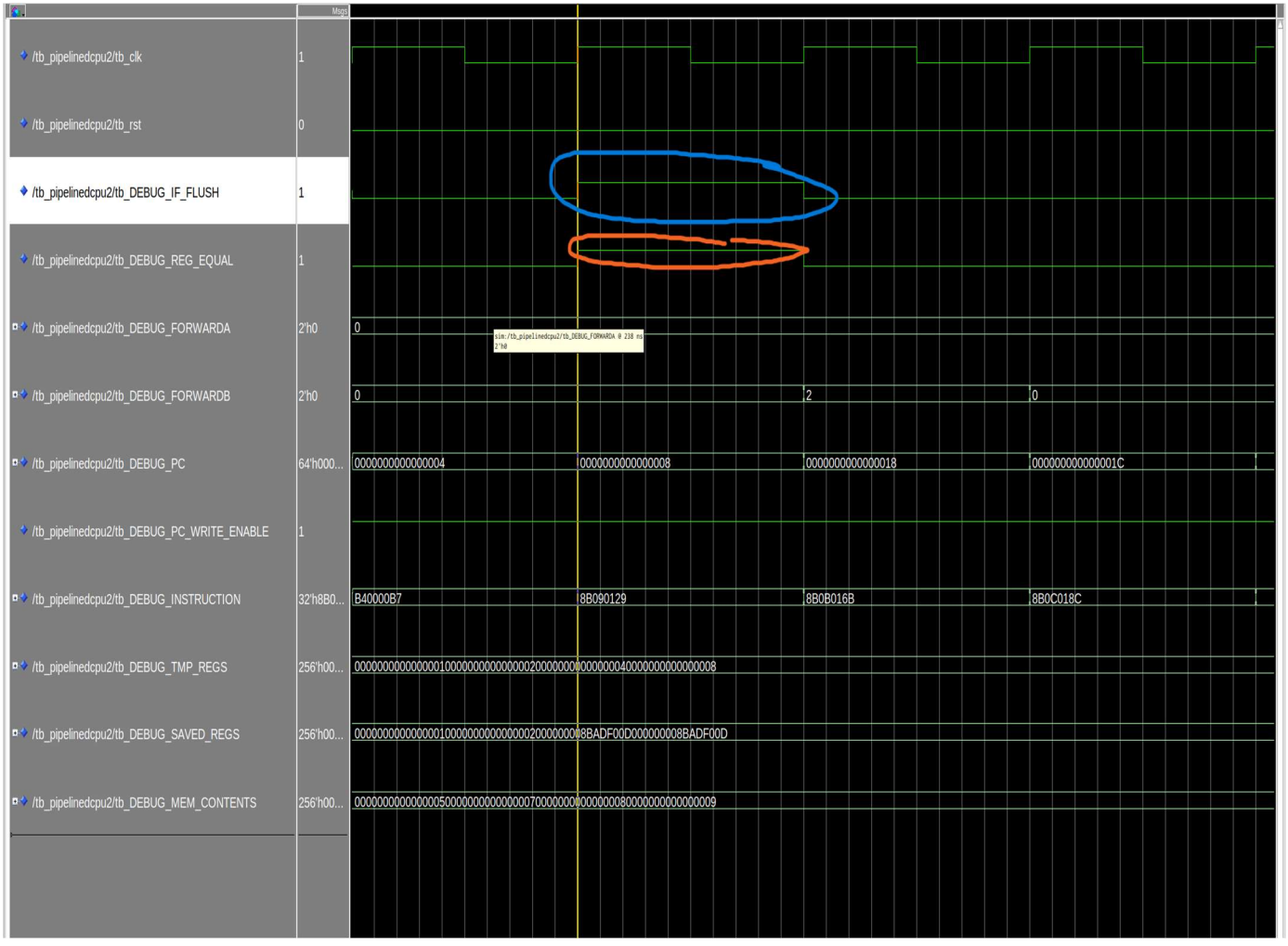
II. Procedure:

Figure 1:



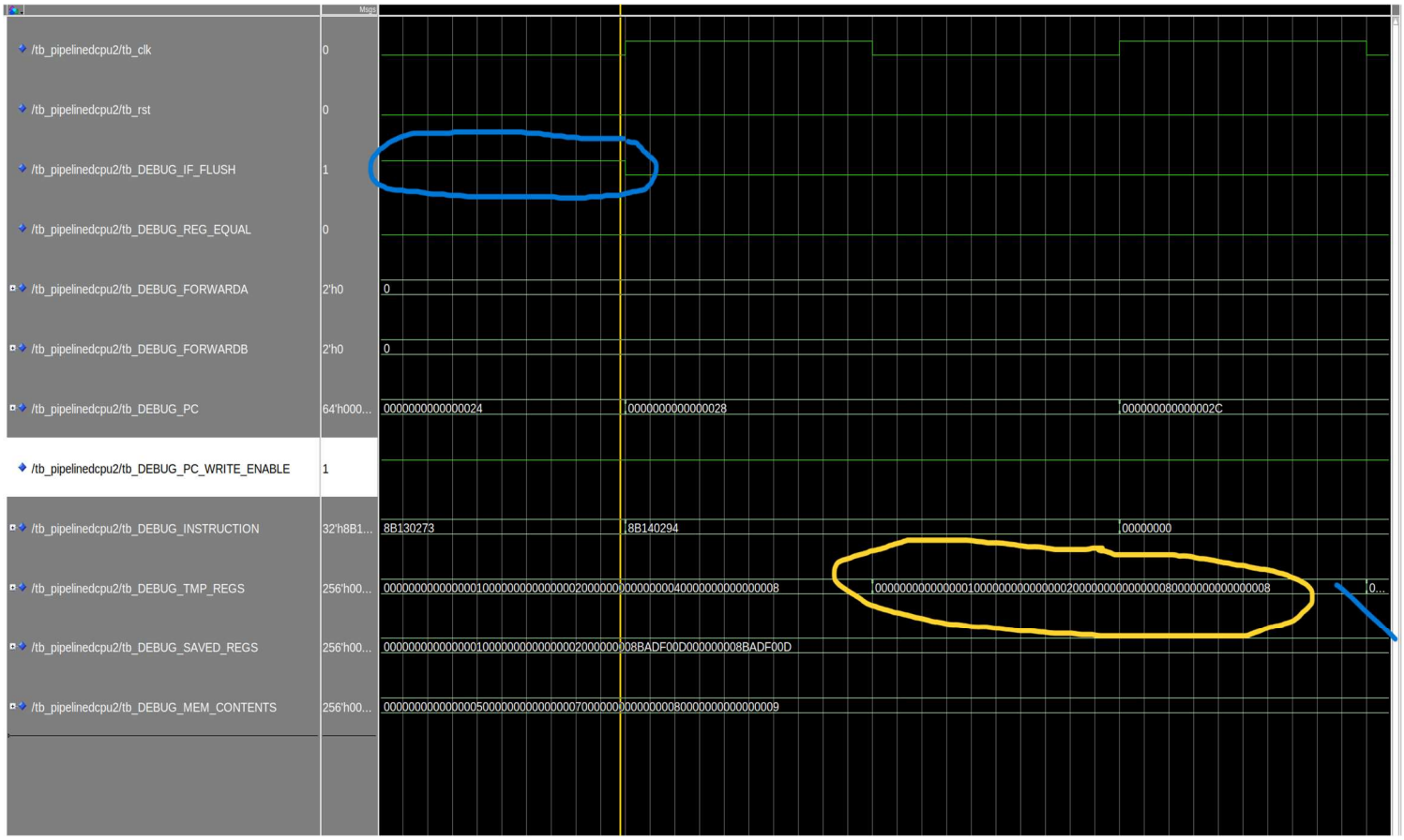
- Figure 1 is the full pipeline processing going through the clock cycles. The key cycles would be cycle 3, where the processor starts to flush and branch into the next address. Data hazards is not being implemented for these branch instructions.
- Another key cycle is cycle 7 in where the instructions starts to branch and go to instruction: “ADD X20, X20, X20”.

Figure 2:



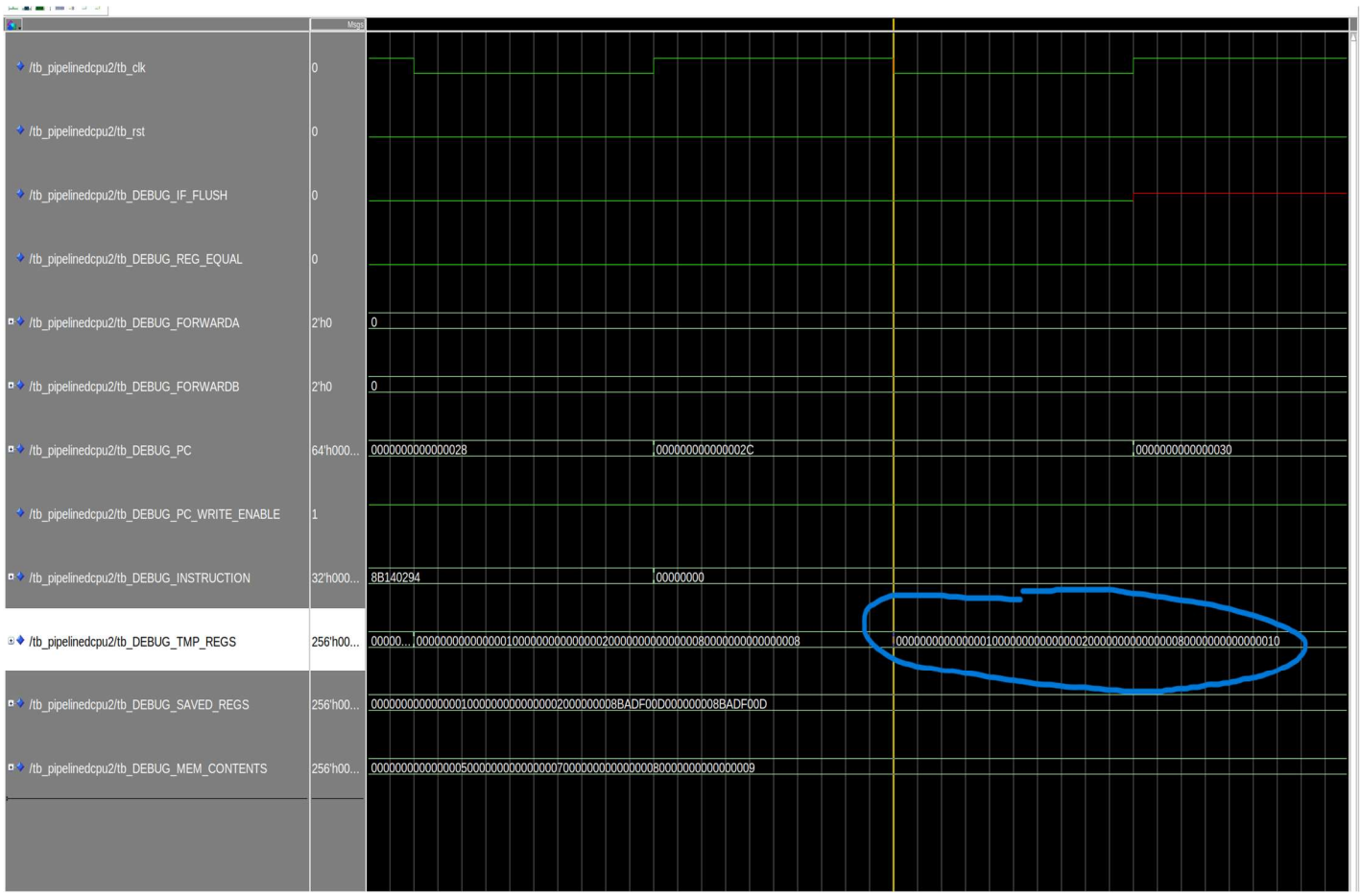
- Figure 2 is the pipeline during cycle 3 in which they start to flush and jump into address x0018, which is instruction “ADD X11, X11, X11”

Figure 3:



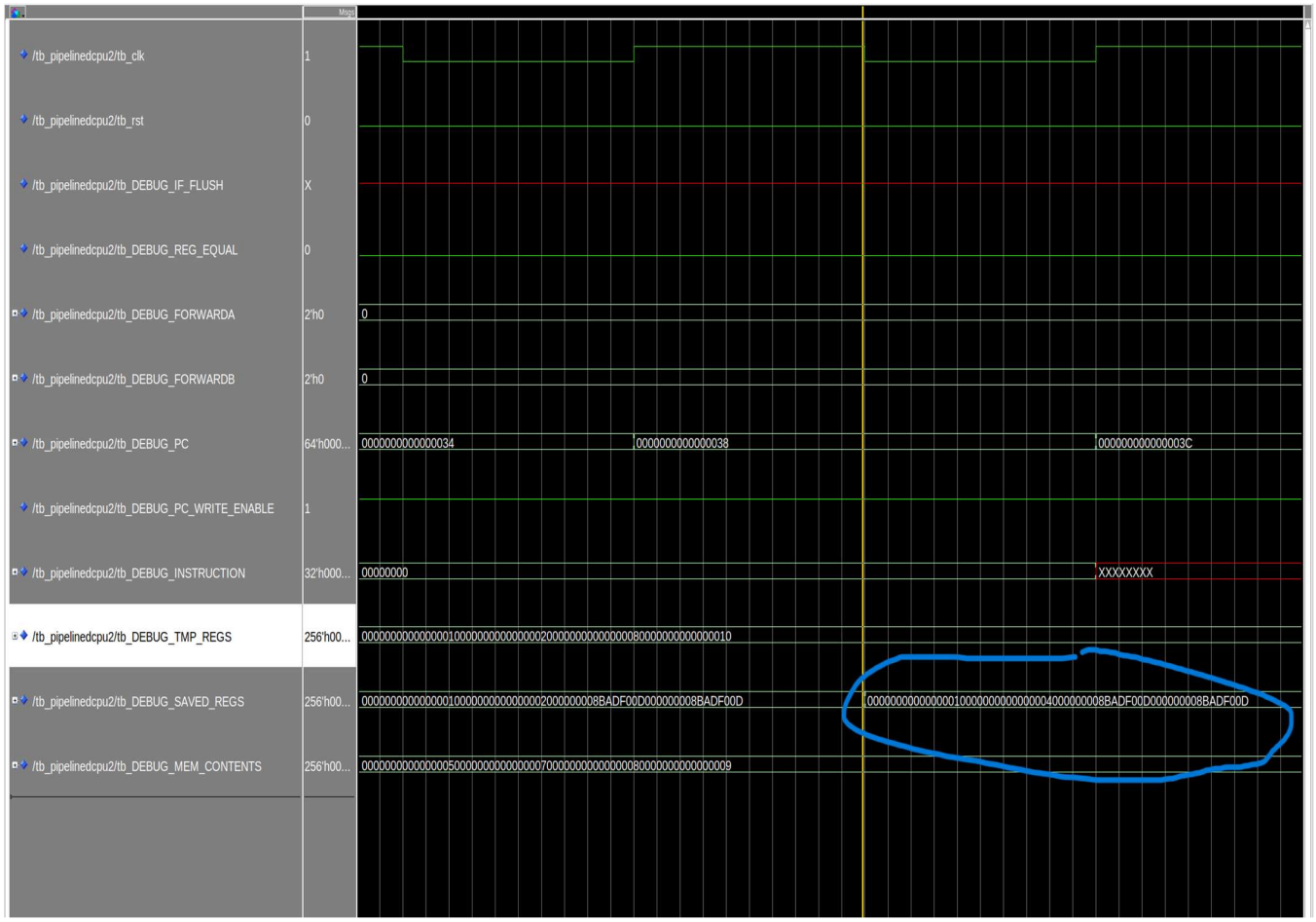
- In figure 3, it is during cycle 7 where instruction starts to branch and flush (blue markup), and registers X11 got updated from the instruction “ADD X11, X11, X11” as it was in the write back stage
- Moreover, we can see the Program Counter has jumped to instruction “ADD X20, X20 , X20”

Figure 4:



- Figure 4 is in cycle 8 in which the instruction after the previous got into the WB stage and updated the registers X12.

Figure 5:



- Figure 5 is when the instruction that got branched got into the WB stage, in which it write into X20.