**IV – Troubleshooting:**

1. **Barrel Jack Footprint:**

* Wrong Orientation of the footprint – easy fix
* Capacitor for the RS232 is bad =>> hot =>> replace RS232

A picture containing text, electronics, circuit

Description automatically generated

1. **RESET & HALT behavior:**

* Reset & halt lines have similar behavior.
* There must be a delay of 150ms to discharge the internal capacitors of the CPU.
* These 2 lines are driven by the hardware.
* Connecting other peripheral devices causes the CPU to halt the simulator – discuss later.
* Problem:
  + Reset Buttons are being driven high =>> which makes the open-collector buffer being useless =>> cannot pull reset & halt line low
  + It does not match the datasheet provided by the DS1813+ Supervisor.

1. **Logical Lines Analysis:**

* BR, BERR, BG, BGACK is Bus Arbitration line, which only needed if you are controlling lines with CPLD =>> drive them high using CPLD
* Mistakes: Driven RESET & HALT using the CPLD with the current hardware reset setup
* Creates oscillating logical lines =>> bad
* Disconnect RESET & HALT using the CPLD.
* RW should be pulled up by resistor (4.7kΩ)

1. **Hardware Check:**

* Checking every voltage line coming into your chips =>> issues come from bad CPLD
* **Diagram, table

  Description automatically generated with medium confidence** Address line A9 never got connected =>> Somehow passed all the hardware test