Op-Amp Mid Written Solution

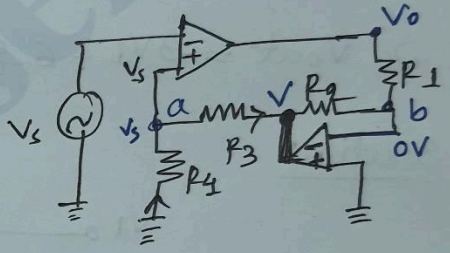
(2) Determine the voltage gain of following op-amp circuit, when $R1 = R2 = X\Omega$ and $R3 = R4 = Y\Omega$

where $X = (\text{last two digit of your student ID} + 1)$

$Y = ((2 * \text{last two digit of your ID}) + 1)$ [4 Marks]

Let, $X = 15+1 = 16$ So, $R1 = R2 = 16\Omega$

$Y = (2\times15)+1 = 31$ $R3 = R4 = 31\Omega$



Solution:

At node a,

$$\frac{0-Vs}{R4} = \frac{Vs-V}{R3}$$

$$\Rightarrow \frac{-Vs}{31} = \frac{Vs-V}{31}$$

$$\Rightarrow -Vs = Vs - V$$

$$\Rightarrow V = 2Vs$$

At node b,

$$\frac{V-0}{R2} = \frac{0-Vo}{R1}$$

$$\Rightarrow \frac{V}{R2} = \frac{-Vo}{R1} \Rightarrow Vo = -V$$

$$\Rightarrow \frac{V}{16} = \frac{-Vo}{16} \uparrow \Rightarrow Vo = -2Vs \Rightarrow \frac{Vo}{Vs} = -2$$

$\therefore$ Voltage gain, $Av = -2$ (Ans:)

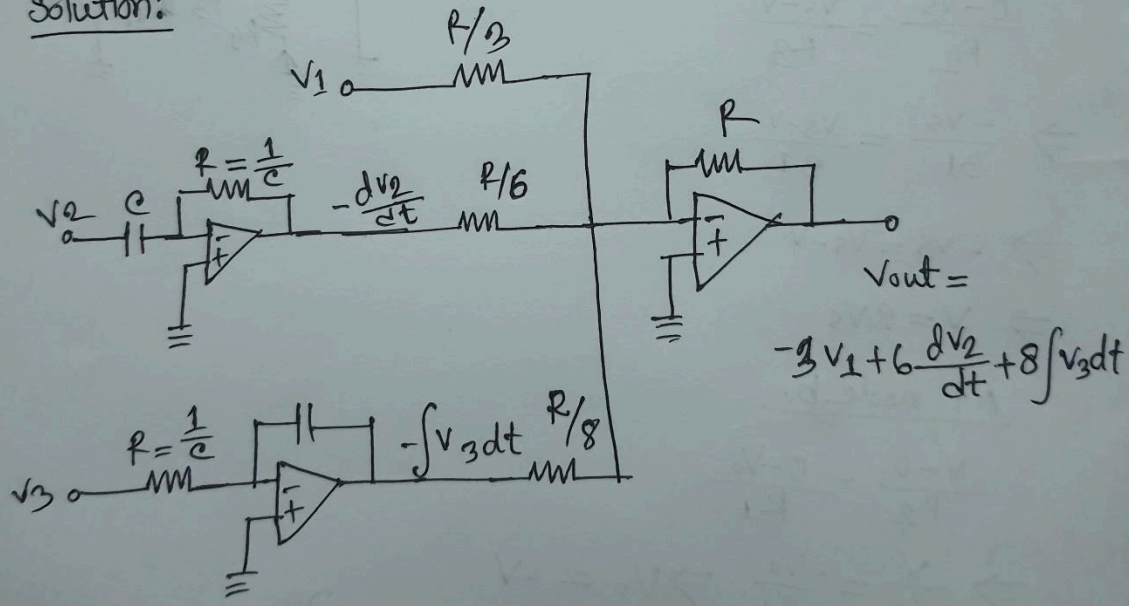
(3) Using an ideal op-amp, design a circuit that will take V_1, V_2 & V_3 as inputs and will produce the following output: $V_{out} = -a V_1 + b\frac{dV_2}{dt} + c\int V_3 dt$ [4 Marks]

$a = Id$
$b = Id+3$
$c = Id+5$

Let Id = 03
$a = 3$
$b = 6$
$c = 8$

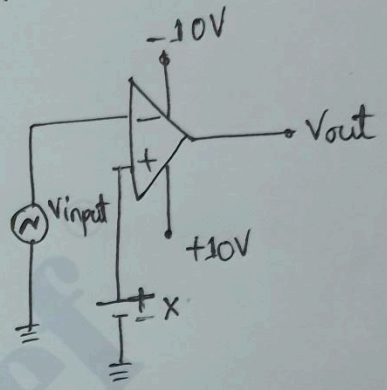
So $V_{out} = -3V_1 + 6\frac{dV_2}{dt} + 8\int V_3 dt$

Solution:



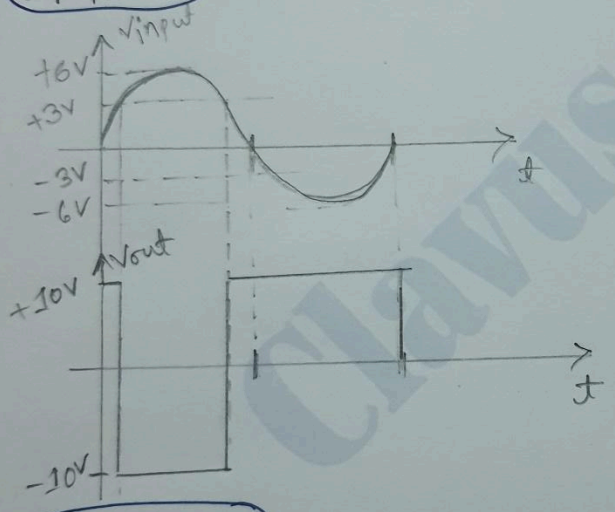
(5) Find the output wave shapes for the sinusoid input of ± 6V (Peak to Peak) given below.

X = last digit of student ID:



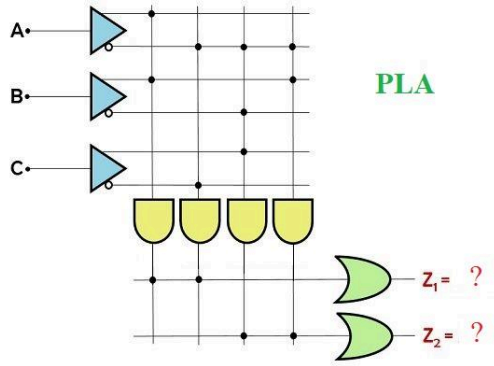
Solution:

Let X = 3V



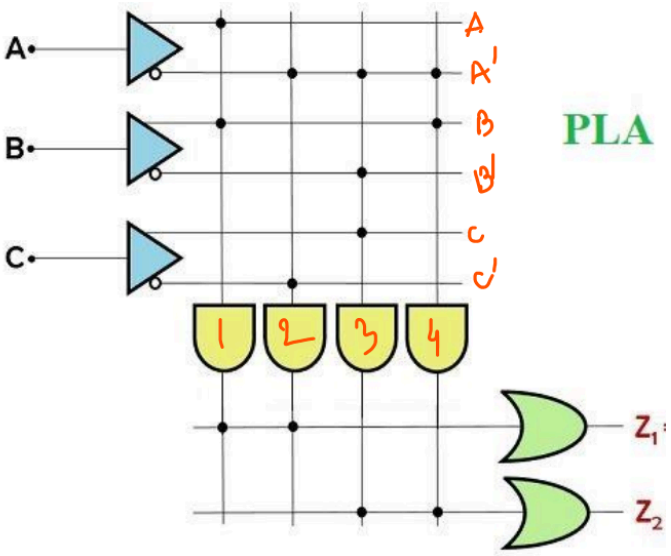
Let X = 8V

WQ4) Find the output (Z_1 & Z_2) of the following Programmable Logic Array (PLA)? [**03**]



Answer: Programmable Logic Array(PLA) is a fixed architecture logic device with programmable AND gates followed by programmable OR gates. PLA is basically a type of programmable logic device used to build a reconfigurable digital circuit. PLDs have an undefined function at the time of manufacturing, but they are programmed before made into use. PLA is a combination of memory and logic.

In the given circuit could be written as by naming the And gates as 1,2,3,4.



Then the output of the And gates are:

$G_1 = AB$; $G_2 = A'\,C'$; $G_3 = A'B'\,C$; $G_4 = A'\,B$

After adding the output of And gates into Or gate we will get the final output as below:

$Z_1 = AB + A'C'$

$Z_2 = A'B'C + A'B$

AQ1) Design a 2-bit Analogue to Digital Converter Circuit and explain its operation with a proper diagram. [03]

Answer: From the name itself it is clear that it is a converter which converts the analog (continuously variable) signal to digital signal. This is really an electronic integrated circuit which directly converts the continuous form of signal to discrete form. It can be expressed as A/D or ADC.

There are mainly two steps involves in the process of conversion. They are i) Sampling and Holding ii) Quantizing and Encoding

The whole ADC conversion process is shown below:

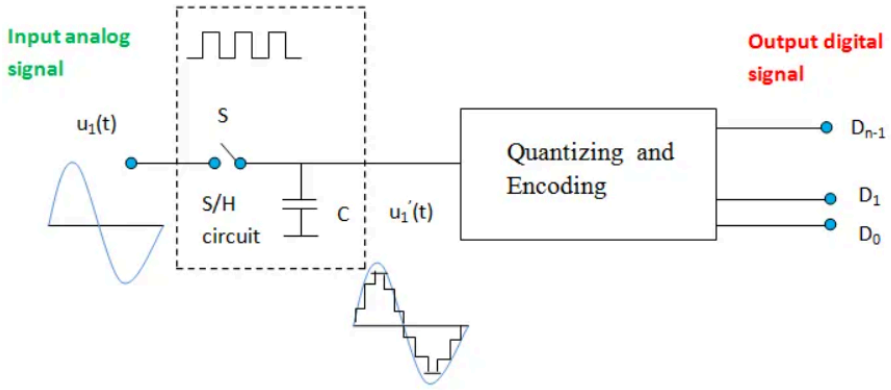
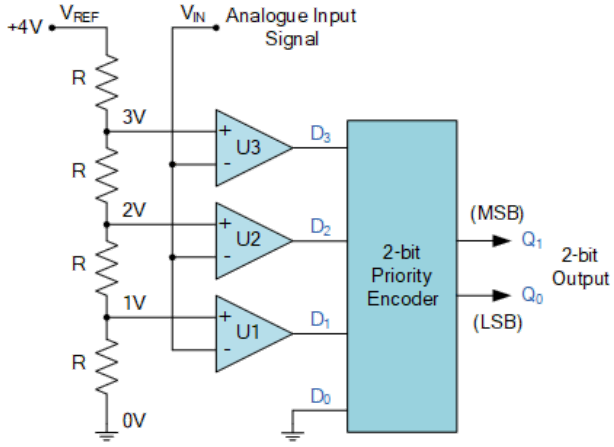


Figure-01: ADC Conversion process

2-bit Analogue to Digital Converter Circuit (Figure:2)



Analogue Input Voltage (V_{IN})	Comparator Outputs				Digital Outputs	
	D_3	D_2	D_1	D_0	Q_1	Q_0
0 to 1 V	0	0	0	**0**	0	0
1 to 2 V	0	0	**1**	X	0	1
2 to 3 V	0	**1**	X	X	1	0
3 to 4 V	**1**	X	X	X	1	1

Figure-02 Figure-03

In figure-03, gives 2-bit output code for all four possible values of analogue input, where: “X” is a “don’t care”, that is either a logic “0” or a logic “1” condition.

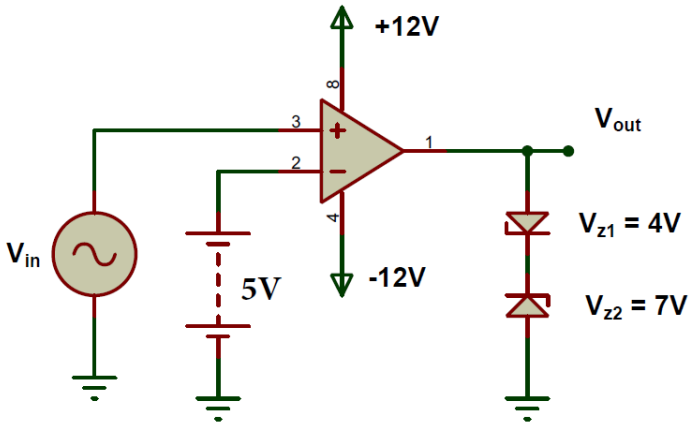
So how does this analogue-to-digital converter work. For an A/D converters to be useful it has to produce a meaningful digital representation of the analogue input signal. Here in this simple 2-bit ADC example we have assumed for simplicity that the input voltage V_{IN} is between 0 and 4 volts, so have set V_{REF} and the resistive voltage-divider network to drop 1 volt across each resistor.

When V_{IN} is between 0 and 1 volt, (<1V) the input on all three comparators will be less than the reference voltage, so their outputs will be LOW and the encoder will output a binary zero (00) condition on pins Q_0 and Q_1. When V_{IN} increases and exceeds 1 volt but is less than 2 volts, ($1V<V_{IN}<2V$) comparator U_1 which has a reference voltage input set at 1 volt, will detect this

voltage difference and produce a HIGH output. The priority encoder which is used as the 4-to-2 bit encoding detects the change of input at D_1 and produces a binary output of "1" (01).

So now as V_{IN} increases above 2 volts, the next reference voltage level, comparator U_2 detects the change and produces a HIGH output. But because input D_2 has a higher priority than inputs D_0 or D_1, the priority encoder outputs a binary "2" (10) code, and so on when V_{IN} exceeds 3 volts producing a binary code output of "3" (11). Clearly as V_{IN} reduces or changes between each reference voltage level, each comparator will output either a HIGH or a LOW condition to the encoder which in turn produces a 2-bit binary code between 00 and 11 relative to V_{IN}.

AQ2) Draw V_{in} with V_{out} of the following comparator circuit, where Vin is 10 v peak sine wave. [03]



Answer: This is a very basic comparator circuit which have a input sinusoidal having peak voltage 10 V (peak to peak 20 V) and a constant 5 volt in another input. To understand the output easily we could divide it's output in two stages like: i) just op-amp output ii) output after considering the Zener diode effects. Here moreover we take the Zener diodes as ideal diode.

First think about the comparator op-amp output.

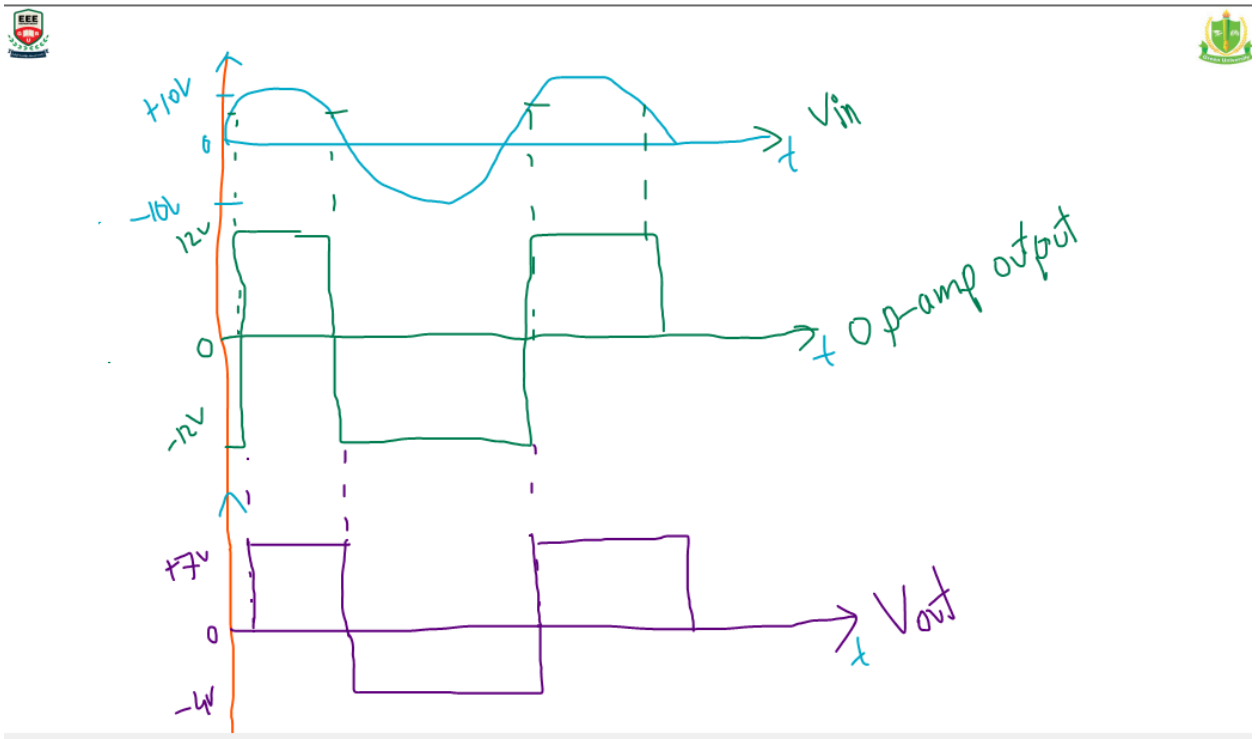
When Vin > 5V thus we will get +12 V as op-amp output. (as +Vsat = +12V)

When Vin <5V thus we will get -12 V as op-amp output. (as - Vsat = - 12V)

Then the output of op-amp, works as input of the Zener diode. Zener diodes forward voltage drop is zero but if the reverse voltage is higher than V_z then voltage across it will be V_z.

When op-amp output is +12V then V_{z1} is in forward bias but V_{z2} is in reverse, so output will be V_{out} = +7 V

Again, when op-amp output is -12V then V_{z2} is in forward bias but V_{z2} is in reverse, so output will be V_{out} = -4V.



Or

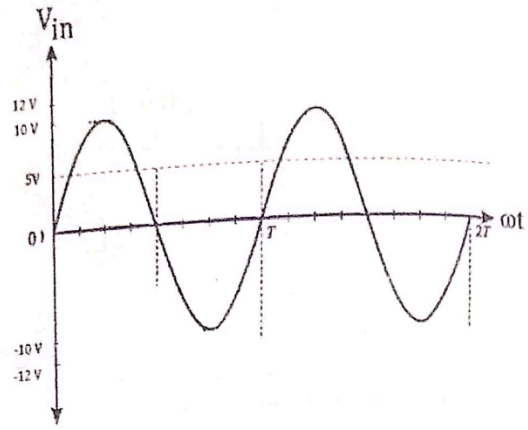


Figure-1: Input sine wave, $V_i = 10 \sin \omega t$

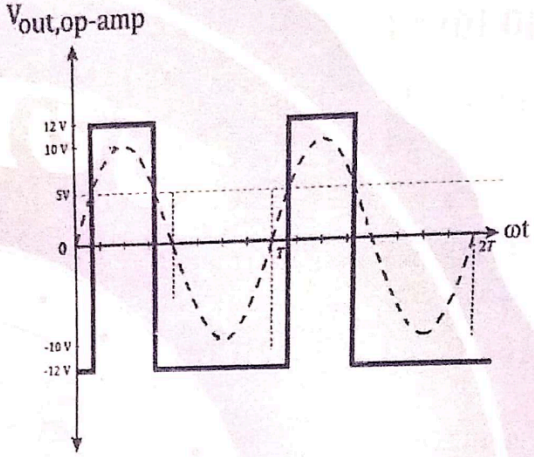


Figure-2: Output of Op-Amp = Input in Zener Diodes

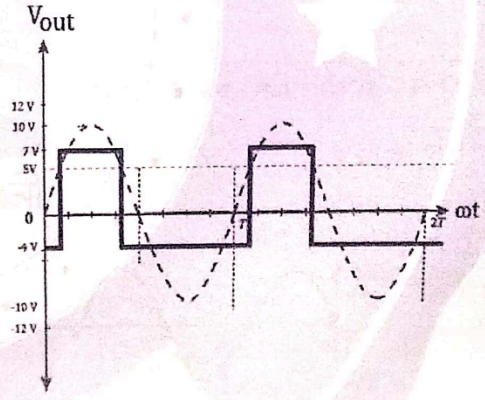
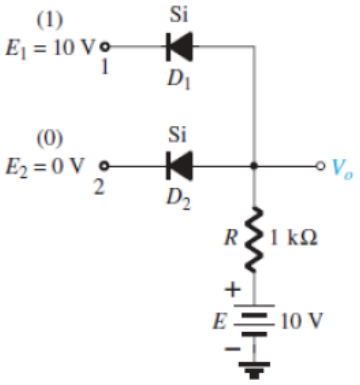
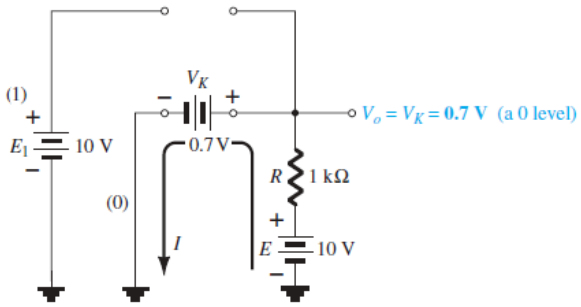


Figure-3: Final Output (after Zener Diodes)

WQ1:





$$I = \frac{E - V_K}{R} = \frac{10\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \mathbf{9.3\text{ mA}}$$

AQ3:

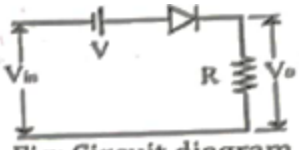


Fig: Circuit diagram

At +Ve half,
$V_0 = (V_m + V)$
At −Ve half,
$V_0 = V$