E/15/202

a)

Address																
0x210	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
0x211	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	1
0x212	0	0	0	0	0	0	1	0	0	0	0	1	0	0	1	0
Address Line	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

Only A1 and A0 are changing

<u>3 decoders</u>
A11 -> A -> 0
A12 -> B -> 0
A13 -> C -> 0 ➔ Y0 -> 0
A9 -> G1 -> 1
A14 -> G2A -> 0
A15 -> G2B -> 0

Y0 -> A -> 0
A10 -> B -> 0
A8 -> C -> 0 ➔ Y1 -> 1
A4 -> G1 -> 1
A7 -> G2A -> 0
A6 -> G2B -> 0

A0 -> A
A1 -> B
A2 -> C -> 0
Y1 -> G1 -> 1
A5 -> G2A -> 0
A3 -> G2B -> 0

A2	A1	A0	
0	0	0	Y0
0	0	1	Y1
0	1	0	Y2

d) Briefly explain the importance of using nIOW, nIOR, AENs line in an ISA bus based interface design.
IOR –This is an active low signal. When this is set to low, CPU read from the I/O device.

IOW- This is also an active low signal. When this is set to low,CPU write to the I/O device

AEN is the Address Enable.This output signal allows the IO device to distinguish between processor bus cycles and DMA bus cycles. A high on AEN indicates that a DMA cycle is occuringand that the address, data and control lines are under the control of the DMA controller. Peripheral IO devices that do not have DMA capability should insure that they only decode address that are generated by the processor (AEN='0') and not a DMA controller.