EE386 – RESISTOR TRANSISTOR LOGIC

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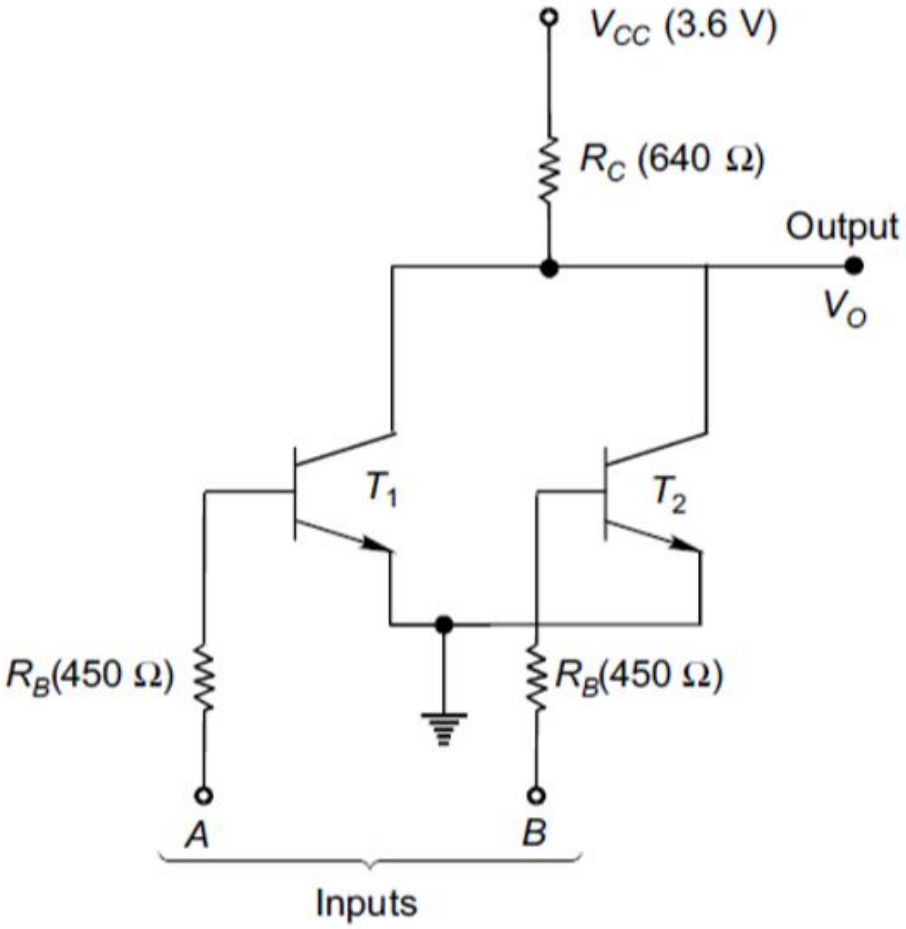

Figure 1

1. Schematic implementation of the above figure 1 is as below.

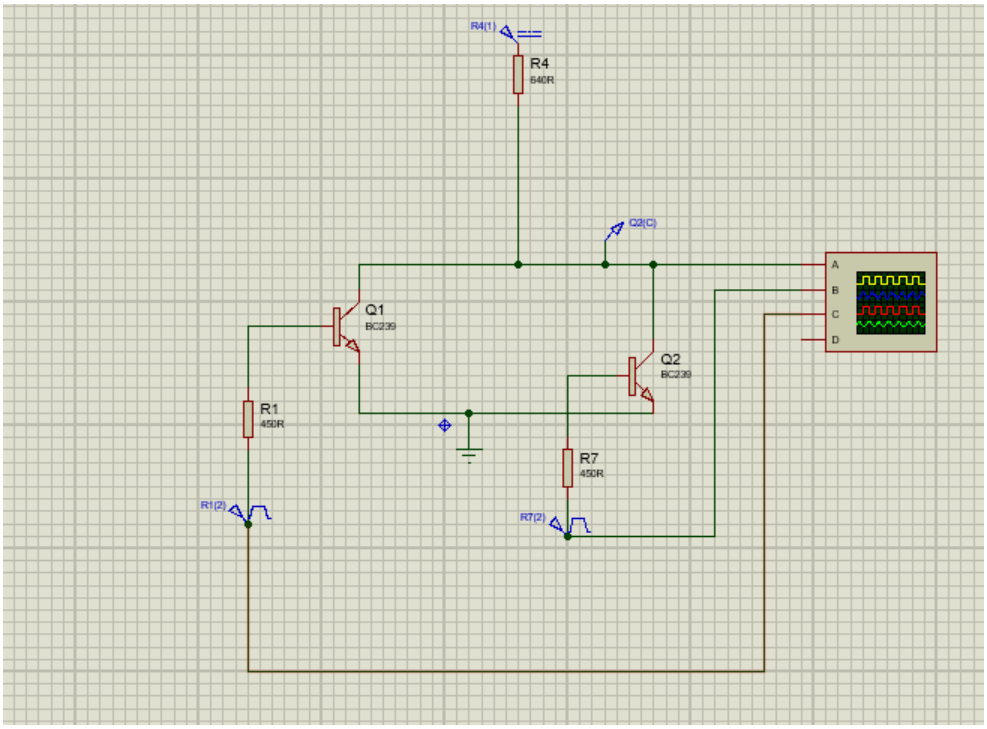

Figure 2

2. b.

V_A(V)	V_B(V)	V_o(V)
0	0	3.6
0	3.6	0.2
3.6	0	0.2
3.6	3.6	0.2

Since logic 'LOW' = 0.2V and logic 'HIGH" = 3.6V

Let's consider logic '0' = 0.2V and logic '1' = 3.6V

V_A(V)	V_B(V)	V_o(V)
0	0	1
0	1	0
1	0	0
1	1	0

So according to the tables we can say that this RTL circuit is performing according to the NOR gate.

3.

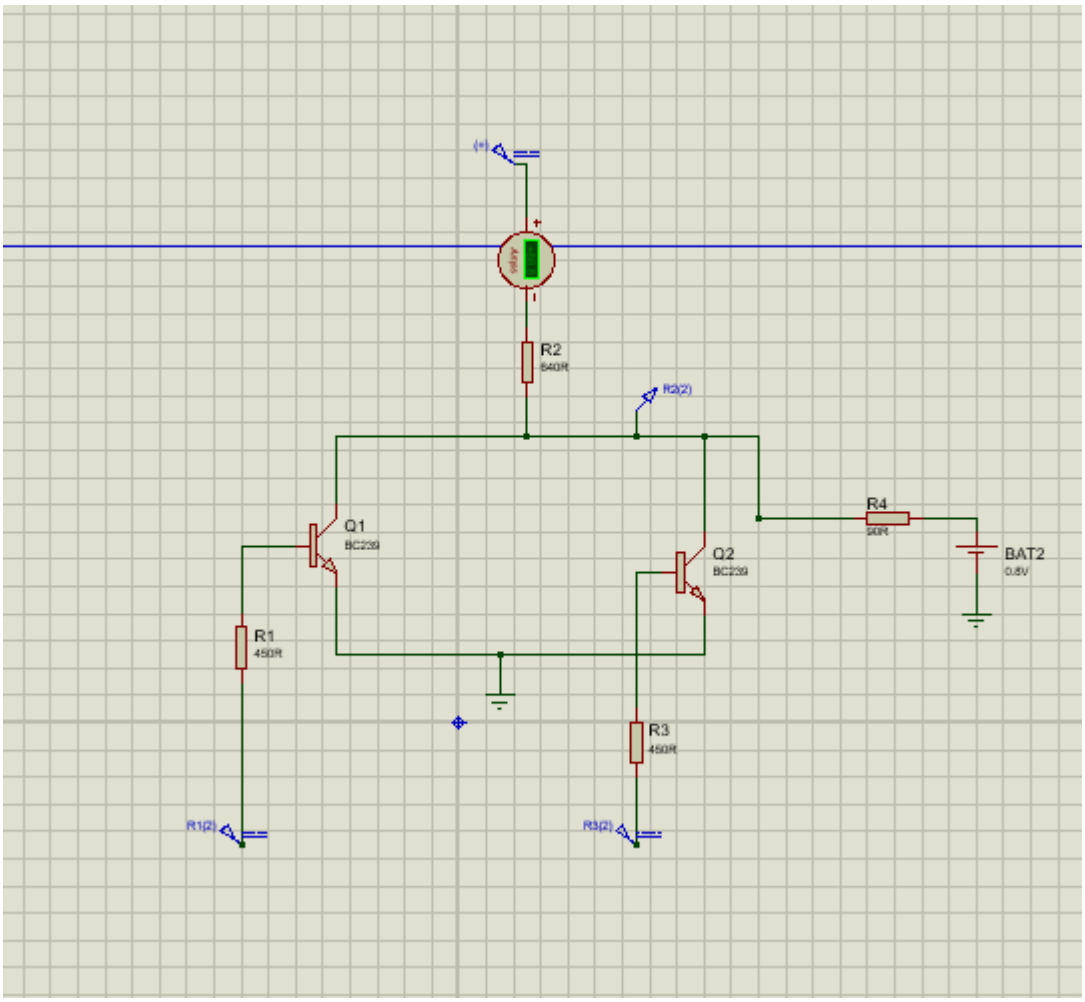

Figure 4

a. So according to the schematic diagram,

logic LOW = 0.198535V ≈ 0.2V

logic HIGH = 1.14521V ≈ 1.15V

b. i) When output is at logic 'LOW' $I_c = 5.31mA$

Power drawn by the circuit = 3.6 × 5.31 = 19.116mw

ii) When output is at logic 'HIGH' $I_c = 3.84mA$

Power drawn by the circuit = 3.6 × 3.84 = 13.824mw

c. Low level noise margin $\Delta L = V_{IL} - V_{OL}$
Assume cut in voltage of a transistor = 0.5V

$$\Delta L = 0.5 - 0.2 = 0.3V$$

$I_c(max) = 5.31mA$ that can flow through the circuit

In saturation $I_c < \beta I_B$
Since β = 30
$I_B > \frac{5.31}{30} = 0.177mA$

$I_B(min) = 0.177mA$

$V_{IH} = I_B(min)R_B + V_{BE,sat}$

$V_{IH} = 0.177 \times 10^{-3} \times 450 + 0.8$
$V_{IH} = 0.88V$

High level noise margin $\Delta H = V_{OH} - V_{IH}$

$$\Delta H = 1.14 - 0.88 = 0.26V$$

4. a.

Steps	Resistance (Ω)	LOW (V)	HIGH (V)
0	-	0.09	3.6
5	90	0.2	1.15
10	45	0.27	0.98
15	30	0.33	0.93
20	22.5	0.38	0.895
25	18	0.42	0.88
30	15	0.45	0.86
35	12.857	0.48	0.855
40	11.25	0.5	0.848
45	10	0.52	0.84
50	9	0.54	0.839

b.

Steps	Resistance (Ω)	$\Delta L = V_{IL} - V_{OL}$ (V)	$\Delta H = V_{OH} - V_{IH}$ (V)	I_C(mA)
0	-	0.41	2.72	5.47
5	90	0.3	0.27	5.31
10	45	0.23	0.102	5.2
15	30	0.17	0.0535	5.1
20	22.5	0.12	0.0195	5.03
25	18	0.08	5.45×10^{-3}	4.97
30	15	0.05	-0.0138	4.92
35	12.857	0.02	-0.0182	4.88
40	11.25	0	-0.0246	4.84
45	10	-0.02	-0.03215	4.81
50	9	-0.04	-0.0327	4.78