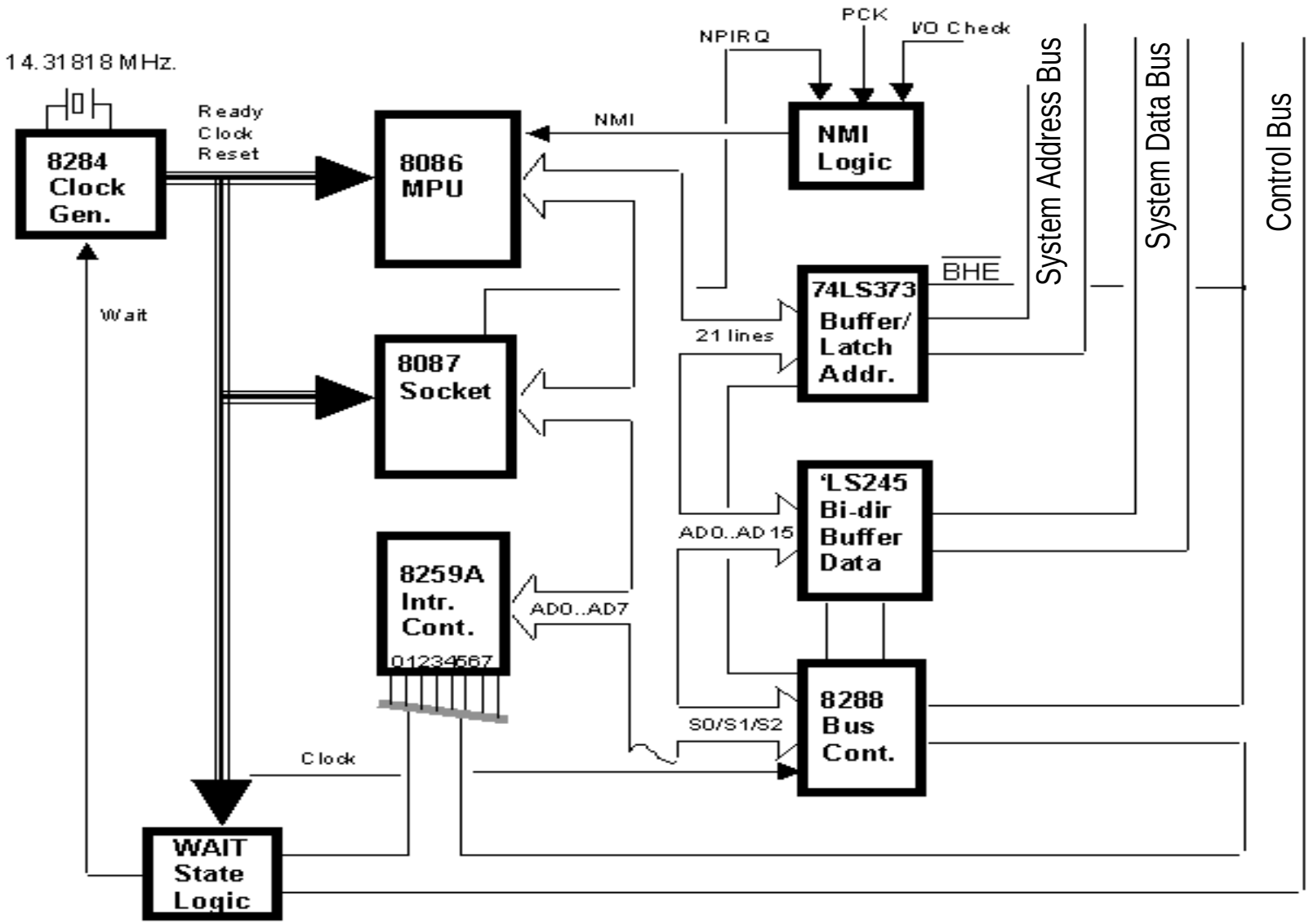
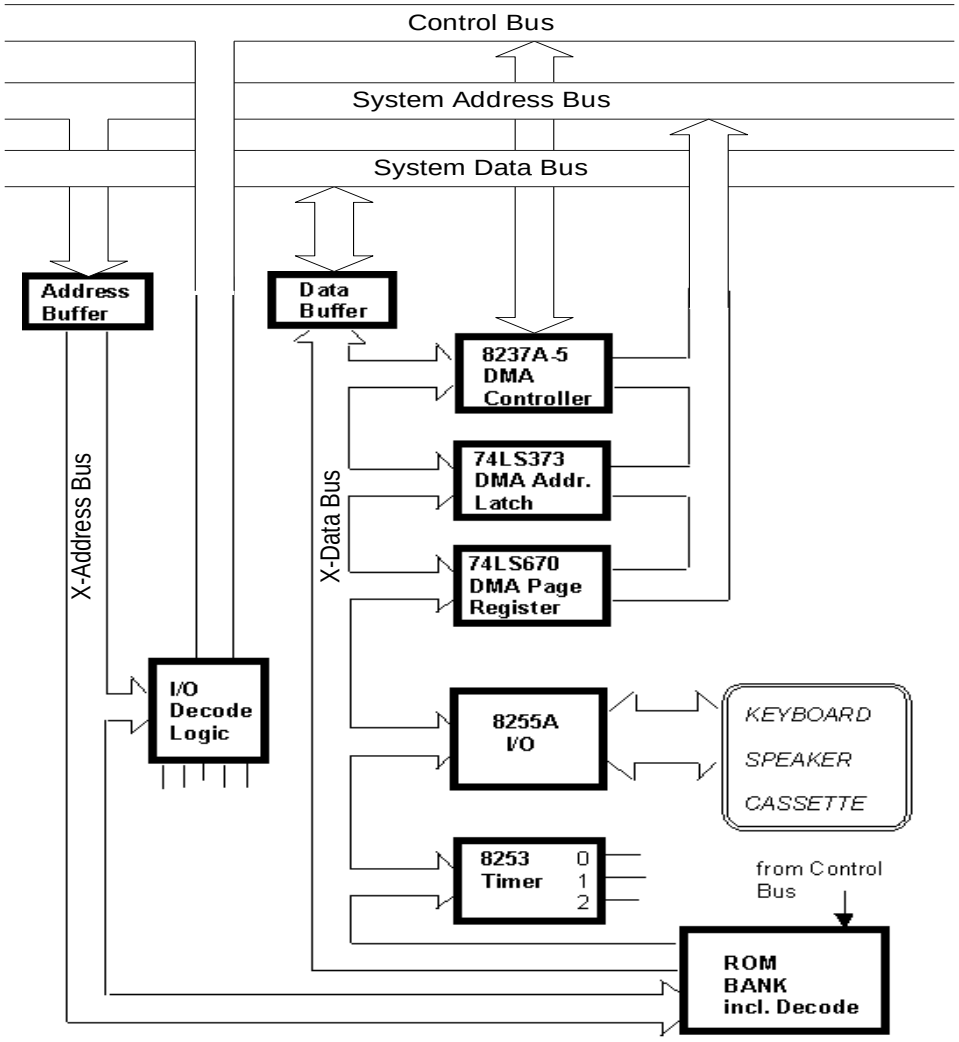
CO326 Computer Systems interfacing through computer busses XT and ISA Buses

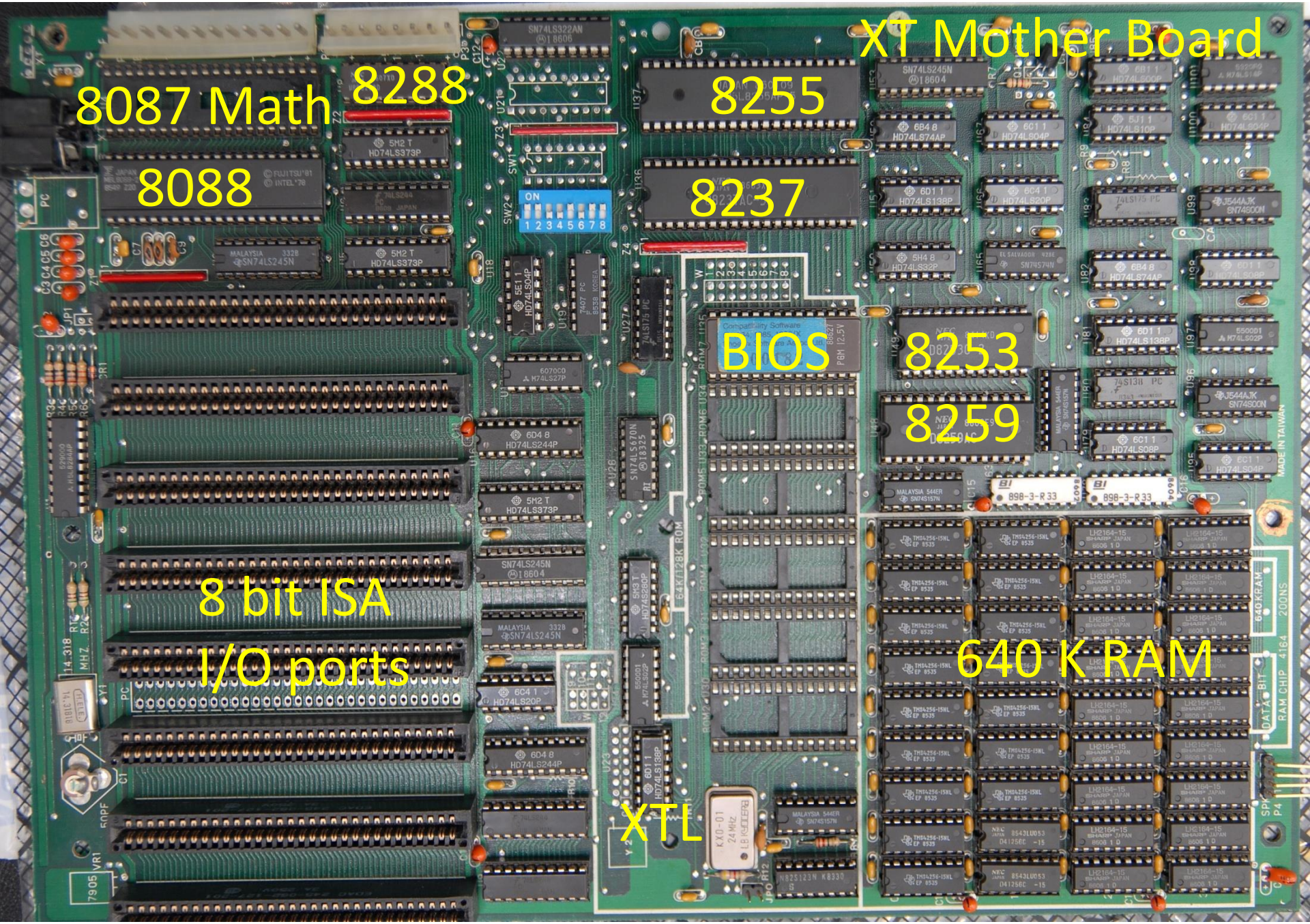
Kamalanath Samarakoon

Early PC Processor Circuitry

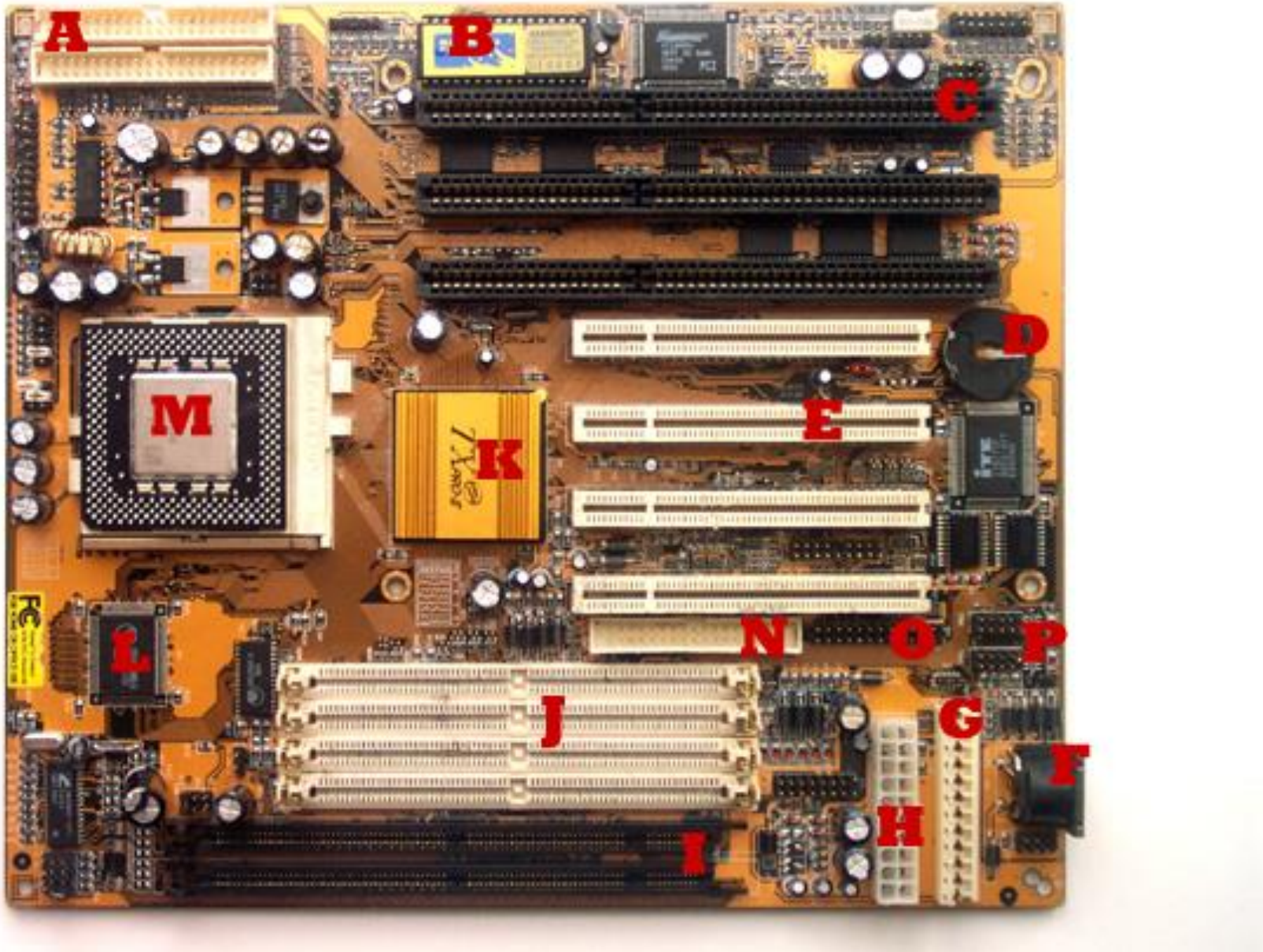


PC/XT: X-Bus and Support Circuitry




XT Mother Board
8087 Math
8288
8088
8255
8237
BIOS
8253
8259
8 bit ISA
I/O ports
640 K RAM
XTL

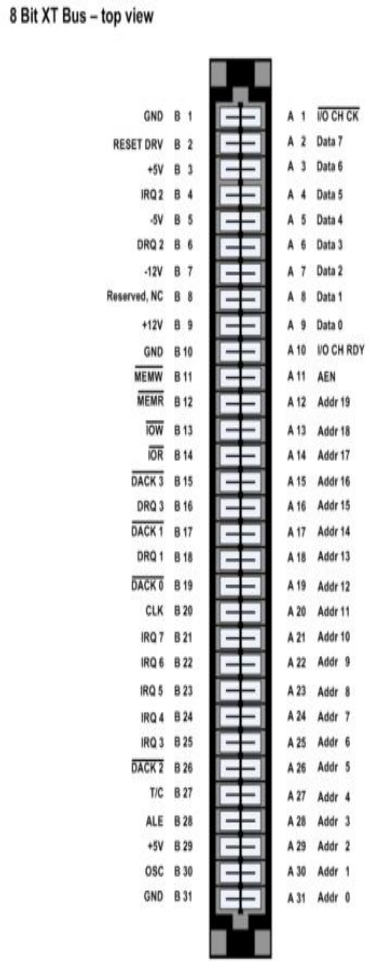
A Motherboard



PC-XT Mother Board

- 8088 Processor
- PC Bus (XT) 62 Lines
  - Data
    - 8 bit
  - Address
    - 20 bit address 1MB Max for Memory and I/O
  - Power (4 lines)
  - Control
    - IRQ (6 lines)
    - DMA(4 lines)

8 Bit XT Bus



8-Bit ISA Bus connector

1	GND	IO CHK
2	RESET	
3	+5V	
4	IRQ9	
5	-5V	
6	DRQ2	
7	-12V	
8	OWS	
9	+12V	
10	GND	IO RDY
11	MEMW	AEN
12	MEMR	
13	IOW	
14	IOR	
15	DACK3	
16	DRQ3	
17	DACK1	
18	DRQ1	
19	DACK0	
20	CLOCK	
21	IRQ7	
22	IRQ6	
23	IRQ5	
24	IRQ4	
25	IRQ3	
26	DACK2	
27	T/C	
28	ALE	
29	+5V	
30	OSC	
31	GND	

D0-D7

A0-A19

ISA Bus Connector Contains

8- bit Data Bus

Demultiplexed 20-bit address Bus

I/O and Memory Control Signals

Interrupt Request Lines (IRQ2->IRQ9)

DMA channels 1-3 Control Signals

Power, RESET and misc. signals

8 Bit XT Bus

-Bit ISA Bus connector

Pin #		
1	GND	IO CHK
2	RESET	
3	+5V	
4	IRQ9	
5	-5V	
6	DRQ2	
7	-12V	
8	OWS	
9	+12V	
10	GND	IO RDY
11	MEMW	AEN
12	MEMR	
13	IOW	
14	IOR	
15	DACK3	
16	DRQ3	
17	DACK1	
18	DRQ1	
19	DACK0	
20	CLOCK	
21	IRQ7	
22	IRQ6	
23	IRQ5	
24	IRQ4	
25	IRQ3	
26	DACK2	
27	T/C	
28	ALE	
29	+5V	
30	OSC	
31	GND	

D0-D7

A0-A19

- IRQ Interrupt request

ISA Bus Connector Contains

8- bit Data Bus

Demultiplexed 20-bit address Bus

I/O and Memory Control Signals

Interrupt Request Lines (IRQ2->IRQ9)

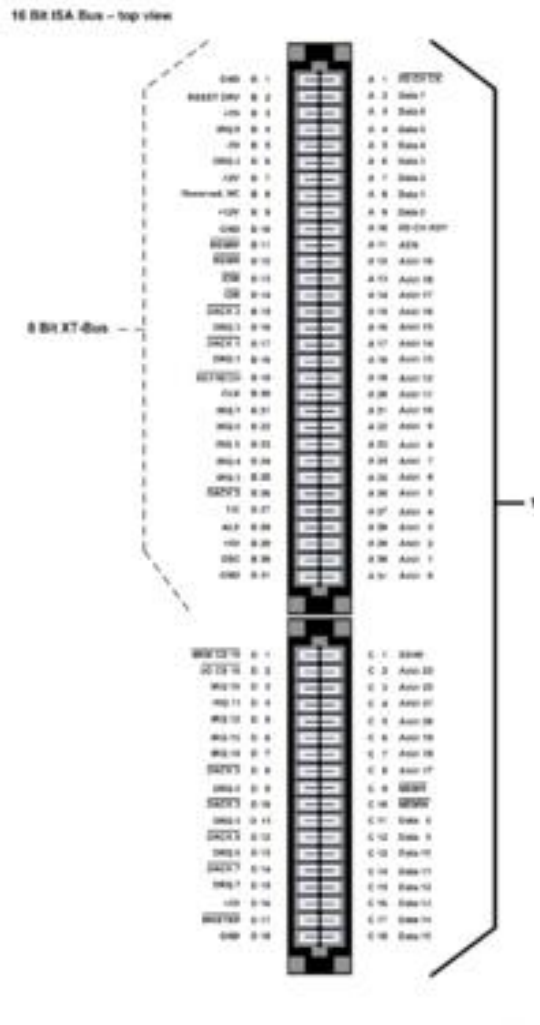
DMA channels 1-3 Control Signals

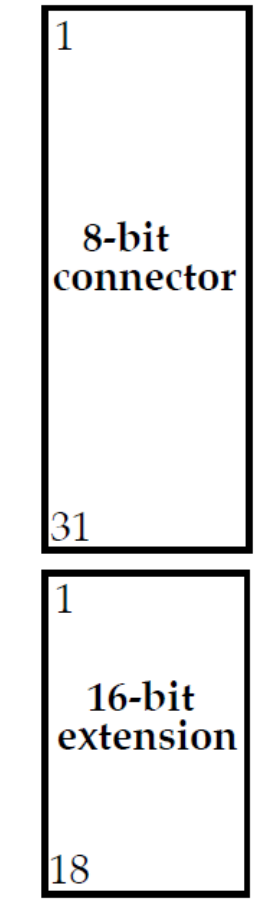
Power, RESET and misc. signals

8 Bit Bus Interface

- 4, 8-bit latches interfaced using an ISA interface for 32 bit parallel data.
- 74LS244 buffers used to ensure only **one lower power TTL load on the bus.**
- Loading is important as many cards can be connected on the bus.
- The DIP switch can be used to change the address thus avoiding address conflicts with other cards in the system.
- 16-bit ISA bus has an additional connector attached behind the 8-bit connector.
- Although 8 additional data bits, D8-D15, are available, the features most often used are the additional interrupt request and DMA request signals.

ISA Bus Connector

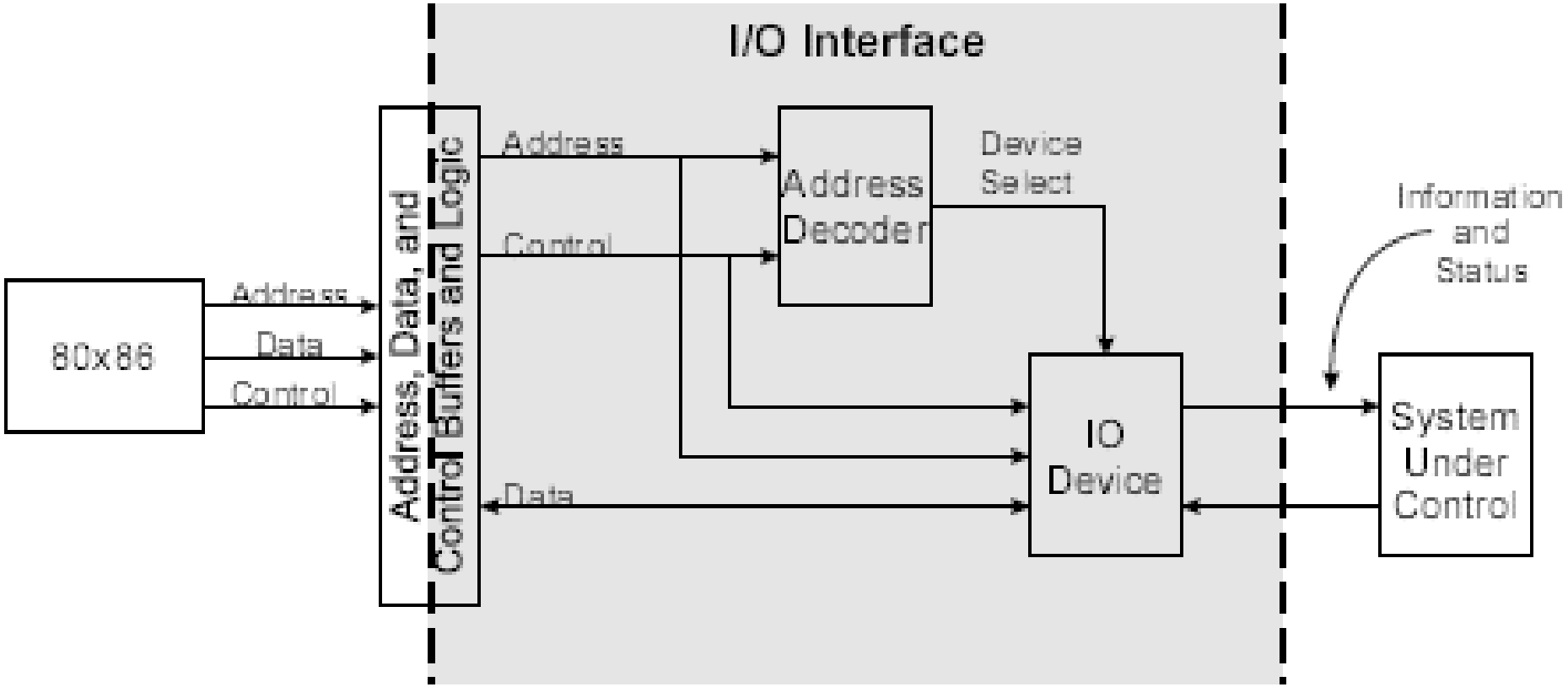




16-bit connector

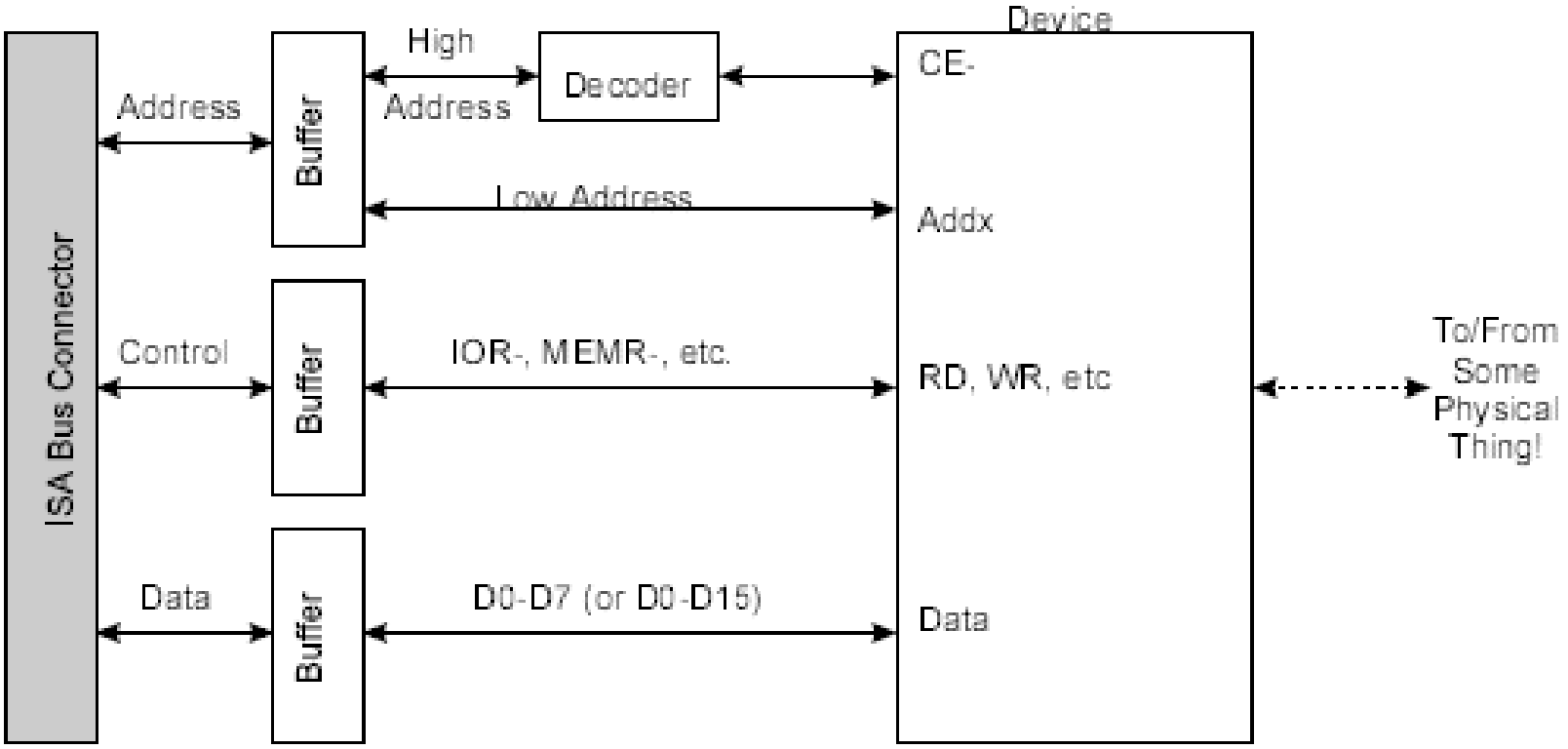
1	$\overline{\text{MCS16}}$	BHE
2	$\overline{\text{IOCS16}}$	A23
3	IRQ10	A22
4	IRQ11	A21
5	IRQ12	A20
6	IRQ15	A19
7	IRQ14	A18
8	$\overline{\text{DACK0}}$	A17
9	DRQ0	$\overline{\text{MEMR}}$
10	$\overline{\text{DACK5}}$	$\overline{\text{MEMW}}$
11	DRQ5	D8
12	$\overline{\text{DACK6}}$	D9
13	DRQ6	D10
14	$\overline{\text{DACK7}}$	D11
15	DRQ7	D12
16	+5V	D13
17	MASTER	D14
18	GND	D15

Basic architecture of ISA bus Interface

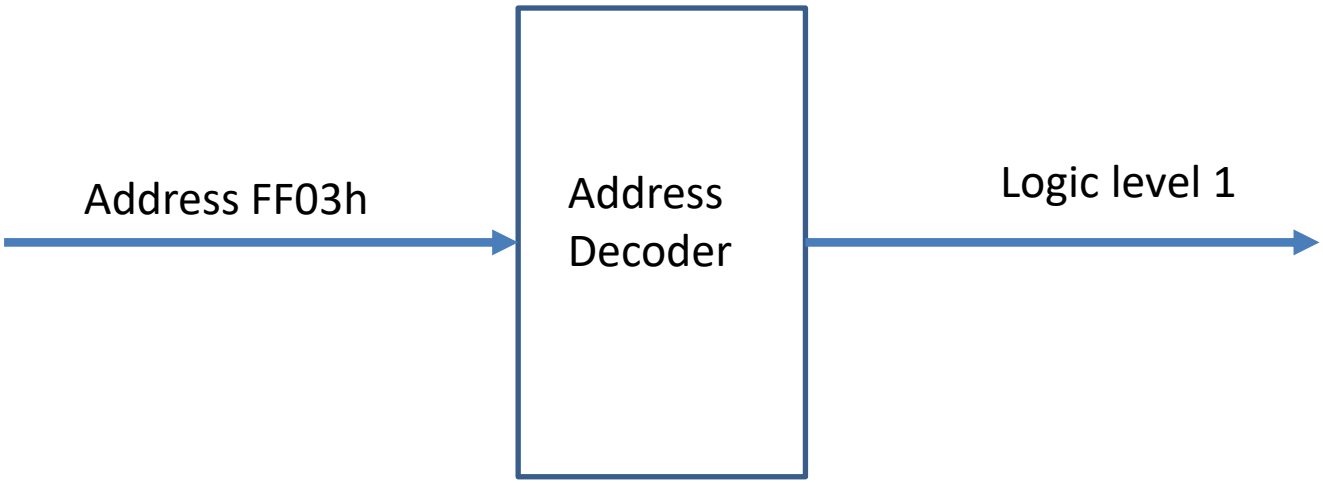


A Generic ISA-Bus Interface Card Design

The basic block diagram of an ISA-Bus interface includes buffers (to isolate the card from the ISA Bus), Address and control decoding (to make sure the card responds to the desired bus condition) and the stuff being controlled (memory or other devices).



Design an address decoder that generate logic level 1 when the address is FF03h



1. To design an interface card for address FF00h, FF01, FF02h, FF03h what is the suitable base address?

2. How many address lines should be connected to the address decoder?

3. How many address lines should be connected to the I/O device?

4. If the data bus is 8 bit how many bits can be input or output in this circuit?

5. Change the above address decoder such that the effective address can be set using dip switches.