EE386 – Electronics II

Lab 1 – Resistor Transistor Logic.

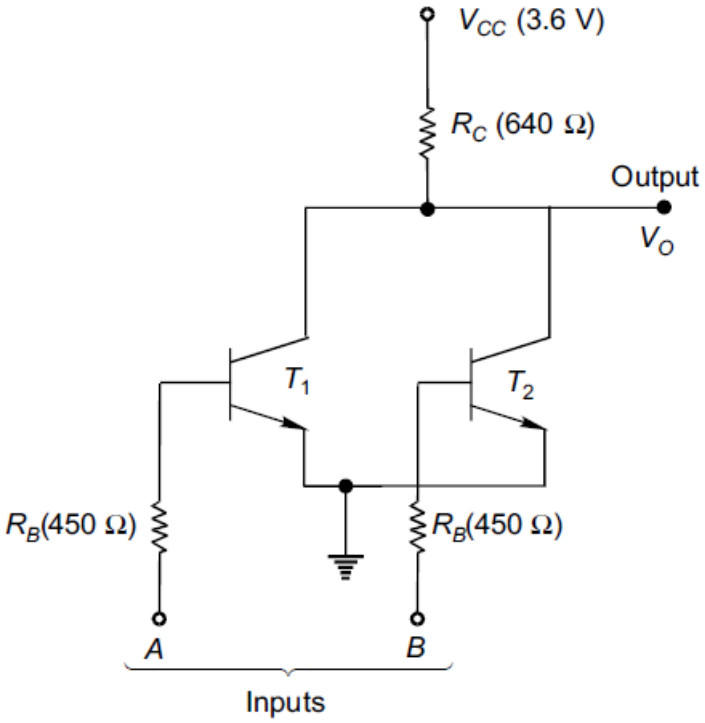
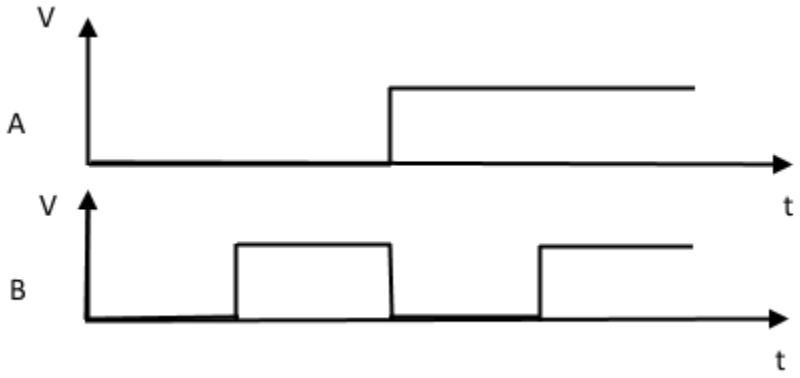


Fig.01

Given in Fig.01 is an unloaded two input Resistor Transistor Logic (RTL) NOR gate.

1. Implement the Circuit given in Fig.01 in your simulation environment using discrete components. Include the schematic of the implementation in your report).
2. Consider output voltage for logic 'LOW' TO BE 0.2 V (VOL=0.2 V) and output voltage for logic 'HIGH' to be 3.6 V (VOH = 3.6 V) and consider the $h_{FE}(\beta)$ of the transistors to be 30. Test the output of the unloaded circuit for following inputs.



   a. Plot the output waveform of the circuit.
   b. Verify the circuit is performing NOR operation.

3. Modify the circuit in Fig.01 to have five (05) load gates. (Include a schematic of the modified circuit in your report)
    a. What are the values of output voltages for logic LOW and logic HIGH.
    b. Calculate the power drawn by the circuit form the supply when
        i. Output is at logic LOW
        ii. Output is at logic HIGH
    c. Calculate the noise margins for logic LOW and logic HIGH.
4. Vary the number of load gates of the circuit in steps of 5, starting from 5 up to 50.
    a. Plot the variation of the output voltages with the number of load gates.
    b. Plot the variation of the noise margins with the number of load gates.