Department of Computer Engineering
Faculty of Engineering, University of Peradeniya

CO224

Computer Architecture - 2018

Skeleton Codes - Lab 5

Note: The following skeleton code is provided to help you understand the requirement. You are free to either use this code or write your own code from scratch.

- **ALU**

  module alu(RESULT, DATA1, DATA2, SELECT);

  //your code here//

  endmodule

- **Register File**

  module regfile8x8a (clk, INaddr, IN, OUT1addr, OUT1, OUT2addr, OUT2);

  //your code here//

  endmodule

- **Control Unit**

  module CU(instruction, OUT1addr, OUT2addr, INaddr);

  //your code here//

  endmodule

- **Instruction Register**

  module Instruction_reg (clk, Read_Addr, instruction);

  //your code here//

  endmodule

- **Program Counter**

  module counter (clk, reset,Read_addr);

  //your code here//

  endmodule

Testing

Implement the given instruction flow in your processor and see if you get the desired output for the following instructions.

loadi 4 X 0xFF

loadi 6 X 0xAA

loadi 3 X 0xBB

add 5 6 3

and 1 4 5

or 2 1 6

mov 7 x 2

sub 4 7 3

Device some more test cases and check your implementation of the processor.