EN2111 Electronic Circuit Design

Assignment: UART Implementation in FPGA

Submission Guidline

- This is a group assignment.
- Evaluation guidelines:

Evaluation	Method
Demonstration	Both simulation and hardware setups
Report	Upload the softcopy to Moodle

- In the written report, you should include observations and discussion with relevant plots to support your answers.

Tasks

1. Find a Verilog RTL for UART Transceiver.
2. Develop a testbench.
3. Implement your RTL design in FPGA and verify the operation with another group using 7segment displays.
4. Show your work to the instructor and get evaluated.
5. Take a snapshot of your FPGA with an oscilloscope showing the waveform (included in the report).

Report

1. RTL code for UART.
2. Testbench.
3. Timing diagram captured on simulation.

Evaluation Criteria

1. Correctness: protocol specification, clock constraints, etc.
2. Simulation verification.
3. FPGA implementation.
4. Documentation.