CS 104.3 Computer Architecture

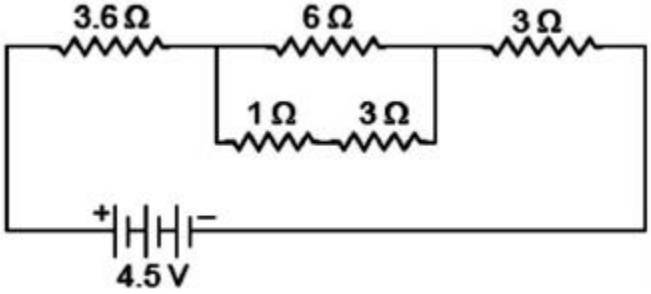
Examination Model Paper 2023 August

Question 1 (25 Marks)

1. Construct the truth table and the logical circuit for the following Boolean expressions.
    a. F = (A'.B'.C') + (A.C)'
    b. F = A XOR (B NAND C) NOR B'
2. Extract the SOP and POS expressions from the following Truth Table.

A	B	C	D	Output
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

3. Simply one of the expressions you extracted from the above table.
4. Construct a logical circuit for the simplified expression.
5. Calculate the total resistance and the current flow of the following circuit.



Question 2 (25 Marks)

1. Describe the sequence of events carried out during the machine cycle when executing the following instructions. (Use diagrams to assist your answer like you used to do in lecturers)

Address	Contents
100	JMP 200
200	LDA 1000
201	MPY 1001
202	STO 1002
1000	5
1001	10

2. Draw a diagram and describe the composition of the Central Processing Unit of the computer system.
3. Describe the components and their characteristics of Primary and Secondary memory. (Use a diagram to assist your answers)
4. Write short notes about the following.
    a. Harvard Architecture
    b. Cache Memory
    c. Dynamic RAM
    d. Program Counter

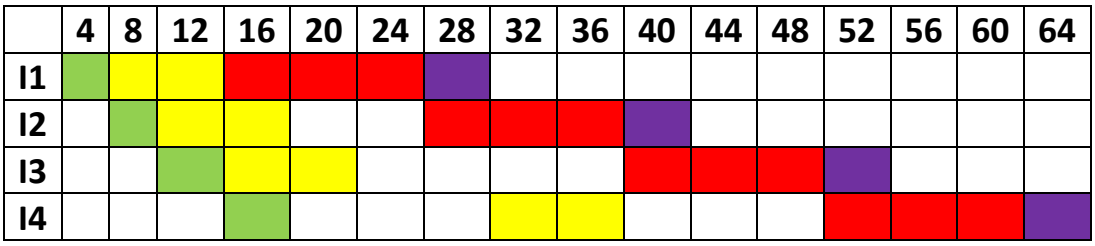
Question 3 (25 Marks)

1. Briefly explain the following two terms,
    a. Opcode
    b. Operand
2. In an instruction set there are 8 lines which are used for both addresses and data propagation. Calculate following.
    a. Amount of data it can carry.
    b. Number of addresses it can access.
3. Construct the truth table for the full adder and extract the expressions for SUM and CARRY.

4. Construct the logical circuit for the Full Adder.
5. Explain the difference between the Multiplexer and the Demultiplexer. (Use diagrams to assist your answer)

Question 4 (25 Marks)

1. Explain the difference between the Combinational Circuit and Sequential Circuit.
2. Demonstrate the functionality of the SR latch based on NOR gates including all the input cases and recheck each case with latching inputs. (Summary truth table and the logical circuit required)
3. Develop the SR latch you construct for the D Flip Flop.
4. The following diagrams shows the execution of 4 instructions in a pipelined processor.



   a. Identify any pipeline hazard if exists.
   b. What you should do to avoid it.
5. Explain what is Branching of Instructions and provide solutions for it.