First Draft of a Report on the EDVAC

The ***First Draft of a Report on the EDVAC*** (commonly shortened to ***First Draft***) is an incomplete 101-page document written by John von Neumann and distributed on June 30, 1945 by Herman Goldstine, security officer on the classified ENIAC project. It contains the first published description of the logical design of a computer using the stored-program concept, which has controversially come to be known as the von Neumann architecture.

Contents

History

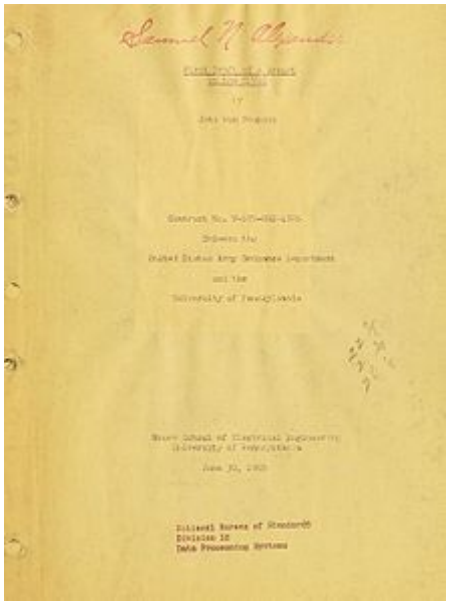
Von Neumann wrote the report by hand while commuting by train to Los Alamos, New Mexico and mailed the handwritten notes back to Philadelphia. Goldstine had the report typed and duplicated. While the date on the typed report is June 30, 24 copies of the *First Draft* were distributed to persons closely connected with the EDVAC project five days earlier on June 25. Interest in the report caused it to be sent all over the world; Maurice Wilkes of Cambridge University cited his excitement over the report's content as the impetus for his decision to travel to the United States for the Moore School Lectures in Summer 1946.

Synopsis

Von Neumann describes a detailed design of a "very high speed automatic digital computing system." He divides it into six major subdivisions: a central arithmetic part, CA, a central control part, CC, memory, M, input, I, output, O, and (slow) external memory, R, such as punched cards, Teletype tape, or magnetic wire or steel tape.

The CA will perform addition, subtraction, multiplication, division and square root. Other mathematical operations, such as logarithms and trigonometric functions are to be done with table look up and interpolation, possibly biquadratic. He notes that multiplication and division could be done with logarithm tables, but to keep the tables small enough, interpolation would be needed and this in turn requires multiplication, though perhaps with less precision.

Numbers are to be represented in binary notation. He estimates 27 binary digits (he did not use the term "bit," which was coined by Claude Shannon in 1948) would be sufficient (yielding 8 decimal place accuracy) but rounds up to 30-bit numbers with a sign bit and a bit to distinguish numbers from orders, resulting in 32-bit word he calls a *minor cycle*. Two's complement arithmetic is to be used, simplifying subtraction. For multiplication and division, he proposes placing the binary point after sign bit, which means all numbers are treated as being between −1 and +1 and therefore computation problems must be scaled accordingly.



Title page the *First Draft*, copy belonging to Samuel N. Alexander, who developed the SEAC computer based on the report.

Circuit design

Vacuum tubes are to be used rather than relays due to tubes' ability operate in one microsecond vs. 10 milliseconds for relays.

Von Neumann suggests (Sec. 5.6) keeping the computer as simple as possible, avoiding any attempt at improving performance by overlapping operations. Arithmetic operations are to be performed one binary digit at a time. He estimates addition of two binary digits as taking one microsecond and that therefore a 30-bit multiplication should take about 30^2 microseconds or about one millisecond, much faster than any computing device available at the time.

Von Neumann's design is built up using what he call "E elements," which are based on the biological neuron as model,[1][2] but are digital devices which he says can be constructed using one or two vacuum tubes. In modern terms his simplest E element is a two input AND gate with one input inverted (the inhibit input). E elements with more inputs have an associated threshold and produce an output when the number of positive input signals meets or exceed the threshold, so long as the (only) inhibit line is not pulsed. He states that E elements with more inputs can be constructed from the simplest version, but suggests they be built directly as vacuum tube circuits as fewer tubes will be needed.

More complex function blocks are to be built from these E elements. He shows how to use these E elements to build circuits for addition, subtraction, multiplication, division and square root, as well as two state memory blocks and control circuits. He does not use Boolean logic terminology.

Circuits are to be synchronous with a master system clock derived from a vacuum tube oscillator, possibly crystal controlled. His logic diagrams include an arrowhead symbol to denote a unit time delay, as time delays must be accounted for in a synchronous design. He points out that in one microsecond an electric pulse moves 300 meters so that until much higher clock speeds, e.g. 10^8 cycles per second (100 MHz), wire length would not be an issue.

The need for error detection and correction is mentioned but not elaborated.

Memory design

A key design concept enunciated, and later named the Von Neumann architecture, is a uniform memory containing both numbers (data) and orders (instructions).

> "The device requires a considerable memory. While it appeared that various parts of this memory have to perform functions which differ somewhat in their nature and considerably in their purpose, it is nevertheless tempting to treat the entire memory as one organ, and to have its parts even as interchangeable as possible for the various functions enumerated above." (Sec. 2.5)
>
> "The orders which are received by CC come from M, i.e. from the same place where the numerical material is stored." (Sec. 14.0)

Von Neumann estimates the amount of memory required based on several classes of mathematical problems, including ordinary and partial differential equations, sorting and probability experiments. Of these, partial differential equations in two dimensions plus time will require the most memory, with three dimensions plus time being beyond what can be done using technology that was then available. He concludes that memory will be the largest subdivision of the system and he proposes 8,192 minor cycles (words) of 32-bits as a design goal, with 2,048 minor cycles still being useful. He estimates a few hundred minor cycles will suffice for storing the program.

He proposes two kinds of fast memory, delay line and Iconoscope tube. Each minor cycle is to be addressed as a unit (word addressing, Sec. 12.8). Instructions are to be executed sequentially, with a special instruction to switch to a different point in memory (i.e. a jump instruction).

Binary digits in a delay line memory pass through the line and are fed back to the beginning. Accessing data in a delay line imposes a time penalty while waiting for the desired data to come around again. After analyzing these timing issues, he proposes organizing the delay line memory into 256 delay line "organs" (DLAs) each storing 1024 bits, or 32 minor cycles, called a *major cycle.* A memory access first selects the DLA (8 bits) and then the minor cycle within the DLA (5 bits), for a total of 13 address bits.

For the Iconoscope memory, he recognizes that each scan point on the tube face is a capacitor and that a capacitor can store one bit. Very high precision scanning will be needed and the memory will only last a short time, perhaps as little as a second, and therefore will need to be periodically recopied (refreshed).

Orders (instructions)

In Sec 14.1 von Neumann proposes the format for orders, which he calls a code. Order types include the basic arithmetic operations, moving minor cycles between CA and M (word load and store in modern terms), an order (*s*) that selects one of two numbers based on the sign of the previous operation, input and output and transferring CC to a memory location elsewhere (a jump). He determines the number of bits needed for the different order types, suggests *immediate orders* where the following word is the operand and discusses the desirability of leaving spare bits in the order format to allow for more addressable memory in the future, as well as other unspecified purposes. The possibility of storing more than one order in a minor cycle is discussed, with little enthusiasm for that approach. A table of orders is provided, but no discussion of input and output instructions was included in the First Draft.

Controversy

The treatment of the preliminary report as a publication (in the legal sense) was the source of bitter acrimony between factions of the EDVAC design team for two reasons.[3] First, publication amounted to a public disclosure that prevented the EDVAC from being patented; second, some on the EDVAC design team contended that the stored-program concept had evolved out of meetings at the University of Pennsylvania's Moore School of Electrical Engineering predating von Neumann's activity as a consultant there, and that much of the work represented in the *First Draft* was no more than a translation of the discussed concepts into the

language of formal logic in which von Neumann was fluent. Hence, failure of von Neumann and Goldstine to list others as authors on the *First Draft* led credit to be attributed to von Neumann alone. (See Matthew effect and Stigler's law.)

See also

- Electronic delay storage automatic calculator (EDSAC), an early British computer inspired by *First Draft of a Report on the EDVAC*
- Harvard Mark I, an early electromechanical computer with instructions and numerical data kept separate (Harvard architecture)

References

1. Von Neumann credits this model to Warren McCulloch and Walter Pitts, *A logical calculus of the ideas immanent in nervous activity* (http://www.cse.chalmers.se/~coquand/AUTOMATA/mcp.pdf), Bull. Math. Biophysics, Vol. 5 (1943), pp. 115–133
2. Von Neumann had worked closely with McCulloch and Pitts. See The Man Who Tried to Redeem the World with Logic (http://nautil.us/issue/21/information/the-man-who-tried-to-redeem-the-world-with-logic), Amanda Gefter, Nautilus, Issue 21, February 4, 2015
3. Moye, William T. (January 1996), *ENIAC: The Army-Sponsored Revolution* (https://web.archive.org/web/20130305070628/http://ftp.arl.army.mil/mike/comphist/96summary/index.html), United States Army Research Laboratory, archived from the original (http://ftp.arl.army.mil/mike/comphist/96summary/index.html) on 2013-03-05, retrieved 2012-11-26

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External links

- Oral history interview with J. Presper Eckert (http://purl.umn.edu/107275), Charles Babbage Institute, University of Minnesota. Eckert, a co-inventor of the ENIAC, discusses its development at the University of Pennsylvania's Moore School of Electrical Engineering; describes difficulties in securing patent rights for the ENIAC and the problems posed by the circulation of John von Neumann's 1945 *First Draft of the Report on EDVAC*, which placed the ENIAC inventions in the public domain. Interview by Nancy Stern, 28 October 1977.