Design Report – Team 02

ELETENG209: Analogue & Digital Design

*Design of a Smart Energy Monitor*

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# Abstract

This report describes the design, validation and operation of a smart energy monitor capable of measuring the power utilised by an appliance using electrical hardware and firmware implementations.

# Introduction

The main objective of this project was to gain valuable expertise and experience and to fulfil the course requirements of ELECTENG 209.

This Smart Energy Monitor can measure the power, peak current, RMS voltage, and total energy supplied to a load within specifications. The analogue circuitry measures, filters, and amplifies signals so they are appropriate digital processing. The microcontroller’s firmware samples these signals and interpolates the resulting data to provide an accurate digital representation of the analogue input signals. Results of the completed processing can be sent to a display, smartphones via Bluetooth, and computers using a USB to Serial cable. This overall architecture is summarised in Fig. 1.

# Diagram Description automatically generated

Fig. 1: A conceptual system diagram [1]

# Literature Research

Table I: A Comparison of existing energy meters

|  |  |  |
| --- | --- | --- |
| Parameter | Neurio Smart Monitor | Efergy Pro |
| Operating voltage range | 90 – 130V | 110-300V AC |
| Accuracy | ±1% of reading | 98% |
| Power Consumption | < 2 W | 0.2 W |
| Communication/Display Method | Wi-Fi, Bluetooth, wired | Wi-Fi |
| Peak Current | --- | 95 mA |
| Operating Temperature | 0 - 65°C | 0 - 35°C |
| Measurements | Irms, Vrms, W, X, Wh | W, Irms, Vrms, Energy (Wh) |

# Design Specifications

The key differences are in the communication type, operating voltage, and types of measurements. The Neurio monitor measures all the quantities this monitor can, but in addition measures reactive power (X). Efergy Pro only measures Energy. The Nuerio monitor provides Wi-Fi capability in addition to the methods used by the monitor described in this report.

Table II: Design Specifications

|  |  |
| --- | --- |
| Parameter | Configuration |
| Source Voltage | 14VRMS ± 10% |
| Source Frequency | 50Hz ± 2% |
| Load Range | 2.5VA to 7.5VA |
| Load Power Factor | 0.75 to 0.99 |
| Measurement Accuracy | 5% of full-scale reading |
| ADC Conversion Rate | 1kHz or slower |
| LCD Display Information | Voltage, current, power and energy |
| LCD Display Units | VRMS, Apk, W and Wmin |
| LCD Scroll Rate | 1s |
| UART Baud Rate | 9600 Baud |
| Information Transferred Via UART | Voltage, Current, Power and Energy |
| PCB Size | 200 mm­­­­2 |
| PCB Technology | Double layer with PTH |
| Device Technology | TH or SMT |

# The Analogue Design

## The Schematic

To maximize the usable range of the ADC, the gain of the signal conditioning circuitry was increased as much as possible. This allows the greatest effective input resolution, and therefore a more accurate sampling of the input signals.

Fig. 2, Schematic of analogue circuitry

## The PCB

An additional current limiting resistor has been added to the output of the linear regulator to ensure correct operation of the regulator package.



Fig. 3, 2D PCB layout Fig. 4, 3D PCB layout

## Design Validation

For naming convention refer to: <https://ee2092020class.github.io/presentations/DigitalL4/presentation.html#5>.

Table III: Key design parameters

|  |  |  |
| --- | --- | --- |
| Parameter | Calculated | Simulated |
| Gvs | (3300/56000 + 3300) = 0.056 | |
| Vvs when VAC is 15.4 Vrms | 0.989 V | 986 mV |
| Vvs when VAC is 12.6 Vrms | 0.81 V | 805 mV |
| Gis | 0.56 | |
| Vis when IAC is 0.60 Arms | 0.47 V | 0.446 V |
| Vis when IAC is 0.16 Arms | 0.127 V | 0.125 V |
| Gvo | (4700/4700) = 1 | |
| Vvo when VAC is 15.4 Vrms | 3.09 V | 3.09 V |
| Vvo when VAC is 12.6 Vrms | 2.91 V | 2.91 V |
| Gio | (56000/22000) = 2.55 | |
| Vio when IAC is 0.60 Arms | 3.1 V | 3.08 V |
| Vio when IAC is 0.16 Arms | 2.37 V | 2.37 V |
| Gvf | 1 | |
| Vvf when VAC is 15.4 Vrms | 3.32 V | 3.29 V |
| Vvf when VAC is 12.6 Vrms | 3.1 V | 3.08 V |
| Gif | 1 | |
| Vif when IAC is 0.60 Arms | 3.31 V | 3.29 V |
| Vif when IAC is 0.16 Arms | 2.42 V | 2.43 V |
| ΔVin of 5V regulator | 2.13 V | 1.56 V |
| ΔV5V of 5V regulator | 0 V | 0 V |

# The Embedded Software Design

## Flowchart

A custom print function was implemented for use by the UART peripheral to reduce clutter, memory used, and to increase functionality. This function can transmit directly to the terminal by using

*print(“xyz: %d %f”, current, voltage);*

Fig. 5, Flowcharts of ADC and UART firmware

Fig. 6, Flowchart of TIMER0 firmware

Additionally, cubic interpolation and Simpsons Rule was used to integrate points for power and RMS voltage. The method interpolation used was specifically chosen due to its ability to accurately predict the peak values of sinusoidal waves.



Fig. 7, Flowchart of digital signal processing firmware

## Peripheral Configurations

Table IV: UART configuration

|  |  |
| --- | --- |
| Parameter | Configuration |
| Number of data bits | 8 |
| Number of stop bits | 1 |
| Baud rate | 9600 |
| Parity mode | None |
| Transmission mode | Simplex (transmit) |
| Transmit mode | Polling (UDRE0) |
| Transmit voltage | 5 V |

Table V: ADC configuration

|  |  |
| --- | --- |
| Parameter | Configuration |
| Prescaler | 4 (sim), 128 (hardware) |
| Timer0 ADC mode | CTC A auto trigger |
| ADC interrupt time | 1ms |
| Voltage reading | ADC channel 0 |
| Current reading | ADC channel 1 |
| OCR0A | 99 (sim), 124 (hardware) |

Table VI: Display Configuration

|  |  |
| --- | --- |
| Parameter | Configuration |
| 7-Segment pin operation | Common Cathode |
| Units display | Ds4 |
| Clock Pulse bit | SH\_CP |
| Timer2 interrupt time | 1ms |
| Timer2 OCR2A | 99 (sim), 124 (hardware) |
| Timer2 display update interval | 10ms |
| 4 Display operation | Shift Register |

Table VII: I/O pins

|  |  |
| --- | --- |
| Parameter | Configuration |
| 7 Seg Display Output | Ds1, Ds2, Ds3, Ds4 (PD4, PD5, PD6, PD7) |
| Reading Shift Register | SH\_DS (PC4) |
| Toggle shift register | SH\_ST (PC5) |
| LED toggle for testing operation | LED (PB5) |

## Design Validation

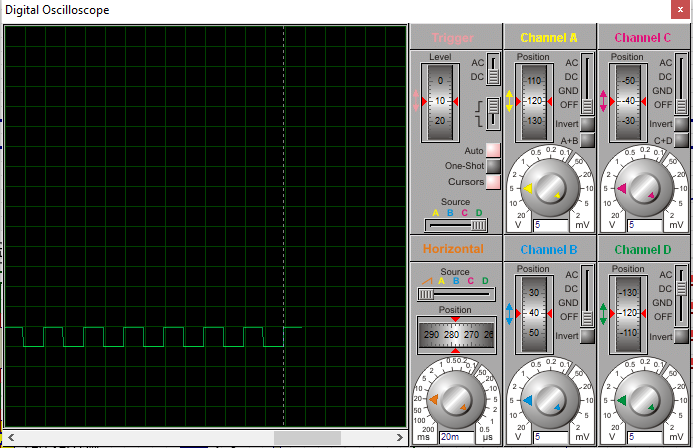
The zero crossing ISR (INT0) triggers every 20ms. The LED triggers as indication for when output compare match A is successful. From Fig. 8, the oscilloscope show that the LED toggles every 20ms.

Fig. 8, Supply voltage of LED toggled by voltage zero crossing interrupt

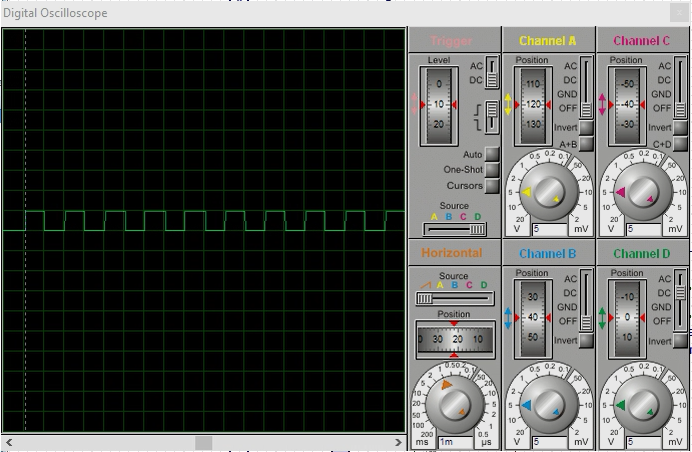


Fig. 9, Supply voltage of LED toggled by ADC complete conversion interrupt. ADC sampling ISR (ADC\_vect) samples the ADC channel and toggles every 1ms.

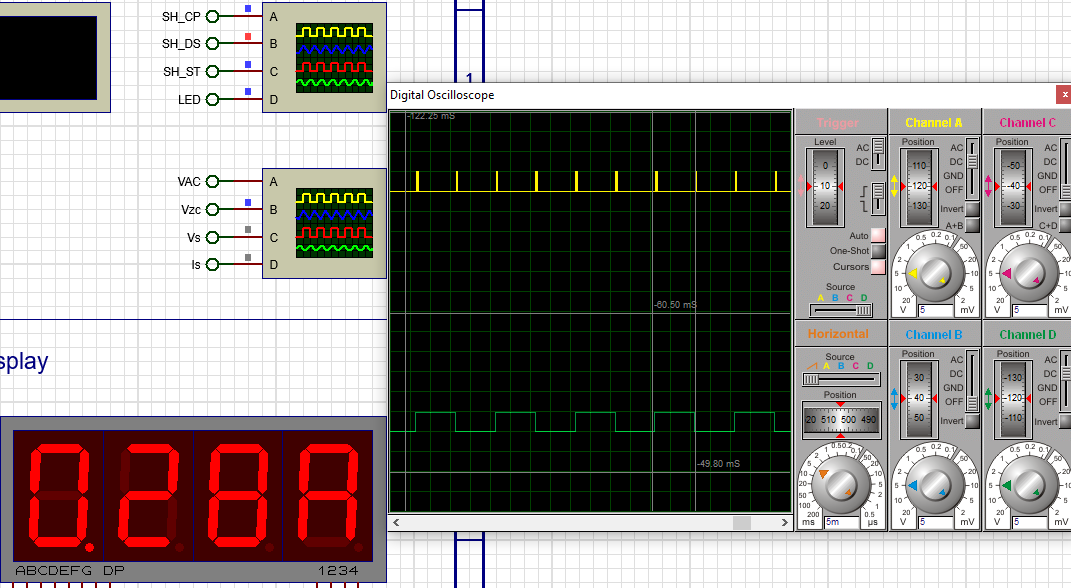
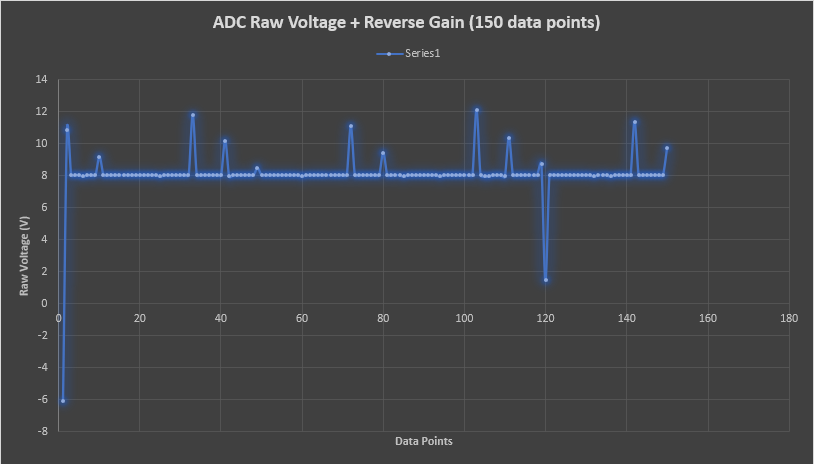
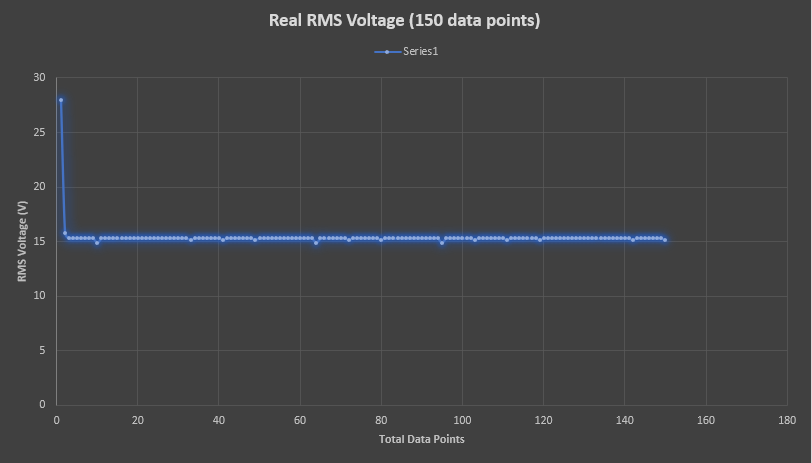
Timer2 triggers approximately every 10.8ms. Timer2 is used to drive the refresh rate of the seven-segment display. Shown in Fig 10, the shift register clock pulse control signal (SH\_CP, in yellow) is used to move data into the shift register.

Fig. 10, Voltage supply to LED toggled by TIMER2 interrupt in green, shift register clock pulse in yellow

When applying a 15.4Vrms DC voltage, the ADC voltage conversion appears constant, with occational deviations. This is believed to be due to ADC sampling errors, must likely in the quantification stage. The deviations fluctuates with 1-7mV error.

After processing the ADC raw voltage through numerical integration and cubic interpolation, the results are more consistant. The deviation error is reduced to between 0.4-0.5mV.

**BEFORE**

**AFTER**

# Performance of the Energy Monitor

## Design Validation

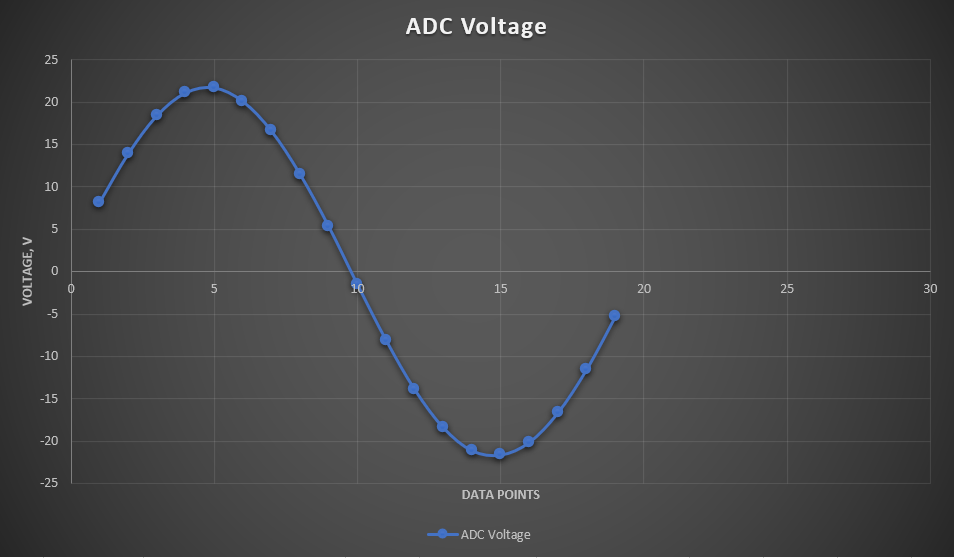
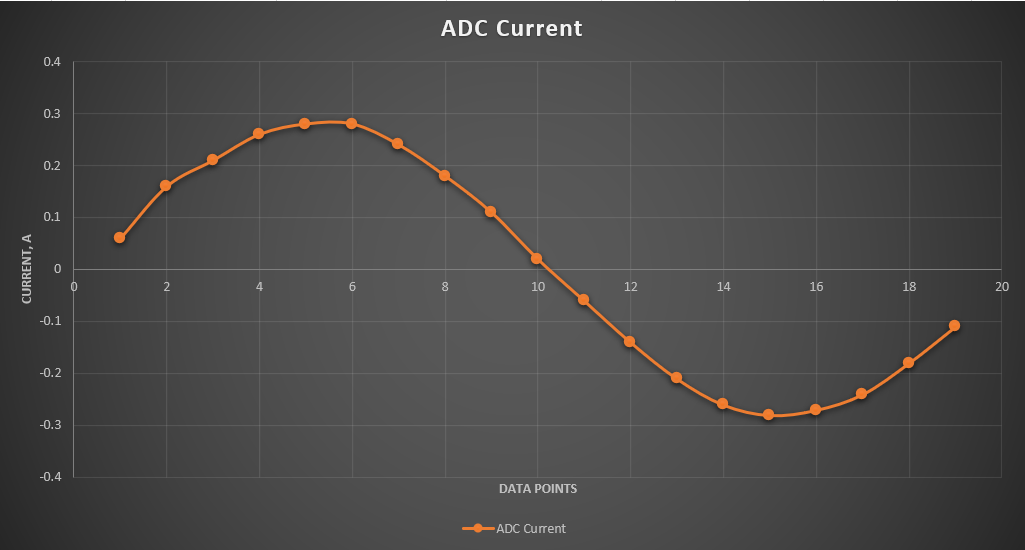
Fig. 11 One cycle of sampled and transformed voltage values

Fig. 12, One cycle of sampled and transformed current values

## The Accuracy

The current measured from Proteus was not the peak current, hence it was multiplied by √2 so it better compares with our calculated values.

Fig. 14, Ideal Peak Current vs Error graph

Fig. 15, Ideal RMS Voltage vs Error graph

Fig. 16, Ideal Average Power vs Error graph

# Conclusions

# In conclusion to our Energy Monitor Project, this report discusses how our Energy Monitor operates in terms of its firmware and hardware, accuracy, workability, and comparisons to commercial grade products. We were able to achieve accurate calculations with the use of software and numerical techniques. We hope that this report has given the reader some insight on our Energy Monitor and how it can be used as a real-world example.

# References

1. D. J. Thrimawithana, Class Lecture, Topic: "Analogue & Embedded Software Design: An Introduction to the Course" ELECTENG 209, Department of Electrical, Computer, and Software Engineering, The University of Auckland, Auckland, October 2020.

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