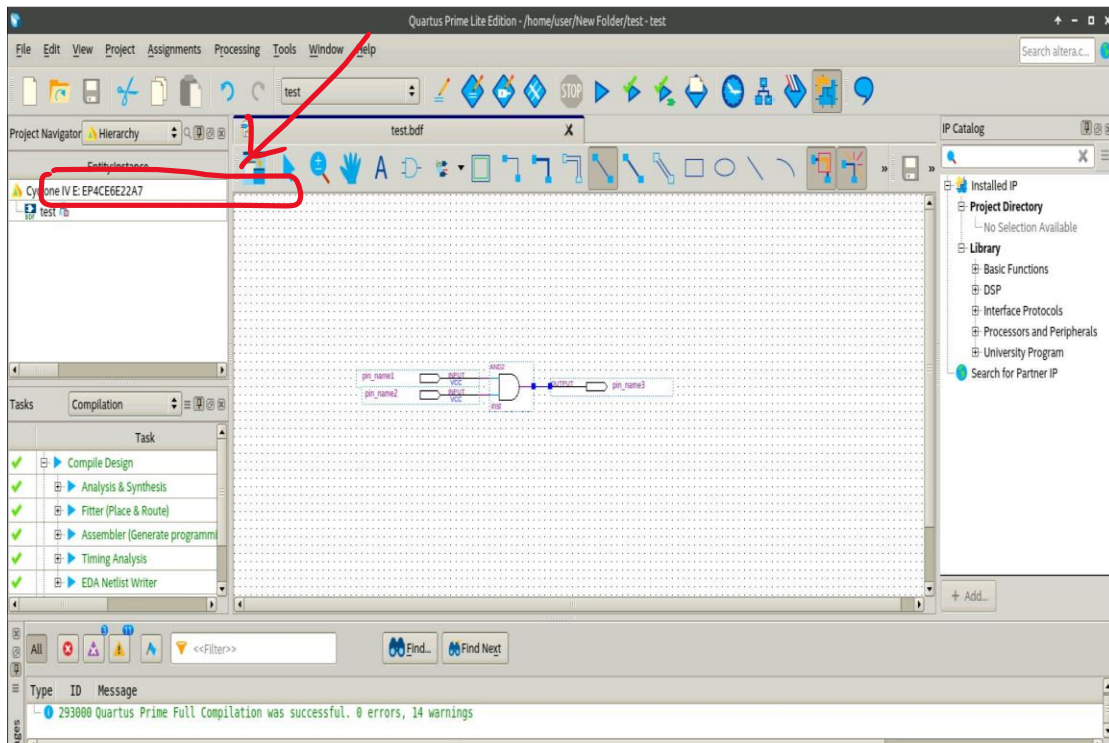


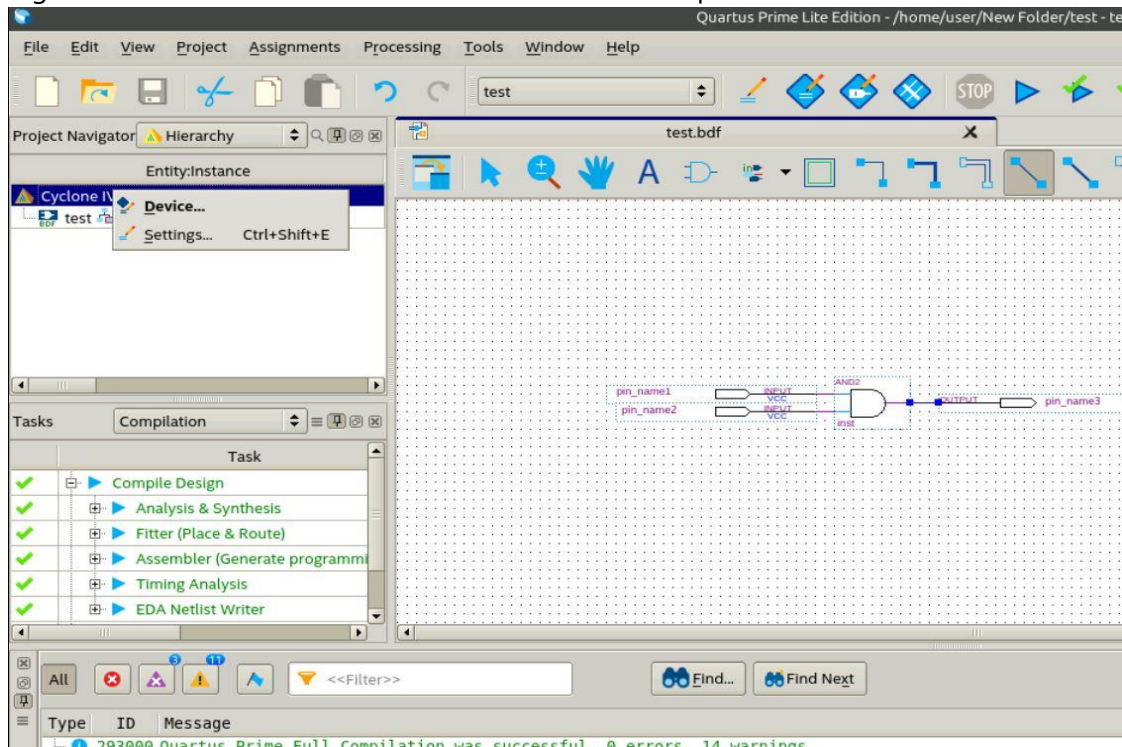
Switch device on Quartus II

some students select the wrong board when creating new project in Quartus and only realize their mistake when they go to burn their code to the board. So, they need to change their board selection. The instruction will provide you how to switch device without recreate a new project again.

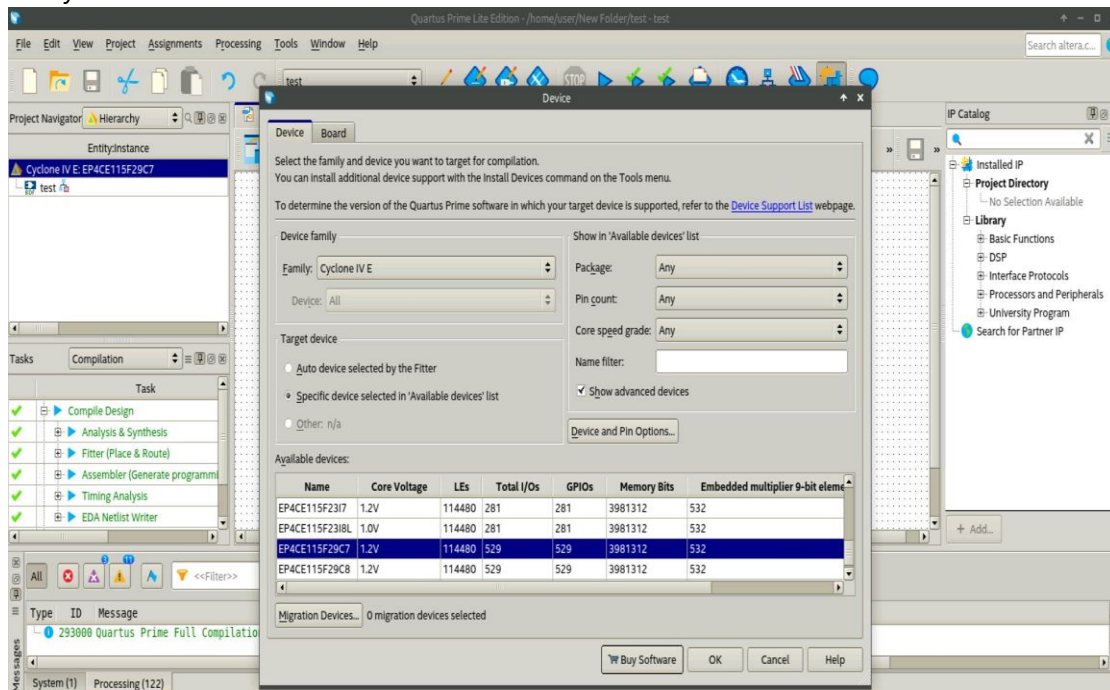
1. First check your device under the project navigator. It should be Cyclone IV E and device EP4CE115F29C7



2. Right click on the current device and select 'Device' to open the device menus



3. Then re-select the correct device, Cyclone IV E and device EP4CE115F29C7. And then click "okay" to finish.



4. Recompile your diagram and confirm that it shows the correct device on your compilation report.

The screenshot shows the Quartus II software interface. The 'Project Navigator' on the left shows the project 'test' with a hierarchy of 'Entity/Instance' and 'test'. The 'Table of Contents' in the center lists various compilation steps, with 'Flow Summary' selected. The 'Flow Summary' panel on the right displays the compilation results. A red circle highlights the 'Device' field, which is 'EP4CE115F29C7', and a red arrow points to it from the top right. The 'Flow Status' is 'Successful - Fri Sep 24 21:29:14 2021'. The 'Quartus Prime Version' is '20.1.1 Build 720 11/11/2020 3J Lite Edition'. The 'Revision Name' is 'test'. The 'Top-level Entity Name' is 'test'. The 'Family' is 'Cyclone IV E'. The 'Device' is 'EP4CE115F29C7'. The 'Timing Models' are 'Final'. The 'Total logic elements' are '1 / 114,480 (< 1 %)'. The 'Total registers' are '0'. The 'Total pins' are '3 / 529 (< 1 %)'. The 'Total virtual pins' are '0'. The 'Total memory bits' are '0 / 3,981,312 (0 %)'. The 'Embedded Multiplier 9-bit elements' are '0 / 532 (0 %)'. The 'Total PLLs' are '0 / 4 (0 %)'.

Flow Status	Successful - Fri Sep 24 21:29:14 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 3J Lite Edition
Revision Name	test
Top-level Entity Name	test
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	1 / 114,480 (< 1 %)
Total registers	0
Total pins	3 / 529 (< 1 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

5. Now you are all good to go. Open a new assignment editor to connect the nodes.