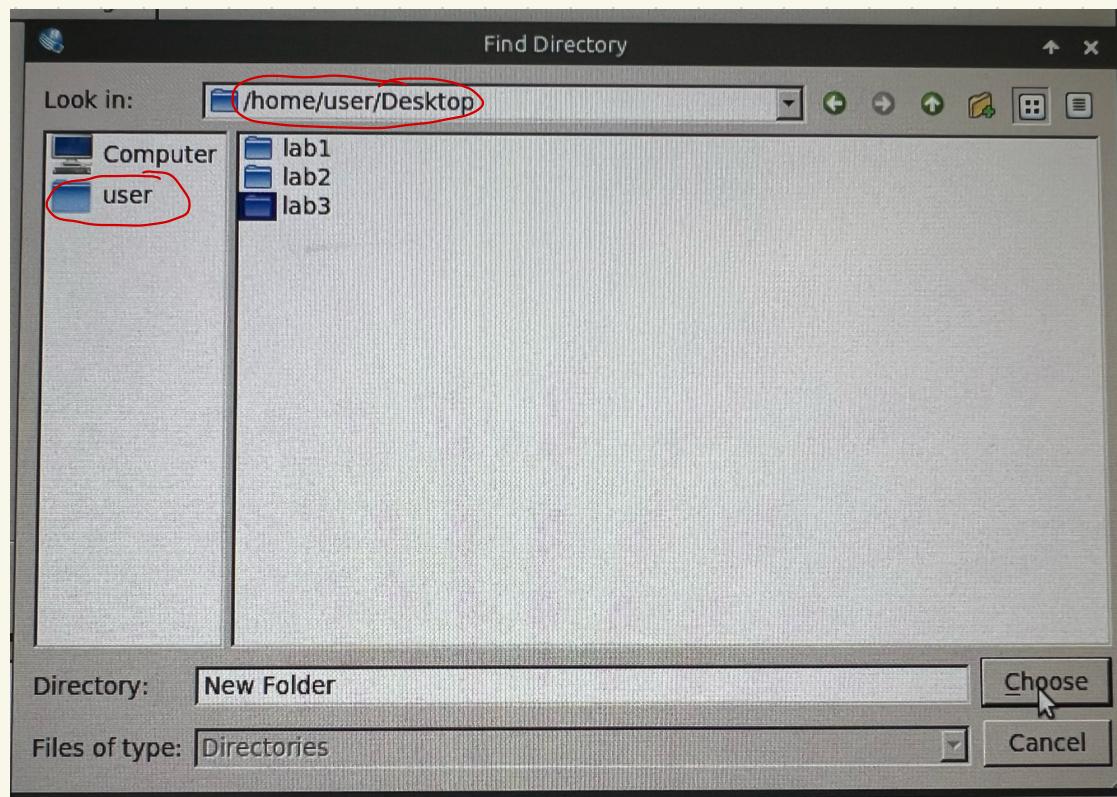




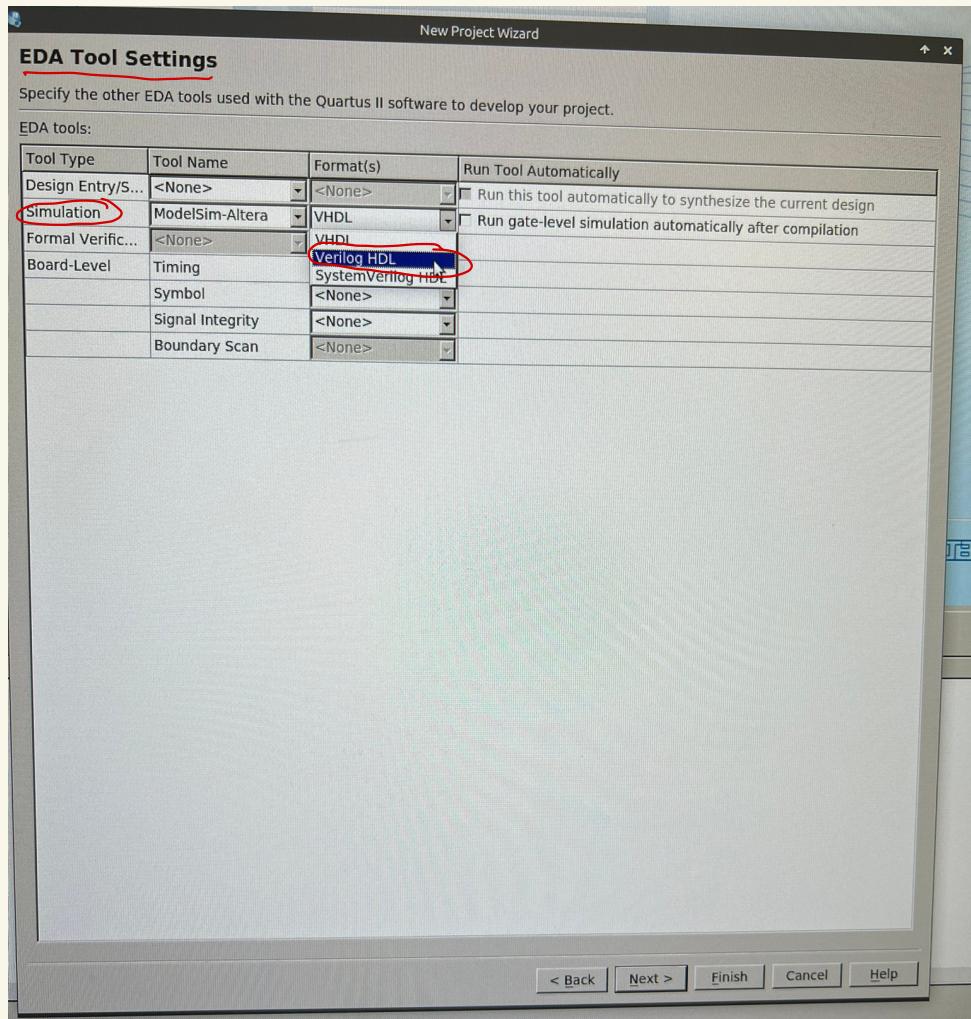
# LAB 1

- Open a project/working directory in Quartus (directly on Linux, Windows virtual machine not needed)
- Design an AND gate
- Run your AND gate on FPGA board

Choose an “easy” working directory



# Choose the correct simulation format: Verilog HDL



# Choose the correct device: EP4CE115F29C7

New Project Wizard

## Family & Device Settings

Select the family and device you want to target for compilation.  
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus II software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone IV E  
Devices: All

Target device

Auto device selected by the Fitter  
 Specific device selected in 'Available devices' list  
 Other: n/a

Show in 'Available devices' list

Package: Any  
Pin count: Any  
Core Speed grade: Any  
Name filter:   
 Show advanced devices

Available devices:

| Name           | Core Voltage | LEs    | Total I/Os | GPIOs | Memory Bits | Embedded multiplier 9-bit ekl <sup>△</sup> |
|----------------|--------------|--------|------------|-------|-------------|--|
| EP4CE75F29I7   | 1.2V         | 75408  | 293        | 293   | 2810880     | 400  |
| EP4CE75F29I8L  | 1.0V         | 75408  | 293        | 293   | 2810880     | 400  |
| EP4CE75F29C6   | 1.2V         | 75408  | 427        | 427   | 2810880     | 400  |
| EP4CE75F29C7   | 1.2V         | 75408  | 427        | 427   | 2810880     | 400  |
| EP4CE75F29C8   | 1.2V         | 75408  | 427        | 427   | 2810880     | 400  |
| EP4CE75F29C8L  | 1.0V         | 75408  | 427        | 427   | 2810880     | 400  |
| EP4CE75F29C9L  | 1.0V         | 75408  | 427        | 427   | 2810880     | 400  |
| EP4CE75F29I7   | 1.2V         | 75408  | 427        | 427   | 2810880     | 400  |
| EP4CE75F29I7   | 1.2V         | 75408  | 427        | 427   | 2810880     | 400  |
| EP4CE75U19I7   | 1.2V         | 75408  | 293        | 293   | 2810880     | 400  |
| EP4CE115F23C7  | 1.2V         | 114480 | 281        | 281   | 3981312     | 532  |
| EP4CE115F23C8  | 1.2V         | 114480 | 281        | 281   | 3981312     | 532  |
| EP4CE115F23C8L | 1.0V         | 114480 | 281        | 281   | 3981312     | 532  |
| EP4CE115F23C9L | 1.0V         | 114480 | 281        | 281   | 3981312     | 532  |
| EP4CE115F23I7  | 1.2V         | 114480 | 281        | 281   | 3981312     | 532  |
| EP4CE115F23I8L | 1.0V         | 114480 | 281        | 281   | 3981312     | 532  |
| EP4CE115F29C7  | 1.2V         | 114480 | 529        | 529   | 3981312     | 532  |
| EP4CE115F29C8  | 1.2V         | 114480 | 529        | 529   | 3981312     | 532  |
| EP4CE115F29C8L | 1.0V         | 114480 | 529        | 529   | 3981312     | 532  |
| EP4CE115F29C9L | 1.0V         | 114480 | 529        | 529   | 3981312     | 532  |
| EP4CE115F29I7  | 1.2V         | 114480 | 529        | 529   | 3981312     | 532  |
| EP4CE115F29I8L | 1.0V         | 114480 | 529        | 529   | 3981312     | 532  |

< Back | Next > | Finish | Cancel | Help

# Design an AND gate

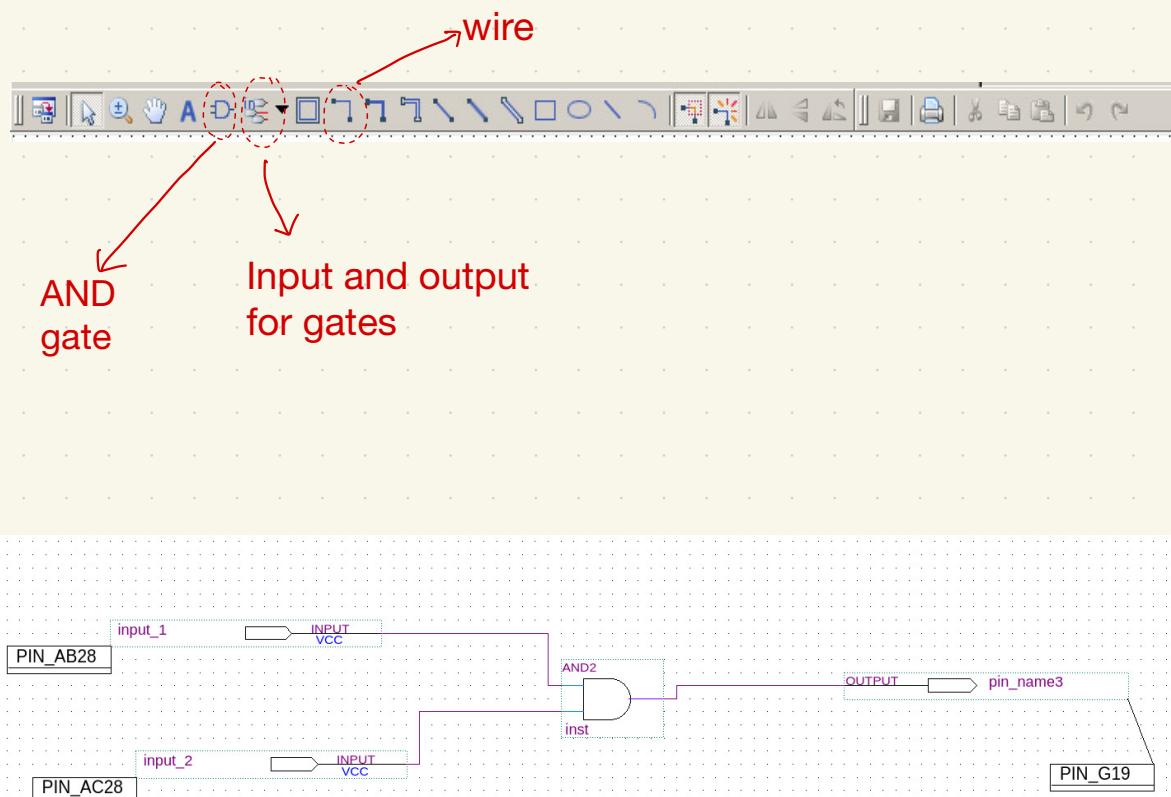
AND:

| Input 1 | Input 2 | Output |
|---------|---------|--------|
| 0       | 0       | 0      |
| 0       | 1       | 0      |
| 1       | 0       | 0      |
| 1       | 1       | 1      |

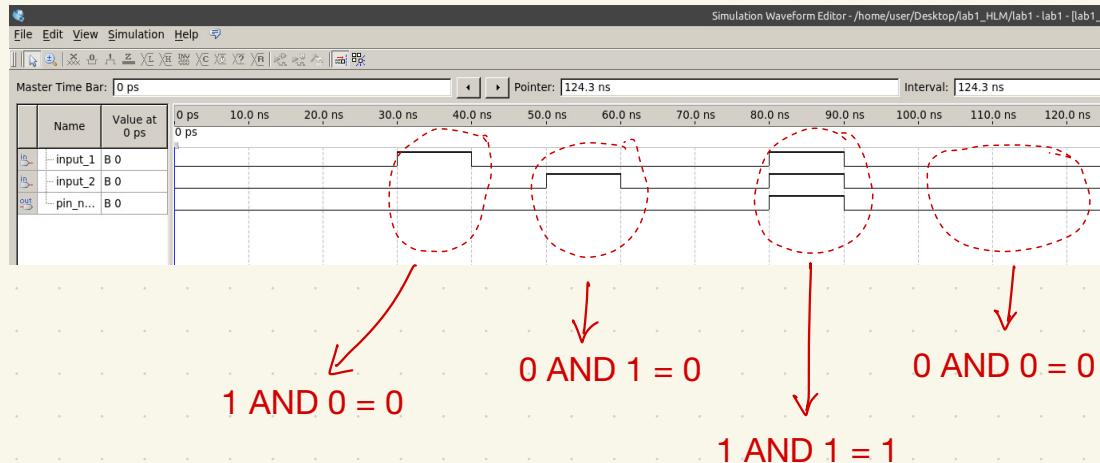
On FPGA:

| Switch 1 | Switch 2 | LED |
|----------|----------|-----|
| OFF      | OFF      | OFF |
| OFF      | ON       | OFF |
| ON       | OFF      | OFF |
| ON       | ON       | ON  |

# Design on Quartus



# Run the Waveform



# Run on FPGA

| <<new>> | From      | To       | Assignment Name | Value | Enabled | Entity | Comment | Tag |
|---------|-----------|----------|-----------------|-------|---------|--------|---------|-----|
| 1 ✓     | pin...me3 | Location | PIN_G19         | Yes   |         |        |         |     |
| 2 ✓     | input_1   | Location | PIN_AB28        | Yes   |         |        |         |     |
| 3 ✓     | input_2   | Location | PIN_AC28        | Yes   |         |        |         |     |
| 4       | <<new>>   | <<new>>  | <<new>>         |       |         |        |         |     |

Check the manual (Section 4.3)

Include in your report your pin assignments

Table 4-1 Pin Assignments for Slide Switches

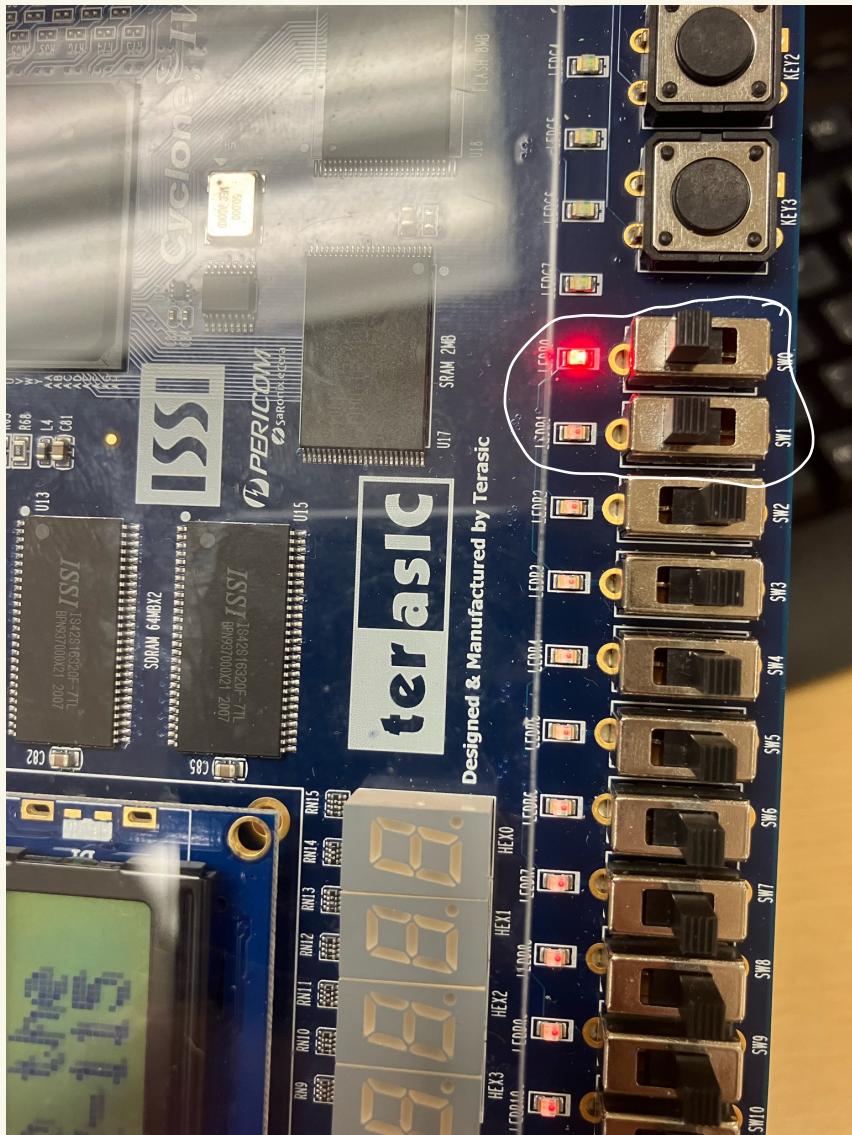
| <i>Signal Name</i> | <i>FPGA Pin No.</i> | <i>Description</i> | <i>I/O Standard</i> |
|--------------------|---------------------|--------------------|---------------------|
| SW[0]              | PIN_AB28            | Slide Switch[0]    | Depending on JP7    |
| SW[1]              | PIN_AC28            | Slide Switch[1]    | Depending on JP7    |
| SW[2]              | PIN_AC27            | Slide Switch[2]    | Depending on JP7    |
| SW[3]              | PIN_AD27            | Slide Switch[3]    | Depending on JP7    |
| SW[4]              | PIN_AB27            | Slide Switch[4]    | Depending on JP7    |
| SW[5]              | PIN_AC26            | Slide Switch[5]    | Depending on JP7    |
| SW[6]              | PIN_AD26            | Slide Switch[6]    | Depending on JP7    |
| SW[7]              | PIN_AB26            | Slide Switch[7]    | Depending on JP7    |
| SW[8]              | PIN_AC25            | Slide Switch[8]    | Depending on JP7    |
| SW[9]              | PIN_AB25            | Slide Switch[9]    | Depending on JP7    |
| SW[10]             | PIN_AC24            | Slide Switch[10]   | Depending on JP7    |
| SW[11]             | PIN_AB24            | Slide Switch[11]   | Depending on JP7    |
| SW[12]             | PIN_AB23            | Slide Switch[12]   | Depending on JP7    |
| SW[13]             | PIN_AA24            | Slide Switch[13]   | Depending on JP7    |
| SW[14]             | PIN_AA23            | Slide Switch[14]   | Depending on JP7    |
| SW[15]             | PIN_AA22            | Slide Switch[15]   | Depending on JP7    |
| SW[16]             | PIN_Y24             | Slide Switch[16]   | Depending on JP7    |
| SW[17]             | PIN_Y23             | Slide Switch[17]   | Depending on JP7    |

Table 4-2 Pin Assignments for Push-buttons

| <i>Signal Name</i> | <i>FPGA Pin No.</i> | <i>Description</i> | <i>I/O Standard</i> |
|--------------------|---------------------|--------------------|---------------------|
| KEY[0]             | PIN_M23             | Push-button[0]     | Depending on JP7    |
| KEY[1]             | PIN_M21             | Push-button[1]     | Depending on JP7    |
| KEY[2]             | PIN_N21             | Push-button[2]     | Depending on JP7    |
| KEY[3]             | PIN_R24             | Push-button[3]     | Depending on JP7    |

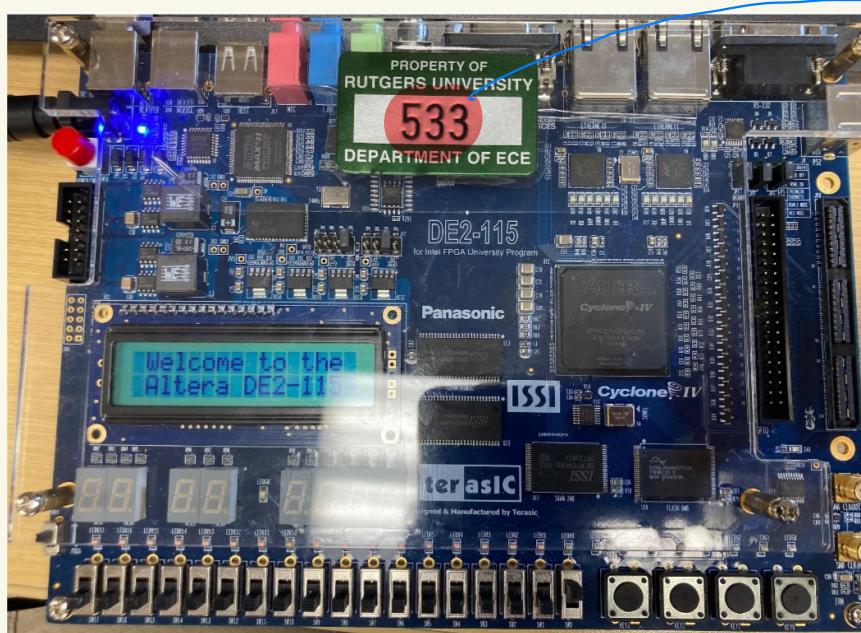
Table 4-3 Pin Assignments for LEDs

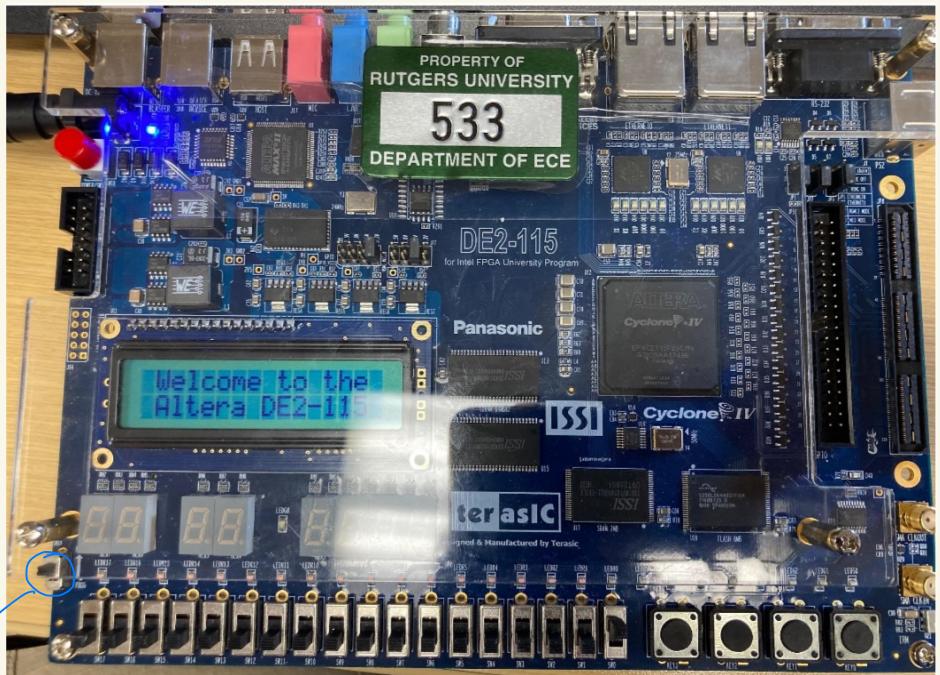
| <i>Signal Name</i> | <i>FPGA Pin No.</i> | <i>Description</i> | <i>I/O Standard</i> |
|--------------------|---------------------|--------------------|---------------------|
| LEDR[0]            | PIN_G19             | LED Red[0]         | 2.5V                |
| LEDR[1]            | PIN_F19             | LED Red[1]         | 2.5V                |
| LEDR[2]            | PIN_E19             | LED Red[2]         | 2.5V                |
| LEDR[3]            | PIN_F21             | LED Red[3]         | 2.5V                |
| LEDR[4]            | PIN_F18             | LED Red[4]         | 2.5V                |
| LEDR[5]            | PIN_E18             | LED Red[5]         | 2.5V                |
| LEDR[6]            | PIN_J19             | LED Red[6]         | 2.5V                |
| LEDR[7] scope      | PIN_H10             | LED Red[7]         | 2.5V                |



## NOTES:

- If you are unable to log in ECE computers --> [ecs.rutgers.edu](http://ecs.rutgers.edu)
  - > Computer Lab Use --> Reset Password
- Check the FPGA board assignment on Canvas:  
Files > Board assignment 2025. **Stick to your board!**
- If you need to change board, check with your TA. Put the board back to locker **at the end of lab session**
- Outside lab hours, freely use 5 boards in wooden boxes





RUN  
PROD