SPECTRUM DIGITAL INCORPORATED

DM816x/C6A816x/AM389x Evaluation Module

Technical Reference

Preliminary

2011 ***DSP Development Systems***

DM816x/C6A816x/AM389x
Evaluation Module
Technical Reference

512875-0001 Rev. A
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Contents

About This Manual

This document describes the board level operations of the DM816x/C6A816x/AM389x Evaluation Module (EVM). The EVM is based on the Texas Instruments DM816x/C6A816x/AM389x Processor.

The DM816x/C6A816x/AM389x Evaluation Module is a table top card that allows engineers and software developers to evaluate certain characteristics of the DM816x/C6A816x/AM389x processor to determine if the processor meets the designers application requirements. Evaluators can create software to execute on board or expand the system in a variety of ways.

Notational Conventions

This document uses the following conventions.

The DM816x/C6A816x/AM389x Evaluation Module will sometimes be referred to as the DM816x/C6A816x/AM389x EVM or EVM.

Program listings, program examples, and interactive displays are shown in a special italic typeface. Here is a sample program listing.

equations
!rd = !strobe&rw;

Information About Cautions

This book may contain cautions.
This is an example of a caution statement.
A caution statement describes a situation that could potentially damage your software, or hardware, or other equipment. The information in a caution is provided for your protection. Please read each caution carefully.

Related Documents, Application Notes and User Guides

Information regarding the DM816x/C6A816x/AM389x can be found at the following Texas Instruments website:

http://www.ti.com

Table 1: Manual History

Revision	History
A	Initial Release

Chapter 1

Introduction to the DM816x/C6A816x/AM389x EVM

Chapter One provides a description of the DM816x/C6A816x/AM389x EVM along with the key features and a block diagram of the circuit board.

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1.1 Key Features

The DM816x/C6A816x/AM389x EVM is a standalone development platform that enables users to evaluate and develop applications for the DM816x/C6A816x/AM389x processor. Schematics and application notes are available to ease hardware development and reduce time to market. The block diagram for this EVM is shown below.

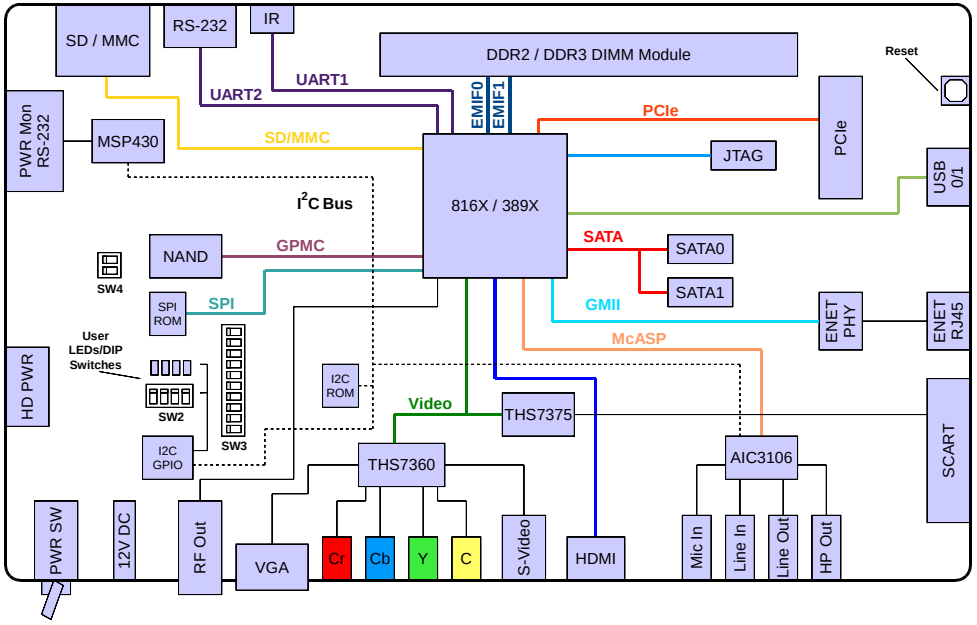

Figure 1-1, Block Diagram DM816x/C6A816x/AM389x EVM

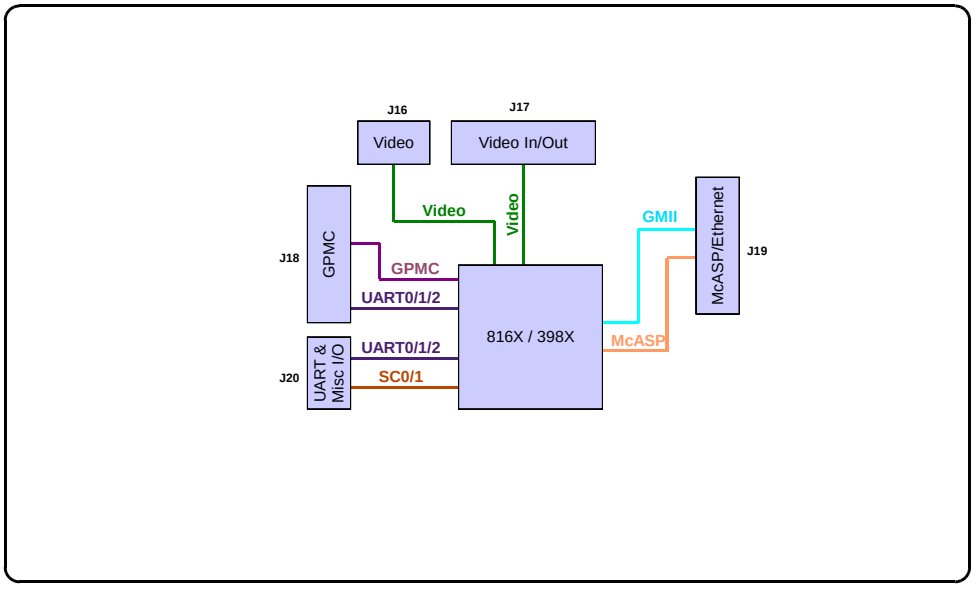

Figure 1-2, Block Diagram DM816x/C6A816x/AM389x EVM Expansion Connectors

The EVM comes with a full complement of on board devices that suit a wide variety of application environments. Key features include:

- A Texas Instruments DM816x/C6A816x/AM389x device with a C674x DSP floating point processor and an ARM Cortex A8 processor operating up to 1 GHz.
- 2 Gigabyte DDR3 RAM soldered to the EVM
- 32 Megabit SPI Flash
- 2 gigabyte NAND Flash
- Composite video out
- Component video out
- Dual Host USB Interfaces
- Video/GPMC/MCASP/Serial Expansion Interfaces
- On-chip HDMI Interface
- 10/100/1000 Ethernet Interface
- SD media card interface
- TLV320AIC3106 Stereo Codec (Line In/Out, Mic in, Headphone out)
- 2 SATA drive interfaces
- PCIe connector with 2 lanes
- RS-232 Interface
- Infra-red receiver
- On chip real time clock
- Configurable boot load options
- 4 user LEDs/4 position user DIP switch
- Single voltage power supply (+12V)
- 20 Pin CTI JTAG Interface
- On board power monitoring

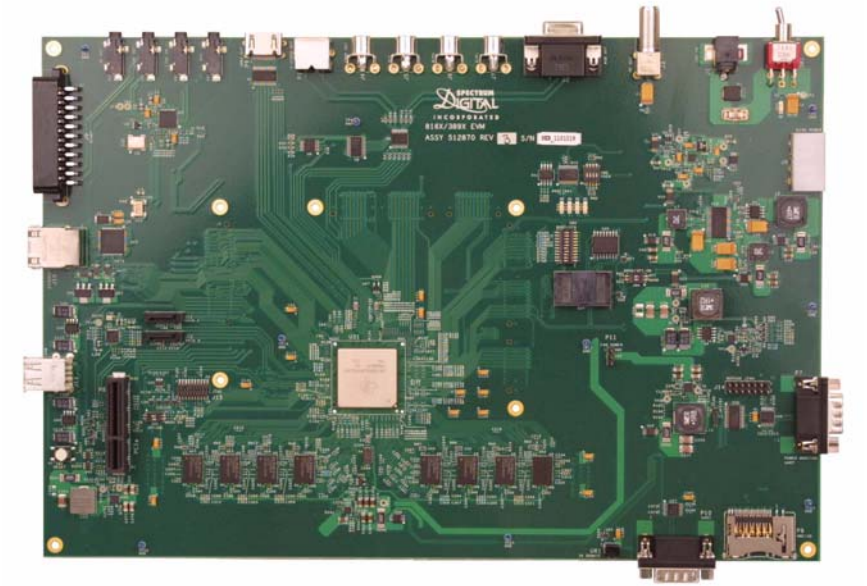

Figure 1-3, DM816x/C6A816x/AM389x EVM

1.2 Functional Overview of the DM816x/C6A816x/AM389x EVM

The DM816x/C6A816x/AM389x on the EVM interfaces to on-board peripherals through multiple on-chip interfaces. The DDR3 memory is soldered down onto the EVM. HDMI and video interfaces support up to 1080p resolution, along with gigabit ethernet and RS-232 interfaces which provide direct support for operating systems running on the EVM.

An on-board AIC3106 codec allows the DSP to transmit and receive analog audio signals. The I^2C bus is used for the codec control interface, while the McASP controls the audio stream. Signal interfacing is done through 3.5mm audio jacks that correspond to microphone input, headphone output, line input, and line output.

The EVM includes 4 user LEDs, a 4 position user DIP switch, and on chip real time clock. On board connectors allows ease of interfacing to the daughter cards.

An included +12V external power supply is used to power the board. On-board switching voltage regulators provide the CPU core voltage, +3.3V, +1.8V for peripheral interfacing. The board is held in reset by the on board power controller until these supplies are within operating specifications.

Code Composer Studio communicates with the EVM through an 20 pin compact TI JTAG header.

1.3 Basic Operation

The EVM is designed to work with TI's Code Composer Studio IDE™, or Ubuntu/Code Sorcery tool environments. Code Composer communicates with the board through an on board JTAG emulator. This EVM is shipped with an EVM specific Code Composer Studio environment.

1.4 Memory Map

The DM816x/C6A816x/AM389x processor has a byte addressable address space. Program code and data can be placed anywhere in the unified address space. Addresses are multiple sizes depending on hardware implementation. Refer to the appropriate device data sheets for more details.

The part incorporates a triple EMIF interface. Two dedicated 32-bit wide DDR2 interface directly to the on board dual DIMM. GPMC (General Purpose Memory Controller) has multiple separate addressable regions called chip enable spaces. The EVM uses this interface as a peripheral interface to daughter card connectors and NAND Flash interfaces. The memory maps for both of the processors in the DM816x/C6A816x/AM389x device can be found in TI document SPRS680. The address ranges for the off chip DDR2 and NAND memory are shown in the table below.

Table 1: DDR2 and NAND Memory Ranges

Interface	Memory Type	Address Range	Size
DDR0	DDR2	0x8000 0000	0x2000 0000
DDR1	DDR2	0xC000 0000	0x2000 0000
GPMC	NAND	GPMC_CS0, see NAND controller information	2 Gigabyte

1.5 Boot Switch Settings

The EVM uses 9 positions of a 10 position DIP switch (SW3) to configure the operational state of the processor when it is released from reset and determine the source for processor booting. Five (5) positions indicate the boot mode and four (4) positions determine the memory configuration. By default as shipped the switches are configured to SD Card boot. The tables below shows the boot mode sources and their respective switch positions.

Table 2: Memory Boot Load Order

BTMODE[4] (Position5)= 1 MEMORY BOOTING PREFERRED				BTMODE[3:0] Switch Position[4:1]
First	**Second**	**Third**	**Fourth**	
XIP	UART	EMAC	SD	0 0 0 0
XIPWAIT	UART	EMAC	SD	0 0 0 1
NAND	NANDI2C	SPI	UART	0 0 1 0
NAND	NANDI2C	SD	UART	0 0 1 1
NAND	NANDI2C	SPI	EMAC	0 1 0 0
NANDI2C	SD	EMAC	UART	0 1 0 1
SPI	SD	UART	EMAC	0 1 1 0
SD	SPI	UART	EMAC	0 1 1 1
SPI	SD	PCIE_32	Reserved	1 0 0 0
SPI	SD	PCIE_32	Reserved	1 0 0 1
Reserved	Reserved	Reserved	Reserved	1 0 1 0
Reserved	Reserved	Reserved	Reserved	1 0 1 1
Reserved	Reserved	Reserved	Reserved	1 1 0 0
Reserved	Reserved	Reserved	Reserved	1 1 0 1
Reserved	Reserved	Reserved	Reserved	1 1 1 0
GP Fast External Boot	EMAC	UART	PCIE_32	1 1 1 1

Table 3: Peripheral Boot Load Order

BTMODE[4] (Position5)= 0 PERIPHERAL BOOTING PREFERRED				BTMODE[3:0] Switch Position[4:1]
First	**Second**	**Third**	**Fourth**	
Reserved	Reserved	Reserved	Reserved	0 0 0 0
UART	XIPWAIT	SD	SPI	0 0 0 1
UART	SPI	NAND	NANDI2C	0 0 1 0
UART	SPI	XIP	SD	0 0 1 1
EMAC	SPI	NAND	NANDI2C	0 1 0 0
Reserved	Reserved	Reserved	Reserved	0 1 0 1
Reserved	Reserved	Reserved	Reserved	0 1 1 0
EMAC	SD	SPI	XIP	0 1 1 1
PCIE_32	Reserved	Reserved	Reserved	1 0 0 0
PCIE_64	Reserved	Reserved	Reserved	1 0 0 1
Reserved	Reserved	Reserved	Reserved	1 0 1 0
Reserved	Reserved	Reserved	Reserved	1 0 1 1
Reserved	Reserved	Reserved	Reserved	1 1 0 0
Reserved	Reserved	Reserved	Reserved	1 1 0 1
Reserved	Reserved	Reserved	Reserved	1 1 1 0
GP Fast External Boot	UART	EMAC	PCIE_64	1 1 1 1

The photo below shows the switch settings for SD card boot.

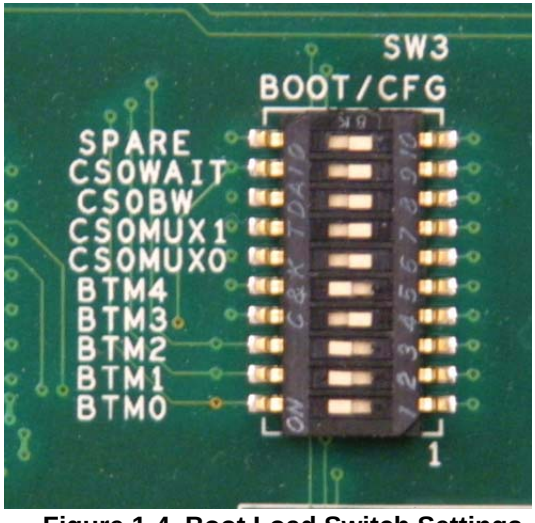

Figure 1-4, Boot Load Switch Settings

An additional switch (SW4) enables the chip select for on board NAND and SPI Flash. This switch allows for daughter cards to override on board configurations. This switch must disable the on board NAND and SPI when SD card boot is selected. The photo below shows the default switch settings for SW4.

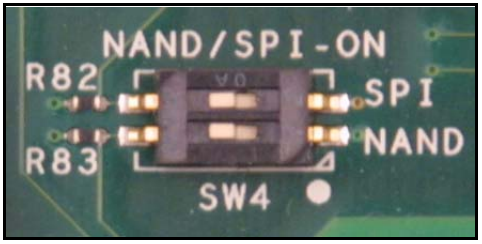

Figure 1-5, SW4, NAND/SPI Select Switch Settings

1.6 Power Supply

The EVM operates from a single +12V external power supply connected to the main power input (J1), a 2.5 MM. barrel-type plug. On the EVM, the +12V input is converted into core voltage (1 volt constant and 1 volt variable [AVS]), +1.5V, +1.8V, +3.3V and +5V using Texas Instruments controllers and regulators. The +3.3V supply is used for the CPU's I/O buffers.

Chapter 2

Board Components

This chapter describes the operation of the major board components on the DM816x/C6A816x/AM389x EVM.

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2.1 GPMC Interface

A separate 16 bit EMIF with multiple chip enables divide up the internal address space and allow for asynchronous memory accesses on the EVM. The EVM uses this interface for memory interfaces to the daughter card and on board NAND Flash.

2.1.1 DDR Memory Interfaces

The DM816x/C6A816x/AM389x device incorporates a dedicated 32 bit wide DDR3 memory interface. The EVM incorporates supports 2 gigabytes of memory for program, data, and video storage. The internal memory controller uses a PLL to control the memory timing. Memory refresh is handled automatically by the processor's internal controller.

2.1.2 Memory Card Interface

The EVM supports SD/MMC media card interfaces. This interface is directly supported via an on chip peripheral.

2.1.3 UART Interface

The internal UART2 on the DM816x/C6A816x/AM389x device is driven to connector P10. The UART's interface is routed to the RS-232 line drivers prior to being brought out to a DB-9 connector.

2.1.4 USB Interface

The DM816x/C6A816x/AM389x incorporates two on chip USB controllers. The two interfaces are brought out to dual host A type connector, J13.

2.1.5 HDMI Interface

The DM816x/C6A816x/AM389x has an on chip HDMI peripheral which supports up to 1080p @ 60 Hz. resolution. This interface is a direct interface to an HDMI connector, P6.

2.1.6 Video DAC

The EVM supports composite, S-video, Scart, and component output via internal video DACs. The interfaces are buffered via THS7360 and THS7375 video DACs to connectors J2, J9, J4, J5, J6, and J7.

2.1.7 PCIe

The EVM provides a PCIe connector and supports 2 lanes of transmit and receive interfaces.

2.2 AIC3106 Interface

The EVM incorporates a Texas Instruments TLV320AIC3106 stereo codec for input and output of audio signals. The codec samples analog signals on the microphone or line inputs and converts them into digital data so it can be processed by the DSP. When the DSP is finished with the data it uses the codec to convert the samples back into analog signals on the line output so the user can hear the output.

The codec communicates using two serial channels, one to control the codec's internal configuration registers and one to send and receive digital audio samples. The I^2C bus is used as the AIC3106's control channel. The control channel is generally only used when configuring the codec, it is typically idle when audio data is being transmitted,

McASP1 is used as the bi-directional data channel. All audio data flows through the data channel. Many data formats are supported based on the three variables of sample width, clock signal source and serial data format. The EVM examples generally use a 16-bit sample width with the codec in master mode so it generates the frame sync and bit clocks at the correct sample rate without effort on the DSP side.

The codec is clocked via a 24.576 Mhz oscillator. The internal sample rate generator subdivides the default system clock to generate common audio frequencies. The sample rate is set by a codec register. The figure below shows the codec interface on the DM816x/C6A816x/AM389x EVM.

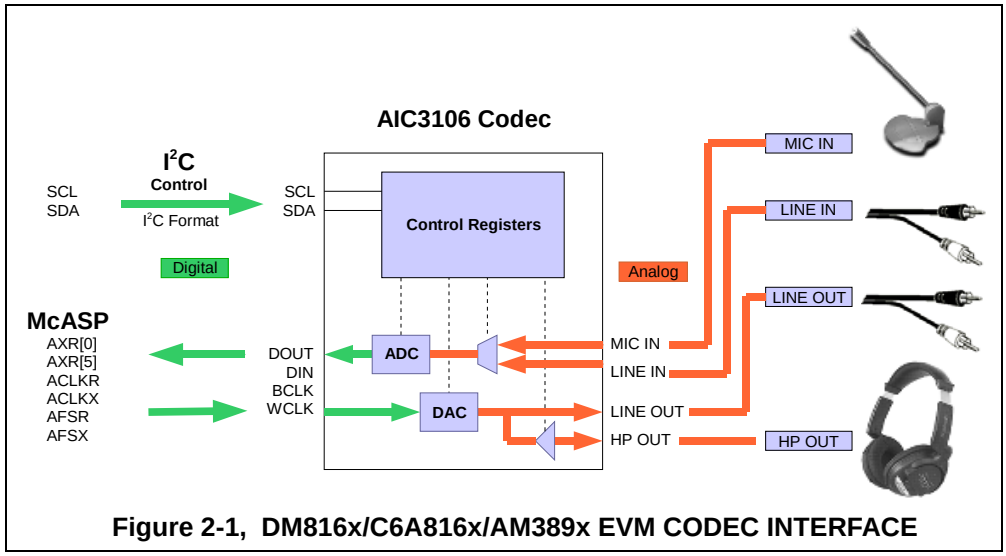

Figure 2-1, DM816x/C6A816x/AM389x EVM CODEC INTERFACE

2.3 Ethernet Interface

The DM816x/C6A816x/AM389x incorporates two ethernet MAC's that support 10/100/1000 Mbit interfaces. Ethernet 0 is interfaced to an external Phy and brought out to an RJ-45 standard ethernet connector, J10. The ethernet address is stored on chip within the CPU.

The RJ-45 jack has 2 LEDs integrated into the connector. The LEDs are green and yellow and provide link and transmit status from the ethernet controller.

2.4 I^2C0, I^2C1 Interfaces

The I^2C0 and I^2C1 bus on the DM816x/C6A816x/AM389x is ideal for interfacing to the control registers of many devices. On the DM816x/C6A816x/AM389x EVM the I^2C0 bus is used to configure the Codec, I^2C ROM, and bit addressable latch. The format of the bus is shown in the figure below.

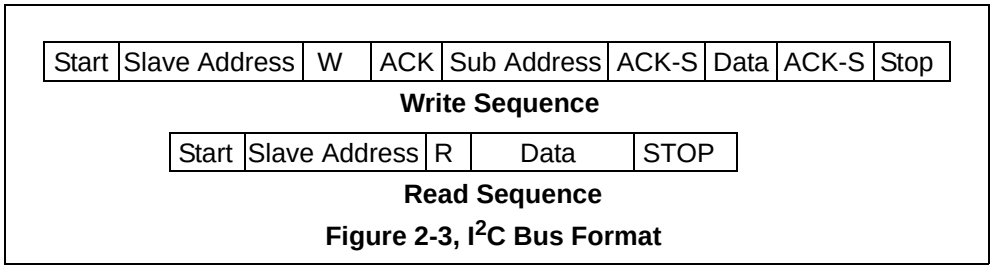

Figure 2-3, I^2C Bus Format

The addresses of the on board peripherals are shown in the tables below.

Table 1: I^2C0 Address Map

Device	Address	R/W	Function
TLV320AIC3106	0x18	R/W	CODEC
PCF8575	0x20	R/W	Bit I/O
MSP430	0x25	R/W	Power Monitor
I^2C EEPROM	0x50	R/W	I^2C EEPROM

Table 2: I^2C1 Address Map

Device	Address	R/W	Function
PCF8575	0x20	R/W	Bit I/O

2.5 SPI Flash

The EVM has a 32 megabit SPI Flash that can be used for booting and/or storage. Note that the switch S2 enables the SPI chip select and must be set properly when using the device.

2.6 Power Monitoring

The EVM uses an MSP430 CPU connected to multiple INA2201DCN I^2C power monitors to monitor the voltage and currents on the EVM. The MSP430 outputs this information in real time via its dedicated RS-232 port, P7.

2.7 Daughter Card Interfaces

The EVM provides expansion connectors that can be used to accept plug-in daughter cards. The daughter card allows users to build on their EVM platform to extend its capabilities and provide customer and application specific I/O. The expansion connectors are interfaces which include McASP, and serial I/O expansion. The EMIF-A signals are brought out as LCD, peripheral, or EMIF signals.

The daughter card connectors used on the EVM are shown in the table below.

Table 3: Daughter Card Connectors

Reference Designator	Part Numbers Used On EVM	Manufacturer
J16	QSH-030-01-L-D-A-K	Samtec
J17	QSH-060-01-L-D-A-K	Samtec
J18	QSH-060-01-L-D-A-K	Samtec
J19	QSH-060-01-L-D-A-K	Samtec
J20	QSH-030-01-L-D-A-K	Samtec

One of the compatible mating daughter card connectors used to interface to the EVM are shown in the table below (other heights are available).

Table 4: Mating Daughter Card Connectors

Reference Designator	Mating connector	Manufacturer
XJ16	QTH-030-02-L-D-A-K	Samtec
XJ17	QTH-060-02-L-D-A-K	Samtec
XJ18	QTH-060-02-L-D-A-K	Samtec
XJ19	QTH-060-02-L-D-A-K	Samtec
XJ20	QTH-030-02-L-D-A-K	Samtec

Chapter 3

Physical Description

This chapter describes the layout of the DM816x/C6A816x/AM389x EVM and its interfaces.

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3.1 Board Layout

The DM816x/C6A816x/AM389x EVM is a 12.5 x 8.4 inch six (6) layer printed circuit board which is powered by an external +5 volt only power supply. Figure 3-1 shows the layout of the top side of the DM816x/C6A816x/AM389x EVM.

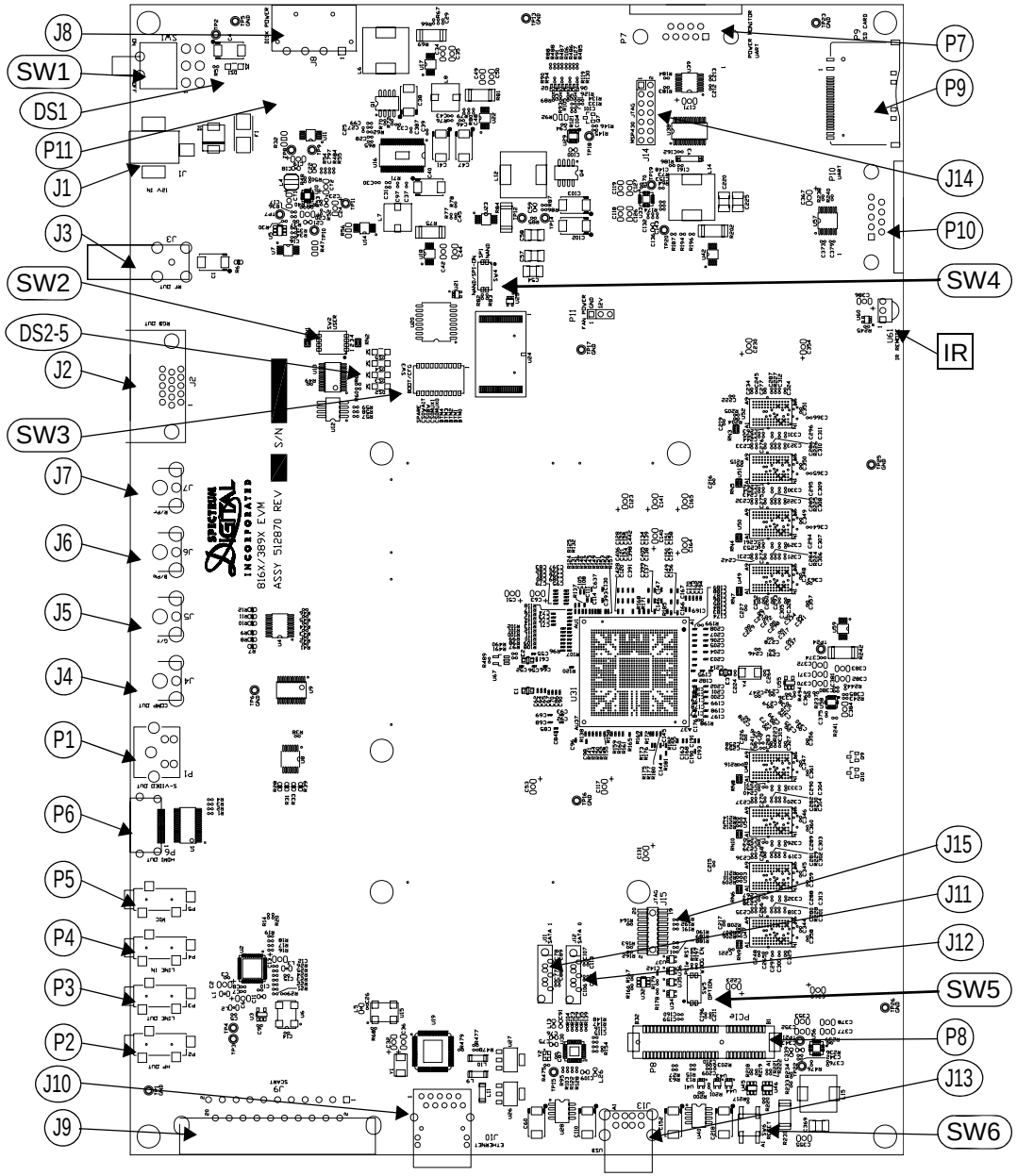


Figure 3-1, DM816x/C6A816x/AM389x EVM, Interfaces Top Side

Figure 3-2 shows the layout of the bottom side of the DM816x/C6A816x/AM389x EVM.

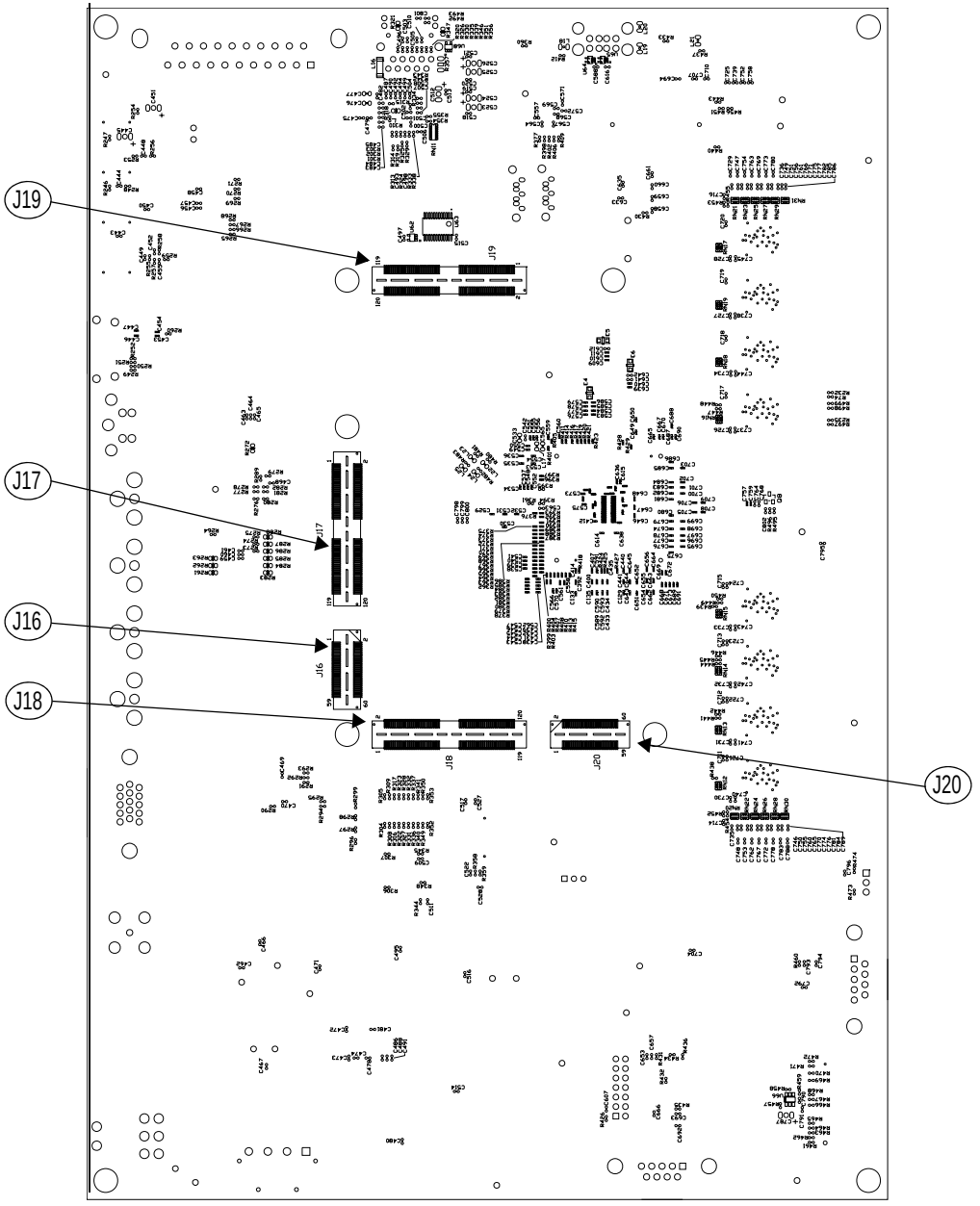


Figure 3-2, DM816x/C6A816x/AM389x EVM, Interfaces Bottom Side

3.2 Connectors

The EVM has numerous connectors and option jumpers to control and provide connections to various peripherals. These connectors and jumpers are described in the following sections.

Table 1: Connectors

Connector	Size	Board Side	Schematic Page	Function
J1	2	Top	56	12V Power In
J2	15	Top	42	HD15 Connector
J3	2	Top	42	F Type Video Connector
J4	2	Top	42	Composite Video
J5	2	Top	42	RCA Jack - Green
J6	2	Top	42	RCA Jack - Blue
J7	2	Top	42	RCA Jack - Red
J8	9	Top	56	Drive Input Power Connector
J9	21	Top	43	SCART21 Connector
J10	14	Top	40	Ethernet Output Connector
J11	9	Top	12	SATA Header
J12	9	Top	12	SATA Header
J13-1	6	Top	30	USB-A Connector
J13-2	6	Top	30	USB-A Connector
J14	2 x 7	Top	50	MSP430 Programming Header
J15	20	Top	14	CTI JTAG Interface
J16	2 x 32	Bottom	45	VLYNQ/Transport Connector
J17	2 x 64	Bottom	44	Video/Transport Connector
J18	2 x 64	Bottom	46	GPMC Expansion Connector
J19	2 x 64	Bottom	48	MCASP/XXX Expansion
J20	2 x 32	Bottom	47	Serial I/O Expansion Connector
P1	7	Top	42	S-video Connector
P2	4	Top	41	Headphone Out
P3	4	Top	41	Line Out
P4	4	Top	41	Line In
P5	4	Top	41	Mic In
P6	23	Top	11	HDMI
P7	11	Top	50	DB9 Connector
P8	2 x 32	Top	28	PCIe Interface
P9	28	Top	35	SD/MMC Connector
P10	11	Top	33	DB9 Connector
P11	3	Top	56	Fan Connector

3.2.1 J1, 12V Power In

Connector J1 is the input power connector. This connector brings in +12 volts to the EVM. This is a 2.5mm. jack. The inside of the jack is tied to through a fuse to EVM_12V. The other side is tied to ground and LED DS1. The figure below shows this connector as viewed from the card edge.

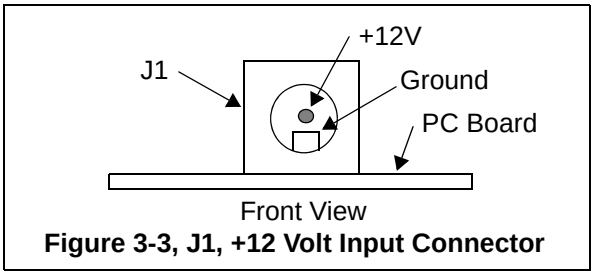


Figure 3-3, J1, +12 Volt Input Connector

3.2.2 J2, HD15 Connector

Connector J2 is a 15 pin header that allows a high definition video device to be plugged into the EVM. The signals on this connector are shown in the table below.

Table 2: J2, HD15 Connector

Pins	Signal
1	U4, Pin 12, SF3_OUT
2	U4, Pin 14, SF1_OUT
3	U4, Pin 13, SF2_OUT
4	NC
5	Ground
6	Ground
7	Ground
8	Ground
9	NC
10	Ground
11	NC
12	NC
13	NC
14	NC
15	NC

3.2.3 J3, F Type Video Connector

Connector J3 provides an RF output (RFOUT) from the processor, U31, Pin AU21.

3.2.4 J4, Composite Video Out

J4 is an RCA jack used as a video output from the THS7360 driver. Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

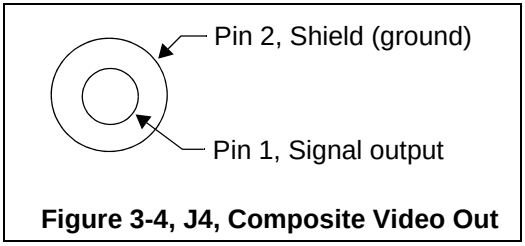


Figure 3-4, J4, Composite Video Out

Table 3: J4, Composite Video Out, RCA Jack

Pin #	Signal Name
1	THS7360, Pin 20, SD1_OUT
2	GND

3.2.5 J5, Component Video, RCA Jack - Green

J5 is an RCA jack used to provide the Green component video output from the THS7360 driver, U4, pin 14, SF1_OUT. The pinout on this connector is shown in the figure below.

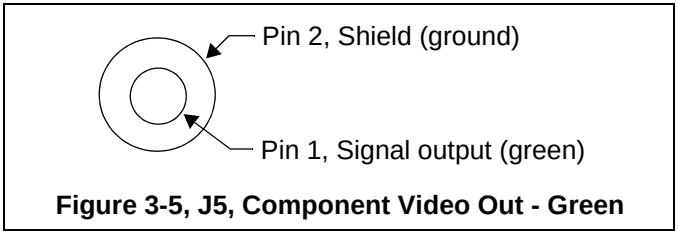


Figure 3-5, J5, Component Video Out - Green

WARNING: Do **NOT** plug into this connector with the power on.

3.2.6 J6, Component Video, RCA Jack - Blue

J6 is an RCA jack used to provide the Blue component video output from the THS7360 driver, U4, pin 13, SF2_OUT. The pinout on this connector is shown in the figure below.

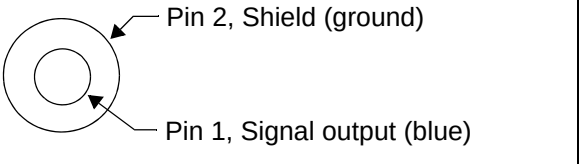


Figure 3-6, J6, Component Video Out - Blue

WARNING: Do **NOT** plug into this connector with the power on.

3.2.7 J7, Component Video, RCA Jack - Red

J7 is an RCA jack used to provide the Red component video output from the THS7360 driver, U4, pin 12, SF3_OUT. The pinout on this connector is shown in the figure below.

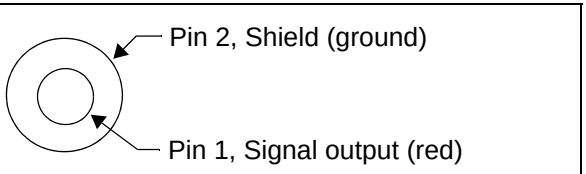


Figure 3-7, J7, Component Video Out - Red

WARNING: Do **NOT** plug into this connector with the power on.

3.2.8 J8, Disk Drive Power Connector

Connector J8 provides power for a hard disk drive. This is the standard connector used on a personal computer. The signals on this connector are shown in the table below.

Table 4: J8, Disk Driver Power Connector

Pin #	Signal Name
1	EVM_12V, +12 volts
2,3	Ground
4	EVM_5V0, +5 volts
6,7,8,9	No connect

3.2.9 J9, SCART21 Connector

Connector J9 is a SCART21 video output connector. The signals on this connector are shown in the table below.

Table 5: J9, SCART21 Connector

Pin #	Signal Name	Pin #	Signal Name
1	SCART_AUDIO_OUT_R		
		2	No connect
3	SCART_AUDIO_OUT_L		
		4	Ground
5	Ground		
		6	No connect
7	U8, Pin 13, CH2_OUT		
		8	No connect
9	Ground		
		10	No connect
11	U8, Pin 14, CH1_OUT		
		12	No connect
13	Ground		
		14	Ground
15	U8, Pin 12, CH3_OUT		
		16	U8, Pin 11, CH4_OUT
17	Ground		
		18	No connect
19	SCART_COMPOSITE		
		20	No connect
21	Ground		

3.2.10 J10, Ethernet Connector

Connector J10 is an Ethernet connector that uses differential signals. The signals on this connector are shown below.

Table 6: J10, Ethernet Connector

Pins	Signal
1	Ground
2	PHY_VDD_2V5
3	TRD[3]P
4	TRD[3]N
5	TRD[2]P
6	TRD[2]N
7	TRD[1]P
8	TRD[1]N
9	TRD[0]P
10	TRD[0]N
11	Earth Ground
12	Earth Ground
D1	ENET_LED_LINK
D2	Ground
D3	ENET_LED_RX
D4	EVM_3V3

3.2.11 J11, SATA Header

J11 is a 9 pin SATA disk interface header. There are 2 pair of differential signals to interface to the processor, U31. This signals on this connector are shown below.

Table 7: J11, SATA Header

Pins	Signal
1	Ground
2	CON.SATA_TXP1, U31, Pin V33
3	CON.SATA_TXN1, U31, Pin U33
4	Ground
5	CON.SATA_RXN1, U31, Pin V35
6	CON.SATA_RXP1, U31, Pin W35
7	Ground
8	No connect
9	No connect

3.2.12 J12, SATA Header

J12 is a 9 pin SATA disk interface header. There are 2 pair of differential signals to interface to the processor, U31. This signals on this connector are shown below.

Table 8: J12, SATA Header

Pins	Signal
1	Ground
2	CON.SATA_TXP0, U31, Pin T32
3	CON.SATA_TXN0, U31, Pin T31
4	Ground
5	CON.SATA_RXN0, U31, Pin V37
6	CON.SATA_RXP0, U31, Pin V36
7	Ground
8	No connect
9	No connect

3.2.13 J13-1/13-2, USB-A Connectors

Connector J13-1, J13-2 are stacked USB connectors. The J13-1 connector is the lower connector in the stacked pair. The signals on each of these connectors are shown in the tables below.

Table 9: J13-1, USB-A Connector

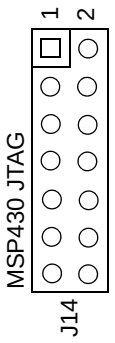
Pin Name	Signal
MHX1/MH1	SHIELD USB0
VBUS/A1	USB0_VBUS_CONN
D-/A2	USB0_DM
D+/A3	USB0_DP
GND/A4	Ground
MH2	SHIELD USB0

Table 10: J13-2, USB-A Connector

Pin Name	Signal
MHX1/MH3	SHIELD USB1
VBUS/B1	USB1_VBUS_CONN
D-/B2	USB1_DM
D+/B3	USB1_DP
GND/B4	Ground
MHX2/MH4	SHIELD USB1

3.2.14 J14, MSP430 Programming Header

J14 is a 2 x 7 double row header used to program the MSP430 microcontroller, U38. This header is only to be used at the factory. The layout of this header is shown in the figure below.



Header Dimensions
Pin-to-Pin spacing, 0.100 in. (X,Y)
Pin width, 0.025-in. square post
Pin length, 0.235-in. nominal

Figure 3-8, J14, MSP430 Programming Header

The signals on the pins of this connector are shown bin the table below.

Table 11: J14, MSP430 Programming Header

Pin #	Signal	Pin #	Signal
1	430_TDO/TDI	2	No connect
3	No connect	4	EVM_3V3
5	No connect	6	No connect
7	MSP430_TCK	8	No connect
9	Ground	10	No connect
11	No connect	12	No connect
13	No connect	14	No connect

3.2.15 J15, CTI JTAG Interface

Connector J15 is a compact 20 pin TI JTAG header. The signals on the pins of this connector are shown in the table below.

Table 12: J15, CTI JTAG Interface

Pin #	Signal	Pin #	Signal
1	TMS	2	TRSTn
3	TDI	4	Ground
5	EVM_3V3	6	No connect (key)
7	TDO	8	Ground
9	RTCK	10	Ground
11	TCK	12	Ground
13	EMU0	14	EMU1
15	EMU_RSTn	16	Ground
17	EMU2	18	EMU3
19	EMU4	20	Ground

3.2.16 J16, VLYNQ/Transport Connector

Connector J16 is the VLYNQ/Transport interface located on the bottom side of the board. The signals on this connector are shown in the table below.

Table 13: J16, VLYNQ/Transport Connector

Pin	Signal	Pin	Signal
2	TSI3_PACVAL	1	TSI6_PACERR
4	Ground	3	Ground
6	TSI4_DCLK	5	TSI2_PACERR
8	TSI3_DATA	7	TSI0_PACVAL
10	Ground	9	Ground
12	TSI2_DCLK	11	TSI2_PACVAL
14	TSI2_DATA	13	TSI0_PACERR
16	Ground	15	Ground
18	TSI6_BYTSTRT	17	TSI0_DCLK
20	TSI6_PACVAL	19	TSO0_DCLK
22	Ground	21	Ground
24	TSI4_PACERR	23	TSI0_BYTSTRT
26	TSI4_BYTSTRT	25	TSO0_DATA
28	Ground	27	Ground
30	TSI3_PACERR	29	TSO0_BYTSTRT
32	VLYNQ_RXD1	31	TSO0_PACERR
34	Ground	33	Ground
36	VLYNQ_TXD1	35	VLYNQ_SCRUN
38	TSO1_PACERR	37	TSO0_PACVAL
40	Ground	39	Ground
42	VLYNQ_TXD3	41	VLYNQ_TXD2
44	VLYNQ_RXD2	43	VLYNQ_CLOCK
46	Ground	45	Ground
48	TSI4_PACVAL	47	TSI1_PACERR
50	VLYNQ_RXD3	49	TSI3_DCLK
52	Ground	51	Ground
54	VLYNQ_TXD0	53	VLYNQ_RXD0
56	No connect	55	No connect
58	Ground	57	Ground
60	No connect	59	No connect
62	Ground	61	Ground
64	Ground	63	Ground

3.2.17 J17, Video/Transport Connector

Connector J17 is the Video/Transport interface located on the bottom side of the board. This connector is in two sections. The signals on each section of this connector are shown in the tables below.

Table 14: J17, Video/Transport Connector, Section 1

Pin	Signal	Pin	Signal
2	VIN0_D0	1	No connect
4	Ground	3	Ground
6	VIN0_D2	5	No connect
8	VIN0_D9	7	VIN0_CLK1
10	Ground	9	Ground
12	VOUT0_G_Y_YC2	11	VIN0_D1
14	VOUT0_G_Y_YC6	13	VIN0_D4
16	Ground	15	Ground
18	VOUT0_R_CR4	17	VIN0_D11
20	VIN0_D6	19	VIN0_D5
22	Ground	21	Ground
24	VIN0_D8	23	VIN0_D12
26	VIN0_D3	25	VIN0_D10
28	Ground	27	Ground
30	VIN0_D7	29	VIN0_D14
32	VOUT0_G_Y_YC4	31	VIN0_D13
34	Ground	33	Ground
36	VOUT0_B_CB_C8	35	VIN0_D15
38	VOUT0_G_Y_YC5	37	VOUT0_CLK
40	Ground	39	Ground
42	VOUT0_B_CB_C6	41	VOUT0_G_Y_YC8
44	VOUT0_B_CB_C5	43	VOUT0_G_Y_YC7
46	Ground	45	Ground
48	EVM_12V	47	EVM_3V3
50	EVM_12V	49	EVM_3V3
52	Ground	51	Ground
54	EVM_12V	53	EVM_5V0
56	EVM_12V	55	EVM_5V0
58	Ground	57	Ground
60	VOUT0_B_CB_C3	59	VOUT0_B_CB_C9

Table 15: J17, Video/Transport Connector, Section 2

Pin	Signal	Pin	Signal
62	VOUT0_B_CB_C7	61	VOUT0_R_CR2
64	Ground	63	Ground
66	VOUT0_G_Y_YC3	65	VOUT0_R_CR6
68	VOUT0_G_Y_YC9	67	VOUT0_R_CR5
70	Ground	69	Ground
72	VIN0_CLK0	71	VOUT0_R_CR9
74	VOUT0_B_CB_C4	73	TSI5_BYTSTRT
76	Ground	75	Ground
78	VOUT0_B_CB_C2	77	TSI5_PACERR
80	VOUT0_R_CR3	79	TSI7_PACERR
82	Ground	81	Ground
84	TSI5_DATA	83	TSO1_DATA
86	TSI5_PACVAL	85	TSI7_PACVAL
88	Ground	87	Ground
90	TSI1_PACVAL	89	TSO1_PACVAL
92	TSI7_DATA	91	TSO1_DCLK
94	Ground	93	Ground
96	TSI5_DCLK	95	TSI6_DATA
98	VOUT0_R_CR7	97	TSI3_BYTSTRT
100	Ground	99	Ground
102	VOUT0_R_CR8	101	TSI2_BYTSTRT
104	TSI7_BYTSTRT	103	TSI4_DATA
106	Ground	105	Ground
108	TSI1_BYTSTRT	107	TSI0_DATA
110	TSI7_DCLK	109	TSI6_DCLK
112	Ground	111	Ground
114	TSI1_DCLK	113	MSP430_SCL
116	TSI1_DATA	115	MSP430_SDA
118	Ground	117	Ground
120	TSO1_BYTSTRT	119	No connect
122	Ground	121	Ground
124	Ground	123	Ground
126	Ground	125	Ground
128	Ground	127	Ground

3.2.18 J18, GPMC Expansion Connector

Connector J18 is the GPMC expansion connector located on the bottom side of the board. This connector is in two sections. The signals on each section of this connector are shown in the tables below.

Table 16: J18, GPMC Expansion Connector, Section 1

Pin	Signal	Pin	Signal
2	MSP430_SCL	1	No connect
4	Ground	3	Ground
6	MSP430_SDA	5	GPMC_CS3
8	No connect	7	GPMC_CS0
10	Ground	9	Ground
12	No connect	11	GPMC_CS2
14	No connect	13	GPMC_CS1
16	Ground	15	Ground
18	GPMC_CS4	17	GPMC_WEN
20	GPMC_A8	19	GPMC_CS5
22	Ground	21	Ground
24	GPMC_A7	23	GPMC_OEN_REN
26	GPMC_A3	25	GPMC_BE1N
28	Ground	27	Ground
30	GPMC_A2	29	GPMC_A5
32	GPMC_A1	31	GPMC_A4
34	Ground	33	Ground
36	GPMC_A0	35	GPMC_A9
38	GPMC_DIR	37	GPMC_A10
40	Ground	39	Ground
42	GPMC_WAIT	41	GPMC_A11
44	GPMC_WPN	43	GPMC_D0
46	Ground	45	Ground
48	EVM_12V	47	EVM_3V3
50	EVM_12V	49	EVM_3V3
52	Ground	51	Ground
54	EVM_12V	53	EVM_5V0
56	EVM_12V	55	EVM_5V0
58	Ground	57	Ground
60	GPMC_A6	59	GPMC_D2

Table 17: J18, GPMC Expansion Connector, Section 2

Pin	Signal	Pin	Signal
62	GPMC_BE0N_CLE	61	GPMC_D5
64	Ground	63	Ground
66	GPMC_D4	65	GPMC_D7
68	GPMC_D3	67	GPMC_D9
70	Ground	69	Ground
72	GPMC_D1	71	GPMC_D12
74	GPMC_A27	73	GPMC_D11
76	Ground	75	Ground
78	GPMC_ADVN_ALE	77	GPMC_D10
80	GPMC_D6	79	GPMC_CLK
82	Ground	81	Ground
84	GPMC_D8	83	GPMC_D15
86	GPMC_D13	85	No connect
88	Ground	87	Ground
90	No connect	89	No connect
92	No connect	91	No connect
94	Ground	93	Ground
96	No connect	95	No connect
98	No connect	97	No connect
100	Ground	99	Ground
102	GPMC_D14	101	SPI_CS0
104	No connect	103	SPI_SCLK
106	Ground	105	Ground
108	SPI_MOSI	107	SPI_CS3
110	SOI_MISO	109	SPI_CS1
112	Ground	111	Ground
114	UART0_RXD	113	UART1_RXD
116	UART0_RTSN	115	UART1_TXD
118	Ground	117	Ground
120	UART0_TXD	119	UART2_RXD
122	Ground	121	Ground
124	Ground	123	Ground
126	Ground	125	Ground
128	Ground	127	Ground

3.2.19 J19, MCASP/XXX Expansion

Connector J19 is the MCASP/XXX expansion connector located on the bottom side of the board. This connector is in two sections. The signals on each section of this connector are shown in the tables below.

Table 18: J19, MCASP/XXX Expansion Connector, Section 1

Pin	Signal	Pin	Signal
2	IIC1_SDA	1	PM_I2C_SCL
4	Ground	3	Ground
6	IIC1_SCL	5	PM_I2C_SDA
8	IIC0_SDA	7	EXP_MCA2_AXR0
10	Ground	9	Ground
12	IIC0_SCL	11	EXP_MCA2_AMUTE
14	No connect	13	EXP_MCA2_AXR1
16	Ground	15	Ground
18	MCA0_AMUTE	17	EXP_MCA2_ACLKHX
20	MCA0_AXR3	19	EXP_MCA2_ACLKX
22	Ground	21	Ground
24	MCA0_AXR2	23	EXP_MCA2_AFSR
26	MCA1_AMUTE	25	EXP_MCA2_AFSX
28	Ground	27	Ground
30	MCA0_ACLKHX	29	EXP_MCA2_AHCLKR
32	MCA0_AFSR	31	EXP_MCA2_ACLKR
34	Ground	33	Ground
36	MCA0_ACLKX	35	MCA1_AXR1
38	MCA0_AFSX	37	MCA1_AXR0
40	Ground	39	Ground
42	MCA1_AFSX	41	MTSO_DATA1
44	MCA0_AXR1	43	MTSI_DATA5
46	Ground	45	Ground
48	EVM_12V	47	EVM_3V3
50	EVM_12V	49	EVM_3V3
52	Ground	51	Ground
54	EVM_12V	53	EVM_5V0
56	EVM_12V	55	EVM_5V0
58	Ground	57	Ground
60	MTSI_DATA7	59	MCA1_ACLKHX

Table 19: J19, MCASP/XXX Expansion Connector, Section 2

Pin	Signal	Pin	Signal
62	MCA0_AXR5	61	MDIO_MDIO
64	Ground	63	Ground
66	MCA0_AXR4	65	MDIO_MDCLK
68	MCA0_AXR0	67	MCA1_ACLKX
70	Ground	69	Ground
72	MCA1_ACLKR	71	MTSI_DCLK
74	MCA1_AHCLKR	73	MTSI_DATA0
76	Ground	75	Ground
78	MCA1_AFSR	77	MTSI_DATA2
80	MTSO_DATA0	79	MTSI_DATA1
82	Ground	81	Ground
84	MTSO_DATA6	83	MTSI_DATA4
86	MTCL_SDI	85	MTSI_DATA3
88	Ground	87	Ground
90	MTSO_DATA7	89	MTSI_DATA6
92	MCARD_MDET	91	MTSI_BYTSTRT
94	Ground	93	Ground
96	MTCL_SCTL	95	MTSO_DCLK
98	MCARD_CD2	97	MTSO_DATA2
100	Ground	99	Ground
102	MCARD_CD1	101	MTSO_DATA3
104	MCA0_ACLKR	103	MTSO_DATA5
106	Ground	105	Ground
108	MCA0_AHCLKR	107	MTSO_DATA4
110	MCARD_VS1	109	MCTL_SCLK
112	Ground	111	Ground
114	MTCL_SDO	113	MTSO_BYTSTRT
116	MCARD_VCCEN	115	MCARD_VPPEN
118	Ground	117	Ground
120	MCARD_VS2	119	MCARD_RESET
122	Ground	121	Ground
124	Ground	123	Ground
126	Ground	125	Ground
128	Ground	127	Ground

3.2.20 J20, Serial Expansion Connector

Connector J20 is the serial expansion connector located on the bottom side of the board. The signals on this connector are shown in the table below.

Table 20: J20, Serial Expansion Connector

Pin	Signal	Pin	Signal
2	UART0_CTSN	1	UART1_RTSN
4	Ground	3	Ground
6	UART0_DTRN	5	UART2_TXD
8	UART0_DCDN	7	SC0_RST
10	Ground	9	Ground
12	UART0_DSRN	11	SC1_RST
14	UART0_RIN	13	SC1_DET
16	Ground	15	Ground
18	SPI_SCS2	17	TIM6_OUT
20	UART1_CTSN	19	SC1_VPPEN
22	Ground	21	Ground
24	SC0_VPPEN	23	TIM7_OUT
26	SC0_VCCEN	25	SC1_VCCEN
28	Ground	27	Ground
30	SC1_CLK	29	CLK_OUT
32	SC0_C4	31	GP0_IO5
34	Ground	33	Ground
36	UART2_RTSN	35	TIM4_OUT
38	UART2_CTSN	37	No connect
40	Ground	39	Ground
42	SC0_DET	41	No connect
44	RSTOUTn	43	No connect
46	Ground	45	Ground
48	SC0_CLK	47	No connect
50	SC1_C4	49	GP0_IO7
52	Ground	51	Ground
54	SC0_DATA	53	GP0_IO4
56	SC1_DATA	55	EXP_WARM_RESET
58	Ground	57	Ground
60	GP0_IO6	59	TIM5_OUT
62	Ground	61	Ground
64	Ground	63	Ground

3.2.21 P1, S-Video Connector

Connector P1 is a four pin mini din S-video connector which interfaces to the THS7360. This connector brings out a video signal (LUMA). Do **NOT** plug into this connector with the power on. The figure below shows this connector as viewed from the card edge.

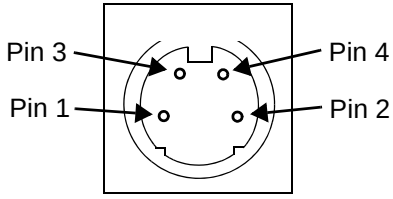


Figure 3-9, P1, Front View, Mini Din Connector

Table 21: P1, S-Video Connector

Pin #	Signal Name
1,2,5,6	Ground
3	S-VIDEO_LUMA, U4, Pin 19, SD2_OUT
4	U4, Pin 18, SD3_OUT
7	No connect

3.2.22 P2, Headphone Out

The P2 connector is a 3.5 mm. stereo headphone output from the TVL320AIC3106 on the EVM. The signals on the mating plug are shown in the figure below The signals present on this connector are defined in the following table.

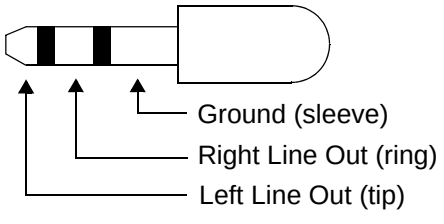


Figure 3-10, P2, Headphone Out Stereo Jack

Table 22: P2, Headphone Out Interface

Pin #	AIC3106 Signal
1(sleeve)	GND_AC
2(ring	U2, Pin 18, HPLOUT
3(tip)	U2, Pin 23,HPROUT
4	NC

3.2.23 P3, Line Out

The audio line out connector P3, is a stereo output. The output connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

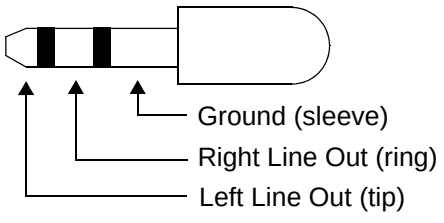


Figure 3-11, P3, Audio Line Out Stereo Jack

Table 23: P3, Audio Line Out Stereo Jack

Pin #	AIC3106 Signal
1 (sleeve)	GND_AC
2 (ring)	U2, Pin 29, LEFT_LO+
3 (tip)	U2, Pin 31, RIGHT_LO+
4 (sleeve)	NC

3.2.24 P4, Line In

Connector P4 is an stereo audio line input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

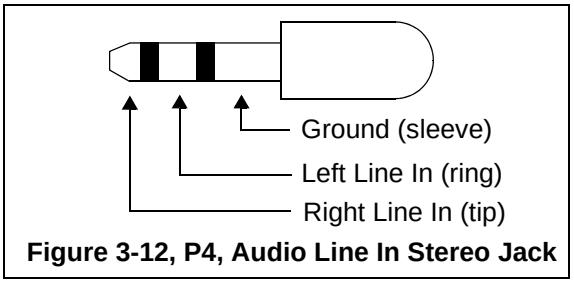


Figure 3-12, P4, Audio Line In Stereo Jack

Table 24: P4, Line In Interface

Pin #	AIC3106 Signal
1 (sleeve)	GND_AC
2 (ring)	U2, Pin 3, LINE1L+
3 (tip)	U2, Pin 5, LINE1R+
4 (sleeve)	GND_AC

3.2.25 P5, Mic In

Connector P5 is an stereo microphone line input. The input connector is a 3.5 mm stereo jack. The signals on the mating plug are shown in the figure below.

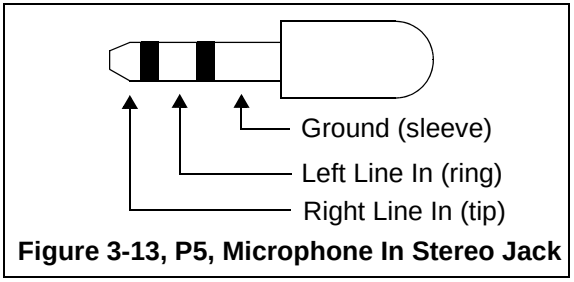


Figure 3-13, P5, Microphone In Stereo Jack

Table 25: P5, Microphone In Interface

Pin #	AIC3106 Signal
1 (sleeve)	GND_AC
2 (ring)	U2, Pin 11,14, MIC3L/MIC3R
3 (tip)	U2, Pin 11/14, MIC3L/MIC3R
4 (sleeve)	GND_AC

3.2.26 P6, HDMI Connector

Connector P6 provides an HDMI interface for the processor card. The signals on this connector are shown below.

Table 26: P6, HDMI Connector

Pins	Signal
1	HDMI_TMDSDP2
2	Ground
3	HDMI_TMDSDN2
4	HDMI_TMDSDP1
5	Ground
6	HDMI_TMDSDN1
7	HDMI_TMDSDP0
8	Ground
9	HDMI_TMDSDN0
10	HDMI_TMDSCLKP
11	Ground
12	HDMI_TMDSCLKN
13	U1, Pin 23,CE_REMOTE_OUT
14	No connect
15	U1, Pin 22, DDC_CLK_OUT
16	U1, Pin 21, DDC_DAT_OUT
17	Ground
18	U1, Pin 38, 5V_OUT
19	U1, Pin 20, HOTPLUG_DET_OUT
MTG1	Ground
MTG2	Ground
MTG3	Ground
MTG4	Ground

3.2.27 P7, DB9 Connector

The P7 connector is a 9 pin male D-connector which provides a UART interface to the EVM. This connector interfaces to the MAX 3221 RS-232 line driver (U39) and is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

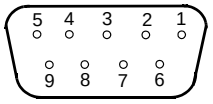


Figure 3-14, P7, DB9 Male Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 27: P7, RS-232 Pinout

Pin #	Signal Name
1	NC
2	R_IN, U39, Pin 8
3	T_OUT, U39, Pin 13
4	NC
5	GND
6	NC
7	Pin 8
8	Pin 7
9	NC

3.2.28 P8, PCIe Interface

Connector P8 provides a PCIe interface on the processors board. The signals on this connector are shown in the table below.

Table 28: P8, PCIe Interface

Pin	Signal	Pin	Signal
B1	EVM_12V	A1	Pin B31
B2	EVM_12V	A2	EVM_12V
B3	EVM_12V	A3	EVM_12V
B4	Ground	A4	Ground
B5	No connect	A5	Ground
B6	No connect	A6	PCI_3V3
B7	Ground	A7	No connect
B8	PCI_3V3	A8	PCI_3V3
B9	Ground	A9	PCI_3V3
B10	No connect	A10	PCI_3V3
B11	No connect	A11	U43, Pin 4, U41, Pin 2,EVM_3V3
KEY			
B12	No connect	A12	Ground
B13	Ground	A14	REFCLKp
B14	CON.PCIE_TXP0	A14	REFCLKn
B15	CON.PCIE_TXN0	A15	Ground
B16	Ground	A16	CON.PCIE_RXP0
B17	No connect	A17	CON.PCIE_RXN0
B18	Ground	A18	Ground
B19	CON.PCIE_TXP1	A19	No connect
B20	CON.PCIE_TXN1	A20	Ground
B21	Ground	A21	CON.PCIE_RXP1
B22	Ground	A22	CON.PCIE_RXN1
B23	No connect	A23	Ground
B24	No connect	A24	Ground
B25	Ground	A25	No connect
B26	Ground	A26	No connect
B27	No connect	A27	Ground
B28	No connect	A28	Ground
B29	Ground	A29	No connect
B30	No connect	A30	No connect
B31	Pin A1	A31	Ground
B32	Ground	A31	No connect

3.2.29 P9, SD/MMC Connector

The P92 MMC/SD connector is located on the top side of the board and is used to provide an interface to the following: MMC+, SD, and MMC. The pinout for the P9 connector is shown in the table below.

Table 29: P9, MMC/SD Connector

Pin #	Signal
1	MMC_DAT3
2	MMC_CMD
3	Ground
4	U66, Pin 2,3
5	MMC_CLK
6	Ground
7	MMC_DAT0
8	MMC_DAT1
9	MMC_DAT2
10	No connect
11	No connect
12	No connect
13	No connect
14	MMC_SD_WP
15	MMC_SD_CD
16	No connect
17	No connect
18	Ground
19	No connect
20	No connect
21	Ground
22	No connect
23	No connect
24	No connect
25	No connect
26	No connect
27	Ground
28	Ground

3.2.30 P10, DB9 Connector

The P10 connector is a 9 pin male D-connector which provides a UART interface to the EVM. This connector interfaces to the MAX 3221 RS-232 line driver (U57) and is located on the top side of the board. A view of the connector from the card edge is shown in the figure below. The signals present on this connector are defined in the following table.

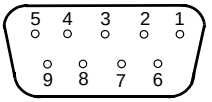


Figure 3-15, P10, DB9 Male Connector

The pin numbers and their corresponding signals are shown in the table below. This corresponds to a standard dual row to DB-9 connector interface used on personal computers.

Table 30: P10, RS-232 Pinout

Pin #	Signal Name
1	NC
2	R_IN, U57, Pin 8
3	T_OUT, U57, Pin 13
4	NC
5	GND
6	NC
7	Pin 8
8	Pin 7
9	NC

3.2.31 P11, Fan Connector

Connector P11 provides power for a 12 volt DC fan. The layout of the connector is shown in the figure below.

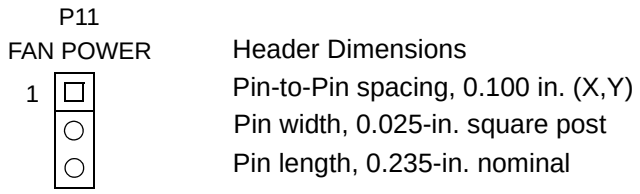


Figure 3-16, P11, Fan Connector

The signals on the pins of this connector are shown bin the table below.

Table 31: P11, Fan Connector

Pin #	Signal
1	Ground
2	EVM_12V
3	No connect

3.3 LEDs

The EVM has five (5) LEDs which are located on the top side of the board. Information regarding the LEDs are shown in the table below.

Table 32: LEDs

LED #	Schematic Page	Use	Color
DS1	56	Power LED	Green
DS2	32	USER_LED1	Green
DS3	32	USER_LED2	Green
DS4	32	USER_LED3	Green
DS5	32	USER_LED4	Green

3.4 Switches

The EVM has six (6) switches. The function of these switches are shown in the table below.

Table 33: Switches

Switch	Schematic Page	Function	Type
SW1	56	On/Off Power Switch	Toggle
SW2	32	User Readable Switches	4 Position DIP
SW3	6	Boot Load Select	10 Position DIP
SW4	6	On Board Memory Enable	2 Position DIP
SW5	28	PCI/WDOG Reset Enable	2 Position DIP
SW6	56	Reset Switch	Push Button/Momentary

3.4.1 SW1, On/Off Power Switch

Switch SW1 is an on/off toggle switch that allows +12 volts from the J1 connector to be applied to the board.

3.4.2 SW2, User Readable Switches

Switch SW2 is a 4 position DIP switch that is read via the I^2C bus. A board image of the switch is shown in the figure below.

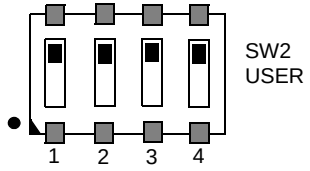


Figure 3-17, SW2, User Readable 4 Position DIP Switch

The table below shows what signal each position appears on.

Table 34: SW3, User Readable 4 Position DIP Switch

Position	Signal
1 - 8	USER_SW1
2 - 7	USER_SW2
3 - 6	USER_SW3
4 - 5	USER_SW4

3.4.3 SW3, Boot Mode/Configuration Switch

Switch SW3 is a 10 position DIP switch. Five (5) of the positions are used for selecting the boot load option. Four (4) positions are used for system configuration. The remaining switch position is a spare unused position. An image of the switch is shown in the figure below in the as shipped configuration.

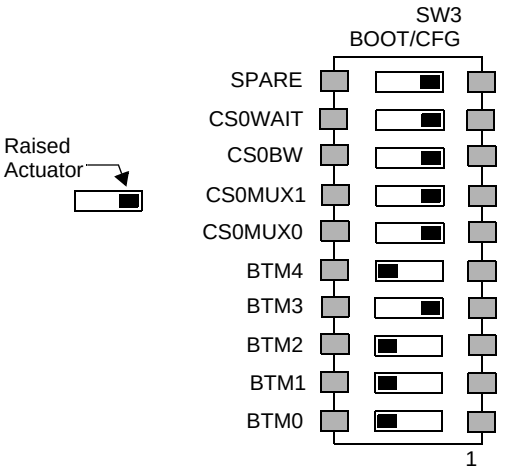


Figure 3-18, SW3, Boot Mode/Configuration Switch

The boot mode options are described in the table below.

Table 35: SW3, Boot Mode Select DIP Switch

Position	Label	Pins	Signal
1	BTM0	1-20	BTMODE0
2	BTM1	2-19	BTMODE1
3	BTM2	3-18	BTMODE2
4	BTM3	4-17	BTMODE3
5	BTM4	5-16	BTMODE4

The tables below shows the boot mode sources and their respective switch positions.

Table 36: Memory Boot Load Order

BTMODE[4] (Position5)= 1 MEMORY BOOTING PREFERRED				BTMODE[3:0] Switch Position[4:1]
First	**Second**	**Third**	**Fourth**	
XIP	UART	EMAC	SD	0 0 0 0
XIPWAIT	UART	EMAC	SD	0 0 0 1
NAND	NANDI2C	SPI	UART	0 0 1 0
NAND	NANDI2C	SD	UART	0 0 1 1
NAND	NANDI2C	SPI	EMAC	0 1 0 0
NANDI2C	SD	EMAC	UART	0 1 0 1
SPI	SD	UART	EMAC	0 1 1 0
SD	SPI	UART	EMAC	0 1 1 1
SPI	SD	PCIE_32	Reserved	1 0 0 0
SPI	SD	PCIE_32	Reserved	1 0 0 1
Reserved	Reserved	Reserved	Reserved	1 0 1 0
Reserved	Reserved	Reserved	Reserved	1 0 1 1
Reserved	Reserved	Reserved	Reserved	1 1 0 0
Reserved	Reserved	Reserved	Reserved	1 1 0 1
Reserved	Reserved	Reserved	Reserved	1 1 1 0
GP Fast External Boot	EMAC	UART	PCIE_32	1 1 1 1

Table 37: Peripheral Boot Load Order

BTMODE[4] (Position5)= 0 PERIPHERAL BOOTING PREFERRED				BTMODE[3:0] Switch Position[4:1]
First	Second	Third	Fourth	
Reserved	Reserved	Reserved	Reserved	0 0 0 0
UART	XIPWAIT	SD	SPI	0 0 0 1
UART	SPI	NAND	NANDI2C	0 0 1 0
UART	SPI	XIP	SD	0 0 1 1
EMAC	SPI	NAND	NANDI2C	0 1 0 0
Reserved	Reserved	Reserved	Reserved	0 1 0 1
Reserved	Reserved	Reserved	Reserved	0 1 1 0
EMAC	SD	SPI	XIP	0 1 1 1
PCIE_32	Reserved	Reserved	Reserved	1 0 0 0
PCIE_64	Reserved	Reserved	Reserved	1 0 0 1
Reserved	Reserved	Reserved	Reserved	1 0 1 0
Reserved	Reserved	Reserved	Reserved	1 0 1 1
Reserved	Reserved	Reserved	Reserved	1 1 0 0
Reserved	Reserved	Reserved	Reserved	1 1 0 1
Reserved	Reserved	Reserved	Reserved	1 1 1 0
GP Fast External Boot	UART	EMAC	PCIE_64	1 1 1 1

The configuration options are described in the table below.

Table 38: SW3, Configuration Switches

Position	Label	Pins	Signal	State	Function
6	CS0MUX0	5-16	CS0MUX0	Open	
				Closed	
7	CS0MUX1	6-15	CS0MUX1	Open	
				Closed	
8	CS0BW	7-14	CS0BW	Open	
				Closed	
9	CS0WAIT	8-13	CS0WAIT	Open	
				Closed	

3.4.4 SW4, On Board Memory Enable Switch

Switch SW4 is a 2 position DIP switch which allows the user to select which on board memory device to boot from. Only one device should be enabled at any given time. A board image of the switch is shown in the figure below in the as shipped configuration.

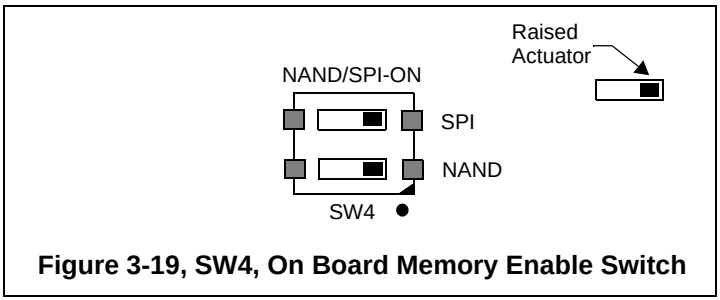


Figure 3-19, SW4, On Board Memory Enable Switch

The table below shows what signal each position appears on.

Table 39: SW4, On Board Memory Enable Switch

Position	Signal
1 - 4	NAND_BOOTn
2 - 3	SPI_BOOTn

3.4.5 SW5, PCI/WDOG Reset Enable Switch

Switch SW5 is a 2 position DIP switch which allows the user to select two items; the PCI reset mode, and enable/disable the watchdog reset. A board image of the switch is shown in the figure below.

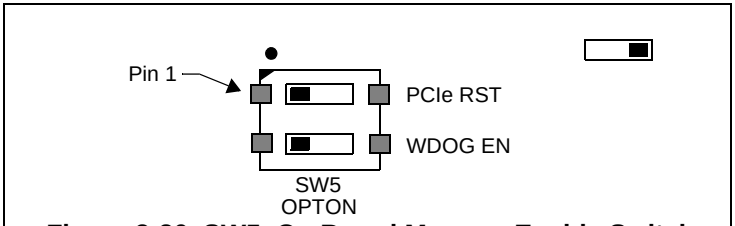


Figure 3-20, SW5, On Board Memory Enable Switch

The table below shows what signal each position appears on.

Table 40: SW5, On Board Memory Enable Switch

Position	Signal
1 - 4	OPT_SW1, PCI reset mode IN or OUT
2 - 3	OPT_SW2, WDOG reset enabled

3.4.6 SW6, Reset Switch

Switch SW6 is a push button reset switch that will RESET the board.

3.5 Infra-red Receiver

The EVM has an infra-red receiver, U61. This is used to receive signals from a television remote control handset. The logic for this is shown on page 29 of the schematics.

3.6 Test Points

The EVM has 26 test points which appear on the top of the board. The following figure identifies the position of each test point. The next table lists each test point and the signal appearing on that test point.

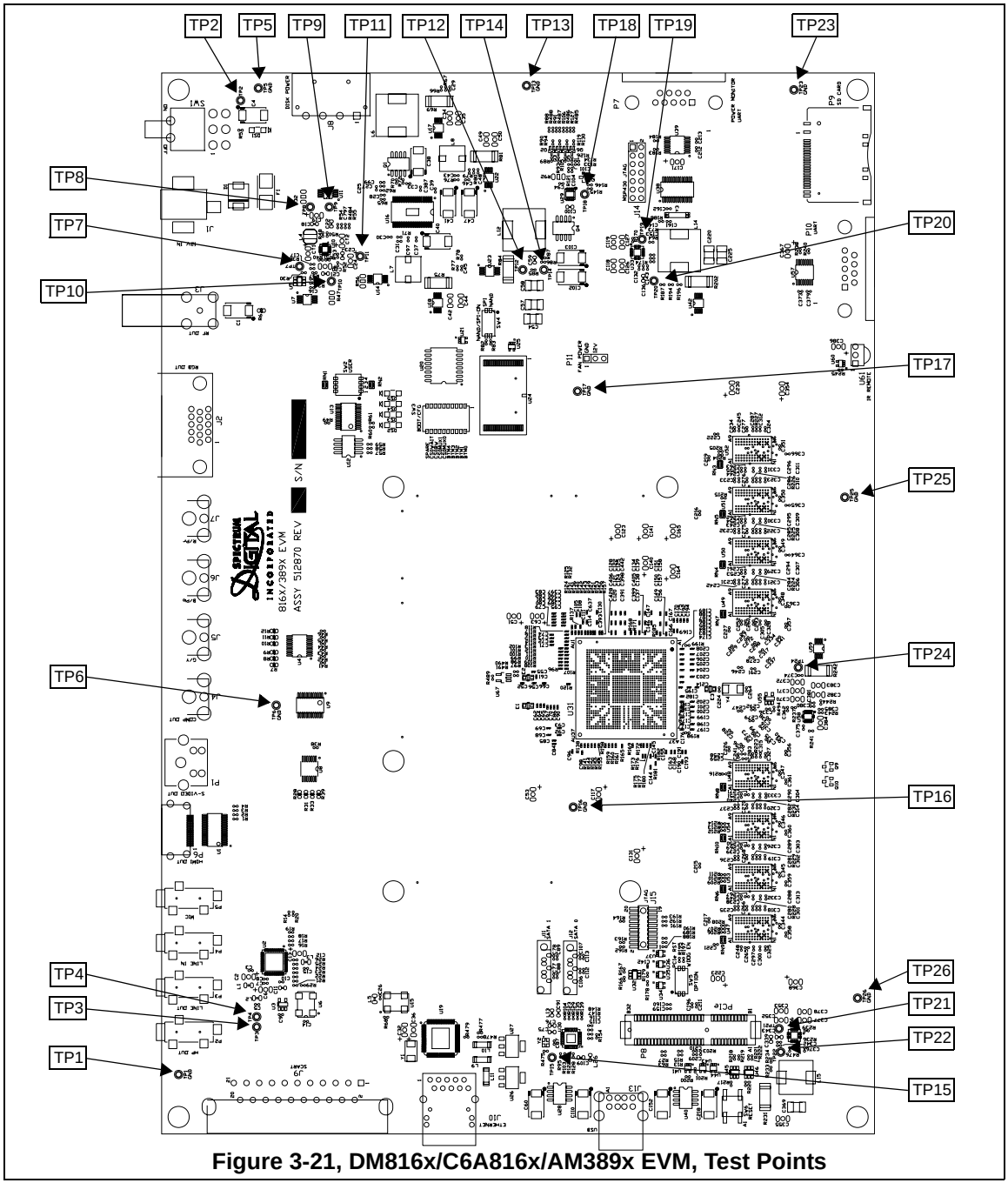


Figure 3-21, DM816x/C6A816x/AM389x EVM, Test Points

Table 41: DM816x/C6A816x/AM389x EVM Test Points

Test Point #	Schematic Page	Signal
TP1	56	Ground
TP2	56	EVM_12V
TP3	41	U2, Pin 27, MONO_LO+
TP4	41	U2, Pin 28, MONO_LO-
TP5	56	Ground
TP6	56	Ground
TP7	55	U5, Pin 1, $\overline{\text{RESET}}$, EVM_3V3
TP8	55	U10, Pin 7, SW, 1V8_DIGITAL
TP9	55	U10, Pin 5, PGn, EVM_5V0
TP10	55	U10, Pin 14, VDLO1, 1V8_ANALOG
TP11	55	U10, Pin 17, VLDO2, 0V9_A
TP12	54	EVM_1V0_AVS
TP13	52	Ground
TP14	54	EVM_1V0_AVS
TP15	13	U30, Pin 23, OSCOUT
TP16	56	Ground
TP17	56	Ground
TP18	54	Ground
TP19	52	U33, Pin 14, PWRGRD
TP20	52	U33, Pin 9, SS/TR
TP21	29	Ground
TP22	29	U56, Pin 9, SS/TR
TP23	56	Ground
TP24	53	U58, Pin 3, VO, VTT
TP25	56	Ground
TP26	56	Ground

Appendix A

Schematics

This appendix contains the schematics for the DM816x/C6A816x/AM389x EVM.

POWER DOMAINS

EVM_12V0	12 VOLT INPUT FROM EXTERNAL POWER SUPPLY
EVM_5V0	5.0 VOLT OUTPUT FROM TPS65232
EVM_3V3	3.3 VOLT OUTPUT FROM TPS65232
EVM_1V8_A	1.8 VOLT ANALOG LDO OUTPUT FROM TPS65001
EVM_1V8_D	1.8 VOLT DIGITAL OUTPUT FROM TPS65001
EVM_1V5	1.5 VOLT OUTPUT FROM TPS54620
EVM_1V0_AVS	1.0 VOLT CORE FROM TPS40041
EVM_1V0_CONN	1.0 VOLT NON-CORE FROM TPS65232
EVM_0V9	0.9 VOLT OUTPUT FROM TPS65001
EVM_DDR_VTT	0.75 VOLT TERMINATOR DDR3

REV	DESCRIPTION	DATE	APPROVED
A	Initial schematic for layout	02/15/2010	RRP
B	Beta build	10/31/2010	RRP
B	Production build	5/15/2011	RRP

SCHEMATIC CONTENTS

I2C0 ADDRESS MAP

BASE BINARY	HEX BASE (RJ)	DEVICE	SHEET
		PCF8575	27
		I2C EEPROM	31
		TLV320AIC3106	36

RJ - Right Justified

I2C1 ADDRESS MAP

BASE BINARY	HEX BASE (RJ)	DEVICE	SHEET
		PCF8575	27

RJ - Right Justified

REVISION STATUS OF SHEETS

REV	A	A	A	A	A	A	A	A		
SH	51	52	53	54	55	56	57	58		
REV	A	A	A	A	A	A	A	A	A	A
SH	41	42	43	44	45	46	47	48	49	50
REV	A	A	A	A	A	A	A	A	A	A
SH	31	32	33	34	35	36	37	38	39	40
REV	A	A	A	A	A	A	A	A	A	A
SH	21	22	23	24	25	26	27	28	29	30
REV	A	A	A	A	A	A	A	A	A	A
SH	11	12	13	14	15	16	17	18	19	20
REV	C	A	A	A	A	A	A	A	A	A
SH	1	2	3	4	5	6	7	8	9	10

NEXT ASSY | USED ON

APPLICATION

DWN	R.R.P.	DATE 02/15/2010
CHK	T.W.K.	DATE 02/15/2010
ENGR	R.R.P.	DATE 02/15/2010
ENGR-MGR	R.R.P.	DATE 02/15/2010
QA	C.M.D.	DATE 02/15/2010
MFG	R.R.P.	DATE 02/15/2010
RLSE	R.R.P.	DATE 02/15/2010

SPECTRUM DIGITAL INCORPORATED

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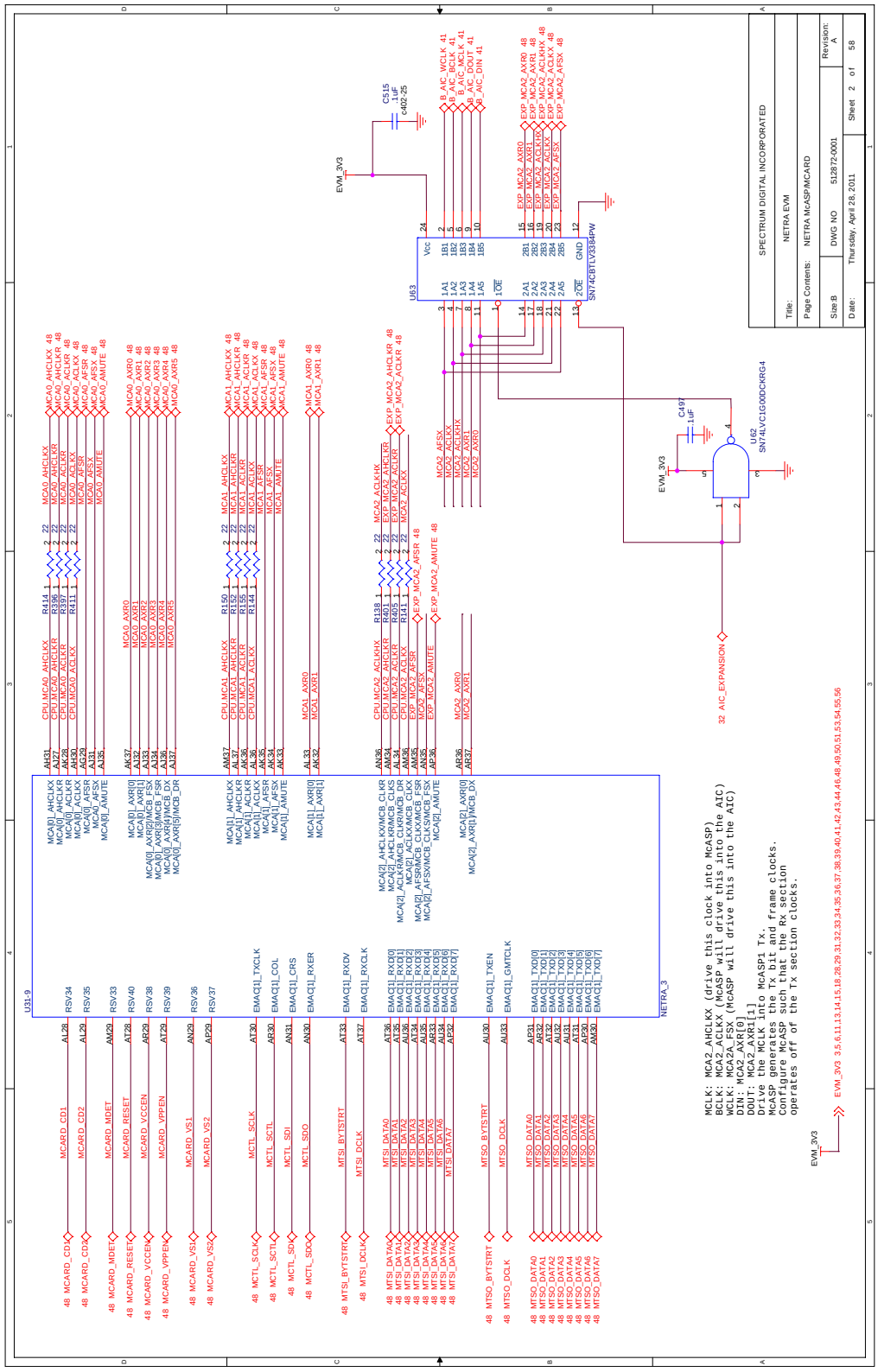
Page Contents:	TITLE PAGE	
Size:B	DWG NO 512872-0001	Revision: C
Date: Tuesday, June 14, 2011	Sheet 1 of 58	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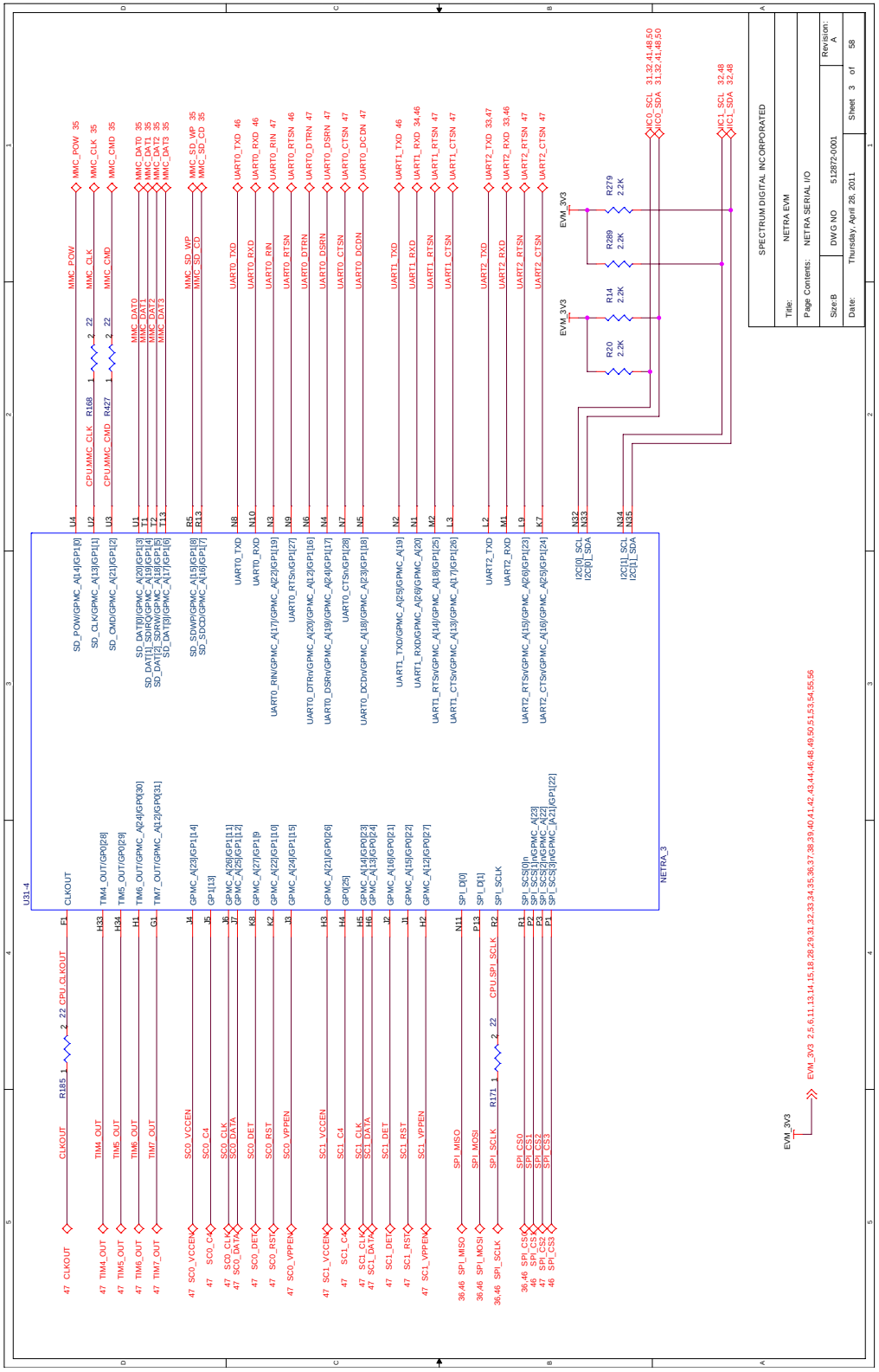
Title: NETRA EVM
Page Contents: NETRA McASP/MCARD
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 2 of 58
MCLK: MCA2_AHCLKX (drive this clock into McASP)
BCLK: MCA2_ACLKX (McASP will drive this into the AIC)
WCLK: MCA2_AFSX (McASP will drive this into the AIC)
DOUT: MCA2_AXR1[1]
Drive the MCLK into McASP1 Tx.
McASP generates the Tx bit and frame clocks.
Configure McASP such that the Rx section
operates off of the Tx section clocks.
U31-9
NETRA_3
U63
SN74CBTLV3384PW
U62
SN74LVC1G00DCKRG4
EVM_3V3
32 AIC_EXPANSION


U31:4
NETRA_3
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Title: NETRA EVM
Page Contents: NETRA SERIAL I/O
Size:B
DWG NO 5128Z2-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 3 of 58
EVM_3V3
R185
R168
R427
R20
R14
R289
R279
CLKOUT
CPU.MMC_CLK
CPU.MMC_CMD
MMC_POW
MMC_CLK
MMC_CMD
MMC_DAT0
MMC_DAT1
MMC_DAT2
MMC_DAT3
MMC_SD_WP
MMC_SD_CD
UART0_TXD
UART0_RXD
UART0_RIN
UART0_RTSN
UART0_DTRN
UART0_DSRN
UART0_CTSN
UART0_DCDN
UART1_TXD
UART1_RXD
UART1_RTSN
UART1_CTSN
UART2_TXD
UART2_RXD
UART2_RTSN
UART2_CTSN
SPI_MISO
SPI_MOSI
SPI_SCLK
SPI_CS0
SPI_CS1
SPI_CS2
SPI_CS3
I2C1_SCL
I2C1_SDA
EVM_3V3


U31-10
NETRA_3
EMAC[0]_GMTCLK
EMAC[0]_RXD[0]
EMAC[0]_RXD[1]
EMAC[0]_RXD[2]
EMAC[0]_RXD[3]
EMAC[0]_RXD[4]
EMAC[0]_RXD[5]
EMAC[0]_RXD[6]
EMAC[0]_RXD[7]
EMAC[0]_RXCLK
EMAC[0]_RXDV
EMAC[0]_RXER
EMAC[0]_COL
EMAC[0]_CRS
EMAC[0]_TXD[0]
EMAC[0]_TXD[1]
EMAC[0]_TXD[2]
EMAC[0]_TXD[3]
EMAC[0]_TXD[4]
EMAC[0]_TXD[5]
EMAC[0]_TXD[6]
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MDIO_MDIO
AC37
AD37
AD36
AC36
AD35
AC35
AD25
AC25
AE26
AE37
AE35
AE34
AB25
AA25
AE33
AE32
AE31
AE30
AA28
AB26
AC26
AG36
AG37
AE27
AH37
AH36
CPU_GMII0_GMTCLK
R165 1
2 22
GMII0_GMTCLK
GMII0_RXD0
GMII0_RXD1
GMII0_RXD2
GMII0_RXD3
GMII0_RXD4
GMII0_RXD5
GMII0_RXD6
GMII0_RXD7
GMII0_RCLK
GMII0_RXDV
GMII0_RXER
GMII0_COL
GMII0_CRS
CPU_GMII0_TXD0
CPU_GMII0_TXD1
CPU_GMII0_TXD2
CPU_GMII0_TXD3
CPU_GMII0_TXD4
CPU_GMII0_TXD5
CPU_GMII0_TXD6
CPU_GMII0_TXD7
R417 1
R419 1
R420 1
R421 1
R163 1
R164 1
R158 1
R416 1
GMII0_TXD0
GMII0_TXD1
GMII0_TXD2
GMII0_TXD3
GMII0_TXD4
GMII0_TXD5
GMII0_TXD6
GMII0_TXD7
CPU_GMII0_TXEN
R159 1
GMII0_TXEN
CPU_GMII0_TCLK
R161 1
GMII0_TCLK
MDIO_MDCLK
MDIO_MDIO
GMII0_GMTCLK 38
GMII0_RXD0 38
GMII0_RXD1 38
GMII0_RXD2 38
GMII0_RXD3 38
GMII0_RXD4 38
GMII0_RXD5 38
GMII0_RXD6 38
GMII0_RXD7 38
GMII0_RCLK 38
GMII0_RXDV 38
GMII0_RXER 38
GMII0_COL 38
GMII0_CRS 38
GMII0_TXD0 38
GMII0_TXD1 38
GMII0_TXD2 38
GMII0_TXD3 38
GMII0_TXD4 38
GMII0_TXD5 38
GMII0_TXD6 38
GMII0_TXD7 38
GMII0_TXEN 38
GMII0_TCLK 38
MDIO_MDCLK 38,48
MDIO_MDIO 38,48
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Title: NETRA EVM
Page Contents: NETRA ETHERNET
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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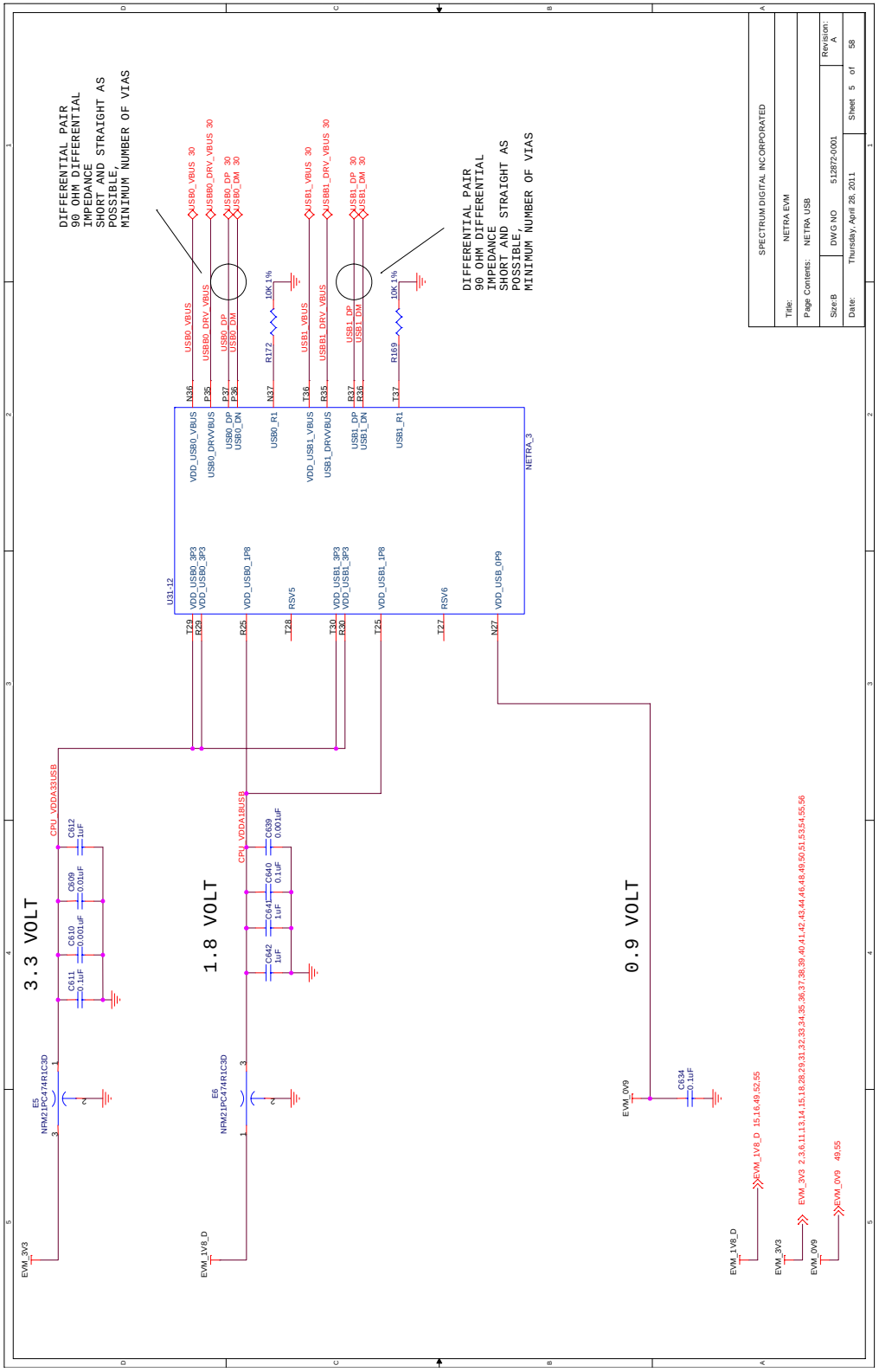
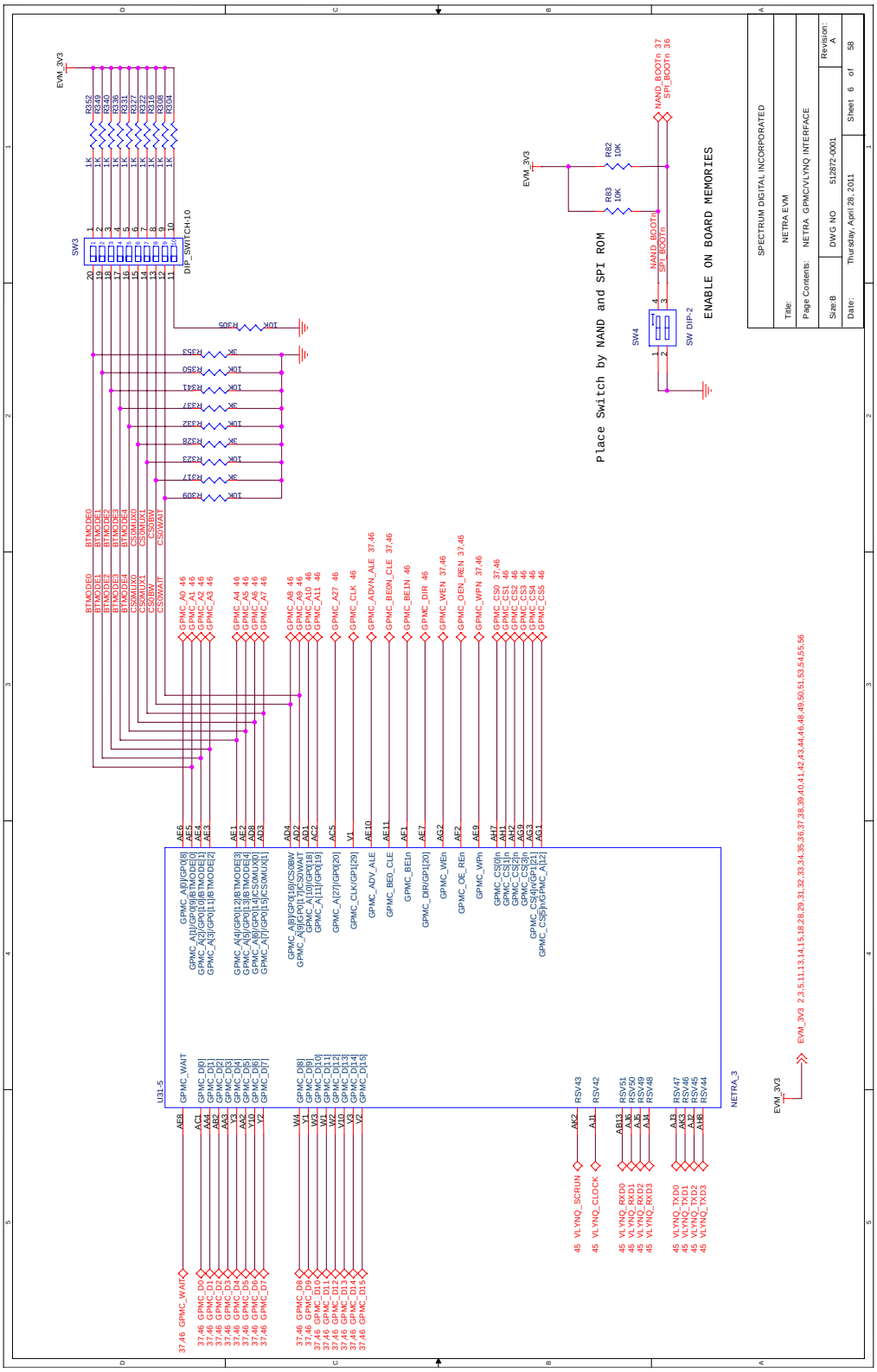

DIFFERENTIAL PAIR
90 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS
DIFFERENTIAL PAIR
90 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS
3.3 VOLT
1.8 VOLT
0.9 VOLT
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: NETRA USB
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 5 of 58
U31-12
NETRA_3
R172
R169
10K 1%
C610
C611
C612
C639
C640
C641
C642
C634
E5
E6
NPM21PC474R1C3D
EVM_3V3
EVM_1V8_D
EVM_0V9


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: NETRA GPMC/VLYNQ INTERFACE
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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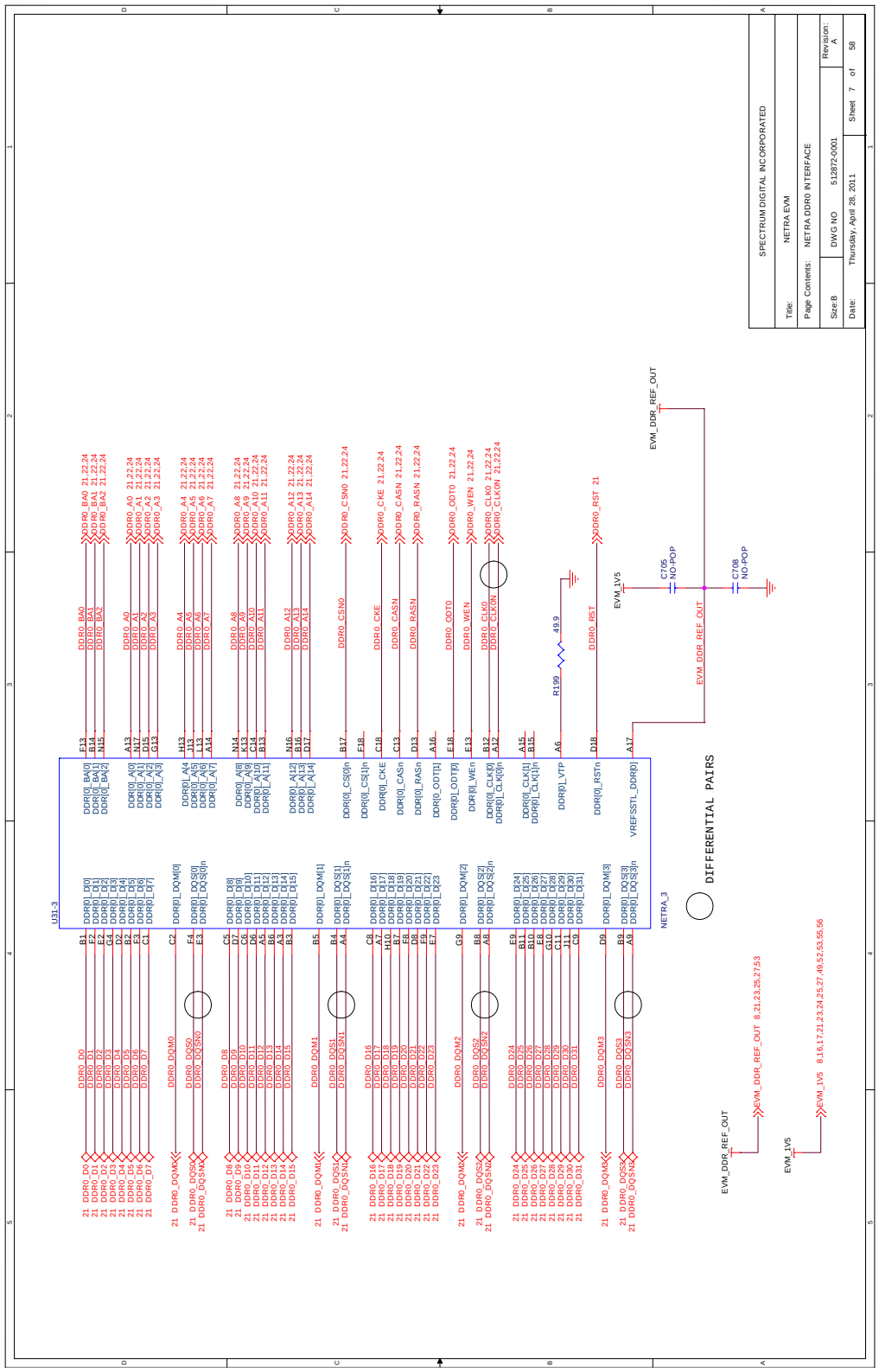
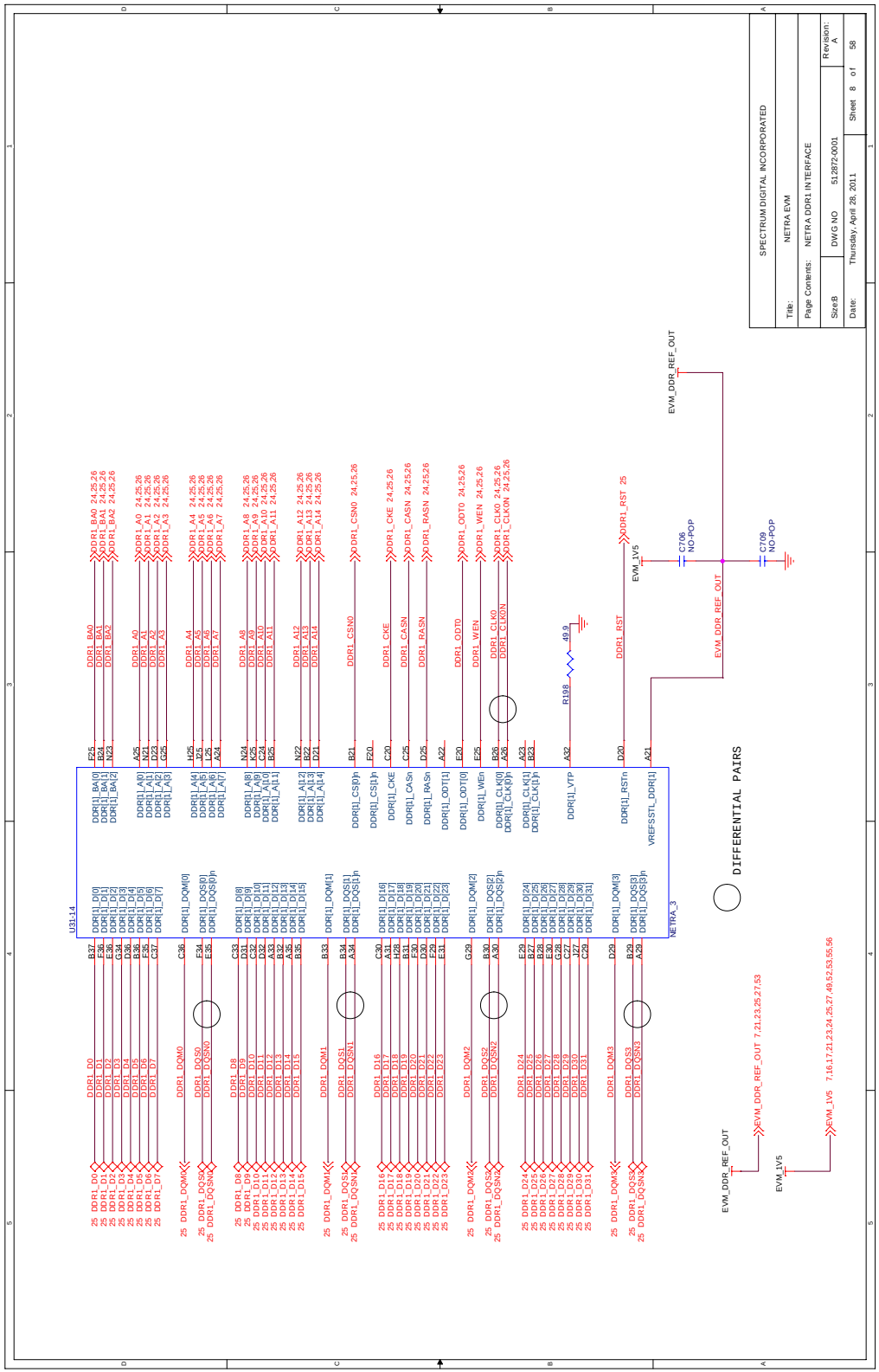
ENABLE ON BOARD MEMORIES
Place Switch by NAND and SPI ROM
SW DIP-2
DIP_SWITCH-10
NETRA_3
U31-5
EVM_3V3
NAND_BOOTn 37
SPI_BOOTn 36
GPMC_WAIT
GPMC_CLK
GPMC_ADV_ALE
GPMC_BEO_CLE
GPMC_BE1n
GPMC_DIR
GPMC_WEn
GPMC_OE_REn
GPMC_WPn
VLYNQ_SCRUN
VLYNQ_CLOCK
VLYNQ_RXD0
VLYNQ_RXD1
VLYNQ_RXD2
VLYNQ_RXD3
VLYNQ_TXD0
VLYNQ_TXD1
VLYNQ_TXD2
VLYNQ_TXD3


U31-3
NETRA_3
DIFFERENTIAL PAIRS
R199 49.9
C705 NO-POP
C708 NO-POP
EVM_1V5
EVM_DDR_REF_OUT
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: NETRA DDR0 INTERFACE
Size:B DWG NO 5128272-0001 Revision: A
Date: Thursday, April 28, 2011 Sheet 7 of 58


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: NETRA DDR1 INTERFACE
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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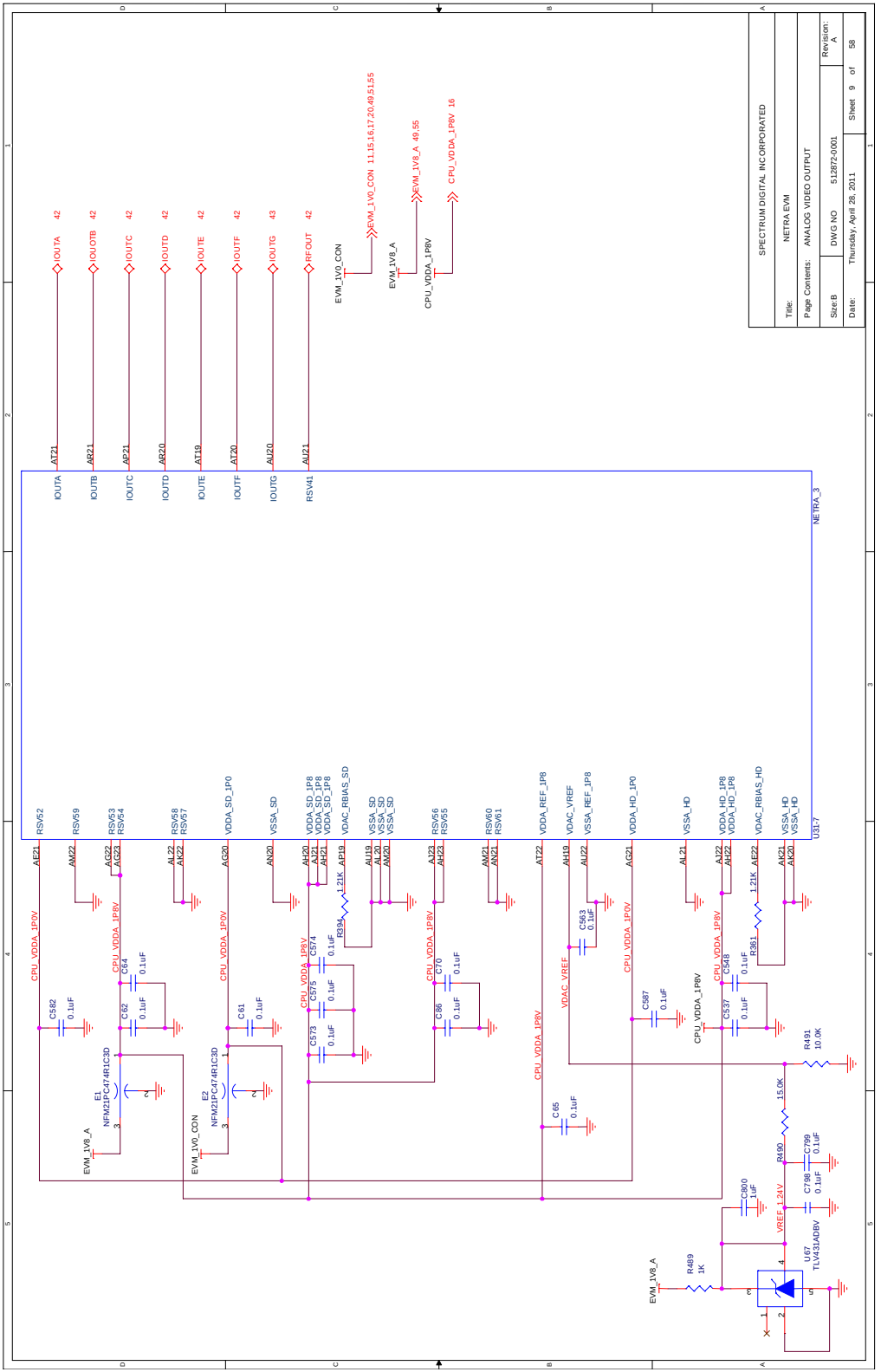
U31:L4
NETRA_3
DIFFERENTIAL PAIRS
VREFSSTL_DDR1
EVM_DDR_REF_OUT
EVM_1V5
C706 NO-POP
C709 NO-POP
R198 49.9
DDR1_RST 25
EVM_DDR_REF_OUT 7,21,23,25,27,53
EVM_1V5 7,16,17,21,23,24,25,27,49,52,53,55,56


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: ANALOG VIDEO OUTPUT
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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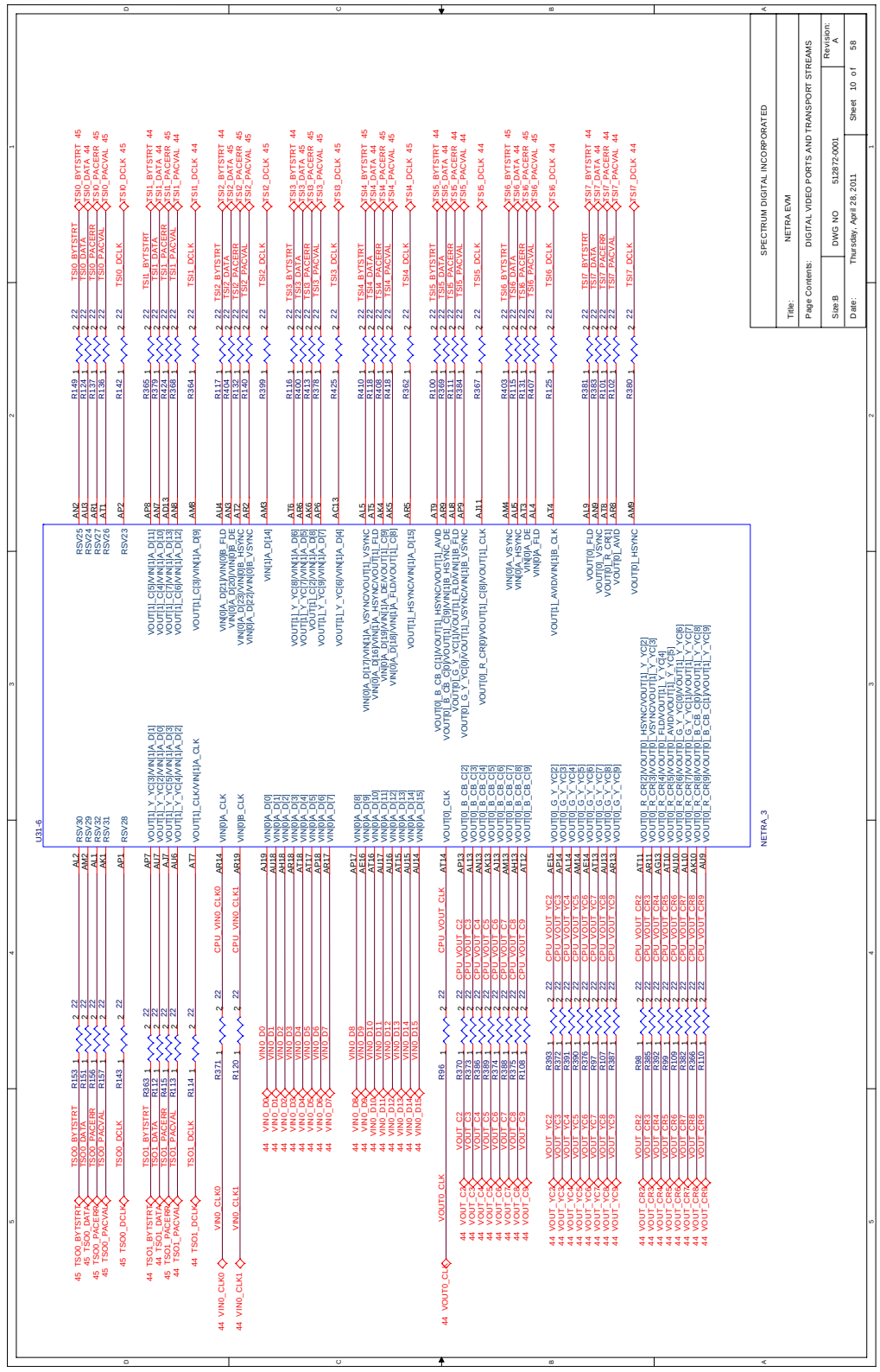
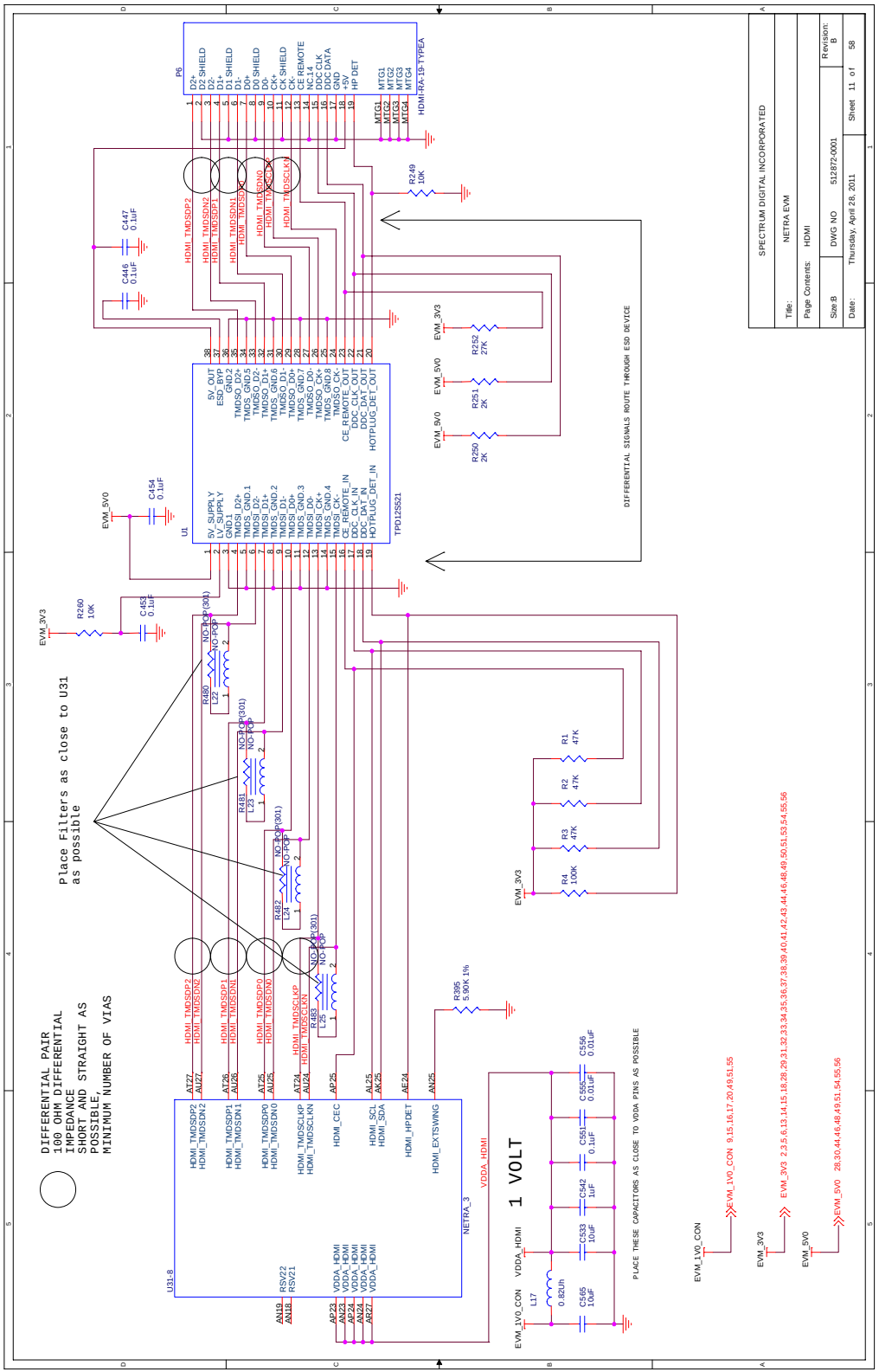
NETRA_3
U31:7
IOUTA 42
IOUTB 42
IOUTC 42
IOUTD 42
IOUTE 42
IOUTF 42
IOUTG 43
RFOUT 42
EVM_1V0_CON 11,15,16,17,20,49,51,55
EVM_1V8_A 49,55
CPU_VDDA_1P8V 16
CPU_VDDA_1P0V
CPU_VDDA_1P8V
VDAC_RBIAS_SD
VDAC_RBIAS_HD
VDAC_VREF
VDDA_REF_1P8
VSSA_REF_1P8
VSSA_SD
VSSA_HD
VDDA_SD_1P0
VDDA_HD_1P0
VDDA_SD_1P8
VDDA_HD_1P8
VREF_1P24V
U67 TLV431ADBV
R489 1K
R490 15.0K
R491 10.0K
R394 1.21K
R361 1.21K
E1 NFM21PC474R1C3D
E2 NFM21PC474R1C3D


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: DIGITAL VIDEO PORTS AND TRANSPORT STREAMS
Size:B DWG NO 5128T2-0001 Revision: A
Date: Thursday, April 28, 2011 Sheet 10 of 58
U31-6
NETRA_3


DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS
Place Filters as close to U31
as possible
1 VOLT
PLACE THESE CAPACITORS AS CLOSE TO VDDA PINS AS POSSIBLE
DIFFERENTIAL SIGNALS ROUTE THROUGH ESD DEVICE
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: HDMI
Size:B
DWG NO 512872-0001
Revision: B
Date: Thursday, April 28, 2011
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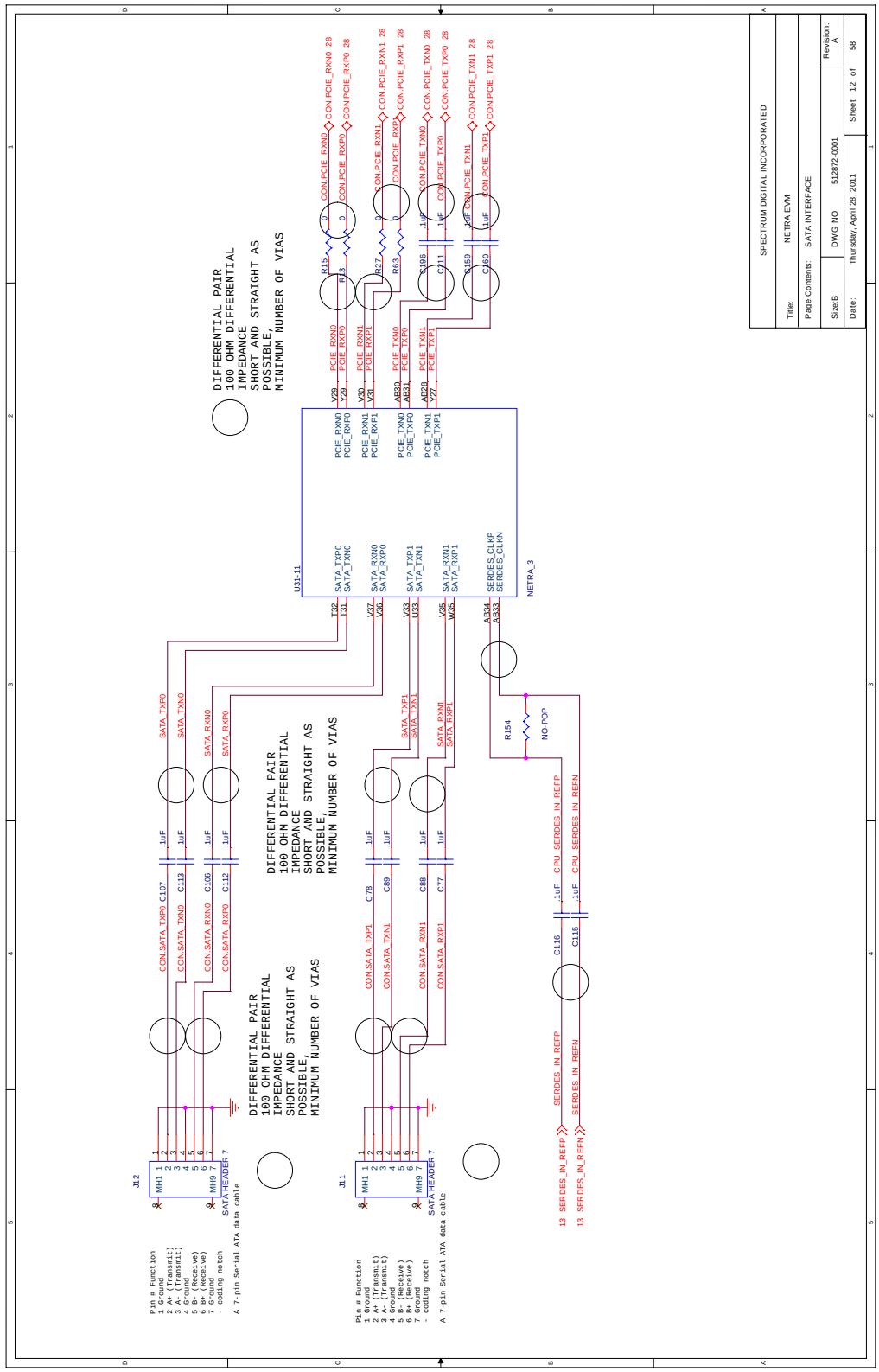
DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS
U31-11
NETRA_3
J12
J11
SATAHEADER 7
A 7-pin Serial ATA data cable
R154
NO-POP
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: SATA INTERFACE
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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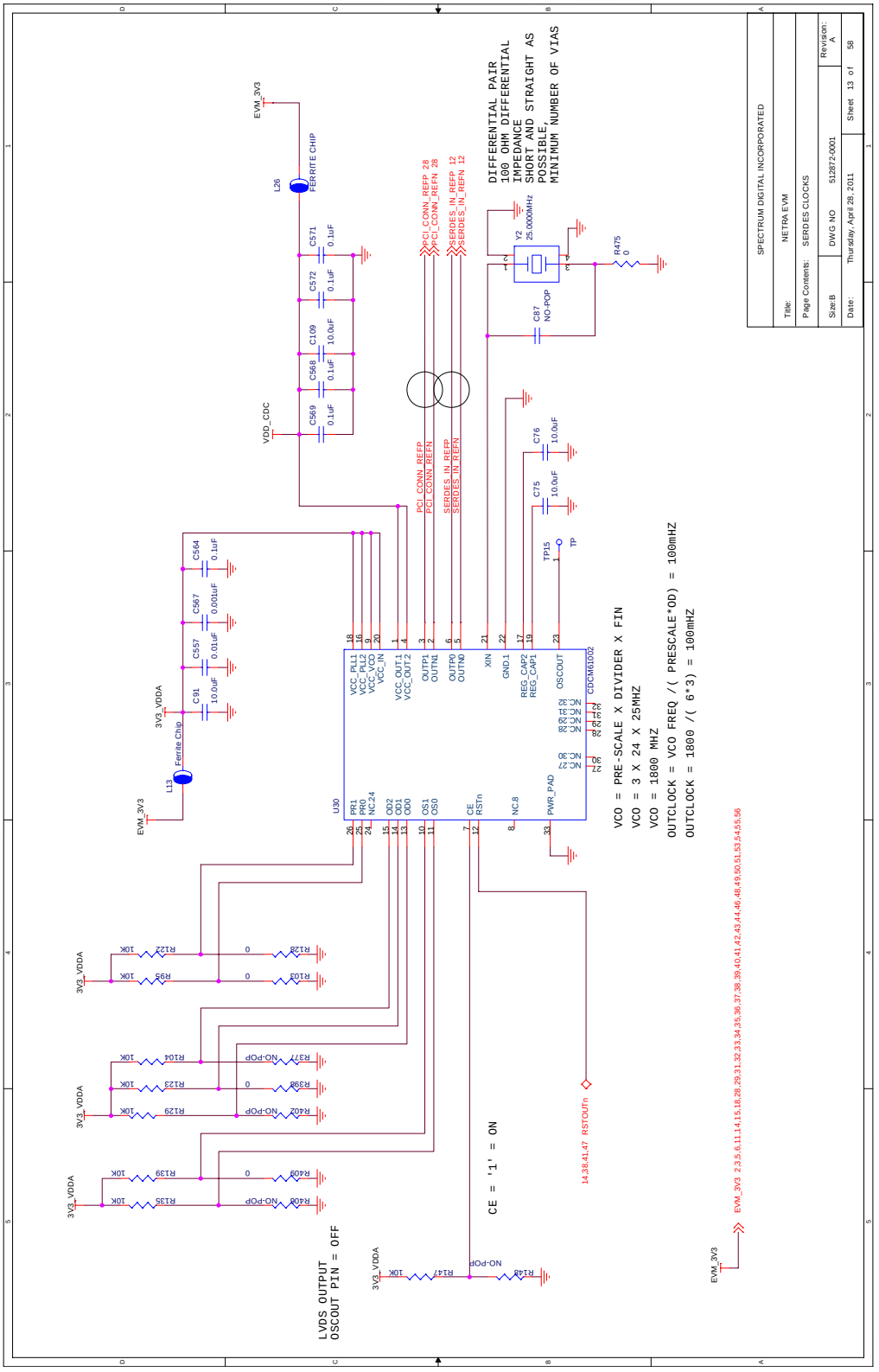
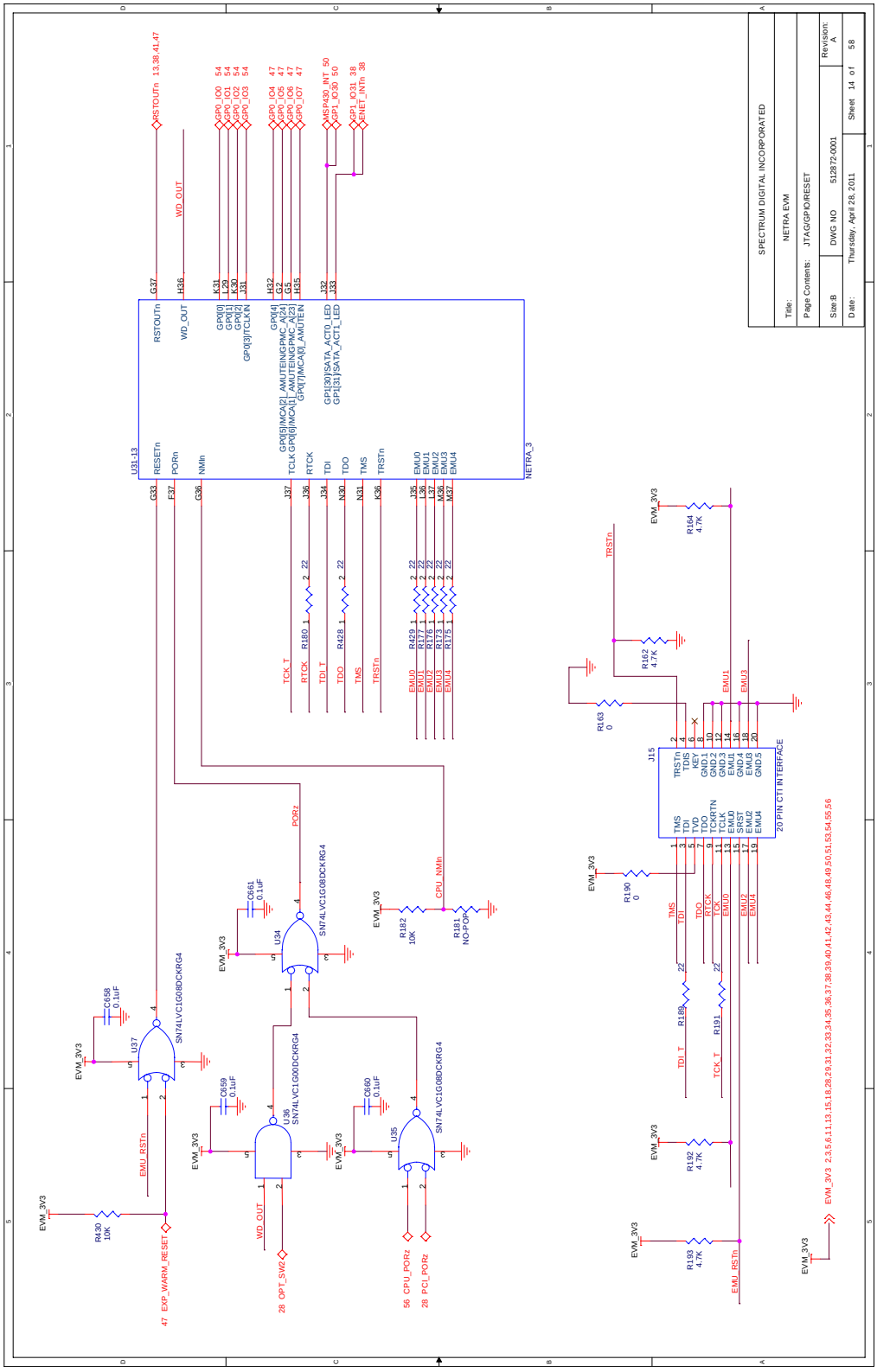

DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS
VCO = PRE-SCALE X DIVIDER X FIN
VCO = 3 X 24 X 25MHZ
VCO = 1800 MHZ
OUTCLOCK = VCO FREQ /(PRESCALE*OD) = 100mHZ
OUTCLOCK = 1800 /(6*3) = 100mHZ
CE = '1' = ON
LVDS OUTPUT
OSCOUT PIN = OFF
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: SERDES CLOCKS
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 13 of 58


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: JTAG/GPIO/RESET
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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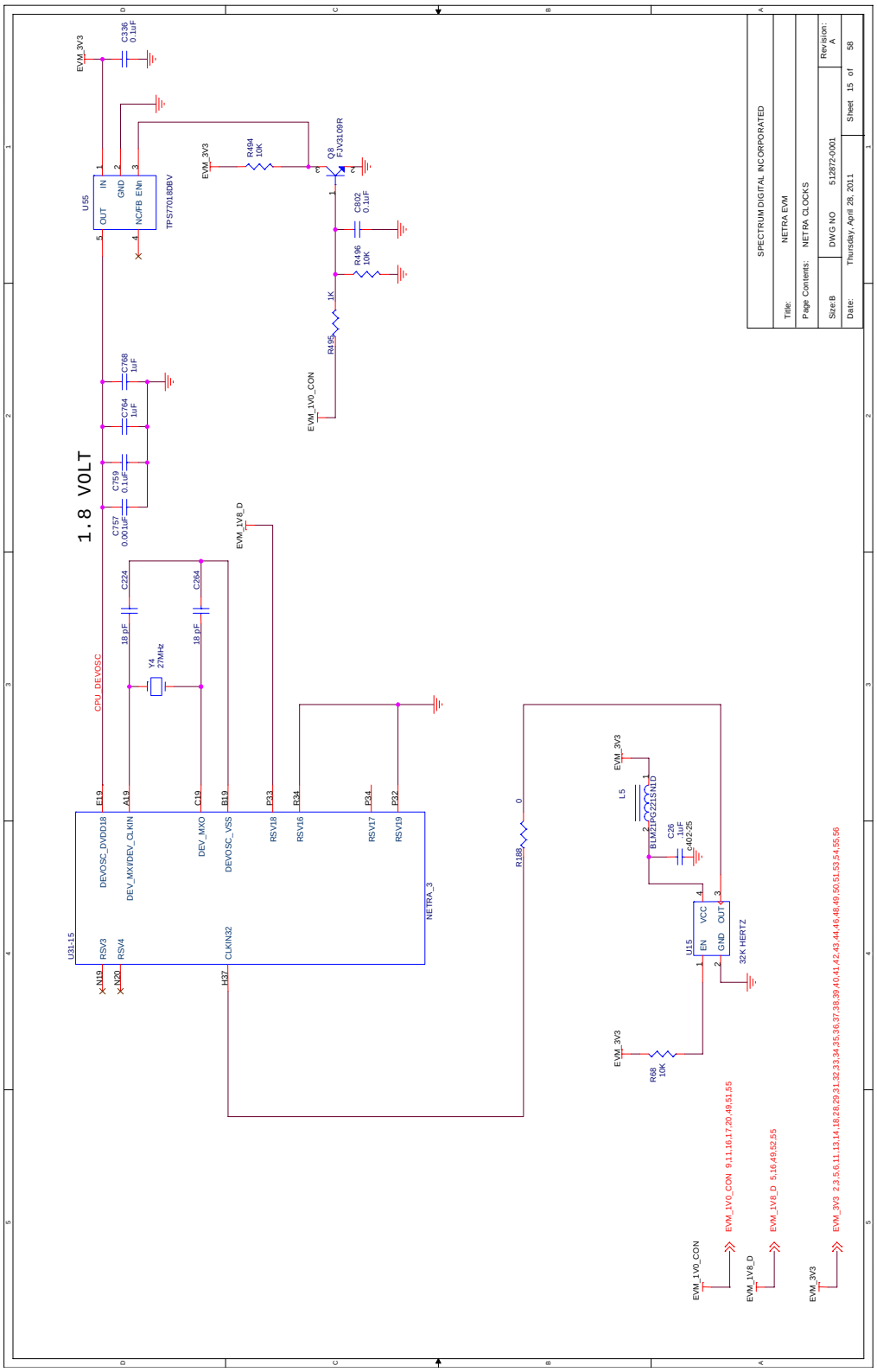
U31-13
NETRA_3
RSTOUTn
WD_OUT
RESETn
PORn
NMIn
RTCK
TDI
TDO
TMS
TRSTn
EMU0
EMU1
EMU2
EMU3
EMU4
GP0[0]
GP0[1]
GP0[2]
GP0[3]/TCLKIN
GP0[4]
GP0[5]/MCA[2]_AMUTEINGPMC_A24
GP0[6]/MCA[1]_AMUTEINGPMC_A23
GP0[7]/MCA[0]_AMUTEIN
GP1[30]/SATA_ACT0_LED
GP1[31]/SATA_ACT1_LED
GP0_IO0
GP0_IO1
GP0_IO2
GP0_IO3
GP0_IO4
GP0_IO5
GP0_IO6
GP0_IO7
MSP430_INT
GP1_IO30
GP1_IO31
ENET_INTn
TCK_T
TDI_T
TRSTn
J15
20 PIN CTI INTERFACE
EMU_RSTn
EXP_WARM_RESET
OPT_SW2
CPU_PORz
PCI_PORz
CPU_NMIn
EVM_3V3
SN74LVC1G08DCKRG4
U37
U34
U36
U35
C658
C659
C660
C661
0.1uF
R430
10K
R182
10K
R181
NO-POP
R163
0
R162
4.7K
R164
4.7K
R190
0
R189
22
R191
22
R192
4.7K
R193
4.7K


1.8 VOLT
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: NETRA CLOCKS
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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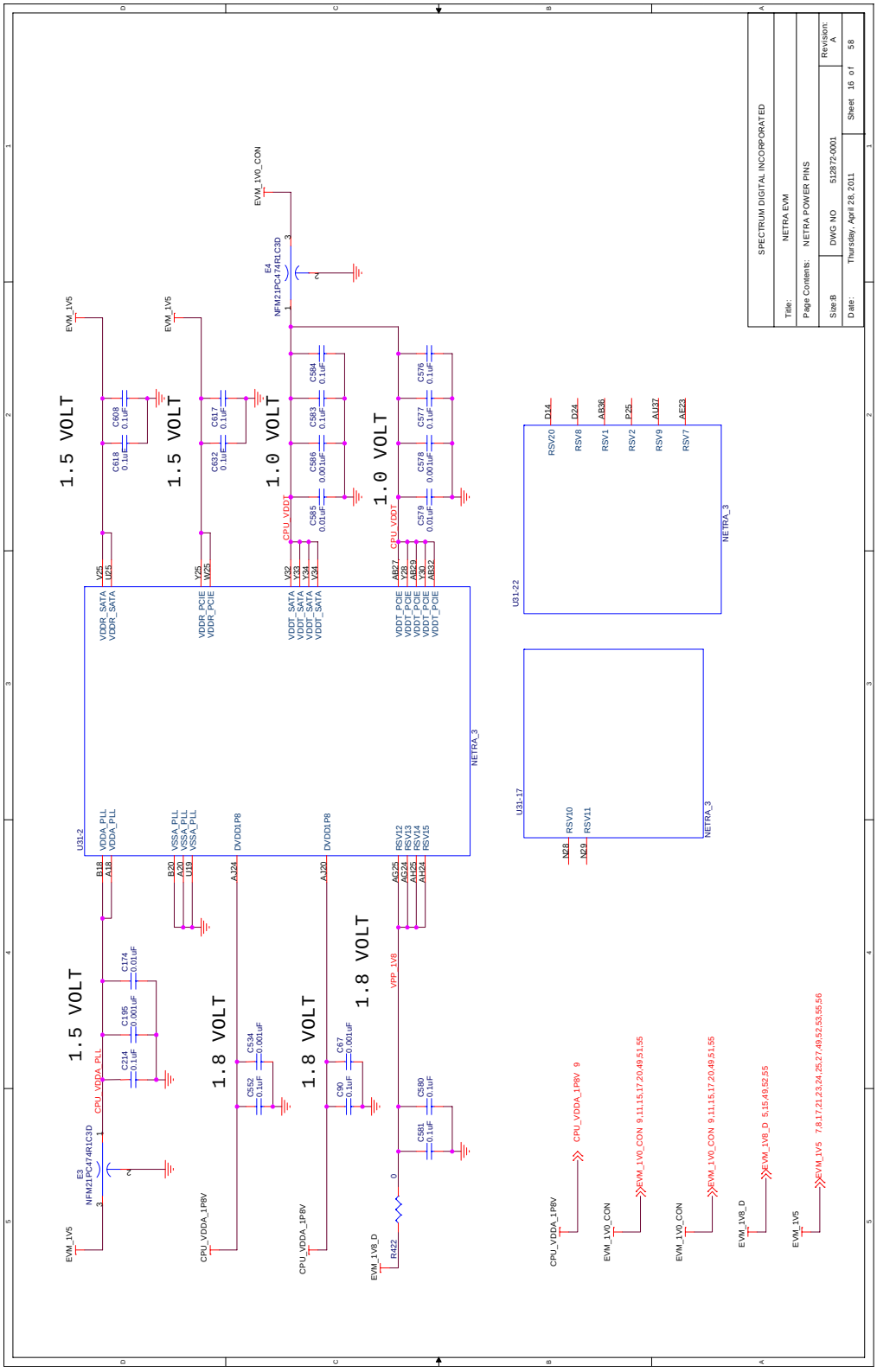
EVM_3V3
EVM_1V0_CON
EVM_1V8_D
CPU_DEVOSC
DEVOSC_DVDD18
DEV_MXI/DEV_CLKIN
DEV_MXO
DEVOSC_VSS
RSV3
RSV4
CLKIN32
NETRA_3
TPS77018DBV
FJV3109R
BLM21PG221SN1D
32K HERTZ
27MHz


1.5 VOLT
1.5 VOLT
1.0 VOLT
1.0 VOLT
1.5 VOLT
1.8 VOLT
1.8 VOLT
1.8 VOLT
EVM_1V5
EVM_1V0_CON
CPU_VDDA_1P8V
EVM_1V8_D
NETRA_3
U31-2
U31-17
U31-22
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: NETRA POWER PINS
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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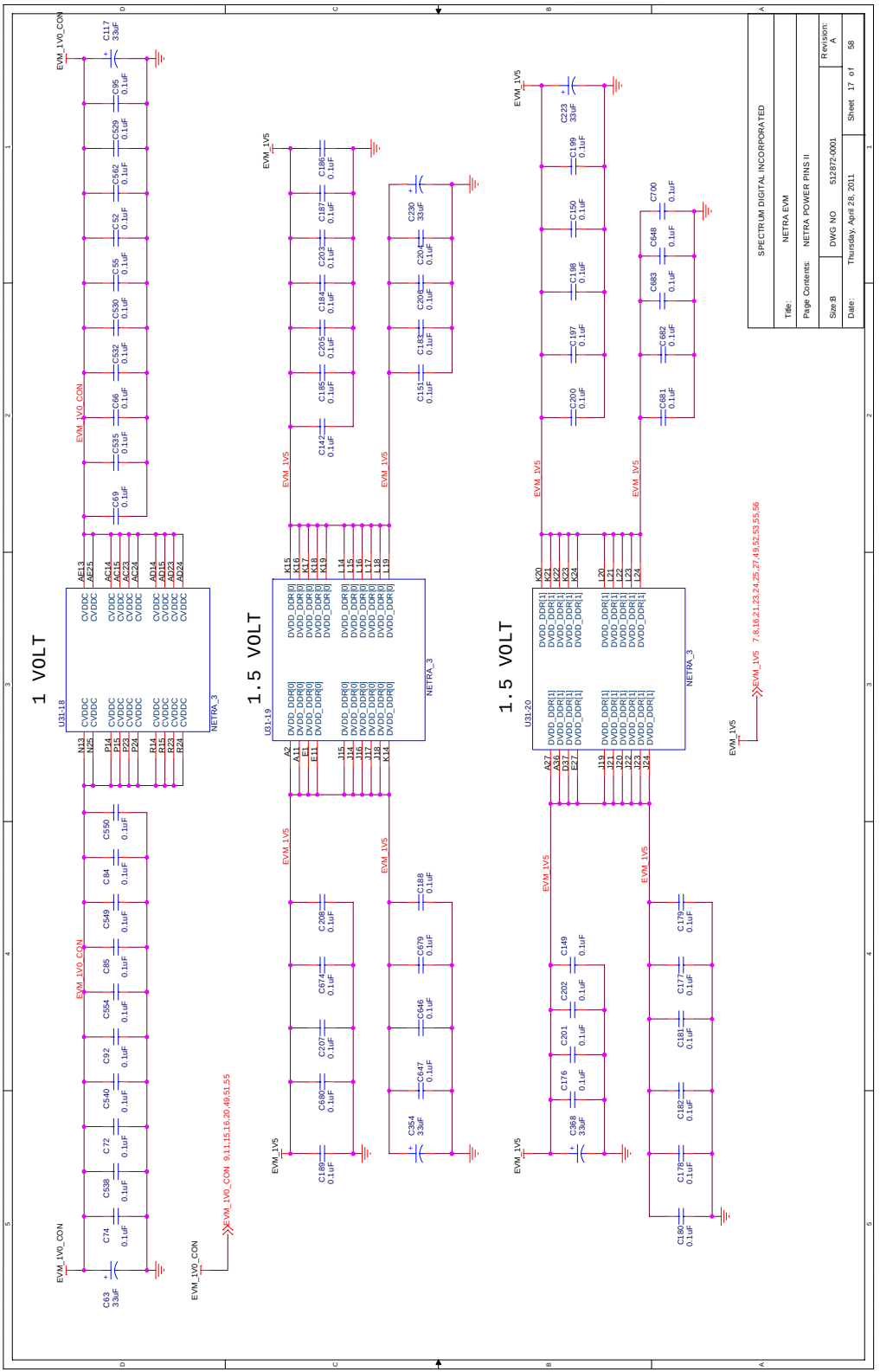
1 VOLT
1.5 VOLT
1.5 VOLT
NETRA_3
EVM_1V0_CON
EVM_1V5
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: NETRA POWER PINS II
Size: B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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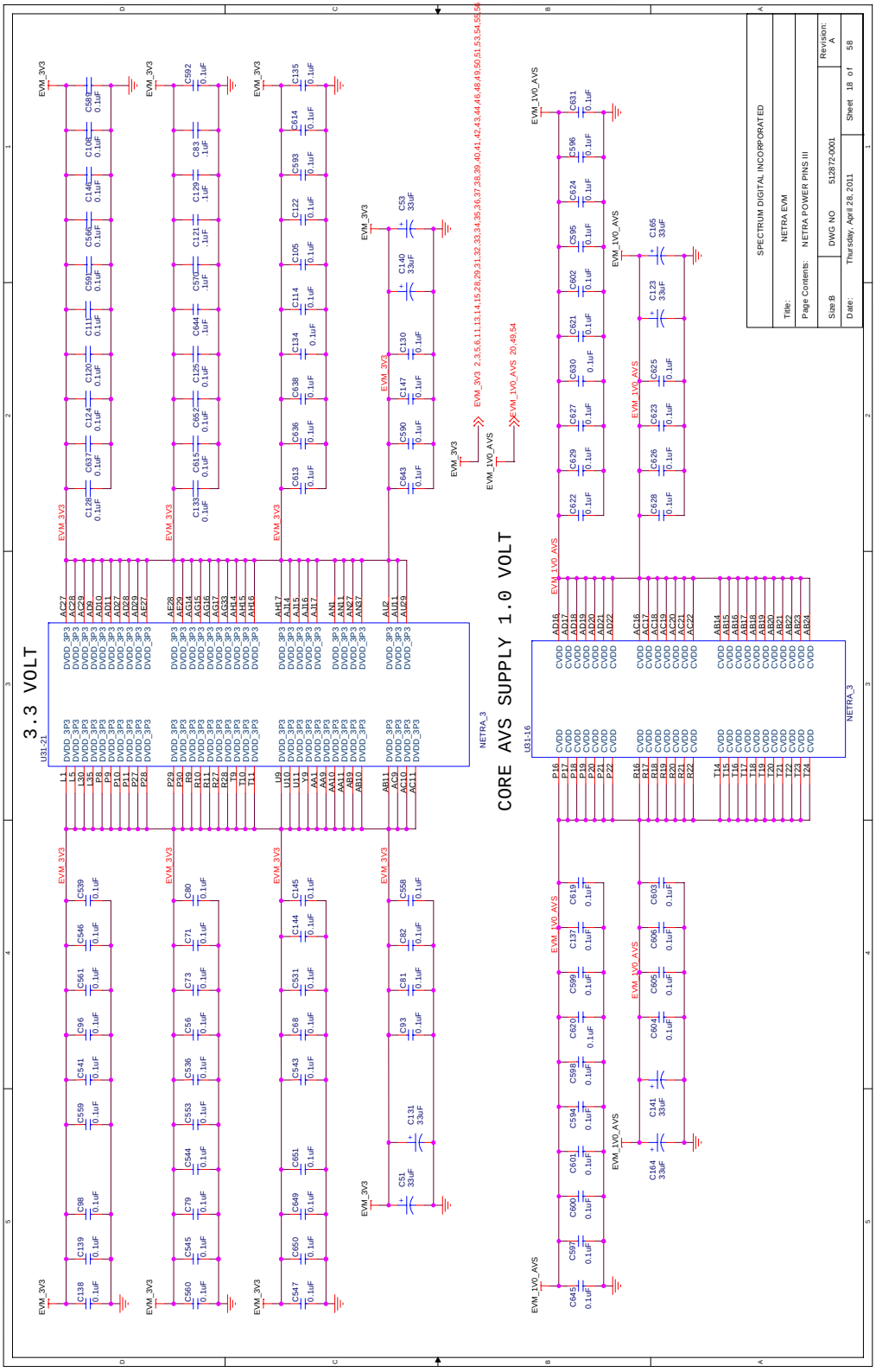
3.3 VOLT
CORE AVS SUPPLY 1.0 VOLT
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: NETRA POWER PINS III
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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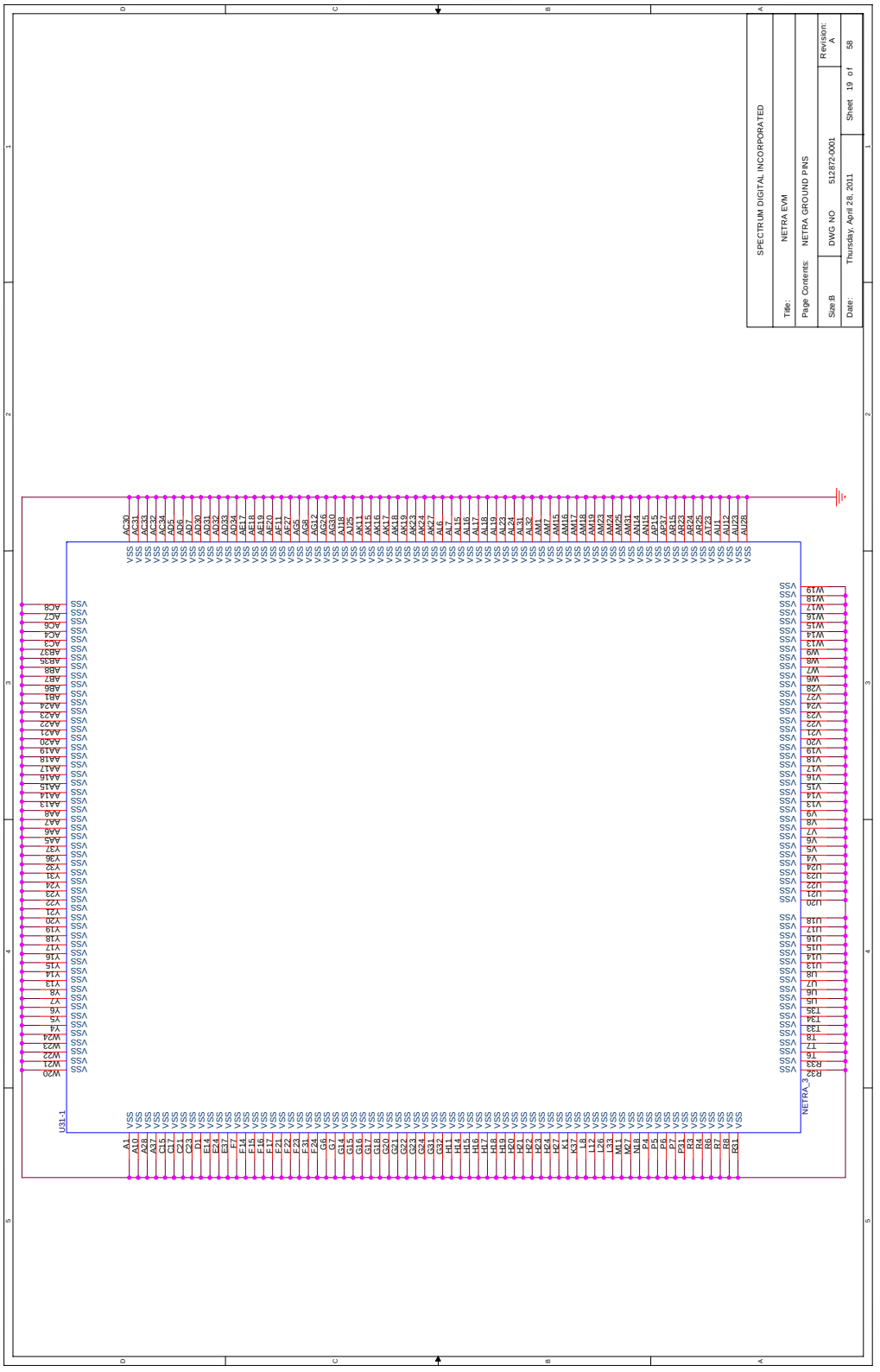
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: NETRA GROUND PINS
Size:B
DWG NO 512872-0001
Revision: A
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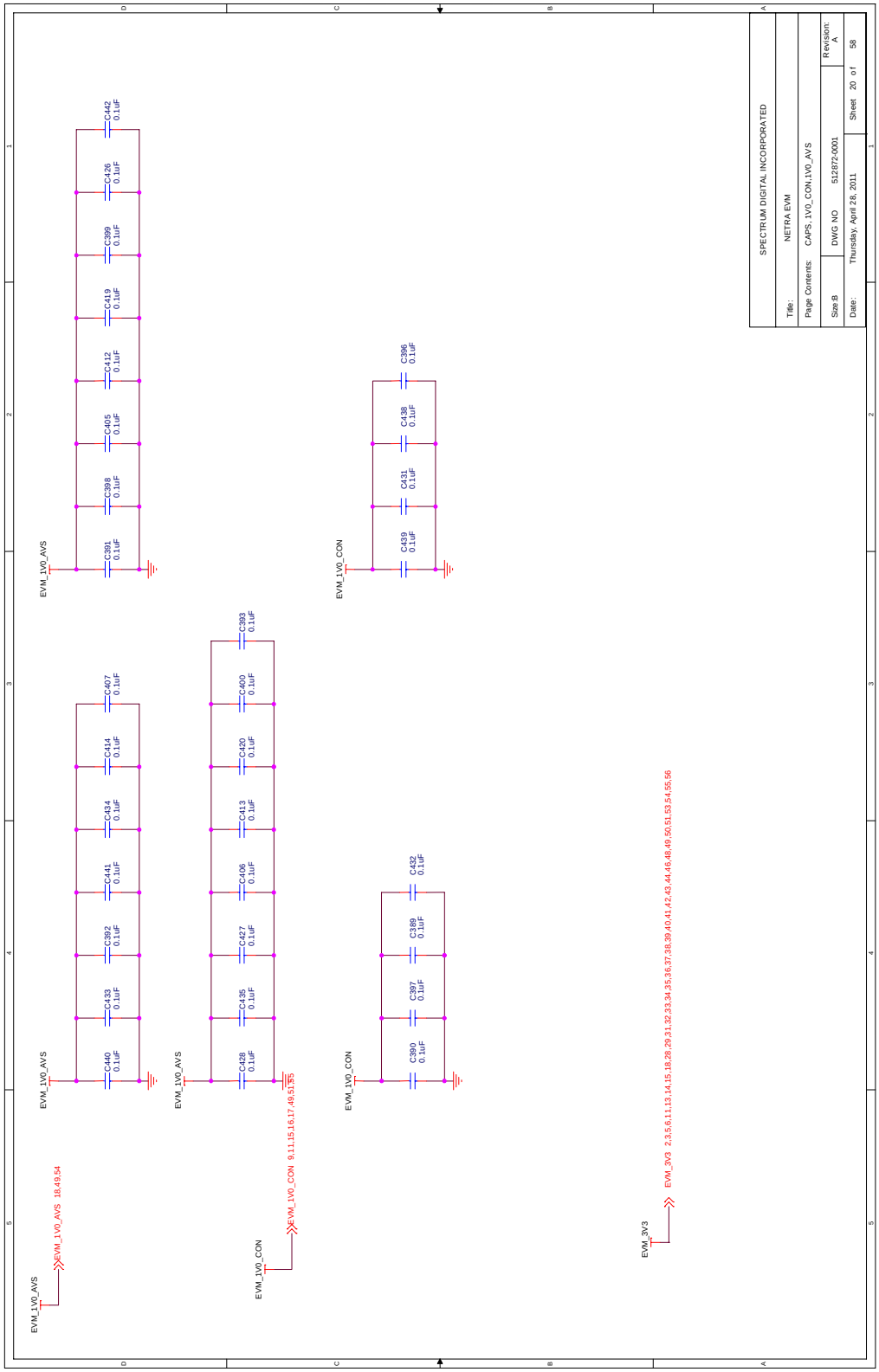
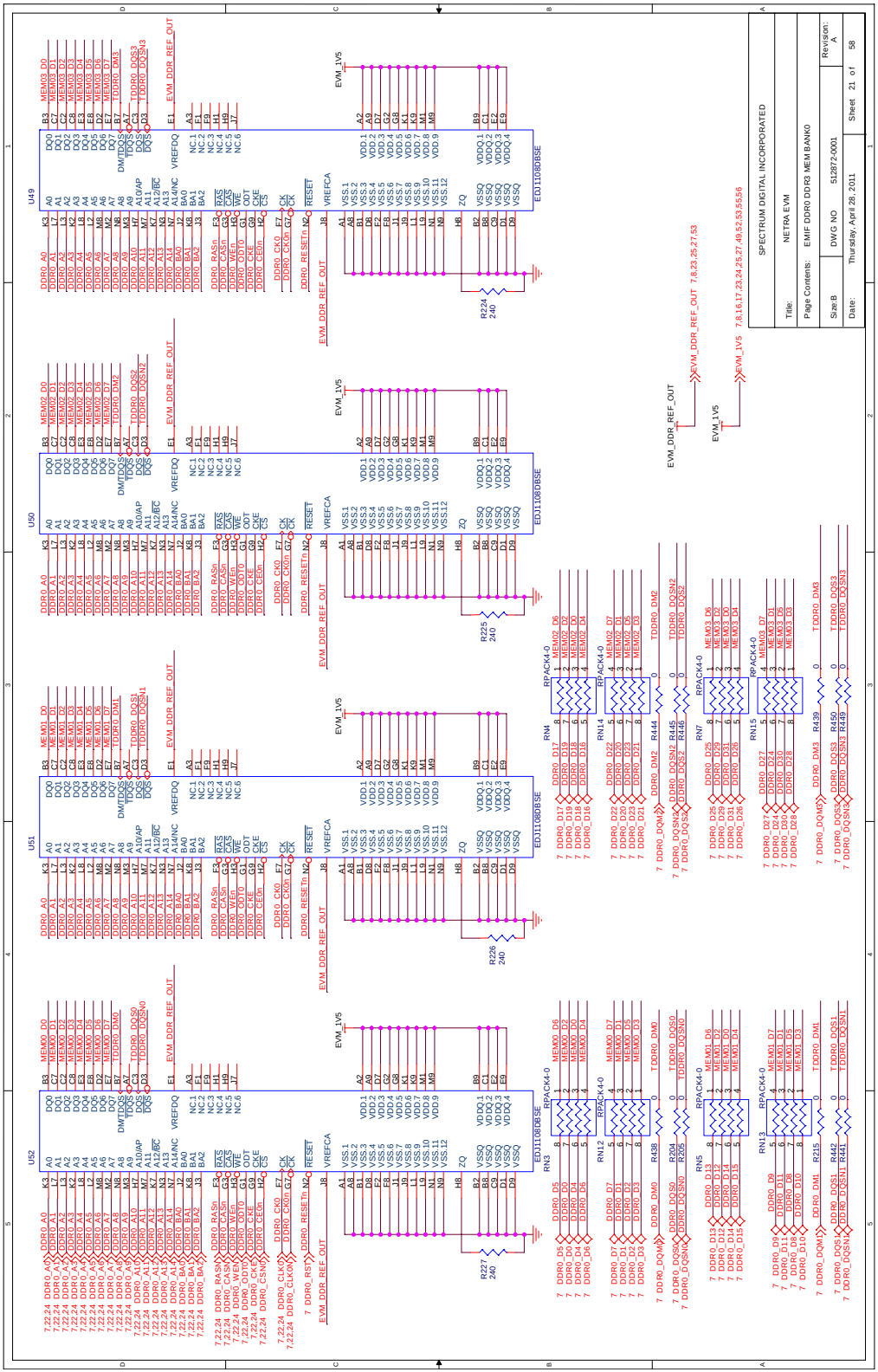
U31-1
NETRA_3


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: CAPS; 1V0_CON;1V0_AVS
Size:B DWG NO 512872-0001 Revision: A
Date: Thursday, April 28, 2011 Sheet 20 of 58
EVM_1V0_AVS
C391 0.1uF
C398 0.1uF
C405 0.1uF
C412 0.1uF
C419 0.1uF
C399 0.1uF
C426 0.1uF
C442 0.1uF
EVM_1V0_CON
C439 0.1uF
C431 0.1uF
C438 0.1uF
C396 0.1uF
EVM_1V0_AVS
C440 0.1uF
C433 0.1uF
C392 0.1uF
C441 0.1uF
C434 0.1uF
C414 0.1uF
C407 0.1uF
EVM_1V0_AVS
C428 0.1uF
C435 0.1uF
C427 0.1uF
C406 0.1uF
C413 0.1uF
C420 0.1uF
C400 0.1uF
C393 0.1uF
EVM_1V0_CON
C390 0.1uF
C397 0.1uF
C389 0.1uF
C432 0.1uF
EVM_1V0_AVS
EVM_1V0_AVS 18,49,54
EVM_1V0_CON
EVM_1V0_CON 9,11,15,16,17,49,53,55
EVM_3V3
EVM_3V3 2,3,5,6,11,13,14,15,18,28,29,31,32,33,34,35,36,37,38,39,40,41,42,43,44,46,48,49,50,51,53,54,55,56


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: EMIF DDR0 DDR3 MEM BANK0
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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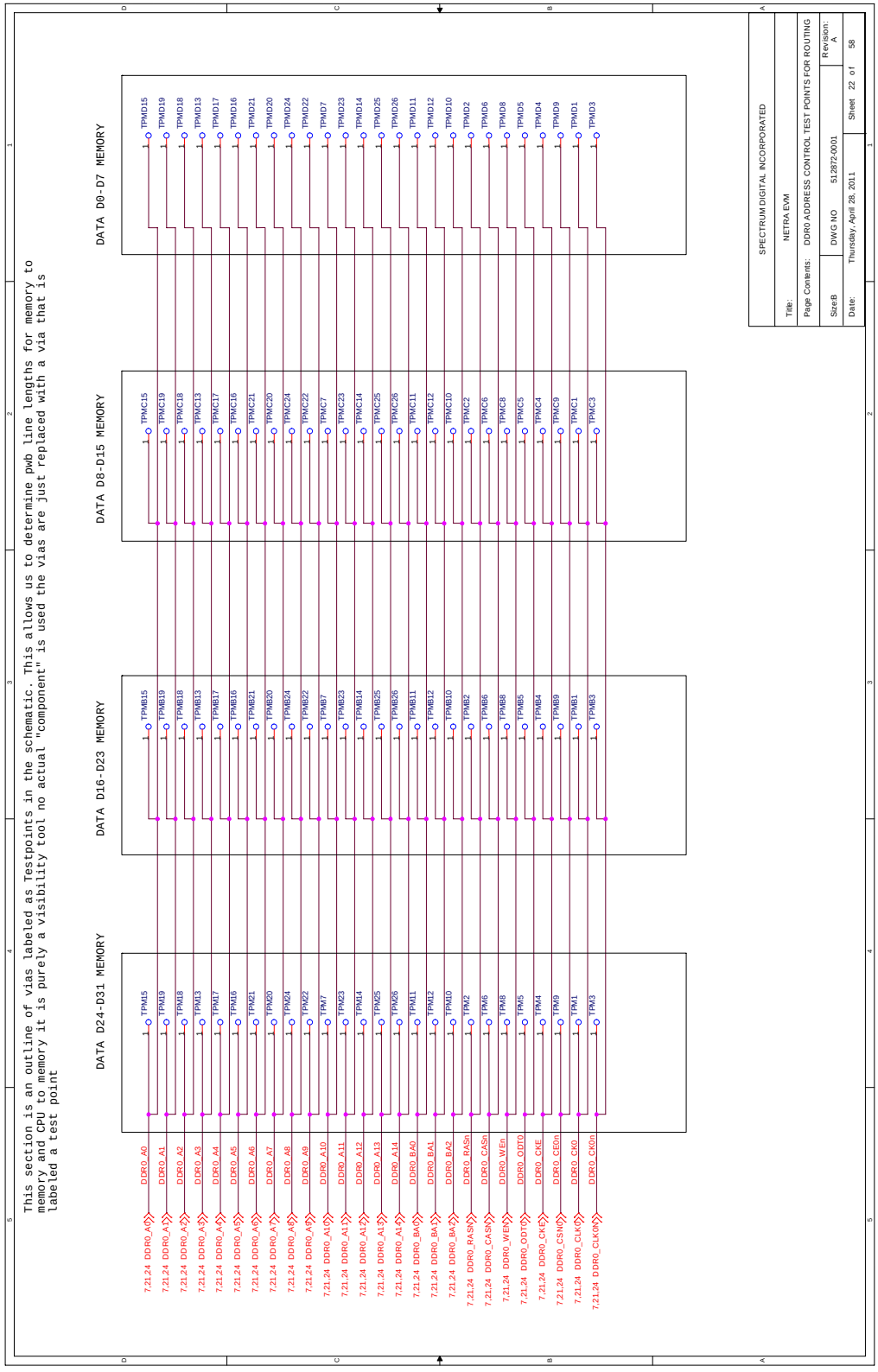
U52
U51
U50
U49
EDJ1108DBSE
EDJ1108DBSE
EDJ1108DBSE
EDJ1108DBSE
RN4
RN5
RN7
RN12
RN13
RN14
RN15
RPACK4-0
EVM_1V5
EVM_DDR_REF_OUT
RESET
VREFCA
DDR0_A0
DDR0_A1
DDR0_A2
DDR0_A3
DDR0_A4
DDR0_A5
DDR0_A6
DDR0_A7
DDR0_A8
DDR0_A9
DDR0_A10
DDR0_A11
DDR0_A12
DDR0_A13
DDR0_BA0
DDR0_BA1
DDR0_BA2
DDR0_RASn
DDR0_CASn
DDR0_WEn
DDR0_ODT0
DDR0_CKE
DDR0_CE0n
DDR0_CK0
DDR0_CK0n
DDR0_RESETn
MEM02_D0
MEM02_D1
MEM02_D2
MEM02_D3
MEM02_D4
MEM02_D5
MEM02_D6
MEM02_D7
MEM02_DM1
MEM02_DQS0
MEM02_DQS0N
MEM02_DQS1
MEM02_DQS1N
MEM01_D0
MEM01_D1
MEM01_D2
MEM01_D3
MEM01_D4
MEM01_D5
MEM01_D6
MEM01_D7
MEM01_DM0
MEM01_DQS0
MEM01_DQS0N
MEM01_DQS1
MEM01_DQS1N
MEM03_D0
MEM03_D1
MEM03_D2
MEM03_D3
MEM03_D4
MEM03_D5
MEM03_D6
MEM03_D7
MEM03_DM3
MEM03_DQS3
MEM03_DQS3N
DDR0_D5
DDR0_D0
DDR0_D4
DDR0_D6
DDR0_D13
DDR0_D12
DDR0_D14
DDR0_D15
DDR0_D9
DDR0_D11
DDR0_D8
DDR0_D10
DDR0_D7
DDR0_D1
DDR0_D2
DDR0_D3
DDR0_D17
DDR0_D19
DDR0_D18
DDR0_D16
DDR0_D22
DDR0_D20
DDR0_D23
DDR0_D21
DDR0_D25
DDR0_D31
DDR0_D28
DDR0_D26
DDR0_D27
DDR0_D24
DDR0_D30
DDR0_D29
DDR0_DM2
DDR0_DQS2N
DDR0_DQS2
DDR0_DM0
DDR0_DQS0N
DDR0_DQS0
DDR0_DM1
DDR0_DQS1N
DDR0_DQS1
DDR0_DM3
DDR0_DQS3N
DDR0_DQS3
R227 240
R226 240
R225 240
R224 240
R438
R204
R205
R215
R441
R442
R444
R445
R446
R447
R450
R448
R438
EVM_DDR_REF_OUT 7,8,23,25,27,53
EVM_1V5 7,8,16,17,23,24,25,27,49,52,53,55,56


This section is an outline of vias labeled as Testpoints in the schematic. This allows us to determine pwb line lengths for memory to memory and CPU to memory it is purely a visibility tool no actual "component" is used the vias are just replaced with a via that is labeled a test point
DATA D24-D31 MEMORY
DATA D16-D23 MEMORY
DATA D8-D15 MEMORY
DATA D0-D7 MEMORY
DDR0_A0
DDR0_A1
DDR0_A2
DDR0_A3
DDR0_A4
DDR0_A5
DDR0_A6
DDR0_A7
DDR0_A8
DDR0_A9
DDR0_A10
DDR0_A11
DDR0_A12
DDR0_A13
DDR0_A14
DDR0_BA0
DDR0_BA1
DDR0_BA2
DDR0_RASn
DDR0_CASn
DDR0_WEn
DDR0_ODT0
DDR0_CKE
DDR0_CS0n
DDR0_CK0
DDR0_CK0n
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: DDR0 ADDRESS CONTROL TEST POINTS FOR ROUTING
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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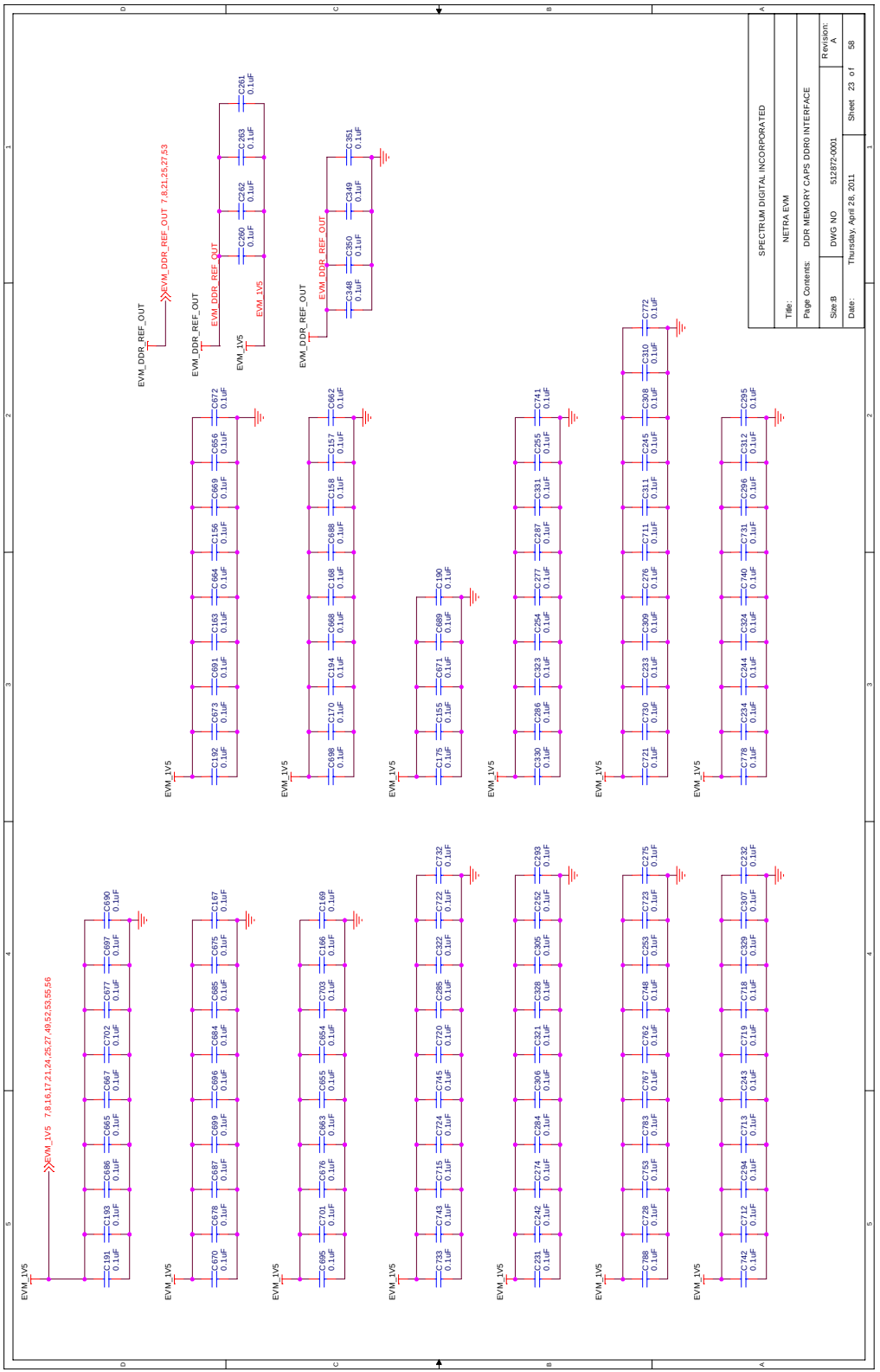
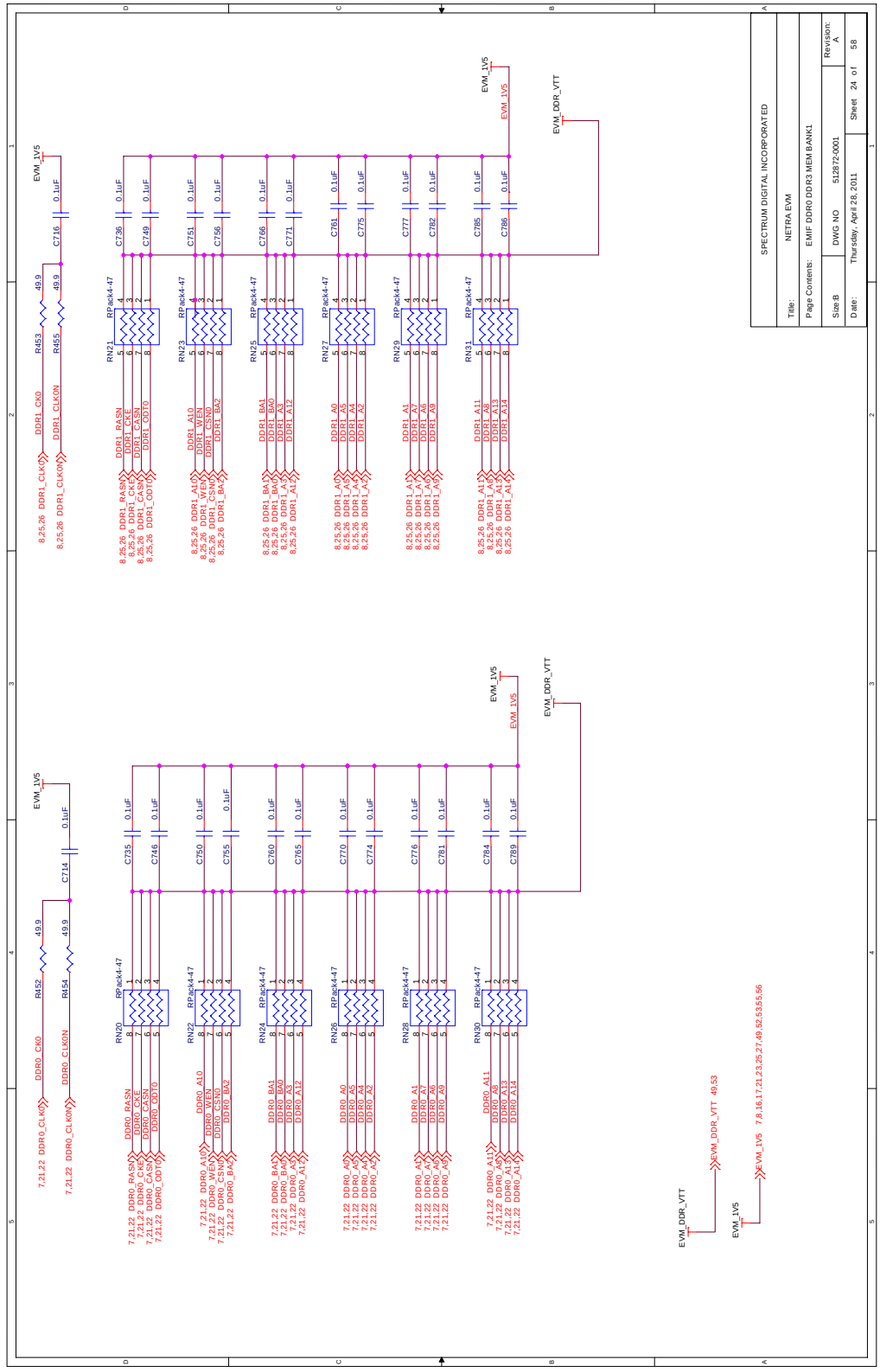
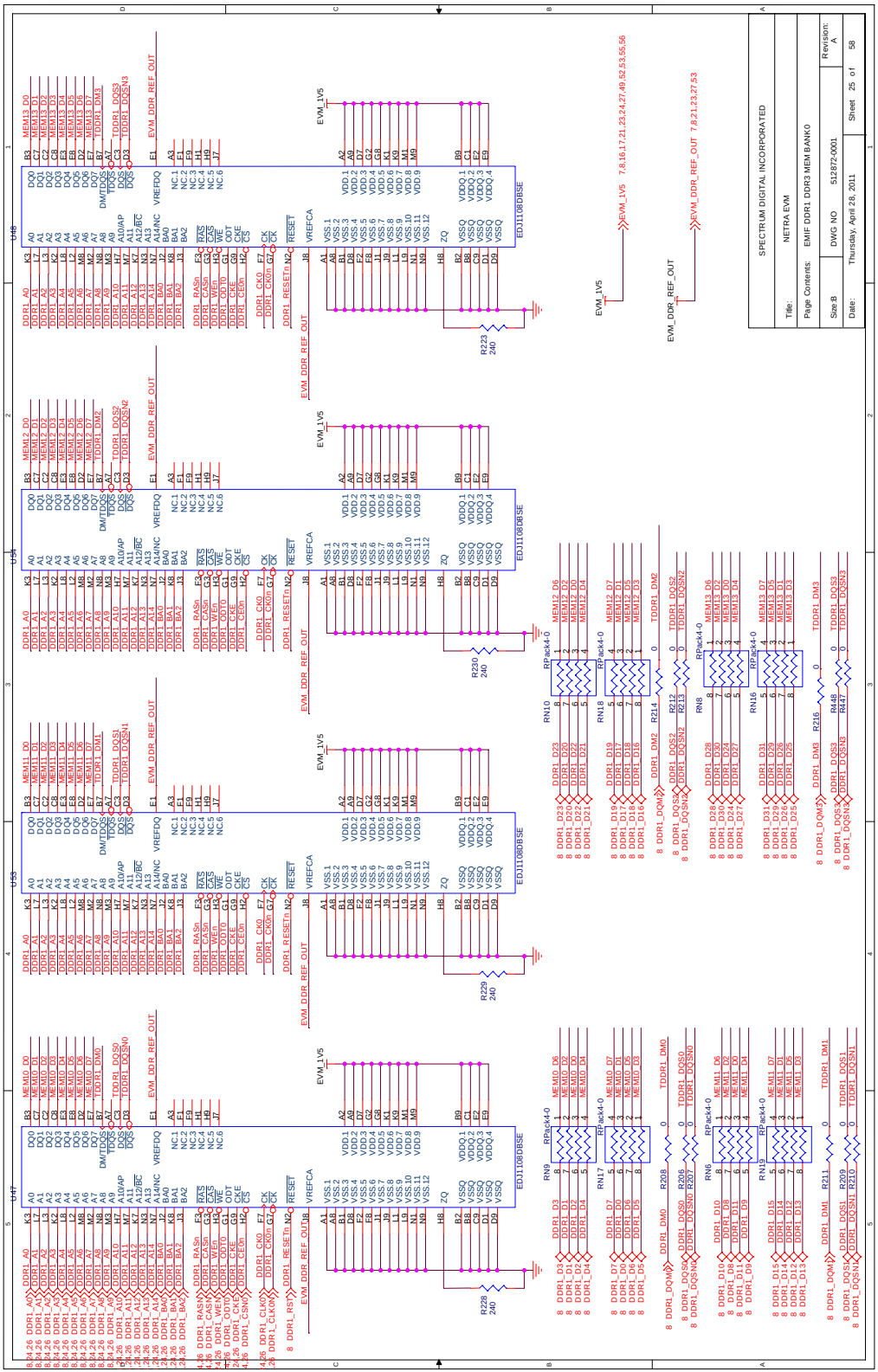
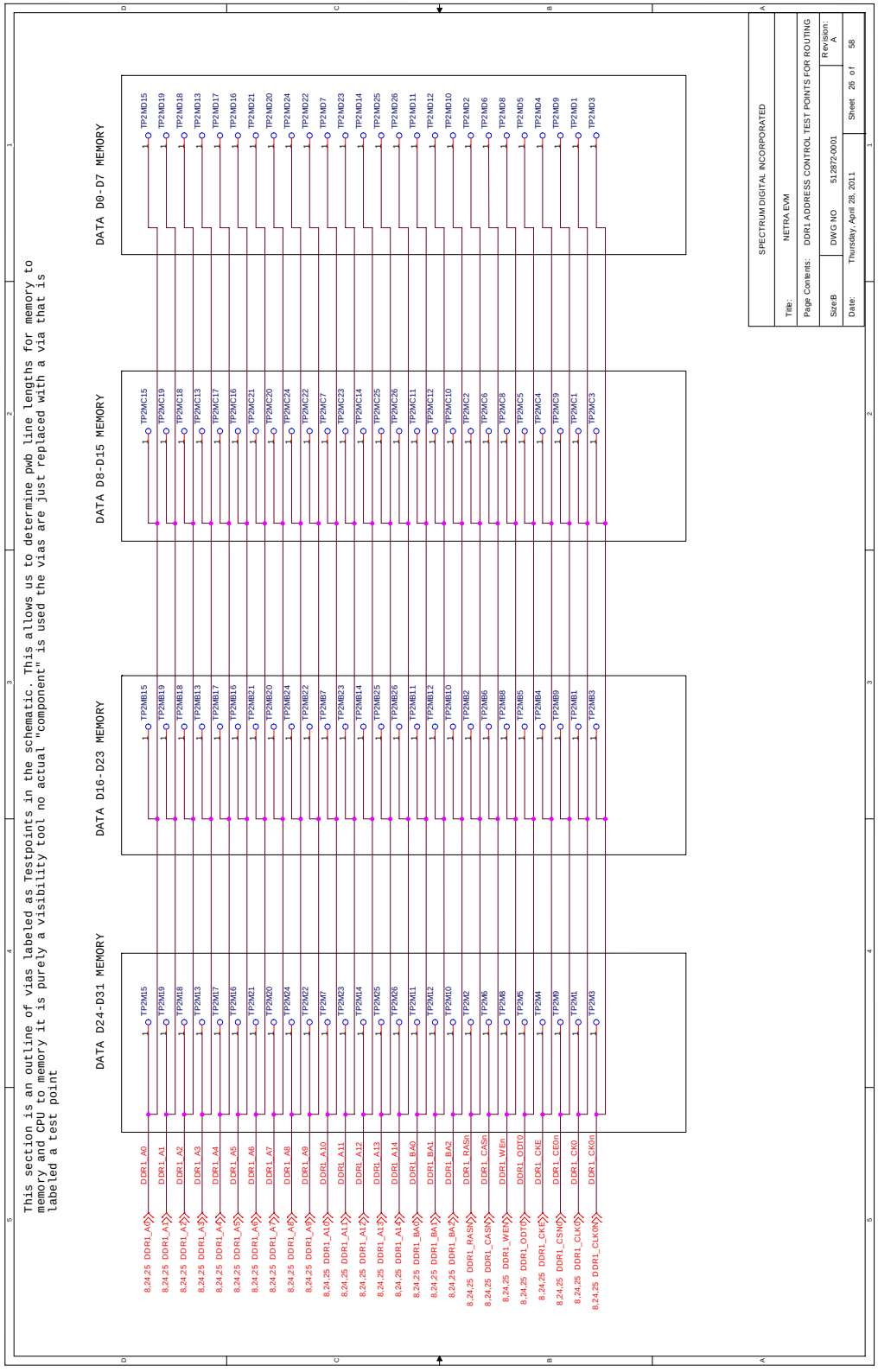

EVM_DDR_REF_OUT
EVM_DDR_REF_OUT 7,8,21,25,27,53
EVM_DDR_REF_OUT
EVM_DDR_REF_OUT
EVM_1V5
EVM_1V5
EVM_DDR_REF_OUT
EVM_DDR_REF_OUT
EVM_1V5
EVM_1V5 7,8,16,17,21,24,25,27,49,52,53,55,56
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: DDR MEMORY CAPS DDR0 INTERFACE
Size:B DWG NO 512872-0001 Revision: A
Date: Thursday, April 28, 2011 Sheet 23 of 58


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: EMIF DDR0 DDR3 MEM BANK1
Size: B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 24 of 58
EVM_1V5
EVM_DDR_VTT
DDR0_CK0
DDR0_CK0N
DDR1_CK0
DDR1_CK0N
R452
R453
R454
R455
49.9
C714
C716
0.1uF
RN20
RN21
RN22
RN23
RN24
RN25
RN26
RN27
RN28
RN29
RN30
RN31
RPack4-47
DDR0_RASN
DDR0_CKE
DDR0_CASN
DDR0_ODT0
DDR0_A10
DDR0_WEN
DDR0_CSN0
DDR0_BA2
DDR0_BA1
DDR0_BA0
DDR0_A13
DDR0_A12
DDR0_A0
DDR0_A5
DDR0_A4
DDR0_A2
DDR0_A1
DDR0_A7
DDR0_A6
DDR0_A9
DDR0_A11
DDR0_A8
DDR0_A13
DDR0_A14
DDR1_RASN
DDR1_CKE
DDR1_CASN
DDR1_ODT0
DDR1_A10
DDR1_WEN
DDR1_CSN0
DDR1_BA2
DDR1_BA1
DDR1_BA0
DDR1_A13
DDR1_A12
DDR1_A0
DDR1_A5
DDR1_A4
DDR1_A2
DDR1_A1
DDR1_A7
DDR1_A6
DDR1_A9
DDR1_A11
DDR1_A8
DDR1_A13
DDR1_A14
C735
C736
C746
C749
C750
C751
C755
C756
C760
C761
C765
C766
C770
C771
C774
C775
C776
C777
C781
C782
C784
C785
C789
C786
EVM_DDR_VTT 49.53
EVM_1V5 7,8,16,17,21,23,25,27,49,52,53,55,56




This section is an outline of vias labeled as Testpoints in the schematic. This allows us to determine pwb line lengths for memory to memory and CPU to memory it is purely a visibility tool no actual "component" is used the vias are just replaced with a via that is labeled a test point
DATA D24-D31 MEMORY
DATA D16-D23 MEMORY
DATA D8-D15 MEMORY
DATA D0-D7 MEMORY
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: DDR1 ADDRESS CONTROL TEST POINTS FOR ROUTING
Size:B
DWG NO 512872-0001
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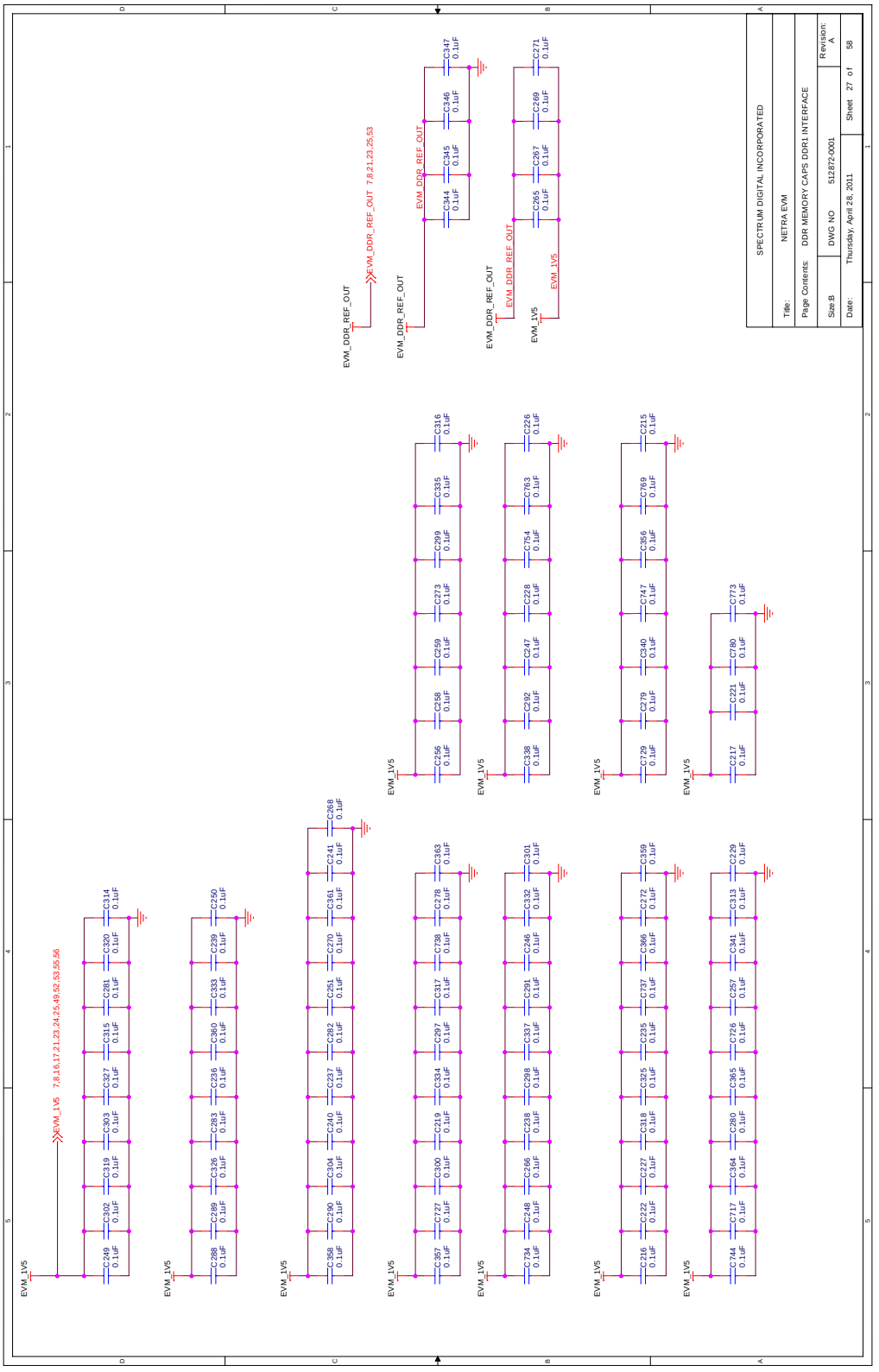
EVM_DDR_REF_OUT
EVM_DDR_REF_OUT 7,8,21,23,25,53
EVM_DDR_REF_OUT
EVM_DDR_REF_OUT
EVM_DDR_REF_OUT
EVM_1V5
EVM_1V5
EVM_1V5 7,8,16,17,21,23,24,25,49,52,53,55,56
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: DDR MEMORY CAPS DDR1 INTERFACE
Size:B DWG NO 512872-0001 Revision: A
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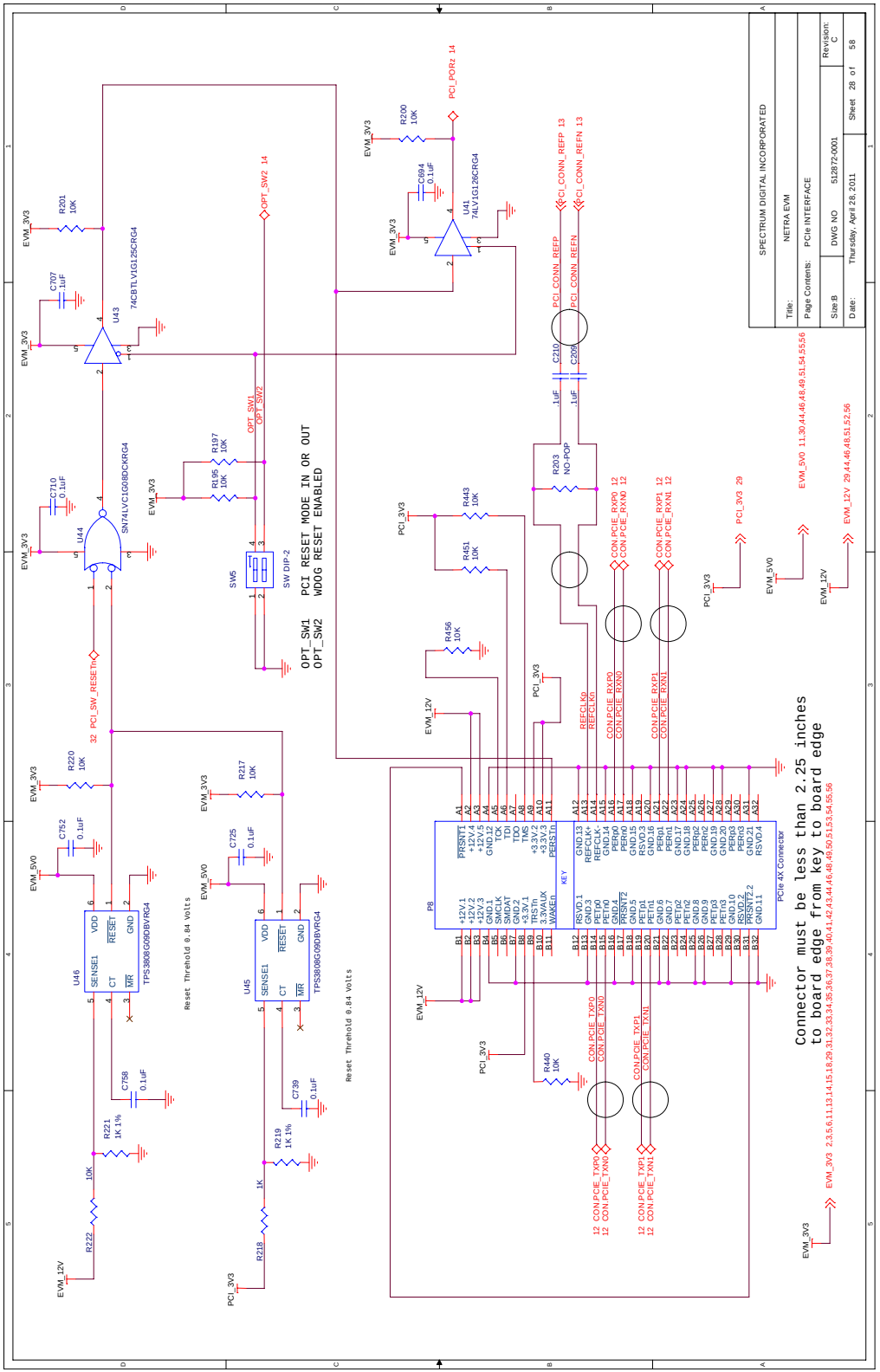
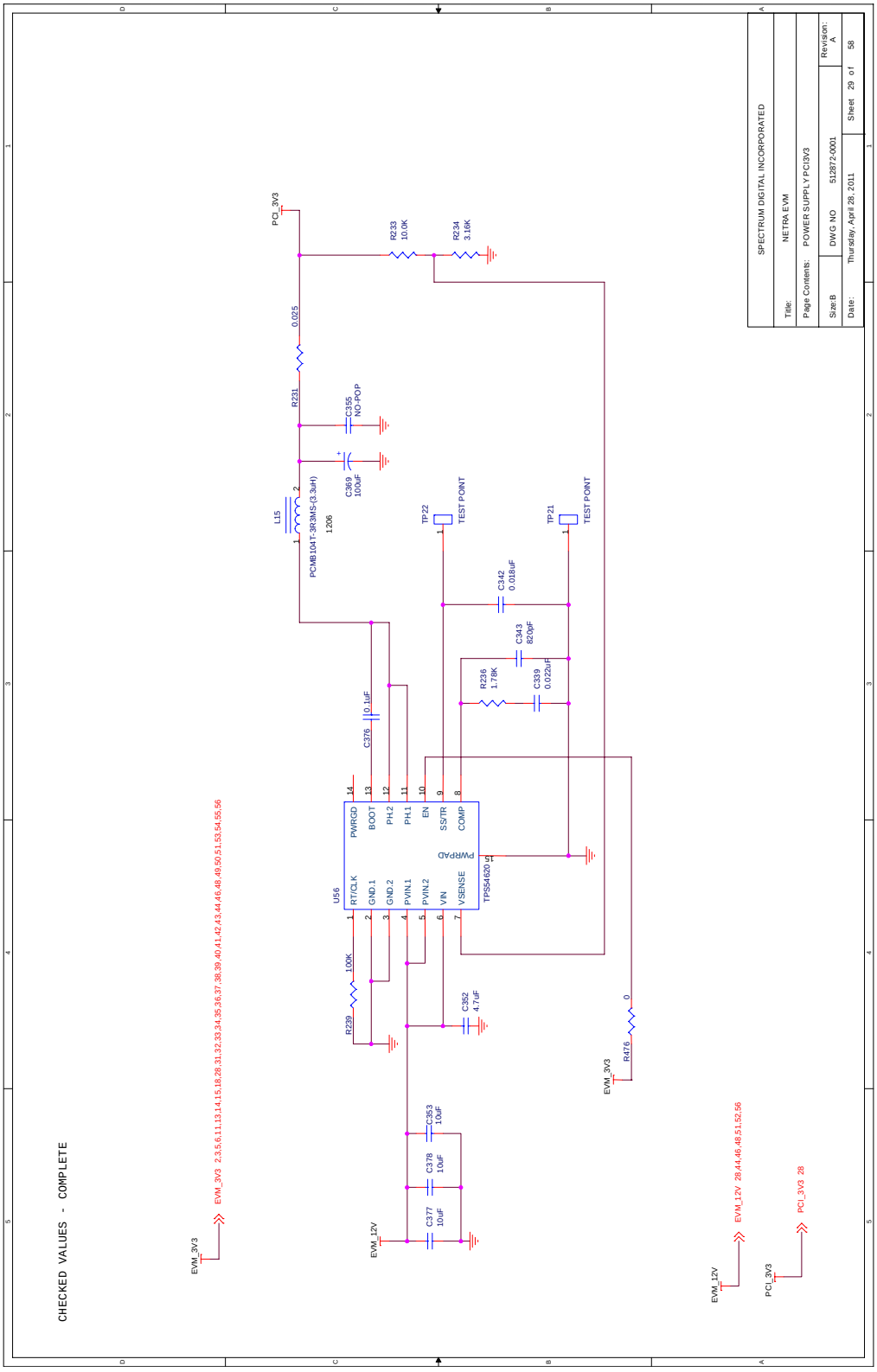
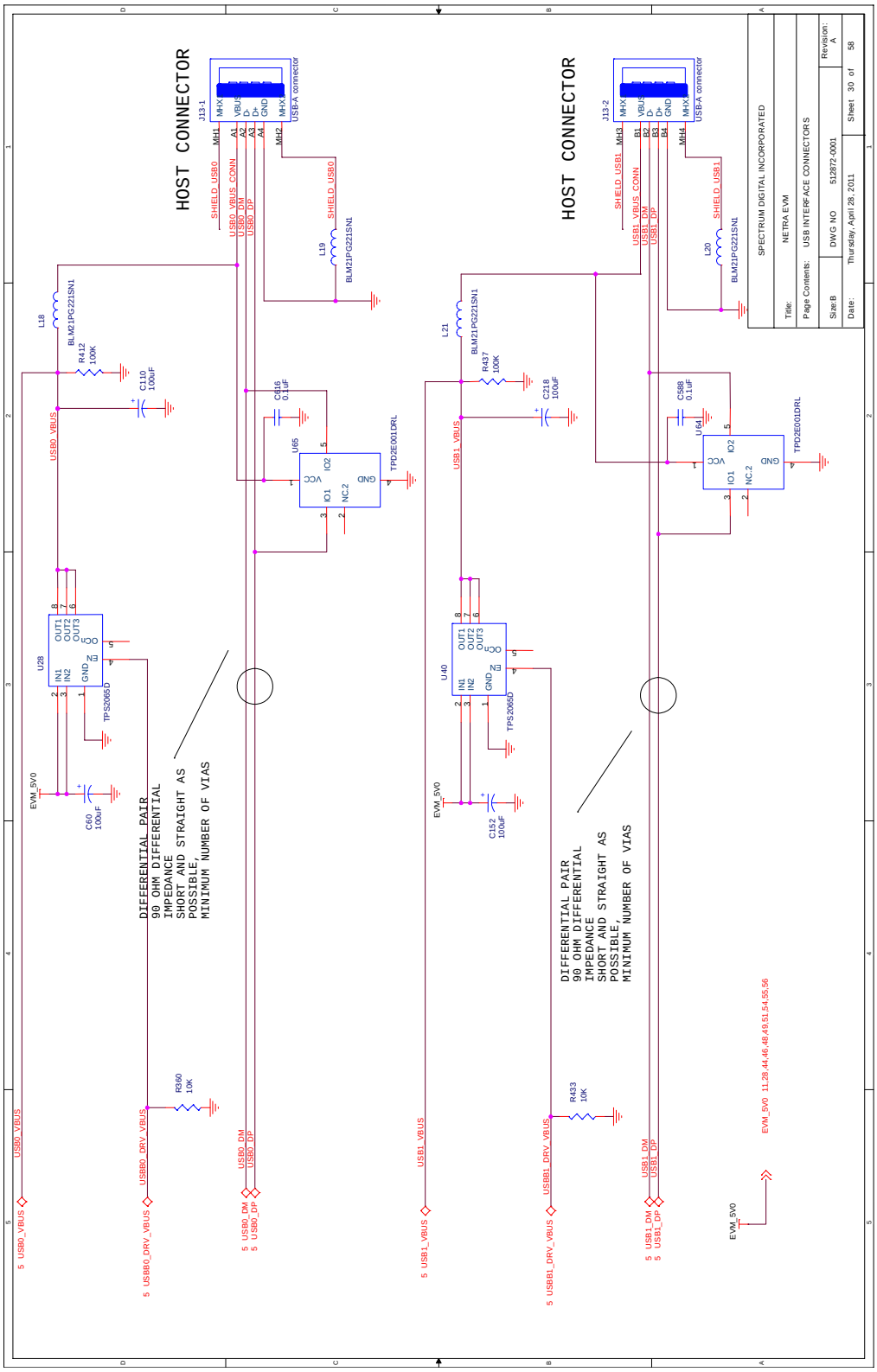
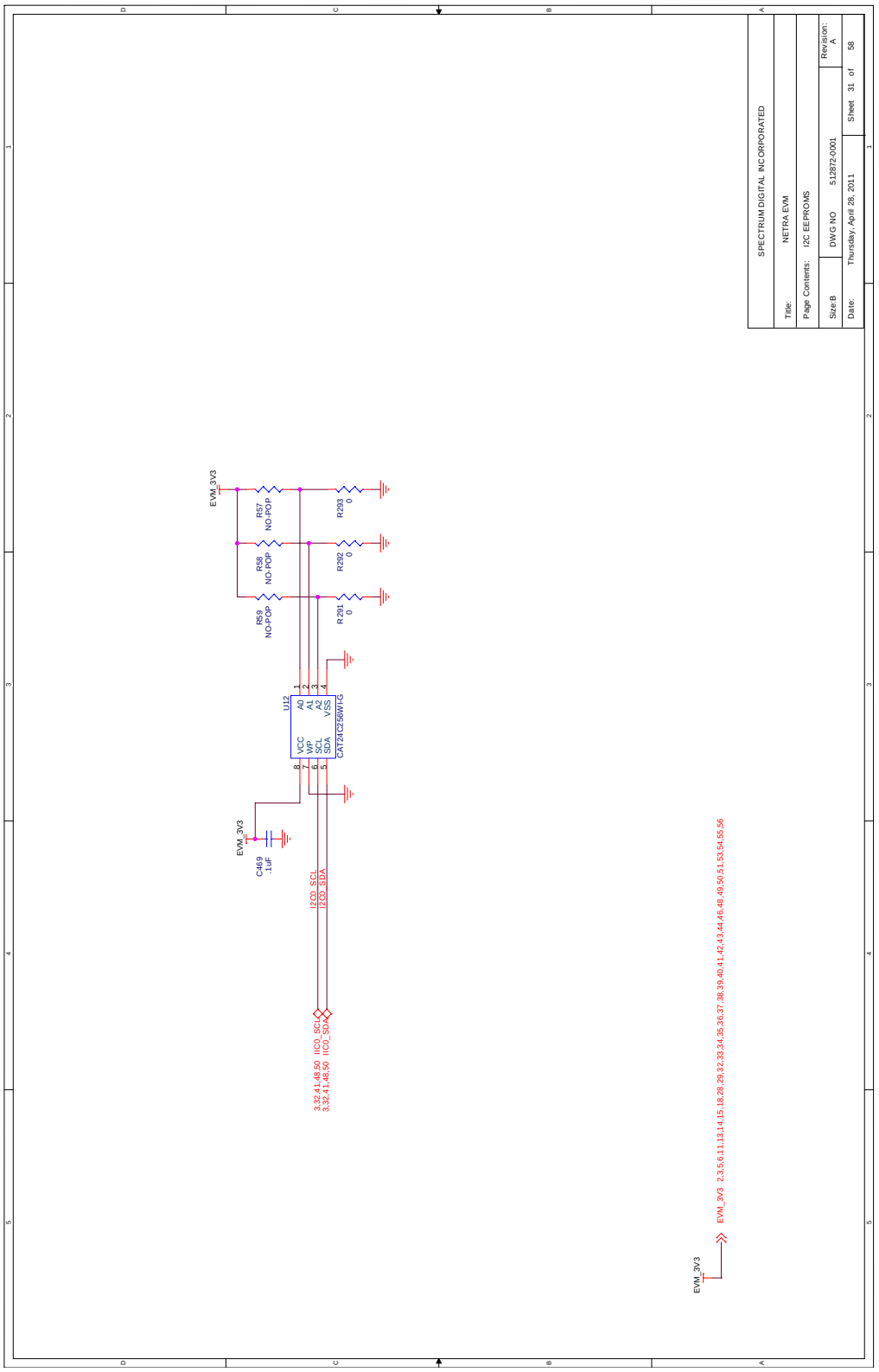
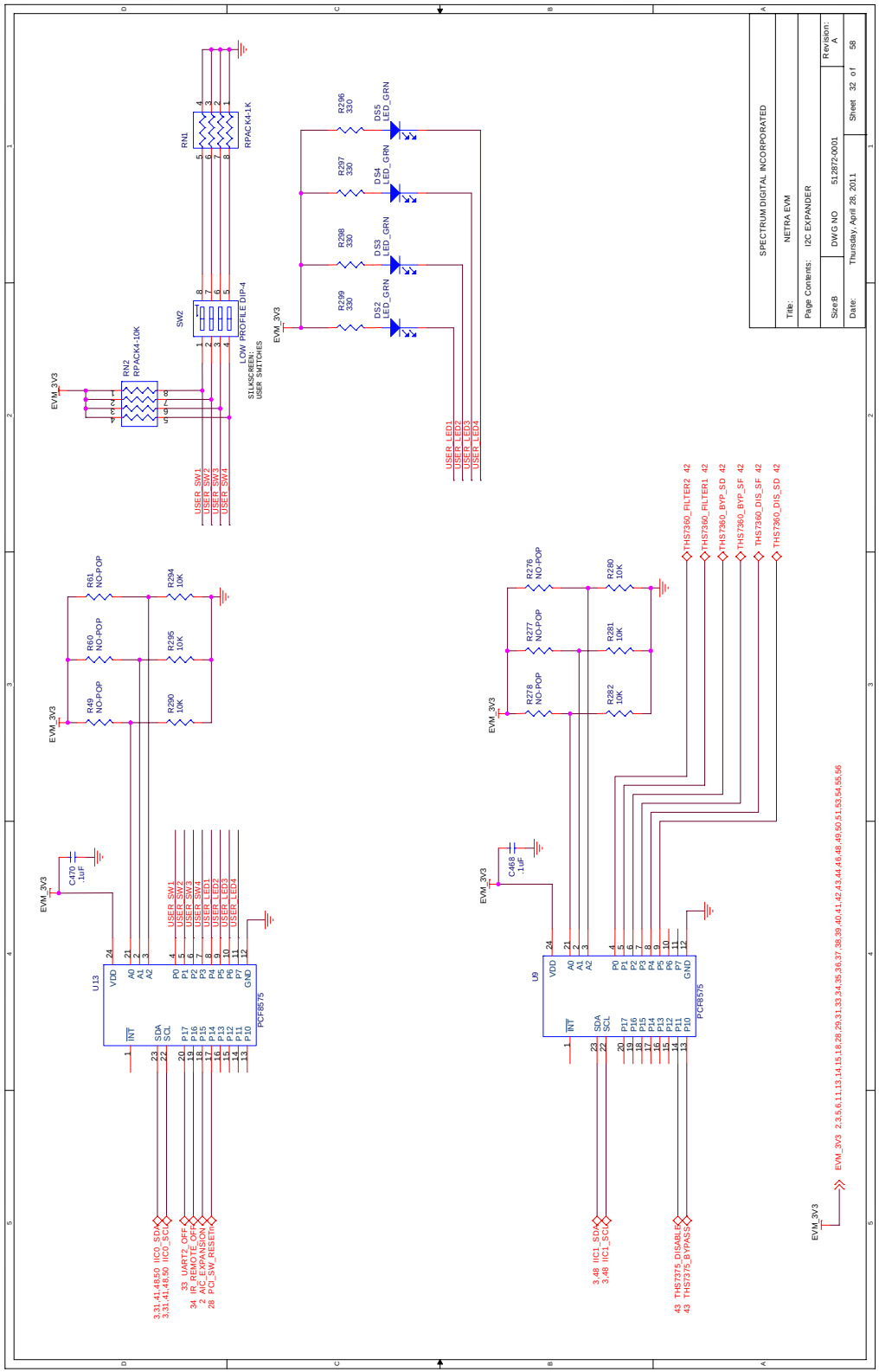
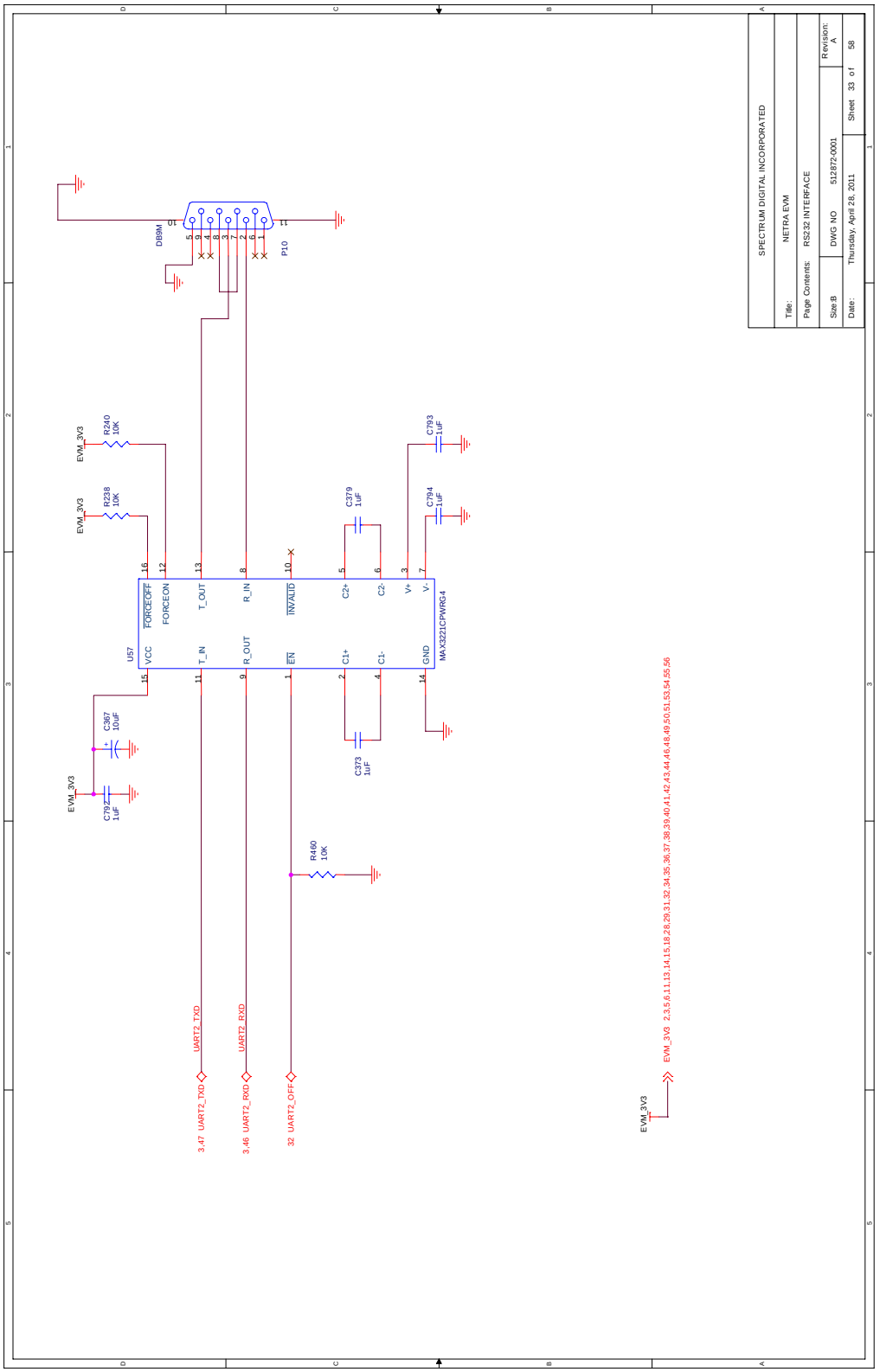

OPT_SW1 PCI RESET MODE IN OR OUT
OPT_SW2 WDOG RESET ENABLED
Connector must be less than 2.25 inches
to board edge from key to board edge
PCIe 4X Connector
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: PCIe INTERFACE
Size:B DWG NO 512872-0001 Revision: C
Date: Thursday, April 28, 2011 Sheet 28 of 58

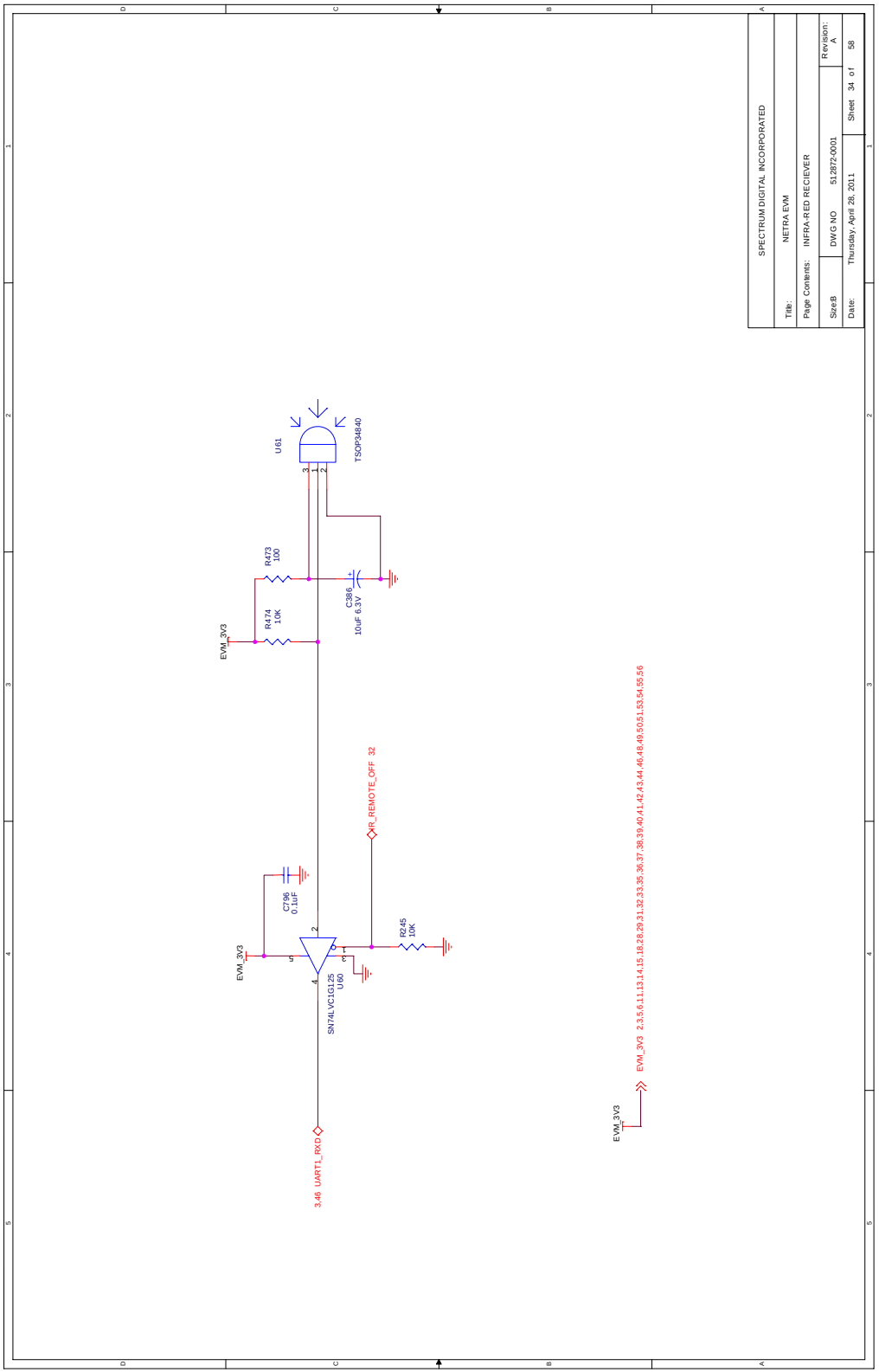

SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: POWER SUPPLY PCI3V3
Size:B DWG NO 512872-0001 Revision: A
Date: Thursday, April 28, 2011 Sheet 29 of 58
CHECKED VALUES - COMPLETE
PCI_3V3
R233 10.0K
R234 3.16K
0.025
R231
C355 NO-POP
C369 100uF
L15
PCMB104T-3R3MS-(3.3uH)
1.206
TP22 TEST POINT
TP21 TEST POINT
C342 0.018uF
C343 820pF
R236 1.78K
C339 0.022uF
C376 0.1uF
U56
TPS54620
PWRGD
BOOT
PH.2
PH.1
EN
SS/TR
COMP
PWRPAD
RT/CLK
GND.1
GND.2
PVIN.1
PVIN.2
VIN
VSENSE
R239 100K
C352 4.7uF
R476 0
EVM_3V3
C353 10uF
C378 10uF
C377 10uF
EVM_12V
EVM_3V3 2,3,5,6,11,13,14,15,18,28,31,32,33,34,35,36,37,38,39,40,41,42,43,44,46,48,49,50,51,53,54,55,56
EVM_12V 28,44,46,48,51,52,56
PCI_3V3 28


HOST CONNECTOR
J13-1
USB-A connector
SHIELD_USB0
USB0_VBUS_CONN
USB0_DM
USB0_DP
L18
BLM21PG221SN1
R412
100K
C110
100uF
L19
BLM21PG221SN1
C616
0.1uF
U65
TPD2E001DRL
U28
TPS2065D
C60
100uF
EVM_5V0
USB0_VBUS
USB0_DRV_VBUS
R360
10K
USB0_DM
USB0_DP
DIFFERENTIAL PAIR
90 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS
HOST CONNECTOR
J13-2
USB-A connector
SHIELD_USB1
USB1_VBUS_CONN
USB1_DM
USB1_DP
L21
BLM21PG221SN1
R437
100K
C218
100uF
L20
BLM21PG221SN1
C588
0.1uF
U64
TPD2E001DRL
U40
TPS2065D
C152
100uF
EVM_5V0
USB1_VBUS
USB1_DRV_VBUS
R433
10K
USB1_DM
USB1_DP
DIFFERENTIAL PAIR
90 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: USB INTERFACE CONNECTORS
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 30 of 58


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: I2C EEPROMS
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 31 of 58
EVM_3V3
R57 NO-POP
R58 NO-POP
R59 NO-POP
R293 0
R292 0
R 291 0
U12
A0
A1
A2
VSS
VCC
WP
SCL
SDA
CAT24C256WI-G
C469 .1uF
I2C0_SCL
I2C0_SDA
3,32,41,48,50 IIC0_SCL
3,32,41,48,50 IIC0_SDA
EVM_3V3 2,3,5,6,11,13,14,15,18,28,29,32,33,34,35,36,37,38,39,40,41,42,43,44,46,48,49,50,51,53,54,55,56
EVM_3V3


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: I2C EXPANDER
Size:B
DWG NO 5128272-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 32 of 58
RN1 RPACK4-1K
RN2 RPACK4-10K
SW2 LOW PROFILE DIP-4
SW1 SILKSCREEN: USER SWITCHES
DS2 LED_GRN
DS3 LED_GRN
DS4 LED_GRN
DS5 LED_GRN
R296 330
R297 330
R298 330
R299 330
USER_LED1
USER_LED2
USER_LED3
USER_LED4
USER_SW1
USER_SW2
USER_SW3
USER_SW4
U13 PCF8575
U9 PCF8575
R61 NO-POP
R60 NO-POP
R49 NO-POP
R294 10K
R295 10K
R290 10K
R276 NO-POP
R277 NO-POP
R278 NO-POP
R280 10K
R281 10K
R282 10K
C470 .1uF
C468 .1uF
EVM_3V3
THS7360_FILTER2 42
THS7360_FILTER1 42
THS7360_BYP_SD 42
THS7360_BYP_SF 42
THS7360_DIS_SF 42
THS7360_DIS_SD 42
3,31,41,48,50 I2C0_SDA
3,31,41,48,50 I2C0_SCL
30 UART2_OFF
34 IR_REMOTE_OFF
2 AIC_EXPANSION
28 PCI_SW_RESET#
3,48 I2C1_SDA
3,48 I2C1_SCL
43 THS7375_DISABLE
43 THS7375_BYPASS
EVM_3V3 2,3,5,6,11,13,14,15,18,28,29,31,33,34,35,36,37,38,39,40,41,42,43,44,46,48,49,50,51,53,54,55,56


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: RS232 INTERFACE
Size:B DWG NO 512872-0001 Revision: A
Date: Thursday, April 28, 2011 Sheet 33 of 58
DB9M
P10
U57
MAX3221CPWRG4
FORCEOFF
FORCEON
T_OUT
R_IN
INVALID
C2+
C2-
V+
V-
VCC
T_IN
R_OUT
EN
C1+
C1-
GND
R240 10K
R238 10K
R460 10K
C367 10uF
C379 1uF
C373 1uF
C793 1uF
C794 1uF
C792 1uF
EVM_3V3
UART2_TXD
UART2_RXD
UART2_OFF
3,47 UART2_TXD
3,46 UART2_RXD
32 UART2_OFF
EVM_3V3 2,3,5,6,11,13,14,15,18,28,29,31,32,34,35,36,37,38,39,40,41,42,43,44,46,48,49,50,51,53,54,55,56


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: INFRA-RED RECIEVER
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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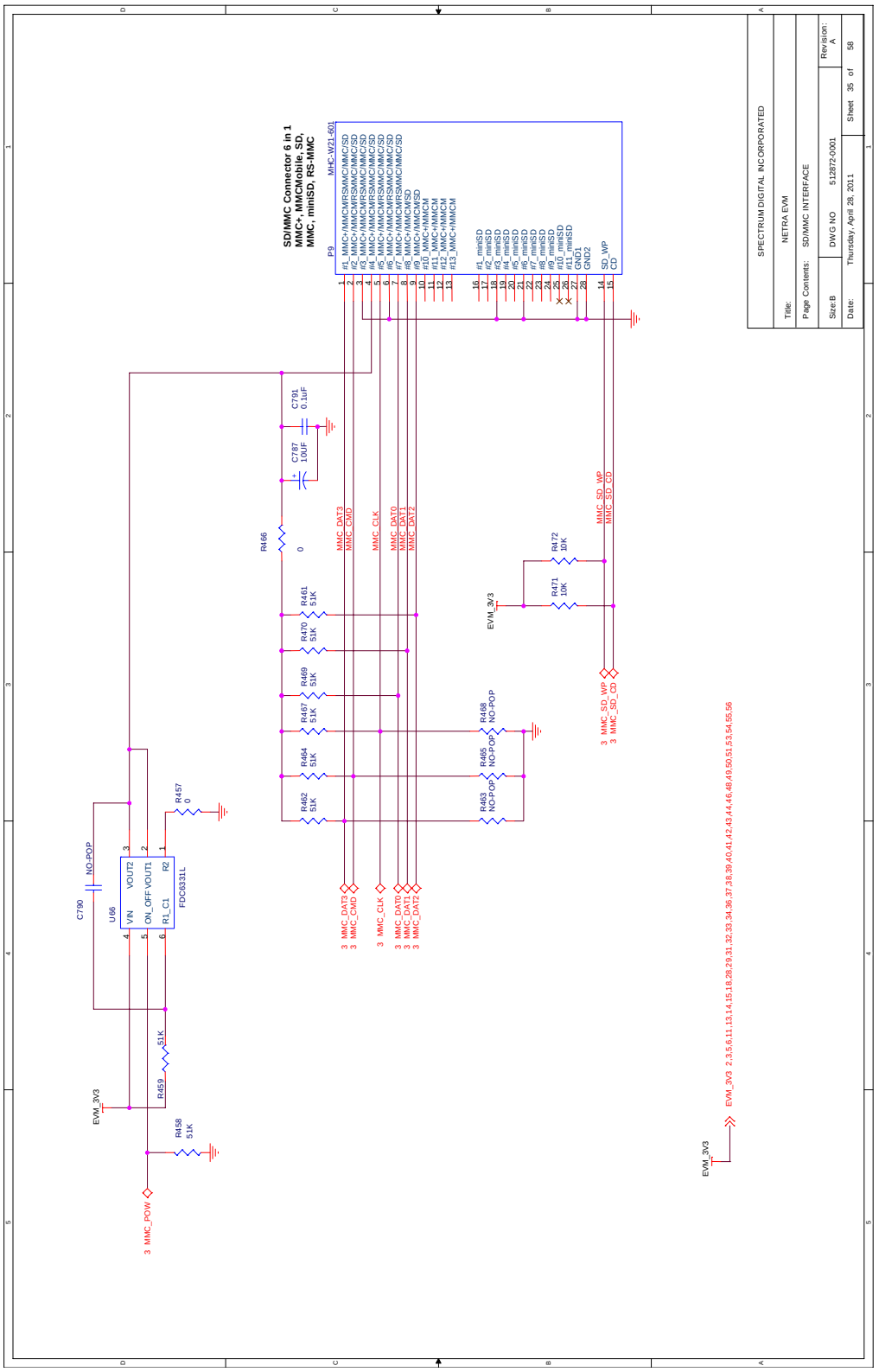
U61
TSOP34840
R473
100
C386
10uF 6.3V
R474
10K
EVM_3V3
C796
0.1uF
IR_REMOTE_OFF 32
R245
10K
SN74LVC1G125
U60
3.46 UART1_RXD
EVM_3V3 2,3,5,6,11,13,14,15,18,28,29,31,32,33,35,36,37,38,39,40,41,42,43,44,46,48,49,50,51,53,54,55,56
EVM_3V3


SD/MMC Connector 6 in 1
MMC+, MMCMobile, SD,
MMC, miniSD, RS-MMC
P9
MHC-W21-601
C791
0.1uF
C787
10UF
R466
0
R461 51K
R470 51K
R469 51K
R467 51K
R464 51K
R462 51K
R468 NO-POP
R465 NO-POP
R463 NO-POP
R472 10K
R471 10K
EVM_3V3
MMC_DAT3
MMC_CMD
MMC_CLK
MMC_DAT0
MMC_DAT1
MMC_DAT2
MMC_SD_WP
MMC_SD_CD
C790
NO-POP
U66
FDC6331L
R457 0
R459 51K
R458 51K
MMC_POW
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: SD/MMC INTERFACE
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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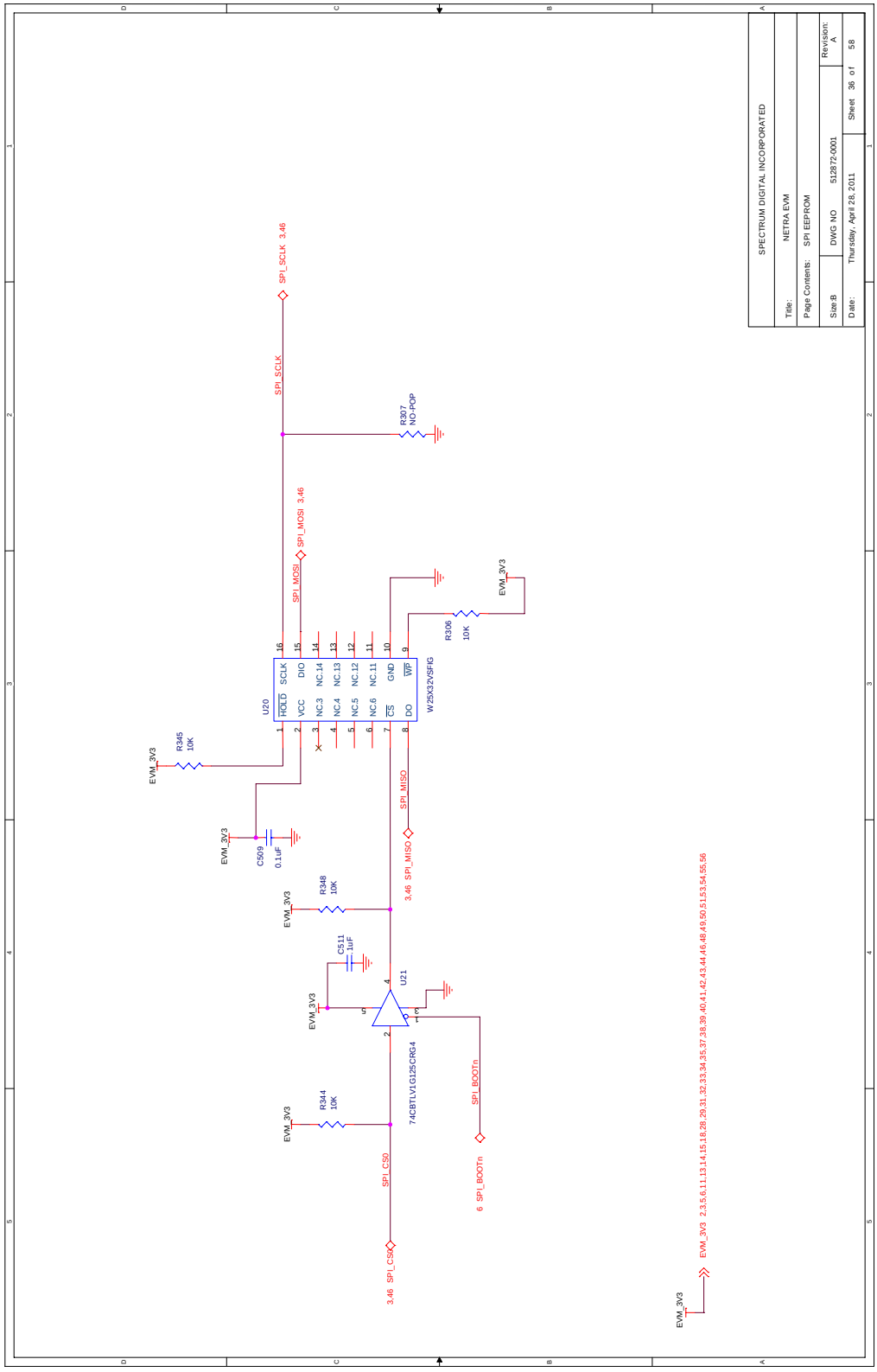
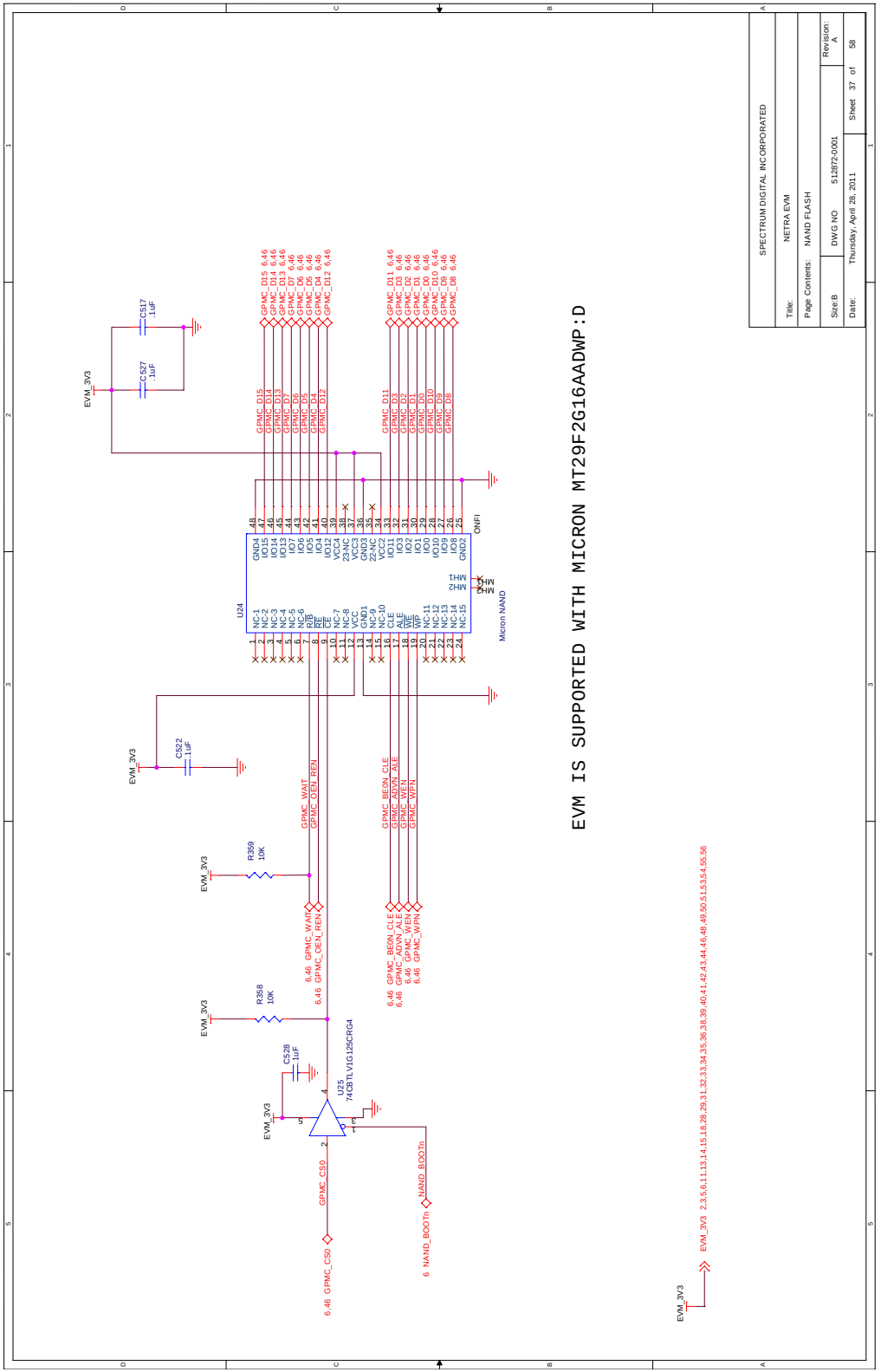
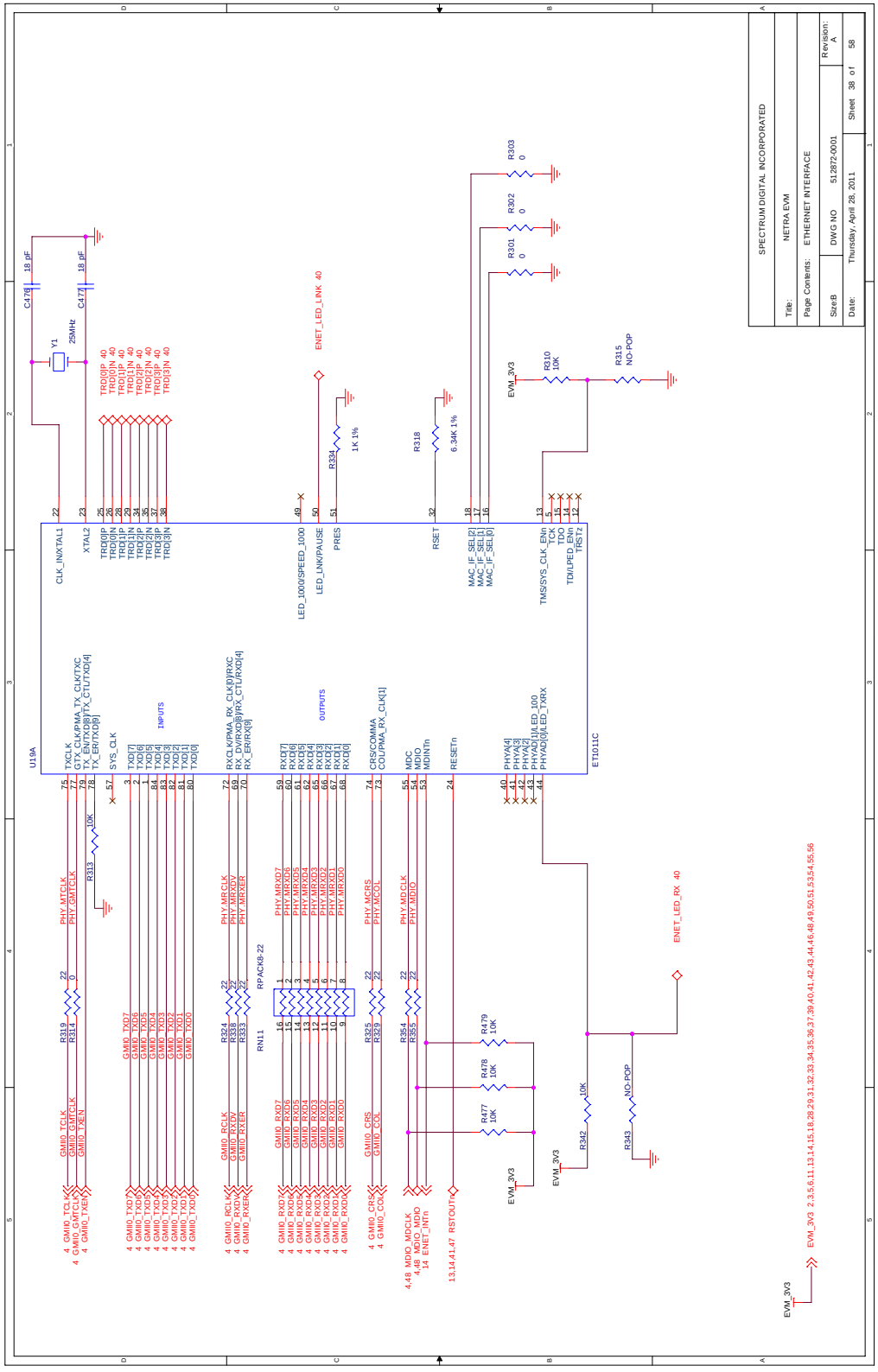

SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: SPI EEPROM
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 36 of 58
SPI_SCLK 3.46
SPI_SCLK
R307 NO-POP
SPI_MOSI 3.46
SPI_MOSI
EVM_3V3
R306 10K
U20
HOLD SCLK DIO VCC NC.3 NC.4 NC.5 NC.6 CS DO NC.11 NC.12 NC.13 NC.14 GND WP
W25X32VSFIG
R345 10K
C509 0.1uF
SPI_MISO
3.46 SPI_MISO
R348 10K
C511 1uF
U21
74CBTLV1G125CRG4
R344 10K
SPI_BOOTn
6 SPI_BOOTn
SPI_CS0
3.46 SPI_CS0
EVM_3V3 2,3,5,6,11,13,14,15,18,28,29,31,32,33,34,35,37,38,39,40,41,42,43,44,46,48,49,50,51,53,54,55,56


EVM IS SUPPORTED WITH MICRON MT29F2G16AADWP:D
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: NAND FLASH
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 37 of 58
U24
Micron NAND
ONFI
U25
74CBTLV1G125CRG4
C517 .1uF
C527 .1uF
C522 .1uF
C528 .1uF
R359 10K
R358 10K
EVM_3V3
GPMC_WAIT
GPMC_OEN_REN
GPMC_BEON_CLE
GPMC_ADVN_ALE
GPMC_WEN
GPMC_WPN
GPMC_CS0
NAND_BOOTn


SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: ETHERNET INTERFACE
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
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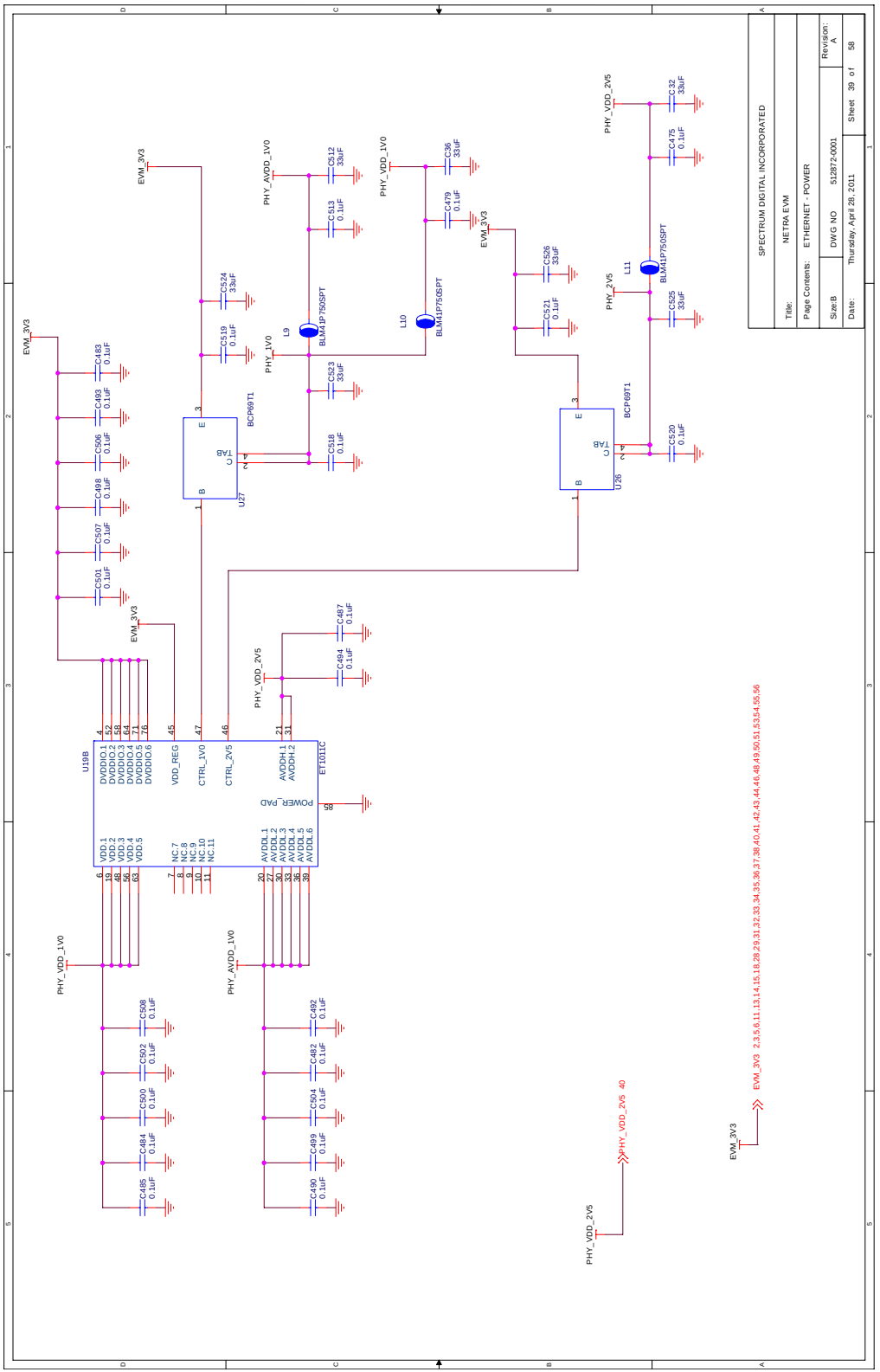
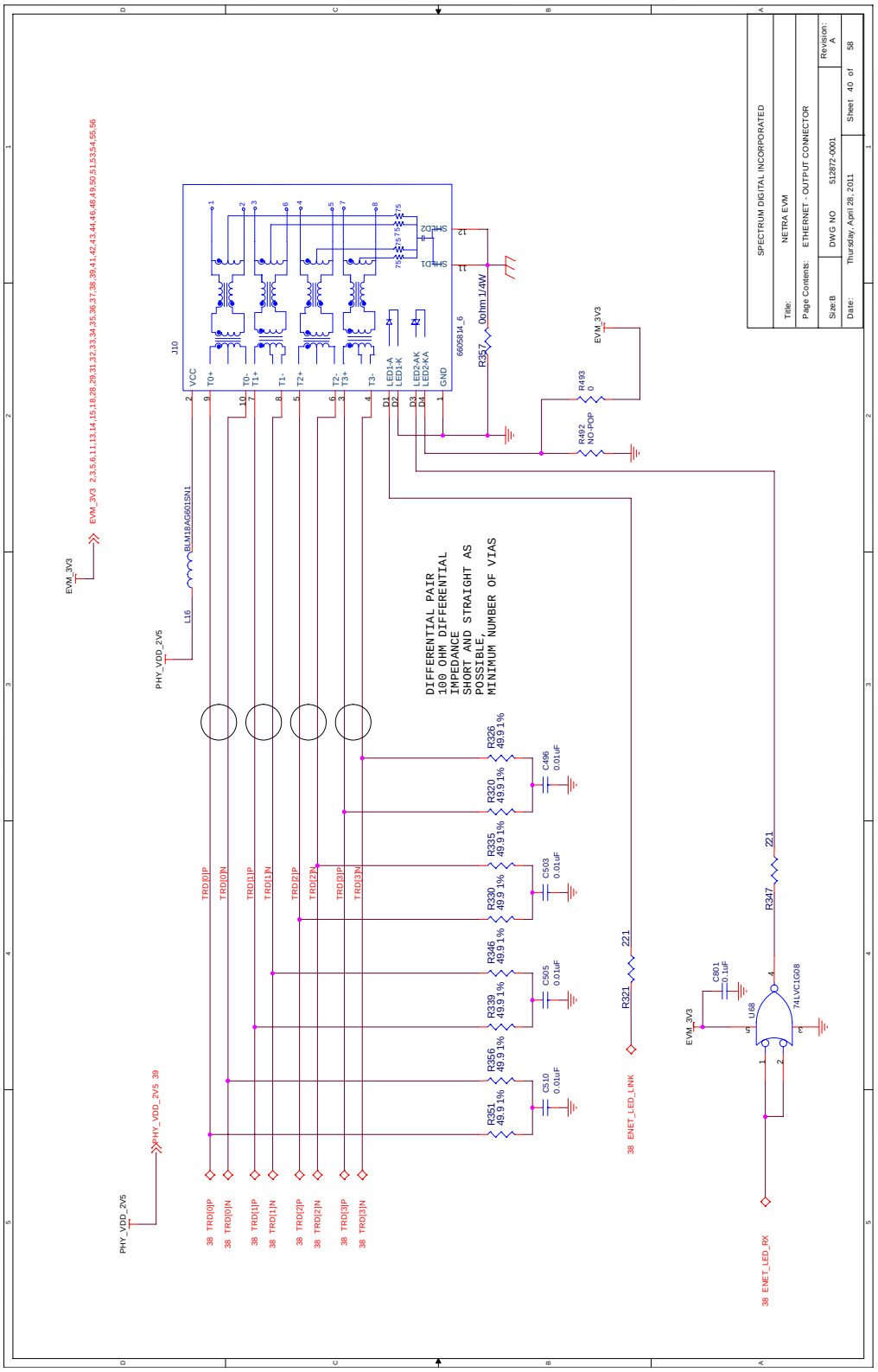
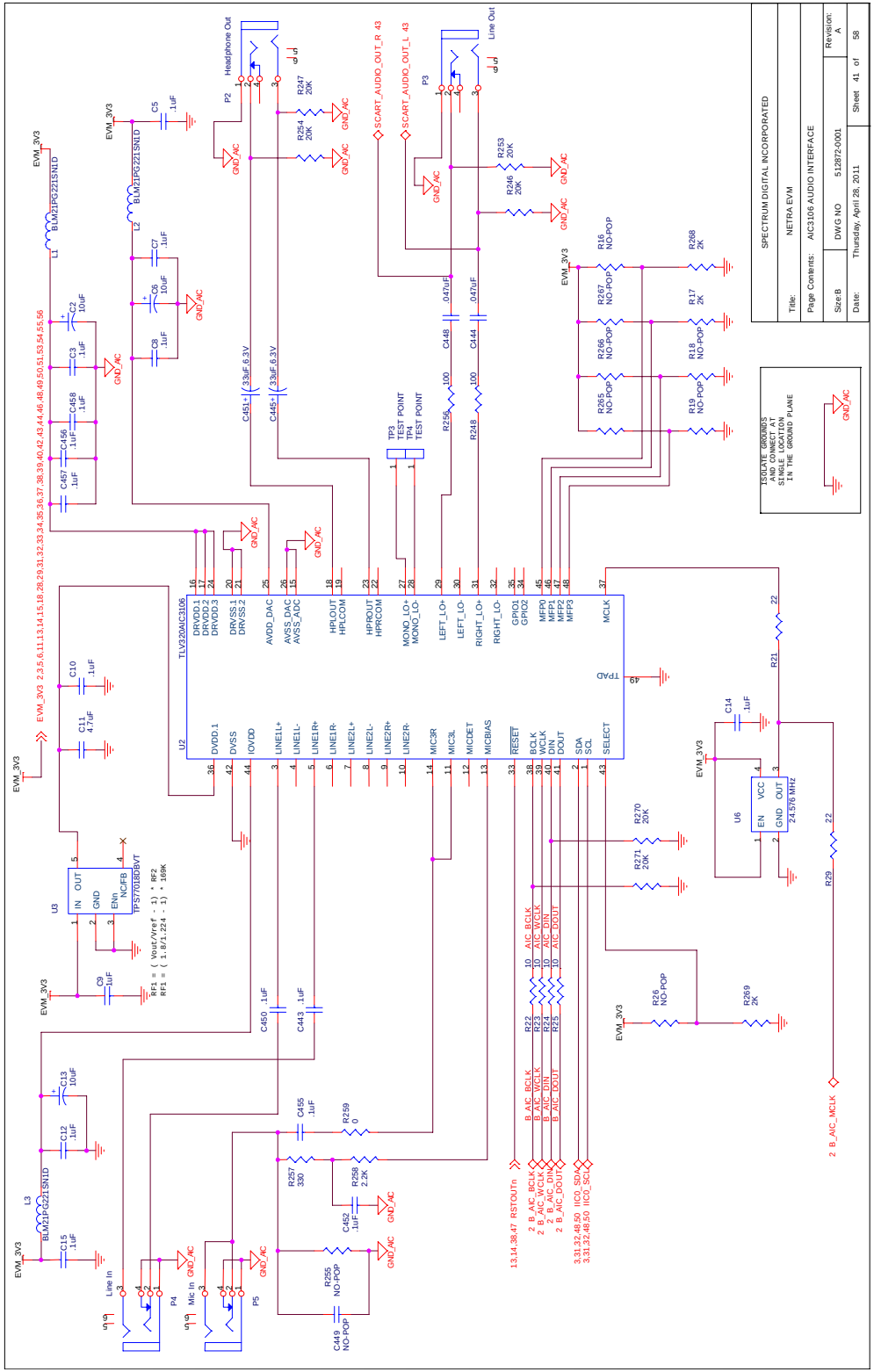
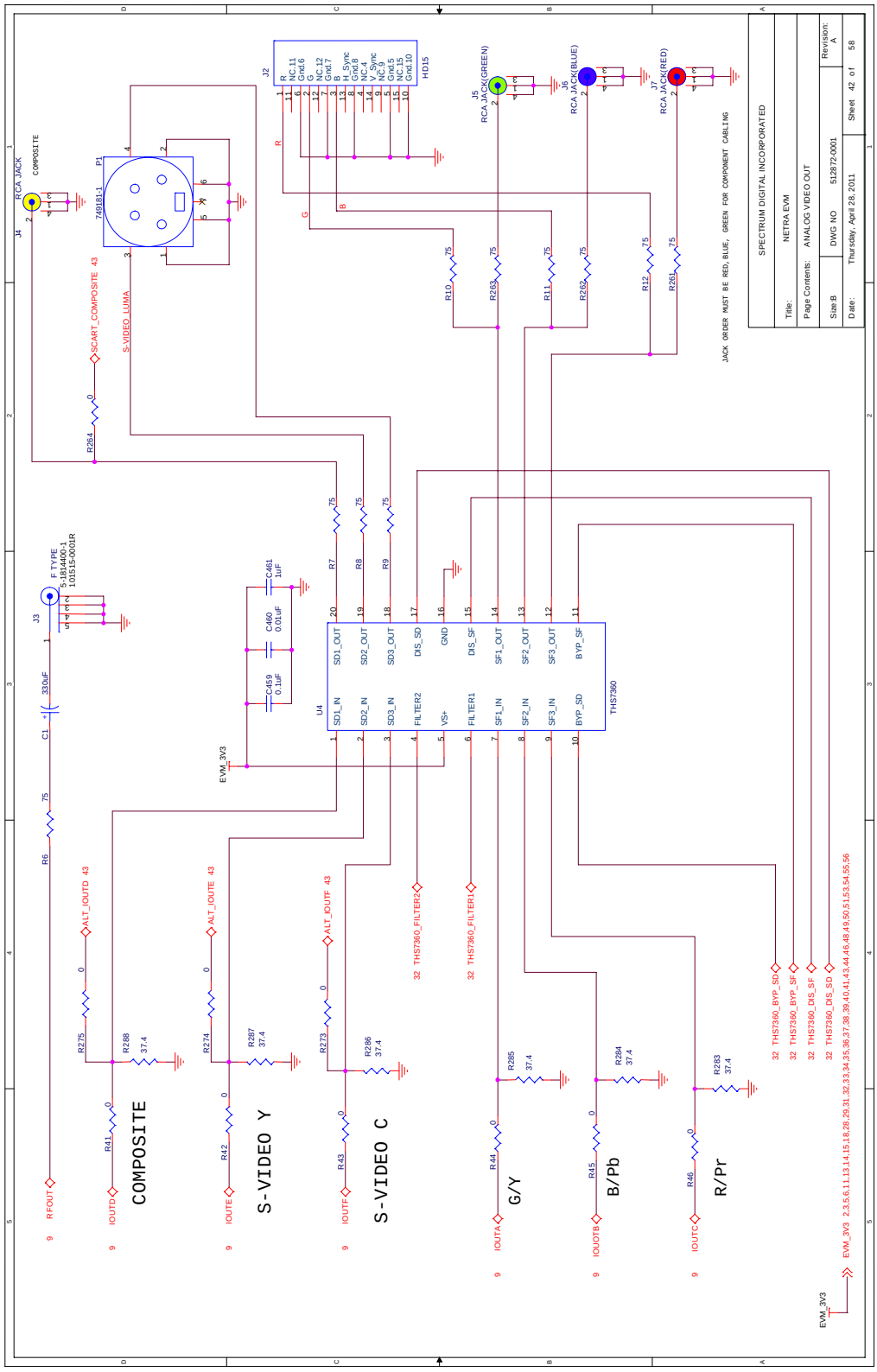
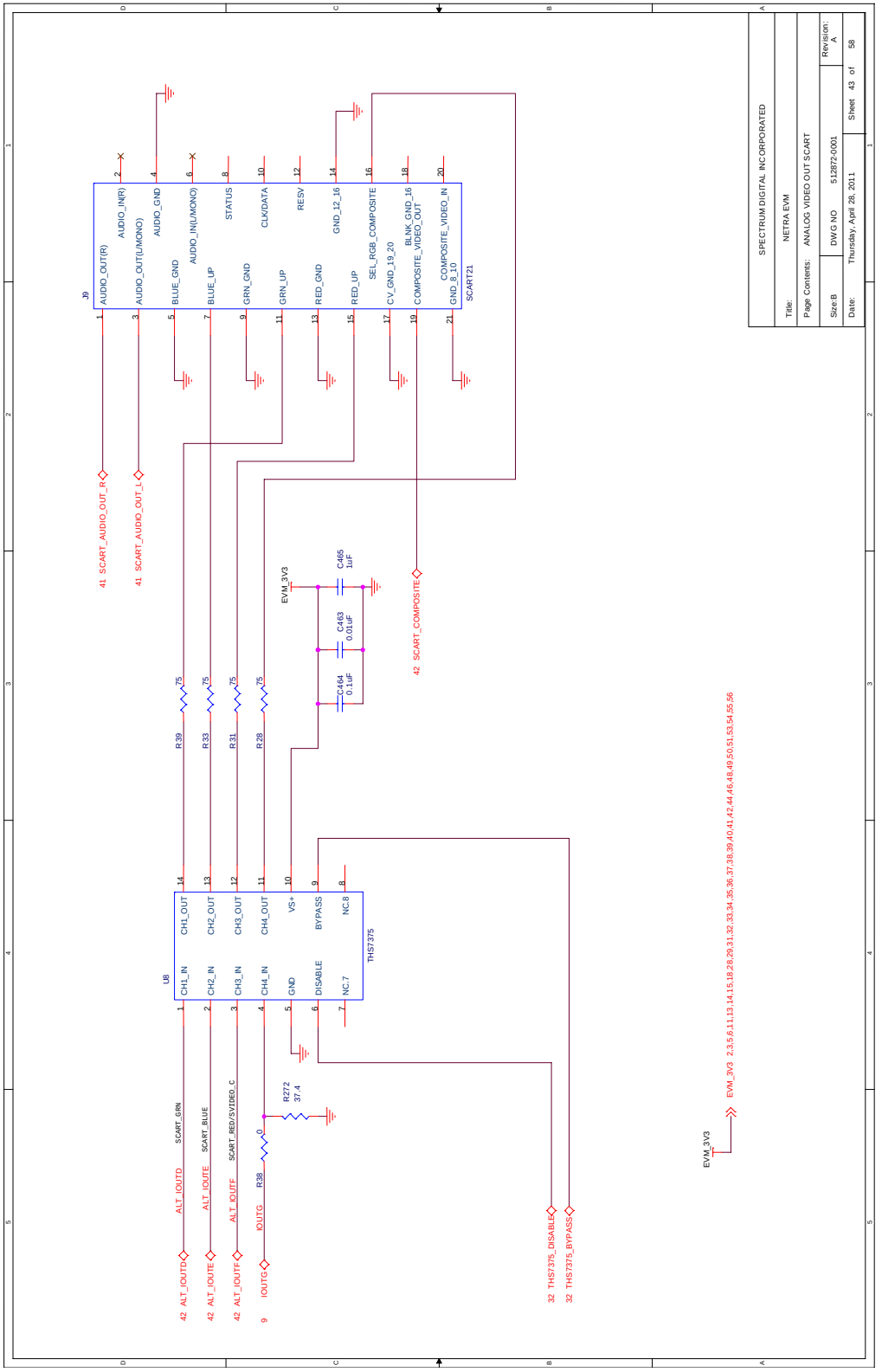
U19A
ETI011C
CLK_IN/XTAL1
XTAL2
TXCLK
GTX_CLK/PMA_TX_CLK/TXC
TX_ENTXD[8]/TX_CTL/TXD[4]
TX_ER/TXD[9]
SYS_CLK
TXD[7]
TXD[6]
TXD[5]
TXD[4]
TXD[3]
TXD[2]
TXD[1]
TXD[0]
INPUTS
RXCLK/PMA_RX_CLK[0]/RXC
RX_DVRXD[8]/RX_CTL/RXD[4]
RX_ER/RX[9]
RXD[7]
RXD[6]
RXD[5]
RXD[4]
RXD[3]
RXD[2]
RXD[1]
RXD[0]
OUTPUTS
CRS/COMMA
COL/PMA_RX_CLK[1]
MDC
MDIO
MDINTn
RESETn
PHYA[4]
PHYA[3]
PHYA[2]
PHYA[1]/LED_100
PHYA[0]/LED_TXRX
LED_1000/SPEED_1000
LED_LNK/PAUSE
PRES
RSET
MAC_IF_SEL[2]
MAC_IF_SEL[1]
MAC_IF_SEL[0]
TMS/SYS_CLK_ENn
TCK
TDO
TDI/LPED_RXn
TRST
TRD[0]P 40
TRD[0]N 40
TRD[1]P 40
TRD[1]N 40
TRD[2]P 40
TRD[2]N 40
TRD[3]P 40
TRD[3]N 40
ENET_LED_LINK 40
ENET_LED_RX 40
Y1
25MHz
C478 18 pF
C477 18 pF
R334 1K 1%
R318 6.34K 1%
R310 10K
R315 NO-POP
R301 0
R302 0
R303 0
R313 10K
R319 22
R314 0
RN11 RPACK8-22
R324 22
R338 22
R333 22
R325 22
R329 22
R354 22
R355 22
R477 10K
R478 10K
R479 10K
R342 10K
R343 NO-POP
EVM_3V3
GMII0_TCLK
GMII0_GMTCLK
GMII0_TXEN
GMII0_TXD7
GMII0_TXD6
GMII0_TXD5
GMII0_TXD4
GMII0_TXD3
GMII0_TXD2
GMII0_TXD1
GMII0_TXD0
GMII0_RCLK
GMII0_RXDV
GMII0_RXER
GMII0_RXD7
GMII0_RXD6
GMII0_RXD5
GMII0_RXD4
GMII0_RXD3
GMII0_RXD2
GMII0_RXD1
GMII0_RXD0
GMII0_CRS
GMII0_COL
MDIO_MDCLK
MDIO_MDIO
ENET_INTn
RSTOUTn
PHY_MTCLK
PHY_GMTCLK
PHY_MRCLK
PHY_MRXDV
PHY_MRXER
PHY_MRXD7
PHY_MRXD6
PHY_MRXD5
PHY_MRXD4
PHY_MRXD3
PHY_MRXD2
PHY_MRXD1
PHY_MRXD0
PHY_MCRS
PHY_MCOL
PHY_MDCLK
PHY_MDIO

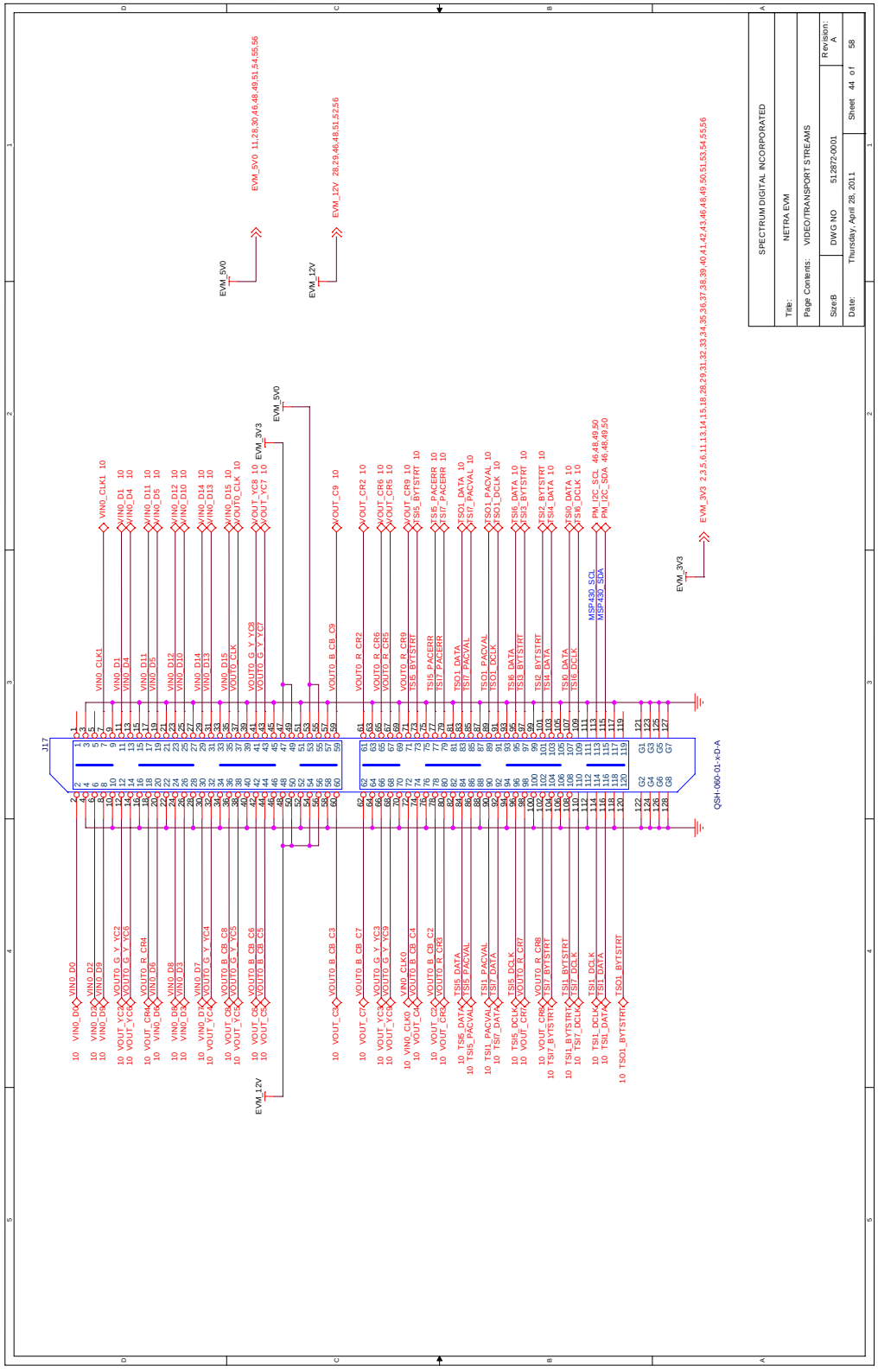

SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: ETHERNET - POWER
Size:B DWG NO 512872-0001 Revision: A
Date: Thursday, April 28, 2011 Sheet 39 of 58
U19B
ET1011C
BCP69T1
BLM41P750SPT
EVM_3V3
PHY_VDD_1V0
PHY_AVDD_1V0
PHY_VDD_2V5
PHY_1V0
PHY_2V5
VDD_REG
CTRL_1V0
CTRL_2V5
POWER_PAD

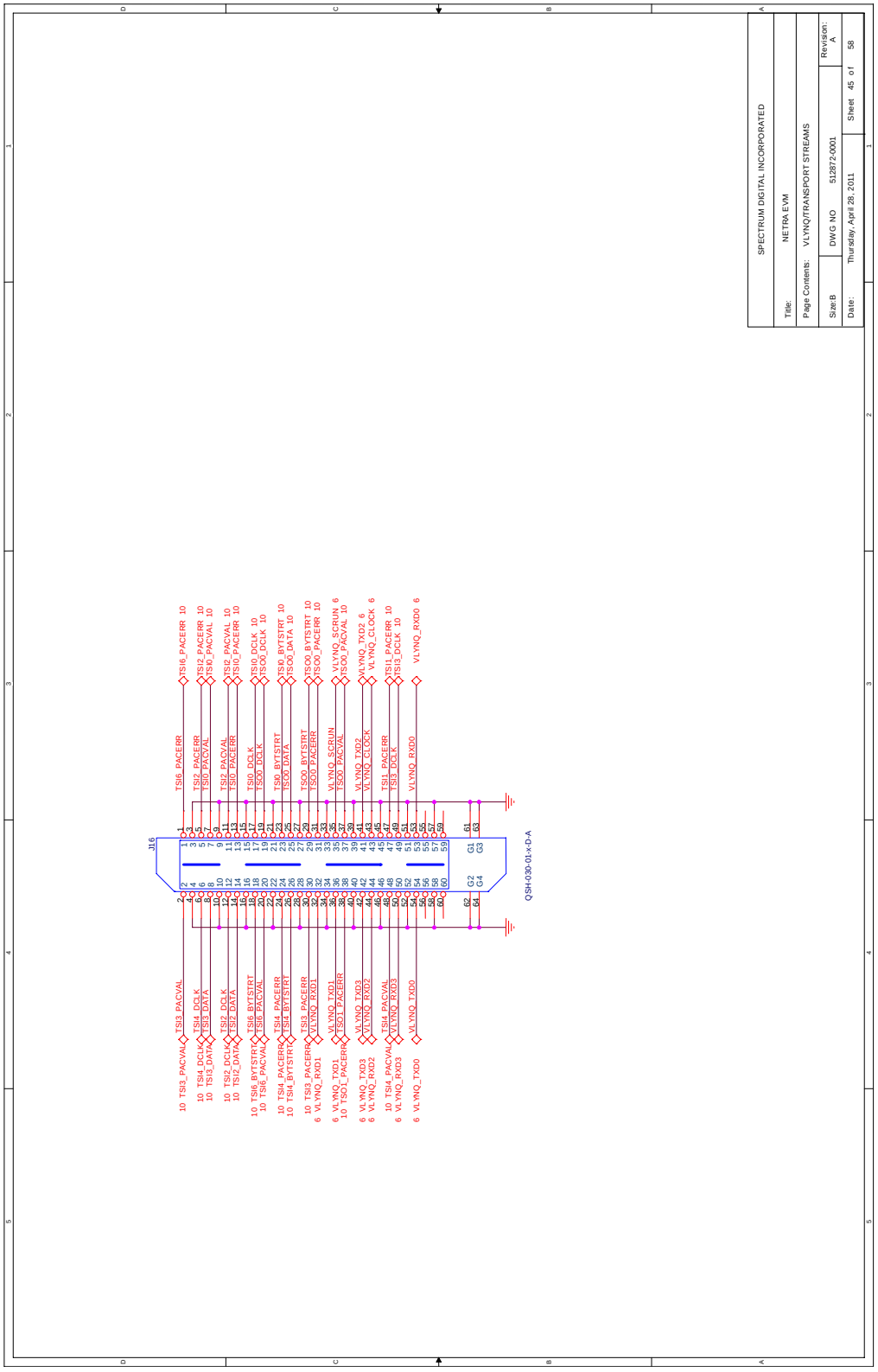

SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: ETHERNET - OUTPUT CONNECTOR
Size: B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 40 of 58
J10
L16
BLM18AG601SN1
EVM_3V3
PHY_VDD_2V5
DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS
R357
0ohm 1/4W
R492
NO-POP
R493
0
R326
R320
R335
R330
R346
R339
R356
R351
49.9 1%
C496
C503
C505
C510
0.01uF
R321
R347
221
U68
74LVC1G08
C801
0.1uF
TRD[0]P
TRD[0]N
TRD[1]P
TRD[1]N
TRD[2]P
TRD[2]N
TRD[3]P
TRD[3]N
ENET_LED_LINK
ENET_LED_RX

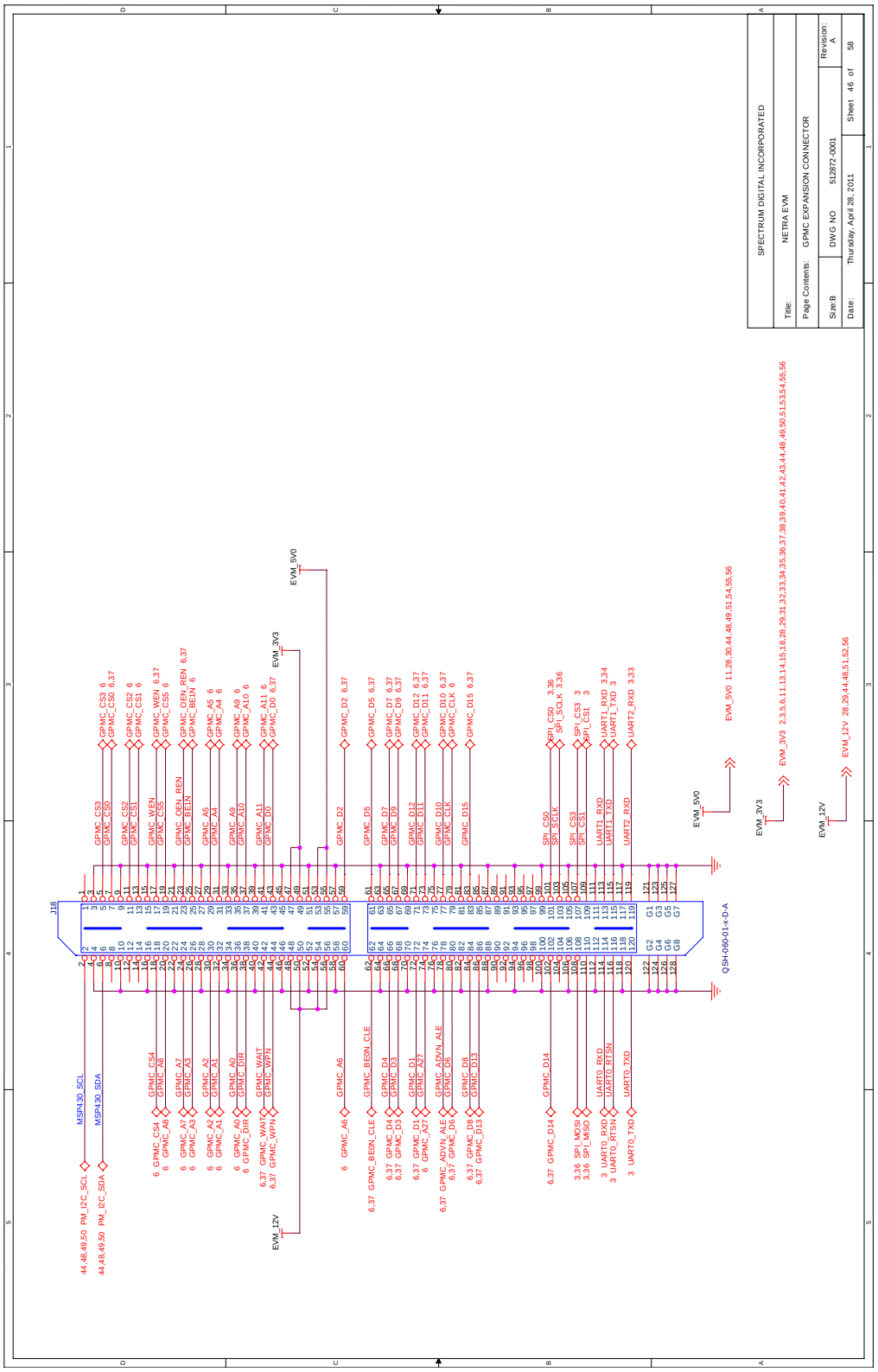

SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: AIC3106 AUDIO INTERFACE
Size:B DWG NO 512872-0001 Revision: A
Date: Thursday, April 28, 2011 Sheet 41 of 58
TLV320AIC3106
TPS77018DBVT
TEST POINT
Headphone Out
Line Out
Line In
Mic In
ISOLATE GROUNDS AND CONNECT AT SINGLE LOCATION IN THE GROUND PLANE

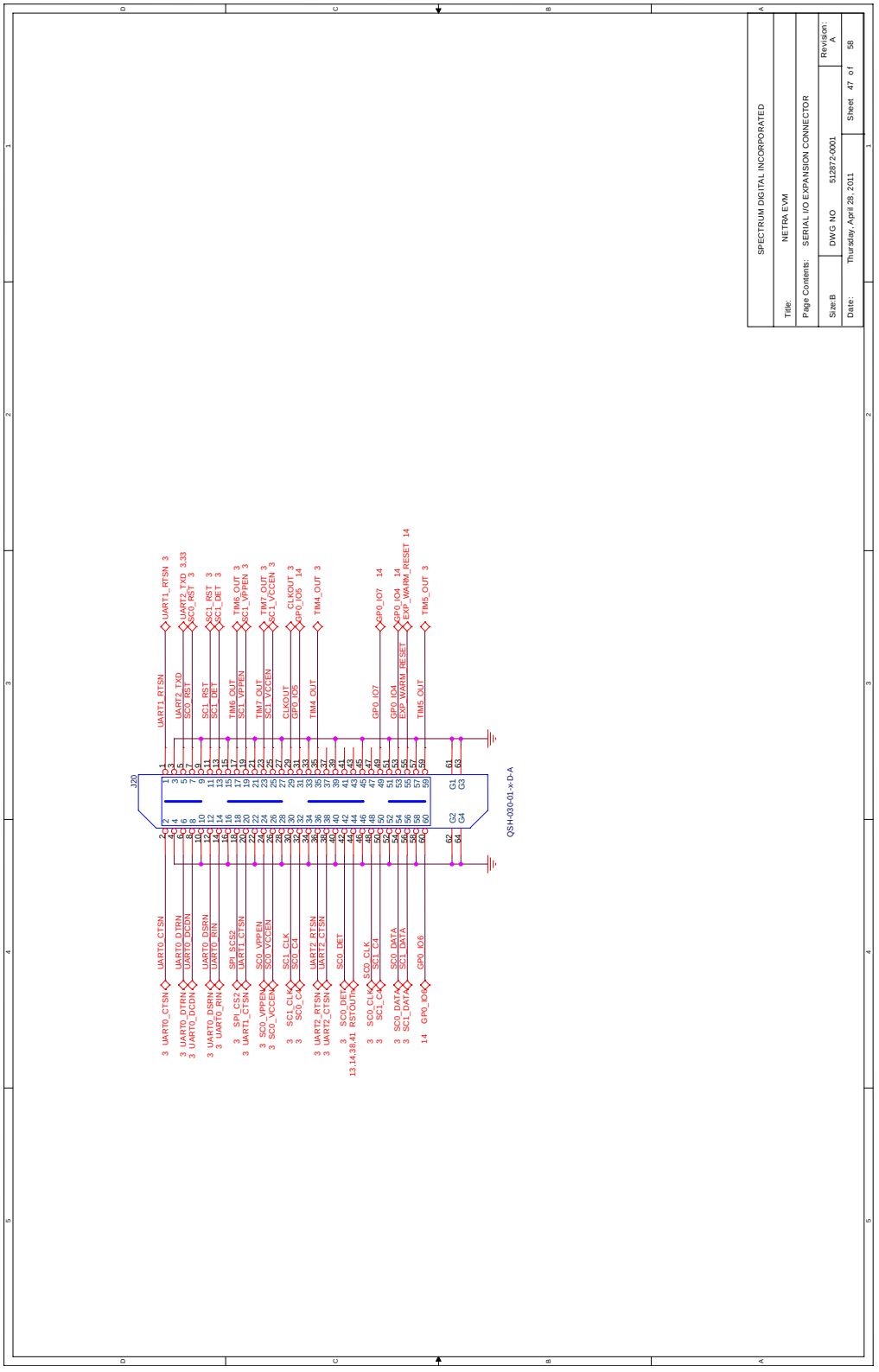

SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: ANALOG VIDEO OUT
Size:B DWG NO 512872-0001 Revision: A
Date: Thursday, April 28, 2011 Sheet 42 of 58
JACK ORDER MUST BE RED, BLUE, GREEN FOR COMPONENT CABLING
COMPOSITE
S-VIDEO Y
S-VIDEO C
G/Y
B/Pb
R/Pr
THS7360
RCA JACK
F TYPE
HD15
RCA JACK(GREEN)
RCA JACK(BLUE)
RCA JACK(RED)
SCART_COMPOSITE
S-VIDEO_LUMA
ALT_IOUTD
ALT_IOUTE
ALT_IOUTF
THS7360_FILTER1
THS7360_FILTER2
THS7360_BYP_SD
THS7360_BYP_SF
THS7360_DIS_SF
THS7360_DIS_SD
EVM_3V3

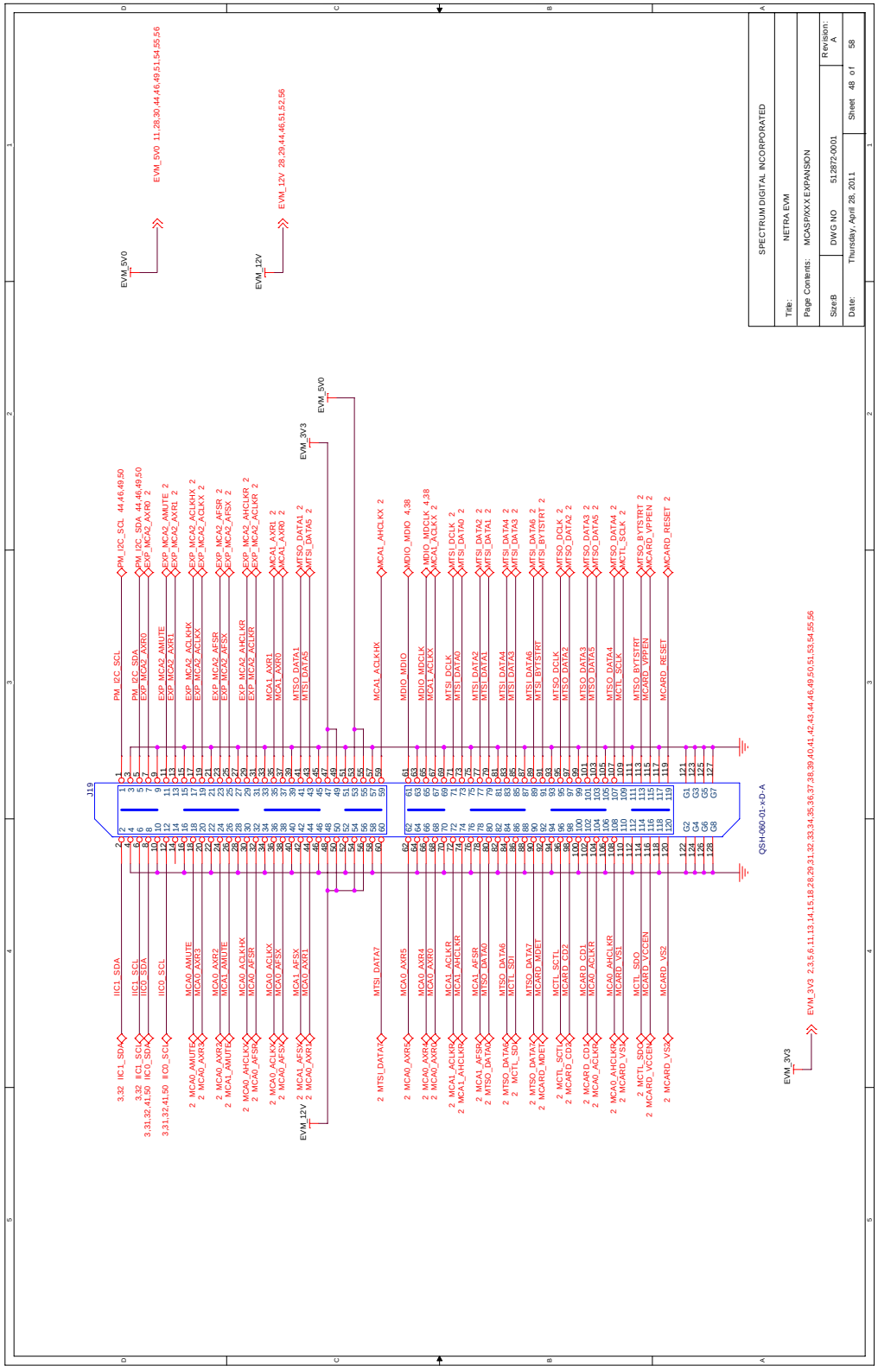

SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: ANALOG VIDEO OUT SCART
Size:B DWG NO 512872-0001 Revision: A
Date: Thursday, April 28, 2011 Sheet 43 of 58
J9
AUDIO_OUT(R)
AUDIO_IN(R)
AUDIO_OUT(L/MONO)
AUDIO_GND
BLUE_GND
AUDIO_IN(L/MONO)
BLUE_UP
STATUS
GRN_GND
CLK/DATA
GRN_UP
RESV
RED_GND
GND_12_16
RED_UP
SEL_RGB_COMPOSITE
CV_GND_19_20
BLNK_GND_16
COMPOSITE_VIDEO_OUT
GND_9_10
COMPOSITE_VIDEO_IN
SCART21
41 SCART_AUDIO_OUT_R
41 SCART_AUDIO_OUT_L
42 SCART_COMPOSITE
EVM_3V3
C465 1uF
C463 0.01uF
C464 0.1uF
R39 75
R33 75
R31 75
R28 75
U8
CH1_IN
CH2_IN
CH3_IN
CH4_IN
GND
DISABLE
NC:7
CH1_OUT
CH2_OUT
CH3_OUT
CH4_OUT
VS+
BYPASS
NC:8
THS7375
R27 2 37.4
R38 0
SCART_GRN
SCART_BLUE
SCART_RED/SVIDEO_C
ALT_IOUTD
ALT_IOUTE
ALT_IOUTF
IOUTG
42 ALT_IOUTD
42 ALT_IOUTE
42 ALT_IOUTF
9 IOUTG
32 THS7375_DISABLE
32 THS7375_BYPASS
EVM_3V3
EVM_3V3 2,3,5,6,11,13,14,15,18,28,29,31,32,33,34,35,36,37,38,39,40,41,42,44,46,48,49,50,51,53,54,55,56

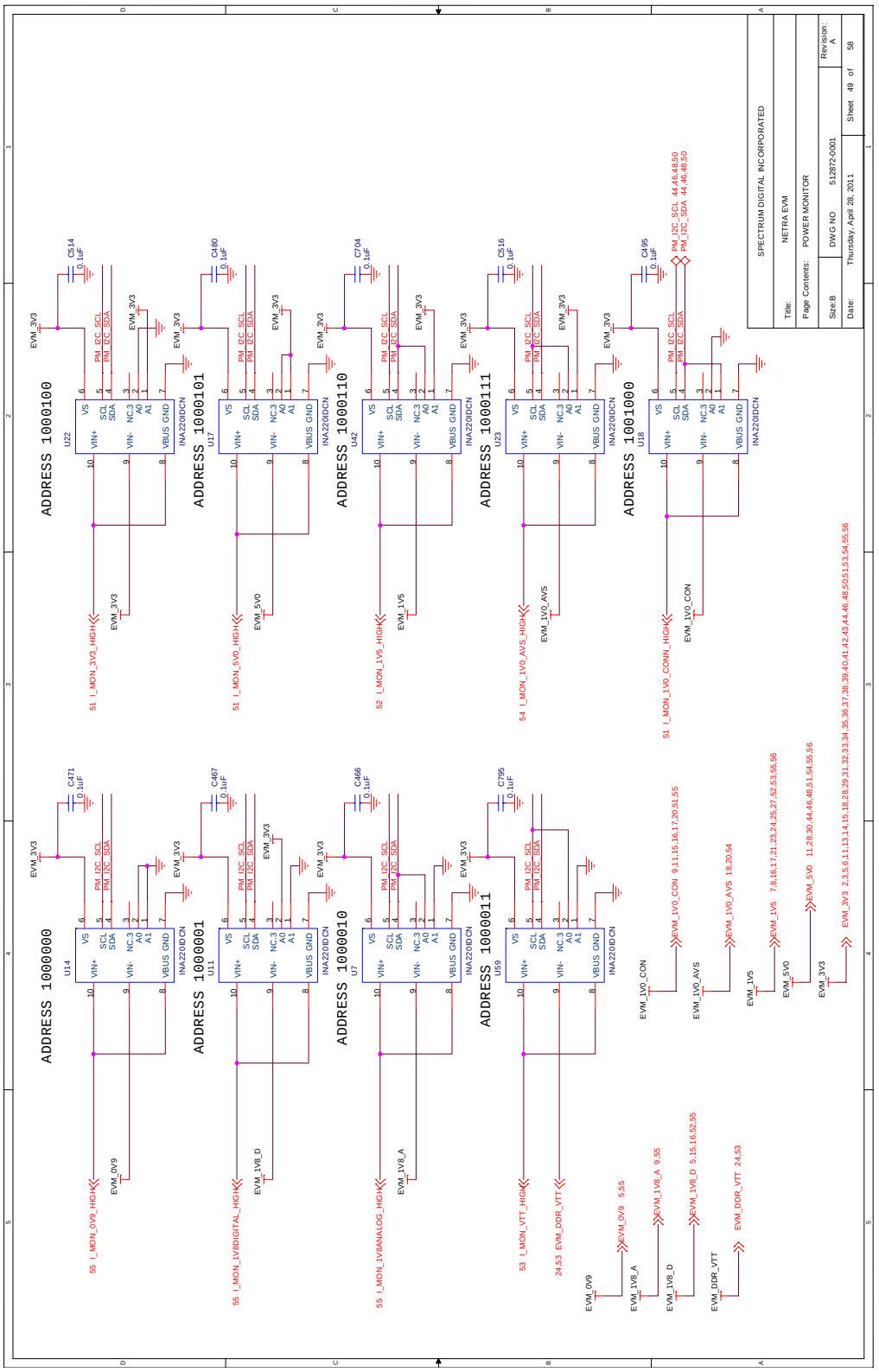

SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: VIDEO/TRANSPORT STREAMS
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 44 of 58
J17
QSH-060-01-x-D-A
EVM_5V0
EVM_12V
EVM_3V3
MSP430_SCL
MSP430_SDA

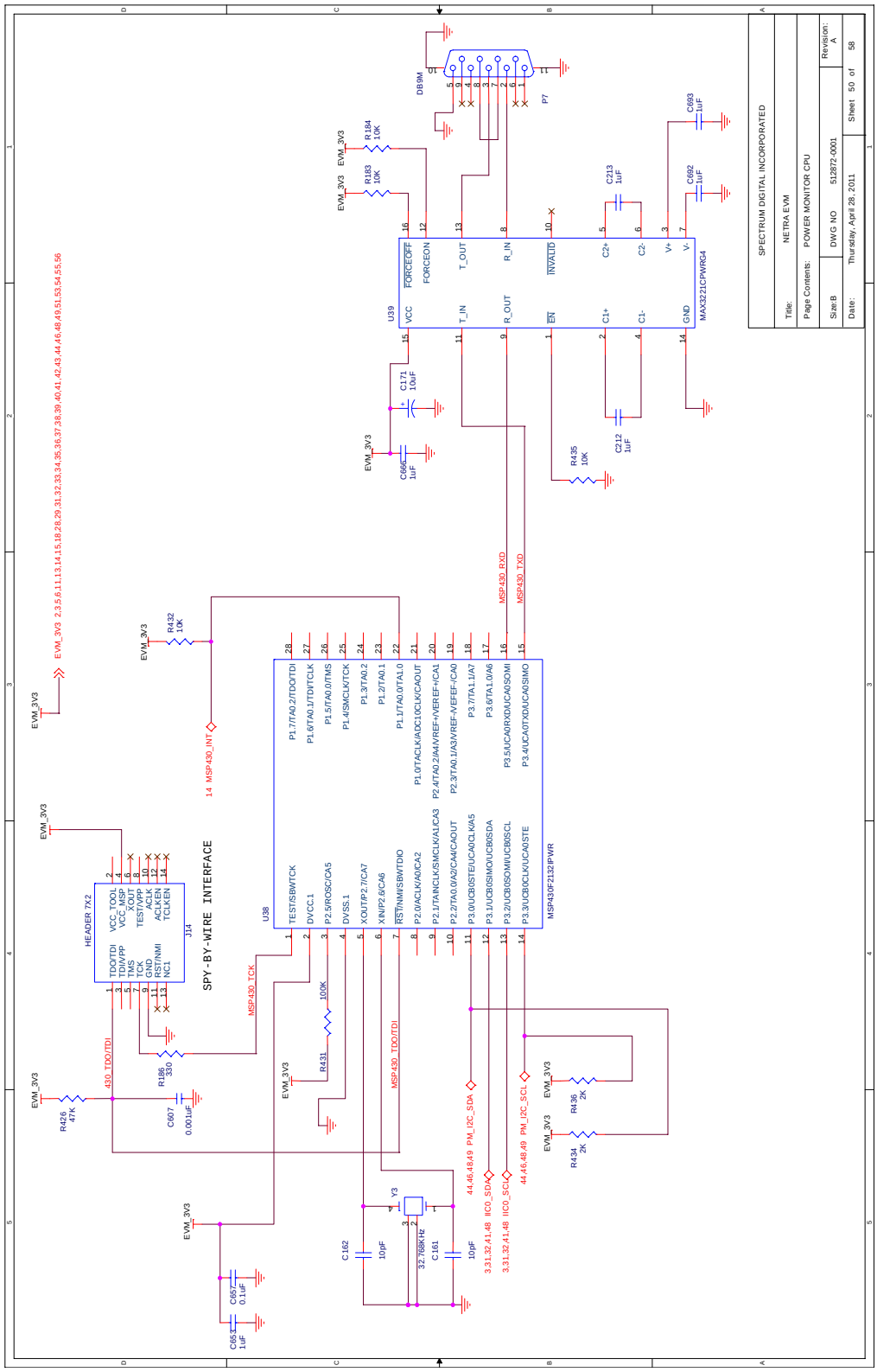

SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: VLYNQ/TRANSPORT STREAMS
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 45 of 58
J16
QSH-030-01-x-D-A
TSI6_PACERR 10
TSI2_PACERR 10
TSI0_PACVAL 10
TSI2_PACVAL 10
TSI2_PACERR 10
TSI0_DCLK 10
TSO0_DCLK 10
TSI0_BYTSTRT 10
TSO0_DATA 10
TSO0_BYTSTRT 10
TSO0_PACERR 10
VLYNQ_SCRUN 6
TSO0_PACVAL 10
VLYNQ_TXD2 6
VLYNQ_CLOCK 6
TSI1_PACERR 10
TSI3_DCLK 10
VLYNQ_RXD0 6
TSI3_PACVAL 10
TSI4_DCLK 10
TSI3_DATA 10
TSI2_DCLK 10
TSI2_DATA 10
TSI6_BYTSTRT 10
TSI6_PACVAL 10
TSI4_PACERR 10
TSI4_BYTSTRT 10
TSI3_PACERR 10
VLYNQ_RXD1 6
VLYNQ_TXD1 6
TSO1_PACERR 10
VLYNQ_TXD3 6
VLYNQ_RXD2 6
TSI4_PACVAL 10
VLYNQ_RXD3 6
VLYNQ_TXD0 6

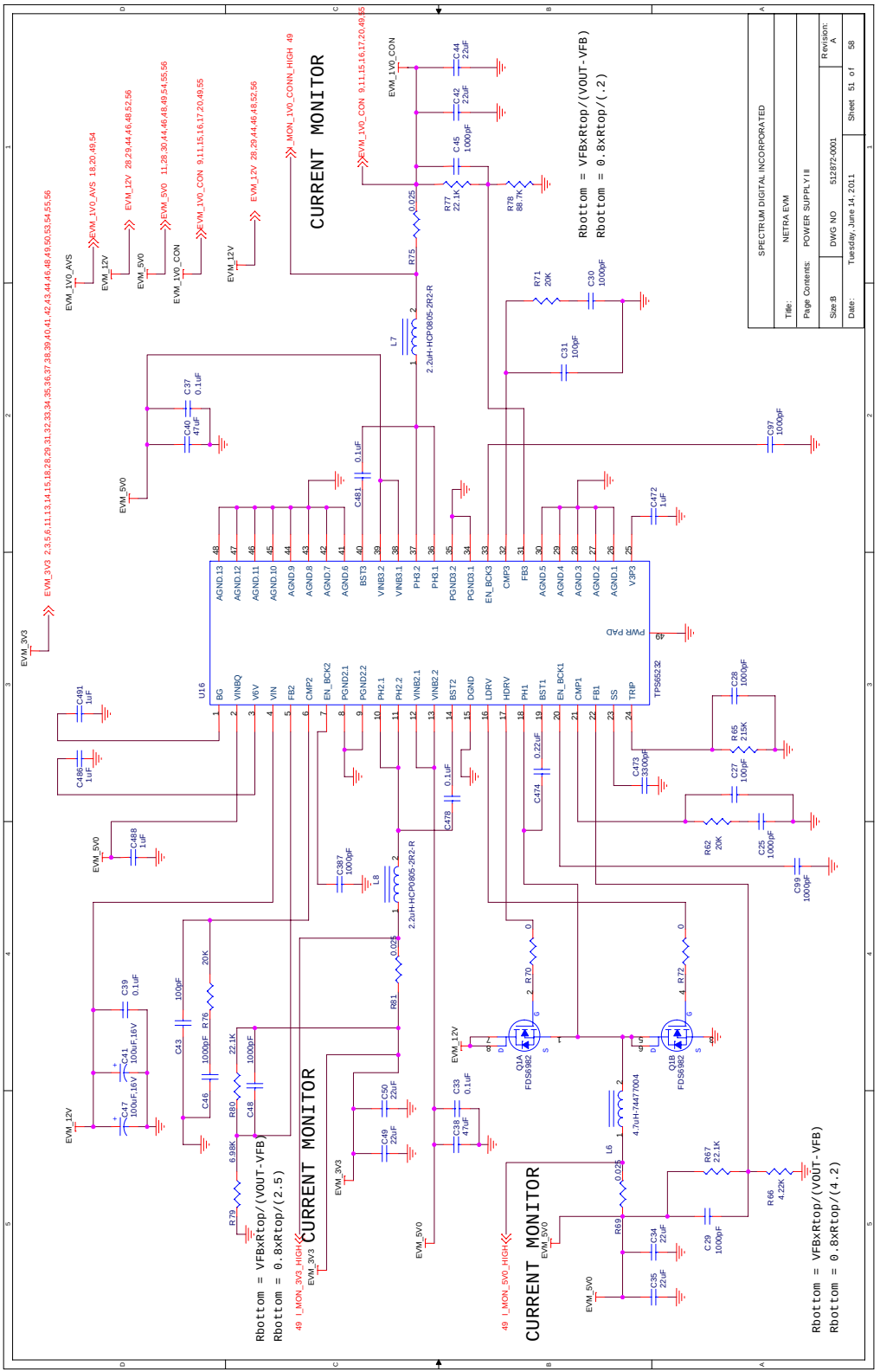

SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: GPMC EXPANSION CONNECTOR
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 46 of 58
J18
QSH-060-01-x-D-A
MSP430_SCL
MSP430_SDA
PM_I2C_SCL
PM_I2C_SDA
GPMC_CS4
GPMC_A8
GPMC_A7
GPMC_A3
GPMC_A2
GPMC_A1
GPMC_A0
GPMC_DIR
GPMC_WAIT
GPMC_WPN
GPMC_A6
GPMC_BE0N_CLE
GPMC_D4
GPMC_D3
GPMC_D1
GPMC_A27
GPMC_ADVN_ALE
GPMC_D6
GPMC_D8
GPMC_D13
GPMC_D14
UART0_RXD
UART0_RTSN
UART0_TXD
GPMC_CS3
GPMC_CS0
GPMC_CS2
GPMC_CS1
GPMC_WEN
GPMC_CS5
GPMC_OEN_REN
GPMC_BE1N
GPMC_A5
GPMC_A4
GPMC_A9
GPMC_A10
GPMC_A11
GPMC_D0
GPMC_D2
GPMC_D5
GPMC_D7
GPMC_D9
GPMC_D12
GPMC_D11
GPMC_D10
GPMC_CLK
GPMC_D15
SPI_CS0
SPI_SCLK
SPI_CS3
SPI_CS1
UART1_RXD
UART1_TXD
UART2_RXD
EVM_5V0
EVM_3V3
EVM_12V
EVM_5V0 11,28,30,44,48,49,51,54,55,56
EVM_3V3 2,3,5,6,11,13,14,15,18,28,29,31,32,33,34,35,36,37,38,39,40,41,42,43,44,48,49,50,51,53,54,55,56
EVM_12V 28,29,44,48,51,52,56

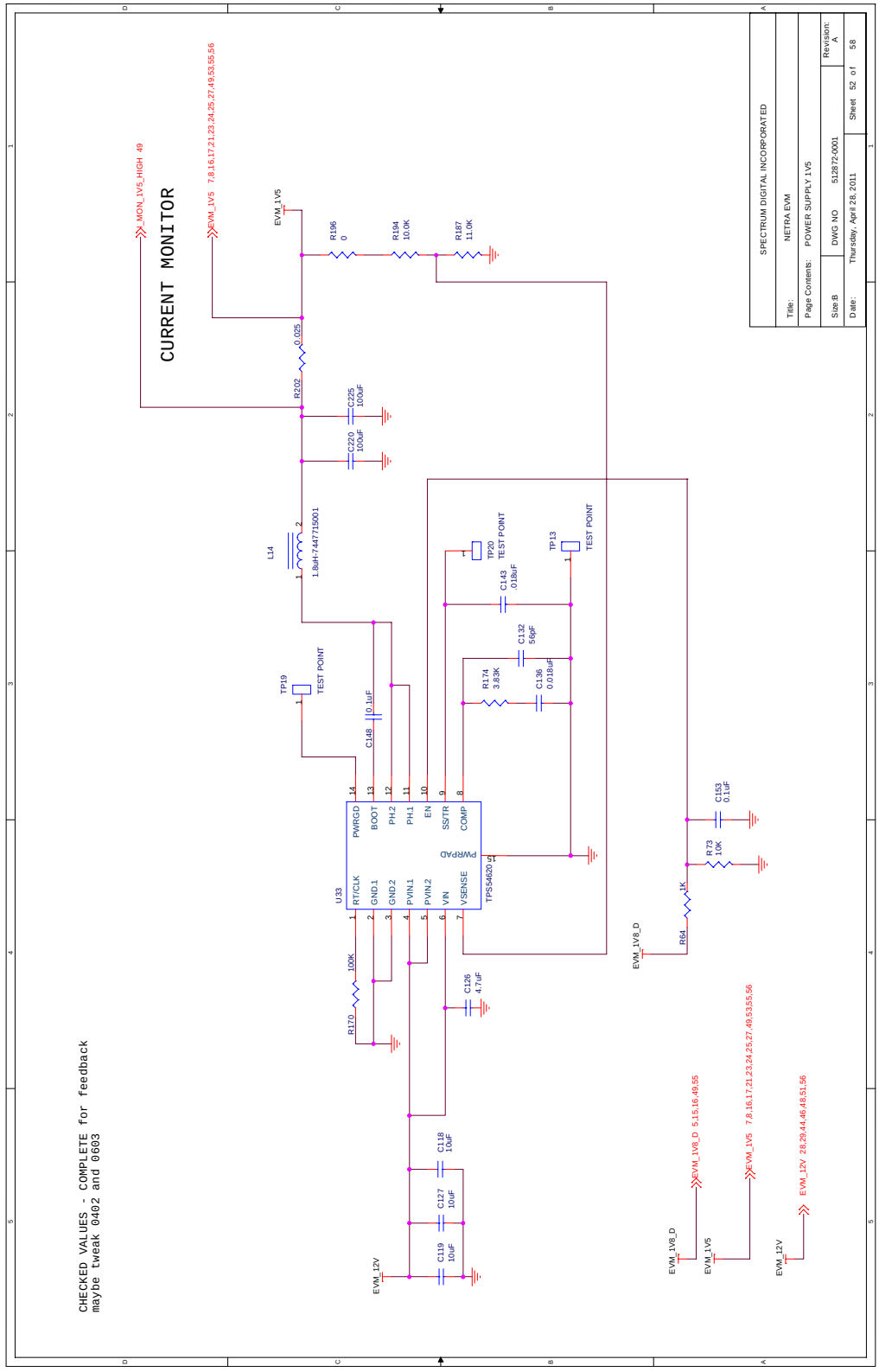

SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: SERIAL I/O EXPANSION CONNECTOR
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 47 of 58
J20
QSH-030-01-x-D-A
UART0_CTSN
UART0_DTRN
UART0_DCDN
UART0_DSRN
UART0_RIN
SPI_CS2
UART1_CTSN
SC0_VPPEN
SC0_VCCEN
SC1_CLK
SC0_C4
UART2_RTSN
UART2_CTSN
SC0_DET
SC0_CLK
SC1_C4
SC0_DATA
SC1_DATA
GP0_IO6
UART1_RTSN
UART2_TXD
SC0_RST
SC1_RST
SC1_DET
TIM6_OUT
SC1_VPPEN
TIM7_OUT
SC1_VCCEN
CLKOUT
GP0_IO5
TIM4_OUT
GP0_IO7
GP0_IO4
EXP_WARM_RESET
TIM5_OUT

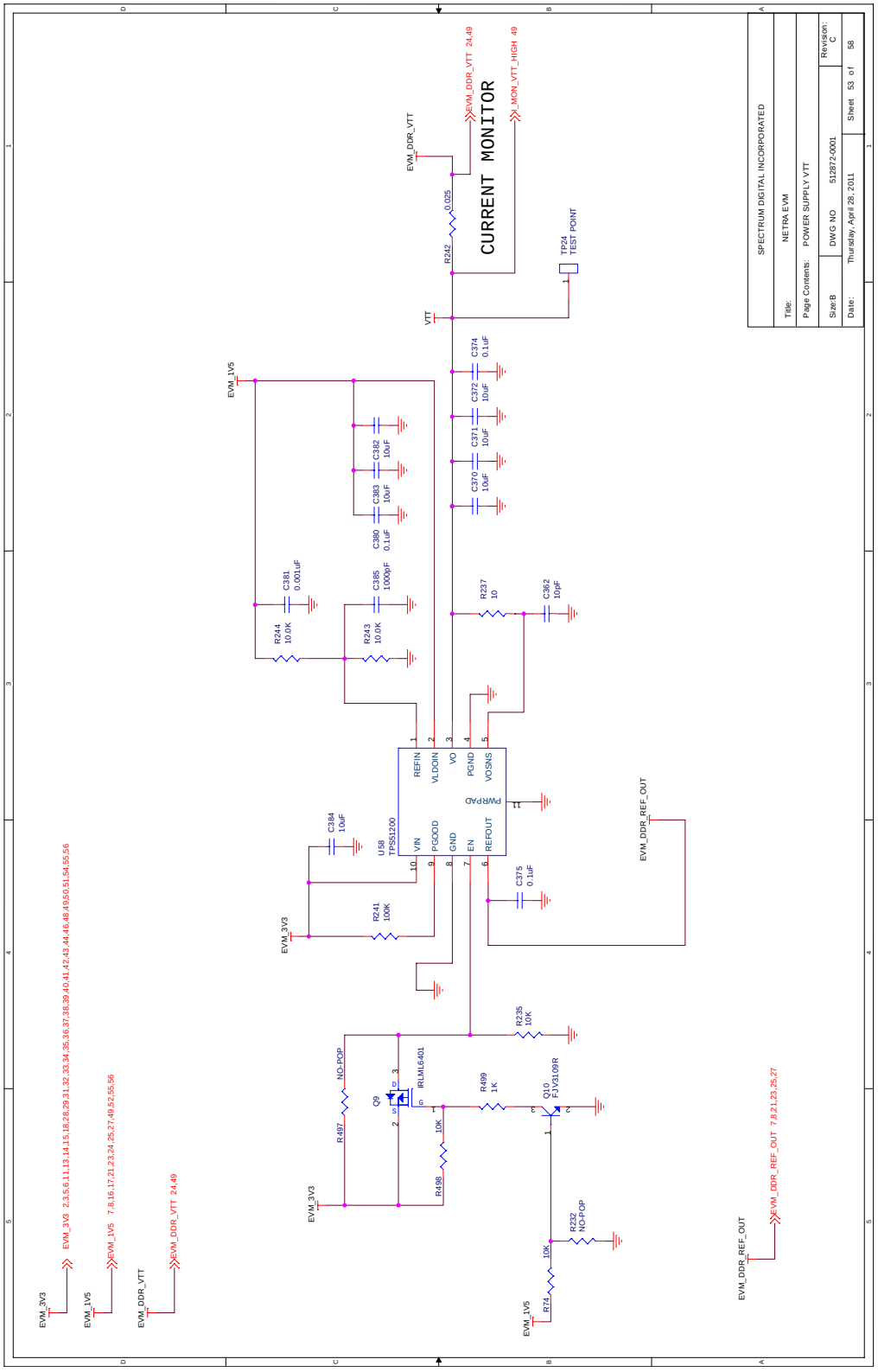

SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: MCASPXXX EXPANSION
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 48 of 58
EVM_5V0
EVM_12V
EVM_3V3
QSH-060-01-x-D-A
PM_I2C_SCL
PM_I2C_SDA
MCA1_AHCLKX
MDIO_MDIO
MDIO_MDCLK
MCA1_ACLKX
MTSI_DCLK
MTSI_DATA0
MTSI_DATA2
MTSI_DATA1
MTSI_DATA4
MTSI_DATA3
MTSI_DATA6
MTSI_BYTSTRT
MTSO_DCLK
MTSO_DATA2
MTSO_DATA3
MTSO_DATA5
MTSO_DATA4
MCTL_SCLK
MTSO_BYTSTRT
MCARD_VPPEN
MCARD_RESET
MTSI_DATA7
MCA0_AXR5
MCA0_AXR4
MCA0_AXR6
MCA1_ACLKR
MCA1_AHCLKR
MCA1_AFSR
MTSO_DATA0
MTSO_DATA6
MCTL_SDI
MTSO_DATA7
MCARD_MDET
MCTL_SCTL
MCARD_CD2
MCARD_CD1
MCA0_ACLKR
MCA0_AHCLKR
MCARD_VSI
MCTL_SDO
MCARD_VCCEN
MCARD_VS2
MCA0_AMUTE
MCA0_AXR3
MCA0_AXR2
MCA1_AMUTE
MCA0_ACLKHX
MCA0_AFSR
MCA0_ACLKX
MCA0_AFSX
MCA1_AFSX
MCA0_AXR1
MCA0_AXR0
MCA1_AXR1
MCA1_AXR0
MTSO_DATA1
MTSI_DATA5
EXP_MCA2_ACLKHX
EXP_MCA2_ACLKX
EXP_MCA2_AFSR
EXP_MCA2_AFSX
EXP_MCA2_AHCLKR
EXP_MCA2_ACLKR
EXP_MCA2_AXR1
EXP_MCA2_AXR0
EXP_MCA2_AMUTE
EXP_MCA2_AXR0
EVM_5V0 11,28,30,44,46,49,51,54,55,56
EVM_12V 28,29,44,46,51,52,56
EVM_3V3 2,3,5,6,11,13,14,15,18,28,29,31,32,33,34,35,36,37,38,39,40,41,42,43,44,46,49,50,51,53,54,55,56

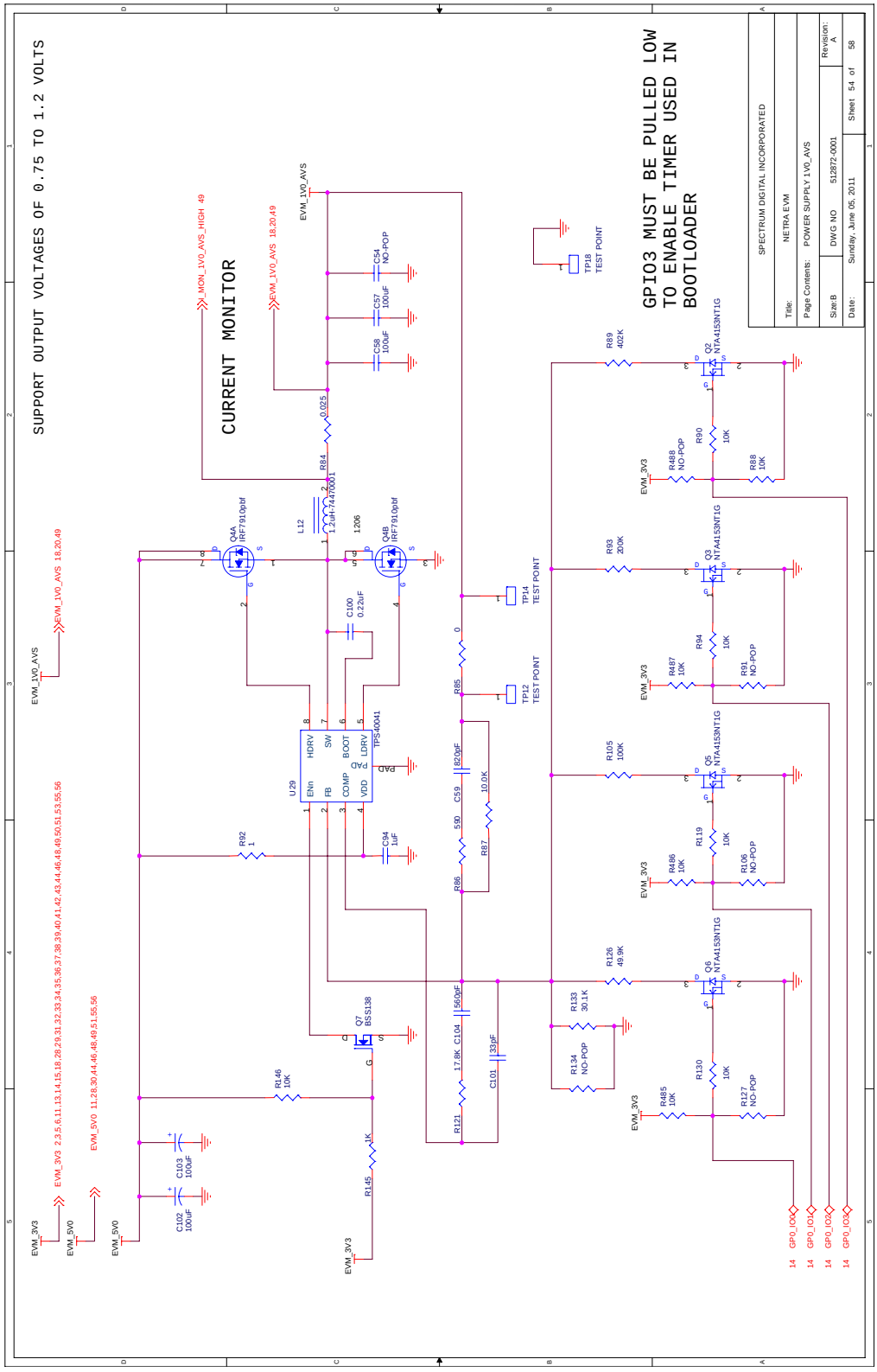

ADDRESS 1000000
ADDRESS 1000001
ADDRESS 1000010
ADDRESS 1000011
ADDRESS 1000100
ADDRESS 1000101
ADDRESS 1000110
ADDRESS 1000111
ADDRESS 1001000
INA220IDCN
EVM_3V3
PM_I2C_SCL
PM_I2C_SDA
EVM_0V9
EVM_1V8_D
EVM_1V8_A
EVM_1V0_CON
EVM_1V0_AVS
EVM_1V5
EVM_5V0
EVM_DDR_VTT
SPECTRUM DIGITAL INCORPORATED
NETRA EVM
POWER MONITOR
Thursday, April 28, 2011
Sheet 49 of 58

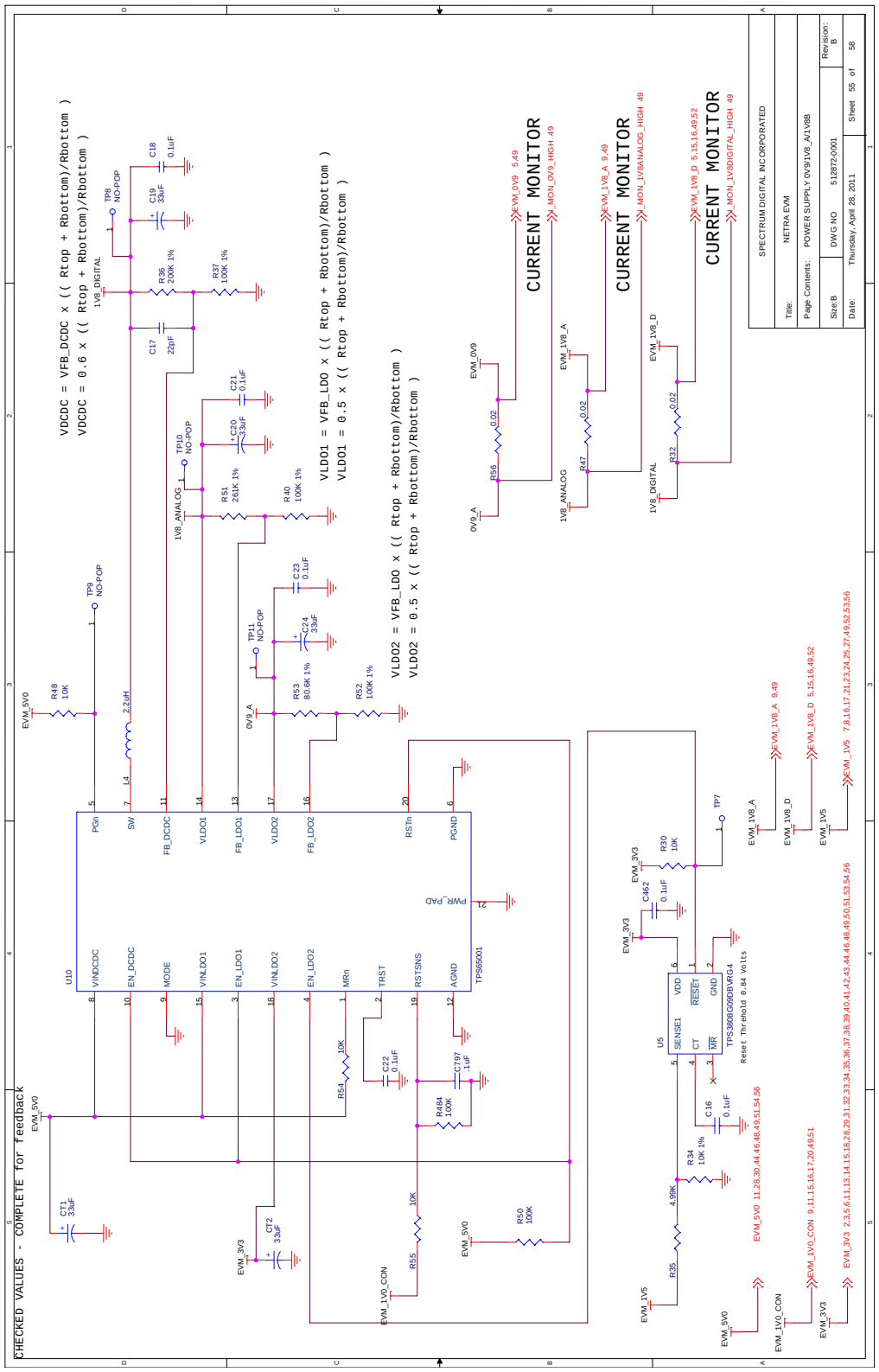

SPY-BY-WIRE INTERFACE
HEADER 7X2
J14
U38
MSP430F2132IPWR
U39
MAX3221CPWRG4
DB9M
P7
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: POWER MONITOR CPU
Size:B
DWG NO 512872-0001
Revision: A
Date: Thursday, April 28, 2011
Sheet 50 of 58

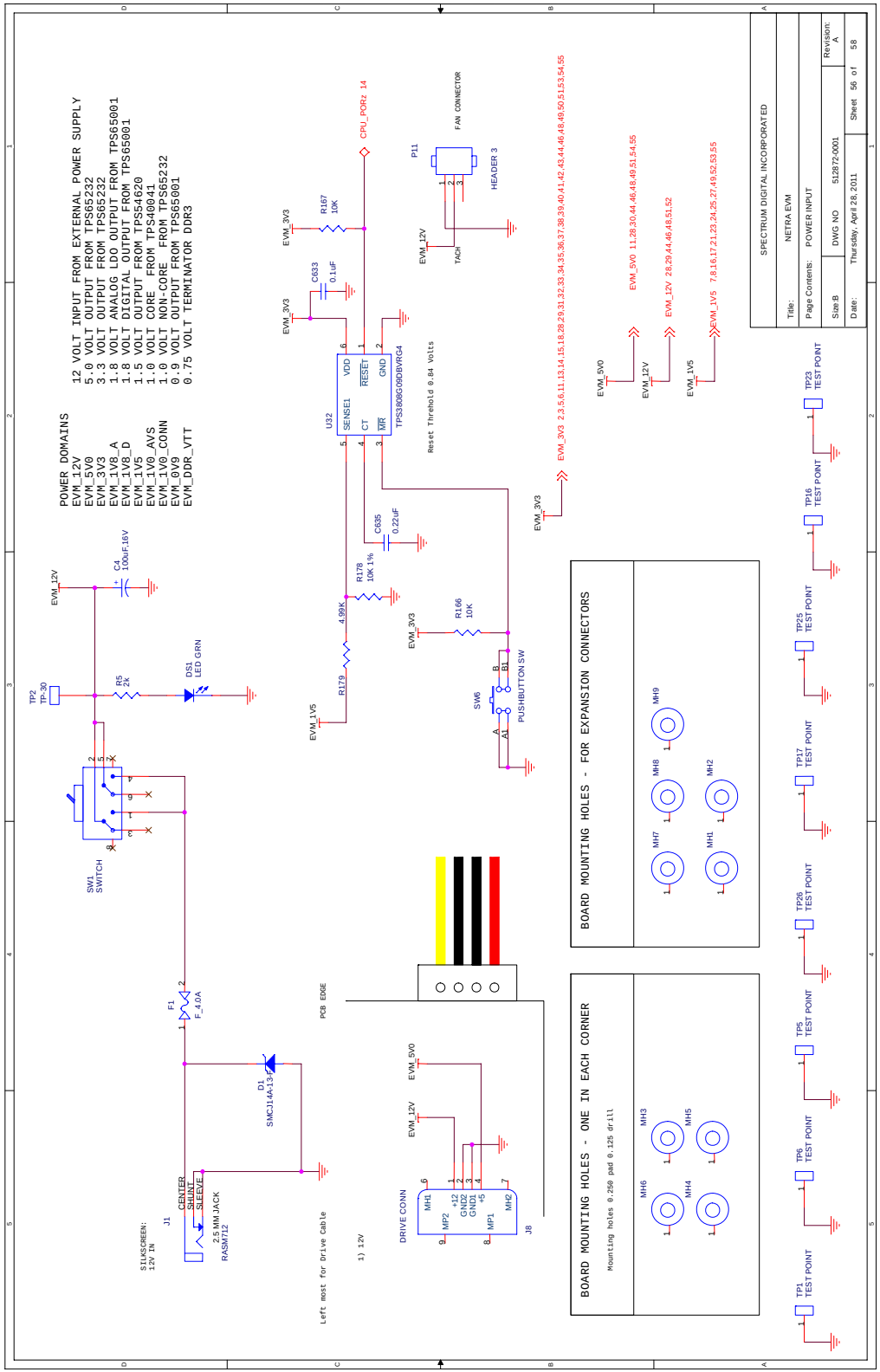

CURRENT MONITOR
CURRENT MONITOR
CURRENT MONITOR
Rbottom = VFBxRtop/(VOUT-VFB)
Rbottom = 0.8xRtop/(2.5)
Rbottom = VFBxRtop/(VOUT-VFB)
Rbottom = 0.8xRtop/(4.2)
Rbottom = VFBxRtop/(VOUT-VFB)
Rbottom = 0.8xRtop/(.2)
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: POWER SUPPLY III
Size:B DWG NO 512872-0001 Revision: A
Date: Tuesday, June 14, 2011 Sheet 51 of 58
U16
TPS65232
L7
L8
L6
Q1A
Q1B
FDS6982
4.7uH-74477004

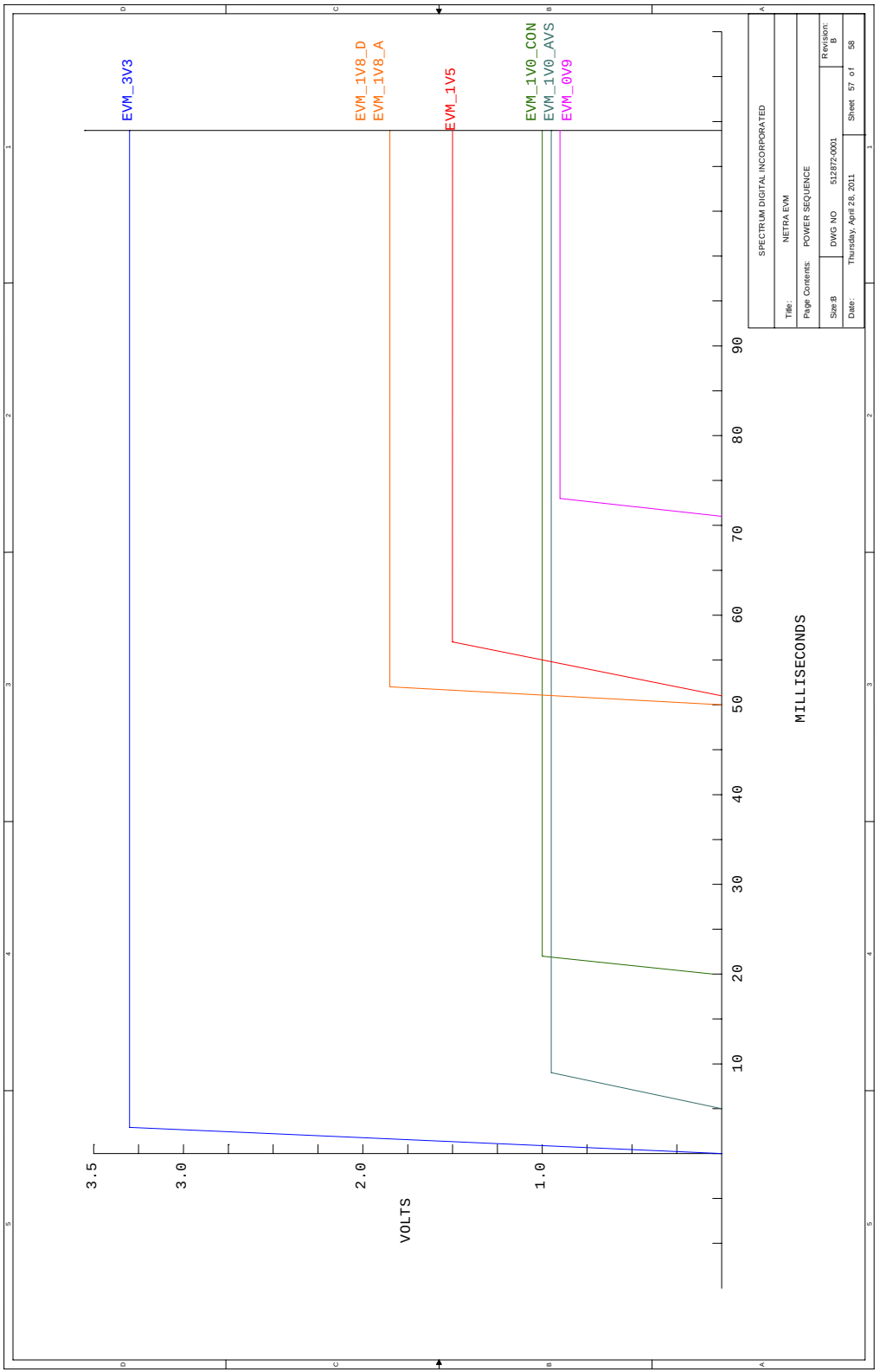

CURRENT MONITOR
I_MON_1V5_HIGH 49
EVM_1V5 7,8,16,17,21,23,24,25,27,49,53,55,56
EVM_1V5
R196 0
R194 10.0K
R187 11.0K
R202 0.025
C225 100uF
C220 100uF
L14 1.8uH-7447715001
TP20 TEST POINT
TP13 TEST POINT
TP19 TEST POINT
C143 .018uF
C132 56pF
C136 0.018uF
R174 3.83K
C148 0.1uF
U33 TPS54620
PWRGD BOOT PH2 PH1 EN SSTR COMP
RT/CLK GND1 GND2 PVIN1 PVIN2 VIN VSENSE PWRPAD
R170 100K
C126 4.7uF
C153 0.1uF
R73 10K
R64 1K
EVM_1V8_D
C118 10uF
C127 10uF
C119 10uF
EVM_12V
EVM_1V8_D 5,15,16,49,55
EVM_1V5 7,8,16,17,21,23,24,25,27,49,53,55,56
EVM_12V 28,29,44,46,48,51,56
CHECKED VALUES - COMPLETE for feedback
maybe tweak 0402 and 0603
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: POWER SUPPLY 1V5
Size:B DWG NO 5128172-0001 Revision: A
Date: Thursday, April 28, 2011 Sheet 52 of 58


CURRENT MONITOR
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: POWER SUPPLY VTT
Size:B
DWG NO 512872-0001
Revision: C
Date: Thursday, April 28, 2011
Sheet 53 of 58
EVM_DDR_VTT 24,49
MON_VTT_HIGH 49
EVM_3V3 2,3,5,6,11,13,14,15,18,28,29,31,32,33,34,35,36,37,38,39,40,41,42,43,44,46,48,49,50,51,54,55,56
EVM_1V5 7,8,16,17,21,23,24,25,27,49,52,55,56
EVM_DDR_VTT 24,49
EVM_DDR_REF_OUT 7,8,21,23,25,27
U58 TPS51200
REFIN
VLDOIN
VO
PGND
VOSNS
PWRPAD
VIN
PGOOD
GND
EN
REFOUT
Q9 IRLML6401
Q10 FJV3109R
R242 0.025
R237 10
R241 100K
R243 10.0K
R244 10.0K
R497 NO-POP
R498 10K
R499 1K
R232 NO-POP
R74 10K
R235 10K
C361 0.001uF
C362 10pF
C370 10uF
C371 10uF
C372 10uF
C374 0.1uF
C375 0.1uF
C380 0.1uF
C382 10uF
C383 10uF
C384 10uF
C385 1000pF
TP24 TEST POINT


SUPPORT OUTPUT VOLTAGES OF 0.75 TO 1.2 VOLTS
CURRENT MONITOR
GPIO3 MUST BE PULLED LOW
TO ENABLE TIMER USED IN
BOOTLOADER
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: POWER SUPPLY 1V0_AVS
Size:B DWG NO 512872-0001 Revision: A
Date: Sunday, June 05, 2011 Sheet 54 of 58
EVM_1V0_AVS
EVM_3V3
EVM_5V0
MON_1V0_AVS_HIGH 49
EVM_1V0_AVS 18,20,49
EVM_3V3 2,3,5,6,11,13,14,15,18,28,29,31,32,33,34,35,36,37,38,39,40,41,42,43,44,46,48,49,50,51,53,55,56
EVM_5V0 11,28,30,44,46,48,49,51,55,56
U29
TPS40041
Q4A IRF7910pbf
Q4B IRF7910pbf
Q2 NTA4153NT1G
Q3 NTA4153NT1G
Q5 NTA4153NT1G
Q6 NTA4153NT1G
Q7 BSS138
L12 1.2uH-7447000J1
R84 0.025
R85 0
R86 590
R87 10.0K
R92 1
R145 1K
R146 10K
R89 402K
R90 10K
R88 10K
R488 NO-POP
R93 200K
R94 10K
R91 NO-POP
R487 10K
R105 100K
R19 10K
R106 NO-POP
R486 10K
R126 49.9K
R133 30.1K
R134 NO-POP
R130 10K
R127 NO-POP
R485 10K
C100 0.22uF
C59 820pF
C94 1uF
C104 5600pF
C101 33pF
R121 17.8K
C102 100uF
C103 100uF
C54 NO-POP
C57 100uF
C58 100uF
TP12 TEST POINT
TP14 TEST POINT
TP18 TEST POINT
GP0_IO00
GP0_IO01
GP0_IO02
GP0_IO03


CHECKED VALUES - COMPLETE for feedback
VDCDC = VFB_DCDC x ((Rtop + Rbottom)/Rbottom)
VDCDC = 0.6 x ((Rtop + Rbottom)/Rbottom)
VLDO1 = VFB_LDO x ((Rtop + Rbottom)/Rbottom)
VLDO1 = 0.5 x ((Rtop + Rbottom)/Rbottom)
VLDO2 = VFB_LDO x ((Rtop + Rbottom)/Rbottom)
VLDO2 = 0.5 x ((Rtop + Rbottom)/Rbottom)
CURRENT MONITOR
CURRENT MONITOR
CURRENT MONITOR
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: POWER SUPPLY 0V9/1V8_A1V8B
Size:B DWG NO 512872-0001 Revision: B
Date: Thursday, April 28, 2011 Sheet 55 of 58
U10
TPS65601
U5
TPS3808G09DBVRG4
Reset Threshold 0.84 Volts


POWER DOMAINS
EVM_12V
EVM_5V0
EVM_3V3
EVM_1V8_A
EVM_1V8_D
EVM_1V5
EVM_1V0_AVS
EVM_1V0_CONN
EVM_0V9
EVM_DDR_VTT
12 VOLT INPUT FROM EXTERNAL POWER SUPPLY
5.0 VOLT OUTPUT FROM TPS65232
3.3 VOLT OUTPUT FROM TPS65232
1.8 VOLT ANALOG LDO OUTPUT FROM TPS65001
1.8 VOLT DIGITAL OUTPUT FROM TPS65001
1.5 VOLT OUTPUT FROM TPS54620
1.0 VOLT CORE FROM TPS40041
1.0 VOLT NON-CORE FROM TPS65232
0.9 VOLT OUTPUT FROM TPS65001
0.75 VOLT TERMINATOR DDR3
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: POWER INPUT
Size:B DWG NO 512872-0001 Revision: A
Date: Thursday, April 28, 2011 Sheet 56 of 58
BOARD MOUNTING HOLES - FOR EXPANSION CONNECTORS
BOARD MOUNTING HOLES - ONE IN EACH CORNER
Mounting holes 0.250 pad 0.125 drill
PUSHBUTTON SW
FAN CONNECTOR
HEADER 3
TPS3809G09DBVRG4
Reset Threhold 0.84 Volts
2.5 MM JACK
RASM712
SMCJ14A-13-F
PCB EDGE
DRIVE CONN
Left most for Drive Cable
1) 12V
SILKSCREEN:
12V IN


EVM_3V3
EVM_1V8_D
EVM_1V8_A
EVM_1V5
EVM_1V0_CON
EVM_1V0_AVS
EVM_0V9
VOLTS
3.5
3.0
2.0
1.0
MILLISECONDS
10
20
30
40
50
60
70
80
90
SPECTRUM DIGITAL INCORPORATED
Title: NETRA EVM
Page Contents: POWER SEQUENCE
Size:B
DWG NO 512872-0001
Revision: B
Date: Thursday, April 28, 2011
Sheet 57 of 58

REVISION A - ASSY 512870

BUILT ON PWB 512871 REVISION A
BUILT ON LOGIC 512872 REVISION A

ENGINEERING UNITS ONLY

REVISION B - ASSY 512870

BUILT ON PWB 512871 REVISION B
BUILT ON LOGIC 512872 REVISION B

UPDATED POWER SEQUENCING FROM REVISION A

REVISION C - ASSY 512870

BUILT ON PWB 512871 REVISION B
BUILT ON LOGIC 512872 REVISION B

INCREASED C635 TO .22uF FOR LONGER POWER ON RESET FIXED USB ISSUE

CHANGED R218 TO 1K TO FIX PCI RESET

REMOVED R232 AND CHANGED R74 TO 0 , TO HELP RAISE VT ENABLE VOLTAGE (STILL A BIT OUT OF SPEC, WILL FIX IN NEXT BOARD REVISION)

REVISION D - ASSY 512870

BUILT ON PWB 512871 REVISION B
BUILT ON LOGIC 512872 REVISION B

CHANGED AVS CIRCUITRY AND CPU HAS AVS ENABLED

REVISION E - ASSY 512870

BUILT ON PWB 512871 REVISION C
BUILT ON LOGIC 512872 REVISION C

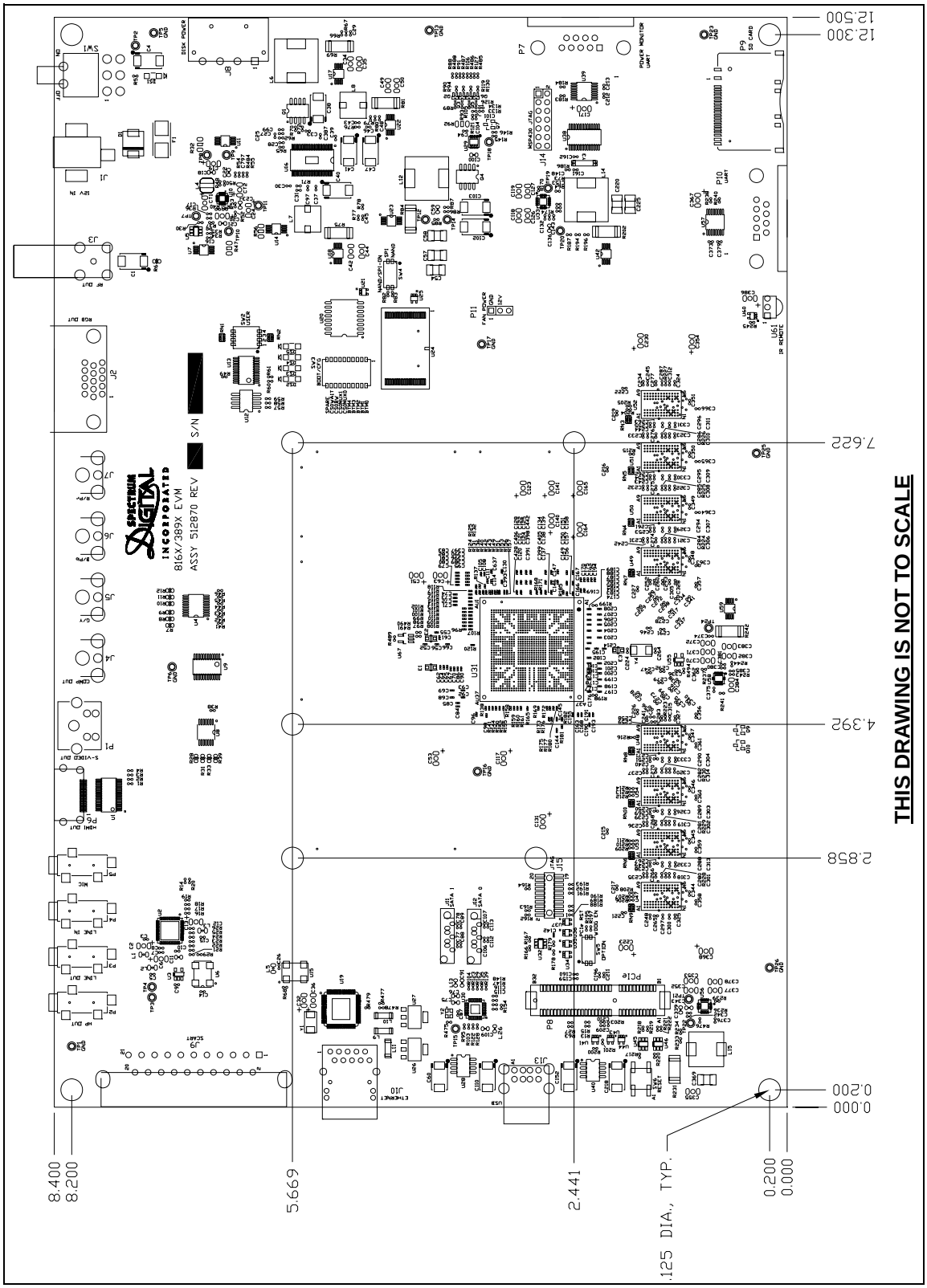
UPDATED CAPS AROUND TPS65232 TO HELP WITH OVERVOLTAGE ON SWITCH OUTPUTS OF THE PART LAYOUT IMPROVEMENT
UPDATED VTT ENABLE TO RAISE ENABLE VOLTAGE PAST 1.7V MIN

SPECTRUM DIGITAL INCORPORATED			
Title: NETRA EVM			
Page Contents: REVISION HISTORY			
Size:B	DWG NO 512872-0001		Revision: C
Date: Tuesday, June 14, 2011		Sheet 58 of 58	

Appendix B

Mechanical Information

This appendix contains the mechanical information about the DM816x/C6A816x/AM389x EVM produced by Spectrum Digital.


12.500
12.300
7.622
4.392
2.858
0.200
0.000
8.400
8.200
5.669
2.441
0.200
0.000
.125 DIA., TYP.
THIS DRAWING IS NOT TO SCALE
SPECTRUM DIGITAL INCORPORATED
816X/389X EVM
ASSY 512870 REV
S/N

SPECTRUM DIGITAL INCORPORATED

Printed in U.S.A., October 2011
512875-0001 Rev A