

Détermination de propriétés de flots de données pour l'amélioration du temps d'exécution pire-cas

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- 1 Introduction
- 2 Problématique et contexte
- 3 Solution
- 4 Ouvertures et conclusion

Plan

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Introduction



Équipe TRACES

Plan

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Estimation du pire temps d'exécution (WCET)

- But : surestimer le temps d'exécution d'une partie de programme
- Exemples
 - Le frein de voiture s'activera au pire 50ms après la commande
 - L'algorithme prendra une décision en moins d'1s
 - ...

Estimation du pire temps d'exécution (WCET)

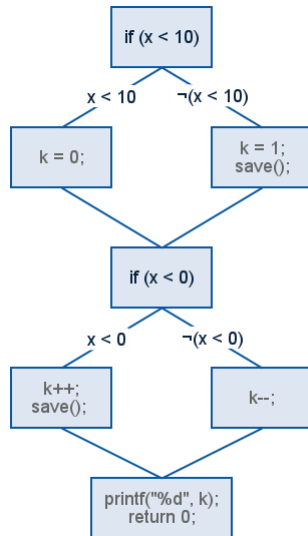
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 - Le frein de voiture s'activera au pire 50ms après la commande
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- Systèmes temps-réel critiques : les mesures ne suffisent pas, il faut une **preuve** !

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 - ...
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- Calcul du pire-temps : maximisation en ILP
 - $WCET = \max \sum x_i t_i$
+ contraintes matérielles + contraintes logicielles

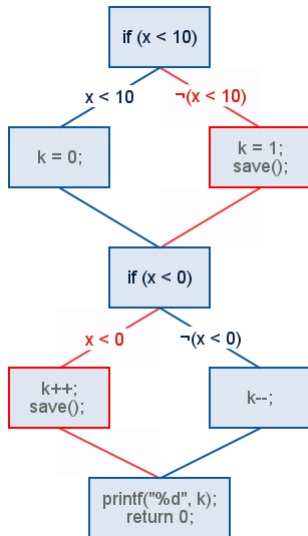
Recherche de chemins infaisables

- Graphe de flot de contrôle



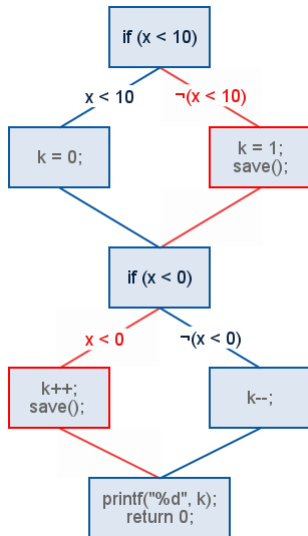
Recherche de chemins infaisables

- Graphe de flot de contrôle
- Chemins + SMT
 - $(x < 10) \wedge (x < 0)$
 - $(x < 10) \wedge \neg(x < 0)$
 - $\neg(x < 10) \wedge (x < 0) \models \perp$
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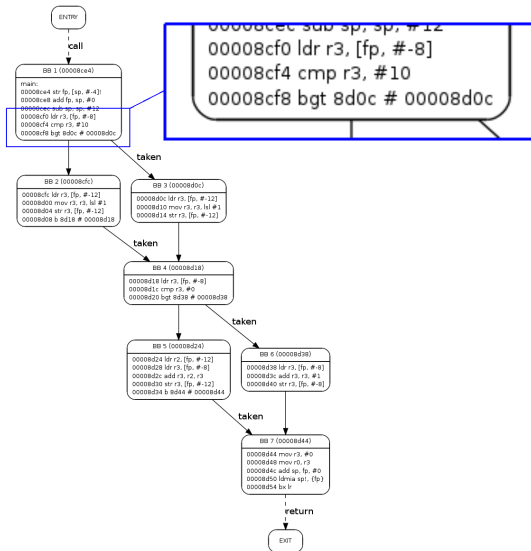


Recherche de chemins infaisables

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 - $\neg(x < 10) \wedge (x < 0) \models \perp$
 - $\neg(x < 10) \wedge \neg(x < 0)$
- Chemin infaisable
 \Rightarrow contrainte ILP
 $n_{(x < 0)} \leq n_{(x < 10)}$



Graphe en langage machine



Choix du solveur SMT

Notre choix de solveur s'est porté sur **CVC4** :

- Open-source, licence très libre



Choix du solveur SMT

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Choix du solveur SMT

Notre choix de solveur s'est porté sur **CVC4** :

- Open-source, licence très libre
- De très bons résultats à la SMT-COMP
- Une API C++ riche et bien documentée



Les instructions sémantiques d'OTAWA

```
ldr r0, [pc, #20]
@ seti ?15, 0x8310
@ seti t2, 0x14
@ add t1, ?15, t2
@ load ?0, t1, uint32
```

```
mov r1, #0
@ seti ?1, 0x0
```

```
mov r2, r1
@ set t1, ?1
@ set ?2, t1
```

```
bl 8574
@ seti t1, 0x8574
@ seti ?14, 0x8318
@ branch t1
```

Les variables d'OTAWA :

- les registres machine ?0, ?1...(16, 32... ou plus selon l'architecture)
- des variables temporaires t1, t2...
 - locales à une instruction machine (détruites à la fin)
 - aident à la traduction en instructions sémantiques

Les instructions sémantiques d'OTAWA

Des instructions...

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- logiques : ~~NOT, AND, OR, XOR~~

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- d'accès mémoire : LOAD, STORE

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- d'accès mémoire : LOAD, STORE

- ~~... et les équivalents *unsigned* : CMPU, MULU, DIVU, MODU~~

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```

15] + ?14 = [(t1 - 4)]
16] - ?4 = [(t1 - t2) - t2]
17] + ?4 = [(t1 - 4) - 4]
18] - ?13 - ((t1 - t2) - t2) = 8
19] + ?13 - ((t1 - 4) - 4) = 8
20] - t2 = 4
21] - ?14 = [t1 - 4]
22] - ?4 = [(t1 - 4) - 4]
23] - ?13 - ((t1 - 4) - 4) = 8
24] bx lr
25] branch ?14
26] Predicates generated: [?0 = 0]
27] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
28] EXIT block reached
29] Processing Edge: BB 5 (000082f4) -> BB 6 (000082fc) (not taken)
30] SMT call: UNSAT
31] [Inf. path found: [1->3, 5->6] (bitcode=101)]
32] Current path identified as infeasible, stopping analysis
33] Processing Edge: BB 1 (000082d8) -> BB 2 (000082e8) (not taken)
34] SMT call: SAT
35] Processing BB 2 (000082e8)
36] bl 8278
37] seti t1, 0x8278 (33400)
38] + t1 = 0x8278
39] seti ?14, 0x82ec (33516)
40] + ?14 = 0x82ec
41] branch t1
42] - t1 = 0x8278
43] Predicates generated: [?14 = 0x82ec]
44] Processing Edge: BB 2 (000082e8) -> BB 4 (000082ec) (not taken)
45] SMT call: SAT
46] Processing BB 4 (000082ec)
47] b 82f4
48] seti t1, 0x82f4 (33524)
49] + t1 = 0x82f4
50] branch t1
51] - t1 = 0x82f4
    
```

```

161] load ?14, t1, shift
162] - (?14 = 0x8318 | 9->10)
163] + ?14 = [t1]
164] add t1, t1, t2
165] [t1 - t2 / t1]
166] - ?14 = [t1]
167] + ?14 = [t1 - t2]
168] - ?4 = [t1 - t2]
169] + ?4 = [(t1 - t2) - t2]
170] - t3 - (t1 - t2) = 8
171] + t3 - ((t1 - t2) - t2) = 8
172] - t1 - t2 = ?13
173] + (t1 - t2) - t2 = ?13
174] set ?13, t3
175] - (t1 - t2) - t2 = ?13
176] + ?13 = t3
177] [?13 / t3]
178] - t3 - ((t1 - t2) - t2) = 8
179] + ?13 - ((t1 - t2) - t2) = 8
180] - ?13 = t3
181] [4 / t2]
182] - ?14 = [t1 - t2]
183] + ?14 = [t1 - 4]
184] - ?4 = [(t1 - t2) - t2]
185] + ?4 = [(t1 - 4) - 4]
186] - ?13 - ((t1 - t2) - t2) = 8
187] + ?13 - ((t1 - 4) - 4) = 8
188] - t2 = 4
189] - ?14 = [t1 - 4]
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192] bx lr
193] branch ?14
194] Predicates generated: [?0 = 0]
195] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
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197] 1 infeasible path found:
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15] + ?13 - ((t1 - 4) - 4) = 8
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10] seti t1, 0x8278 (33400)
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16] SMT call: SAT
16] Processing BB 4 (000082ec)
12] b 82f4
10] seti t1, 0x82f4 (33524)
10] + t1 = 0x82f4
10] branch t1
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```

17] add ?13, t2, #10
117] - (?14 = 0x8318 | 9->10)
188] + ?14 = [t1]
130] add t1, t1, t2
116] [t1 - t2 / t1]
145] - ?14 = [t1]
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131] - (t1 - t2) - t2 = ?13
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100] [?13 / t3]
104] - t3 - ((t1 - t2) - t2) = 8
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27] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
28] EXIT block reached
29] Processing Edge: BB 5 (000082f4) -> BB 6 (000082fc) (not taken)
30] SMT call: UNSAT
31] [Inf. path found: [1->3, 5->6] (bitcode=101)]
32] Current path identified as infeasible, stopping analysis
33] Processing Edge: BB 1 (000082d8) -> BB 2 (000082e8) (not taken)
34] SMT call: SAT
35] Processing BB 2 (000082e8)
36] bl 8278
37] seti t1, 0x8278 (33400)
38] + t1 = 0x8278
39] seti ?14, 0x82ec (33516)
40] + ?14 = 0x82ec
41] branch t1
42] - t1 = 0x8278
43] Predicates generated: [?14 = 0x82ec]
44] Processing Edge: BB 2 (000082e8) -> BB 4 (000082ec) (not taken)
45] SMT call: SAT
46] Processing BB 4 (000082ec)
47] b 82f4
48] seti t1, 0x82f4 (33524)
49] + t1 = 0x82f4
50] branch t1
51] - t1 = 0x82f4

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161] load ?14, t1, 82f4
162] - (?14 = 0x8318 | 9->10)
163] + ?14 = [t1]
164] add t1, t1, t2
165] [t1 - t2 / t1]
166] - ?14 = [t1]
167] + ?14 = [t1 - t2]
168] - ?4 = [t1 - t2]
169] + ?4 = [(t1 - t2) - t2]
170] - t3 - (t1 - t2) = 8
171] + t3 - ((t1 - t2) - t2) = 8
172] - t1 - t2 = ?13
173] + (t1 - t2) - t2 = ?13
174] set ?13, t3
175] - (t1 - t2) - t2 = ?13
176] + ?13 = t3
177] [?13 / t3]
178] - t3 - ((t1 - t2) - t2) = 8
179] + ?13 - ((t1 - t2) - t2) = 8
180] - ?13 = t3
181] [4 / t2]
182] - ?14 = [t1 - t2]
183] + ?14 = [t1 - 4]
184] - ?4 = [(t1 - t2) - t2]
185] + ?4 = [(t1 - 4) - 4]
186] - ?13 - ((t1 - t2) - t2) = 8
187] + ?13 - ((t1 - 4) - 4) = 8
188] - t2 = 4
189] - ?14 = [t1 - 4]
190] - ?4 = [(t1 - 4) - 4]
191] - ?13 - ((t1 - 4) - 4) = 8
192] bx lr
193] branch ?14
194] Predicates generated: [?0 = 0]
195] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
196] EXIT block reached
197] 1 infeasible path found:
198] - [1->3, 5->6]

```

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15] + ?14 = [(t1 - 4)]
14] - ?4 = [(t1 - t2) - t2]
15] + ?4 = [(t1 - 4) - 4]
14] - ?13 - ((t1 - t2) - t2) = 8
15] + ?13 - ((t1 - 4) - 4) = 8
10] - t2 = 4
14] - ?14 = [(t1 - 4)]
14] - ?4 = [(t1 - 4) - 4]
14] - ?13 - ((t1 - 4) - 4) = 8
12] bx lr
10] branch ?14
13] Predicates generated: [?0 = 0]
12] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
12] EXIT block reached
12] Processing Edge: BB 5 (000082f4) -> BB 6 (000082fc) (not taken)
16] SMT call: UNSAT
13] [Inf. path found: [1->3, 5->6] (bitcode=101)]
12] Current path identified as infeasible, stopping analysis
12] Processing Edge: BB 1 (000082d8) -> BB 2 (000082e8) (not taken)
16] SMT call: SAT
16] Processing BB 2 (000082e8)
12] bl 8278
10] seti t1, 0x8278 (33400)
14] + t1 = 0x8278
10] seti ?14, 0x82ec (33516)
14] + ?14 = 0x82ec
10] branch t1
10] - t1 = 0x8278
13] Predicates generated: [?14 = 0x82ec]
12] Processing Edge: BB 2 (000082e8) -> BB 4 (000082ec) (not taken)
16] SMT call: SAT
16] Processing BB 4 (000082ec)
12] b 82f4
10] seti t1, 0x82f4 (33524)
14] + t1 = 0x82f4
10] branch t1
10] - t1 = 0x82f4
    
```

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16] add ?14, t1, #10
117] - (?14 = 0x8318 | 9->10)
188] + ?14 = [t1]
130] add t1, t1, t2
116] [(t1 - t2 / t1)]
145] - ?14 = [t1]
153] + ?14 = [t1 - t2]
145] - ?4 = [t1 - t2]
153] + ?4 = [(t1 - t2) - t2]
145] - t3 - (t1 - t2) = 8
153] + t3 - ((t1 - t2) - t2) = 8
145] - t1 - t2 = ?13
153] + (t1 - t2) - t2 = ?13
130] set ?13, t3
131] - (t1 - t2) - t2 = ?13
188] + ?13 = t3
100] [?13 / t3]
104] - t3 - ((t1 - t2) - t2) = 8
105] + ?13 - ((t1 - t2) - t2) = 8
160] - ?13 = t3
100] [4 / t2]
104] - ?14 = [t1 - t2]
105] + ?14 = [t1 - 4]
104] - ?4 = [(t1 - t2) - t2]
105] + ?4 = [(t1 - 4) - 4]
104] - ?13 - ((t1 - t2) - t2) = 8
105] + ?13 - ((t1 - 4) - 4) = 8
160] - t2 = 4
174] - ?14 = [t1 - 4]
174] - ?4 = [(t1 - 4) - 4]
174] - ?13 - ((t1 - 4) - 4) = 8
122] bx lr
130] branch ?14
103] Predicates generated: [?0 = 0]
102] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
152] EXIT block reached
129] 1 infeasible path found:
144] - [1->3, 5->6]
    
```



```

35] + ?14 = [t1 - 4]
34] - ?4 = [(t1 - t2) - t2]
35] + ?4 = [(t1 - 4) - 4]
34] - ?13 - ((t1 - t2) - t2) = 8
35] + ?13 - ((t1 - 4) - 4) = 8
30] - t2 = 4
34] - ?14 = [t1 - 4]
34] - ?4 = [(t1 - 4) - 4]
34] - ?13 - ((t1 - 4) - 4) = 8
32] bx lr
30] branch ?14
33] Predicates generated: [?0 = 0]
32] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
32] EXIT block reached
32] Processing Edge: BB 5 (000082f4) -> BB 6 (000082fc) (not taken)
36] SMT call: UNSAT
33] [Inf. path found: [1->3, 5->6] (bitcode=101)]
32] Current path identified as infeasible, stopping analysis
32] Processing Edge: BB 1 (000082d8) -> BB 2 (000082e8) (not taken)
36] SMT call: SAT
36] Processing BB 2 (000082e8)
32] bl 8278
30] seti t1, 0x8278 (33400)
38] + t1 = 0x8278
30] seti ?14, 0x82ec (33516)
38] + ?14 = 0x82ec
30] branch t1
30] - t1 = 0x8278
33] Predicates generated: [?14 = 0x82ec]
32] Processing Edge: BB 2 (000082e8) -> BB 4 (000082ec) (not taken)
36] SMT call: SAT
36] Processing BB 4 (000082ec)
32] b 82f4
30] seti t1, 0x82f4 (33524)
38] + t1 = 0x82f4
30] branch t1
30] - t1 = 0x82f4
    
```

```

317] - (?14 = 0x8318 | 9->10)
388] + ?14 = [t1]
330] add t1, t1, t2
316] [t1 - t2 / t1]
345] - ?14 = [t1]
353] + ?14 = [t1 - t2]
345] - ?4 = [t1 - t2]
353] + ?4 = [(t1 - t2) - t2]
345] - t3 - (t1 - t2) = 8
353] + t3 - ((t1 - t2) - t2) = 8
345] - t1 - t2 = ?13
353] + (t1 - t2) - t2 = ?13
330] set ?13, t3
331] - (t1 - t2) - t2 = ?13
388] + ?13 = t3
300] [?13 / t3]
304] - t3 - ((t1 - t2) - t2) = 8
305] + ?13 - ((t1 - t2) - t2) = 8
360] - ?13 = t3
300] [4 / t2]
304] - ?14 = [t1 - t2]
305] + ?14 = [t1 - 4]
304] - ?4 = [(t1 - t2) - t2]
305] + ?4 = [(t1 - 4) - 4]
304] - ?13 - ((t1 - t2) - t2) = 8
305] + ?13 - ((t1 - 4) - 4) = 8
360] - t2 = 4
374] - ?14 = [t1 - 4]
374] - ?4 = [(t1 - 4) - 4]
374] - ?13 - ((t1 - 4) - 4) = 8
322] bx lr
330] branch ?14
303] Predicates generated: [?0 = 0]
302] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
352] EXIT block reached
329] 1 infeasible path found:
344] - [1->3, 5->6]
    
```

```

15] + ?14 = [t1 - 4]
16] - ?4 = [(t1 - t2) - t2]
17] + ?4 = [(t1 - 4) - 4]
18] - ?13 - ((t1 - t2) - t2) = 8
19] + ?13 - ((t1 - 4) - 4) = 8
20] - t2 = 4
21] - ?14 = [t1 - 4]
22] - ?4 = [(t1 - 4) - 4]
23] - ?13 - ((t1 - 4) - 4) = 8
24] bx lr
25] branch ?14
26] Predicates generated: [?0 = 0]
27] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
28] EXIT block reached
29] Processing Edge: BB 5 (000082f4) -> BB 6 (000082fc) (not taken)
30] SMT call: UNSAT
31] [Inf. path found: [1->3, 5->6] (bitcode=101)]
32] Current path identified as infeasible, stopping analysis
33] Processing Edge: BB 1 (000082d8) -> BB 2 (000082e8) (not taken)
34] SMT call: SAT
35] Processing BB 2 (000082e8)
36] bl 8278
37] seti t1, 0x8278 (33400)
38] + t1 = 0x8278
39] seti ?14, 0x82ec (33516)
40] + ?14 = 0x82ec
41] branch t1
42] - t1 = 0x8278
43] Predicates generated: [?14 = 0x82ec]
44] Processing Edge: BB 2 (000082e8) -> BB 4 (000082ec) (not taken)
45] SMT call: SAT
46] Processing BB 4 (000082ec)
47] b 82f4
48] seti t1, 0x82f4 (33524)
49] + t1 = 0x82f4
50] branch t1
51] - t1 = 0x82f4

```

```

167] add ?14, t2, #10
168] - (?14 = 0x8318 | 9->10)
169] + ?14 = [t1]
170] add t1, t1, t2
171] [t1 - t2 / t1]
172] - ?14 = [t1]
173] + ?14 = [t1 - t2]
174] - ?4 = [t1 - t2]
175] + ?4 = [(t1 - t2) - t2]
176] - t3 - (t1 - t2) = 8
177] + t3 - ((t1 - t2) - t2) = 8
178] - t1 - t2 = ?13
179] + (t1 - t2) - t2 = ?13
180] set ?13, t3
181] - (t1 - t2) - t2 = ?13
182] + ?13 = t3
183] [?13 / t3]
184] - t3 - ((t1 - t2) - t2) = 8
185] + ?13 - ((t1 - t2) - t2) = 8
186] - ?13 = t3
187] [4 / t2]
188] - ?14 = [t1 - t2]
189] + ?14 = [t1 - 4]
190] - ?4 = [(t1 - t2) - t2]
191] + ?4 = [(t1 - 4) - 4]
192] - ?13 - ((t1 - t2) - t2) = 8
193] + ?13 - ((t1 - 4) - 4) = 8
194] - t2 = 4
195] - ?14 = [t1 - 4]
196] - ?4 = [(t1 - 4) - 4]
197] - ?13 - ((t1 - 4) - 4) = 8
198] bx lr
199] branch ?14
200] Predicates generated: [?0 = 0]
201] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
202] EXIT block reached
203] 1 infeasible path found:
204] - [1->3, 5->6]

```

```

15] + ?14 = [(t1 - 4)]
16] - ?4 = [(t1 - t2) - t2]
17] + ?4 = [(t1 - 4) - 4]
18] - ?13 - ((t1 - t2) - t2) = 8
19] + ?13 - ((t1 - 4) - 4) = 8
20] - t2 = 4
21] - ?14 = [t1 - 4]
22] - ?4 = [(t1 - 4) - 4]
23] - ?13 - ((t1 - 4) - 4) = 8
24] bx lr
25] branch ?14
26] Predicates generated: [?0 = 0]
27] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
28] EXIT block reached
29] Processing Edge: BB 5 (000082f4) -> BB 6 (000082fc) (not taken)
30] SMT call: UNSAT
31] [Inf. path found: [1->3, 5->6] (bitcode=101)]
32] Current path identified as infeasible, stopping analysis
33] Processing Edge: BB 1 (000082d8) -> BB 2 (000082e8) (not taken)
34] SMT call: SAT
35] Processing BB 2 (000082e8)
36] bl 8278
37] seti t1, 0x8278 (33400)
38] + t1 = 0x8278
39] seti ?14, 0x82ec (33516)
40] + ?14 = 0x82ec
41] branch t1
42] - t1 = 0x8278
43] Predicates generated: [?14 = 0x82ec]
44] Processing Edge: BB 2 (000082e8) -> BB 4 (000082ec) (not taken)
45] SMT call: SAT
46] Processing BB 4 (000082ec)
47] b 82f4
48] seti t1, 0x82f4 (33524)
49] + t1 = 0x82f4
50] branch t1
51] - t1 = 0x82f4
    
```

```

162] load ?14, t1, shift
163] - (?14 = 0x8318 | 9->10)
164] + ?14 = [t1]
165] add t1, t1, t2
166] [t1 - t2 / t1]
167] - ?14 = [t1]
168] + ?14 = [t1 - t2]
169] - ?4 = [t1 - t2]
170] + ?4 = [(t1 - t2) - t2]
171] - t3 - (t1 - t2) = 8
172] + t3 - ((t1 - t2) - t2) = 8
173] - t1 - t2 = ?13
174] + (t1 - t2) - t2 = ?13
175] set ?13, t3
176] - (t1 - t2) - t2 = ?13
177] + ?13 = t3
178] [?13 / t3]
179] - t3 - ((t1 - t2) - t2) = 8
180] + ?13 - ((t1 - t2) - t2) = 8
181] - ?13 = t3
182] [4 / t2]
183] - ?14 = [t1 - t2]
184] + ?14 = [t1 - 4]
185] - ?4 = [(t1 - t2) - t2]
186] + ?4 = [(t1 - 4) - 4]
187] - ?13 - ((t1 - t2) - t2) = 8
188] + ?13 - ((t1 - 4) - 4) = 8
189] - t2 = 4
190] - ?14 = [t1 - 4]
191] - ?4 = [(t1 - 4) - 4]
192] - ?13 - ((t1 - 4) - 4) = 8
193] bx lr
194] branch ?14
195] Predicates generated: [?0 = 0]
196] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
197] EXIT block reached
198] 1 infeasible path found:
199] - [1->3, 5->6]
    
```

```

15] + ?14 = [(t1 - 4)]
14] - ?4 = [(t1 - t2) - t2]
15] + ?4 = [(t1 - 4) - 4]
14] - ?13 - ((t1 - t2) - t2) = 8
15] + ?13 - ((t1 - 4) - 4) = 8
10] - t2 = 4
14] - ?14 = [(t1 - 4)]
14] - ?4 = [(t1 - 4) - 4]
14] - ?13 - ((t1 - 4) - 4) = 8
12] bx lr
10] branch ?14
13] Predicates generated: [?0 = 0]
12] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
12] EXIT block reached
12] Processing Edge: BB 5 (000082f4) -> BB 6 (000082fc) (not taken)
16] SMT call: UNSAT
13] [Inf. path found: [1->3, 5->6] (bitcode=101)]
12] Current path identified as infeasible, stopping analysis
12] Processing Edge: BB 1 (000082d8) -> BB 2 (000082e8) (not taken)
16] SMT call: SAT
16] Processing BB 2 (000082e8)
12] bl 8278
10] seti t1, 0x8278 (33400)
10] + t1 = 0x8278
10] seti ?14, 0x82ec (33516)
10] + ?14 = 0x82ec
10] branch t1
10] - t1 = 0x8278
13] Predicates generated: [?14 = 0x82ec]
12] Processing Edge: BB 2 (000082e8) -> BB 4 (000082ec) (not taken)
16] SMT call: SAT
16] Processing BB 4 (000082ec)
12] b 82f4
10] seti t1, 0x82f4 (33524)
10] + t1 = 0x82f4
10] branch t1
10] - t1 = 0x82f4
    
```

```

16] add ?14, t2, #16
117] - (?14 = 0x8318 | 9->10)
188] + ?14 = [t1]
130] add t1, t1, t2
116] [(t1 - t2 / t1)]
145] - ?14 = [t1]
153] + ?14 = [t1 - t2]
145] - ?4 = [t1 - t2]
153] + ?4 = [(t1 - t2) - t2]
145] - t3 - (t1 - t2) = 8
153] + t3 - ((t1 - t2) - t2) = 8
145] - t1 - t2 = ?13
153] + (t1 - t2) - t2 = ?13
130] set ?13, t3
131] - (t1 - t2) - t2 = ?13
188] + ?13 = t3
100] [?13 / t3]
104] - t3 - ((t1 - t2) - t2) = 8
105] + ?13 - ((t1 - t2) - t2) = 8
160] - ?13 = t3
100] [4 / t2]
104] - ?14 = [t1 - t2]
105] + ?14 = [t1 - 4]
104] - ?4 = [(t1 - t2) - t2]
105] + ?4 = [(t1 - 4) - 4]
104] - ?13 - ((t1 - t2) - t2) = 8
105] + ?13 - ((t1 - 4) - 4) = 8
160] - t2 = 4
174] - ?14 = [t1 - 4]
174] - ?4 = [(t1 - 4) - 4]
174] - ?13 - ((t1 - 4) - 4) = 8
122] bx lr
130] branch ?14
103] Predicates generated: [?0 = 0]
102] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
152] EXIT block reached
129] 1 infeasible path found:
144] - [1->3, 5->6]
    
```

```

15] + ?14 = [(t1 - 4)]
14] - ?4 = [(t1 - t2) - t2]
15] + ?4 = [(t1 - 4) - 4]
14] - ?13 - ((t1 - t2) - t2) = 8
15] + ?13 - ((t1 - 4) - 4) = 8
10] - t2 = 4
14] - ?14 = [(t1 - 4)]
14] - ?4 = [(t1 - 4) - 4]
14] - ?13 - ((t1 - 4) - 4) = 8
12] bx lr
10] branch ?14
13] Predicates generated: [?0 = 0]
12] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
12] EXIT block reached
12] Processing Edge: BB 5 (000082f4) -> BB 6 (000082fc) (not taken)
16] SMT call: UNSAT
13] [Inf. path found: [1->3, 5->6] (bitcode=101)]
12] Current path identified as infeasible, stopping analysis
12] Processing Edge: BB 1 (000082d8) -> BB 2 (000082e8) (not taken)
16] SMT call: SAT
16] Processing BB 2 (000082e8)
12] bl 8278
10] seti t1, 0x8278 (33400)
18] + t1 = 0x8278
10] seti ?14, 0x82ec (33516)
18] + ?14 = 0x82ec
10] branch t1
10] - t1 = 0x8278
13] Predicates generated: [?14 = 0x82ec]
12] Processing Edge: BB 2 (000082e8) -> BB 4 (000082ec) (not taken)
16] SMT call: SAT
16] Processing BB 4 (000082ec)
12] b 82f4
10] seti t1, 0x82f4 (33524)
18] + t1 = 0x82f4
10] branch t1
10] - t1 = 0x82f4
    
```

```

16] add ?13, t2, #10
117] - (?14 = 0x8318 | 9->10)
188] + ?14 = [t1]
130] add t1, t1, t2
116] [(t1 - t2 / t1)]
145] - ?14 = [t1]
153] + ?14 = [t1 - t2]
145] - ?4 = [t1 - t2]
153] + ?4 = [(t1 - t2) - t2]
145] - t3 - (t1 - t2) = 8
153] + t3 - ((t1 - t2) - t2) = 8
145] - t1 - t2 = ?13
153] + (t1 - t2) - t2 = ?13
130] set ?13, t3
131] - (t1 - t2) - t2 = ?13
188] + ?13 = t3
100] [?13 / t3]
104] - t3 - ((t1 - t2) - t2) = 8
105] + ?13 - ((t1 - t2) - t2) = 8
160] - ?13 = t3
100] [4 / t2]
104] - ?14 = [t1 - t2]
105] + ?14 = [t1 - 4]
104] - ?4 = [(t1 - t2) - t2]
105] + ?4 = [(t1 - 4) - 4]
104] - ?13 - ((t1 - t2) - t2) = 8
105] + ?13 - ((t1 - 4) - 4) = 8
160] - t2 = 4
174] - ?14 = [t1 - 4]
174] - ?4 = [(t1 - 4) - 4]
174] - ?13 - ((t1 - 4) - 4) = 8
122] bx lr
130] branch ?14
103] Predicates generated: [?0 = 0]
102] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
152] EXIT block reached
129] 1 infeasible path found:
144] - [1->3, 5->6]
    
```

```

15] + ?14 = [(t1 - 4)]
16] - ?4 = [(t1 - t2) - t2]
17] + ?4 = [(t1 - 4) - 4]
18] - ?13 - ((t1 - t2) - t2) = 8
19] + ?13 - ((t1 - 4) - 4) = 8
20] - t2 = 4
21] - ?14 = [t1 - 4]
22] - ?4 = [(t1 - 4) - 4]
23] - ?13 - ((t1 - 4) - 4) = 8
24] bx lr
25] branch ?14
26] Predicates generated: [?0 = 0]
27] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
28] EXIT block reached
29] Processing Edge: BB 5 (000082f4) -> BB 6 (000082fc) (not taken)
30] SMT call: UNSAT
31] [Inf. path found: [1->3, 5->6] (bitcode=101)]
32] Current path identified as infeasible, stopping analysis
33] Processing Edge: BB 1 (000082d8) -> BB 2 (000082e8) (not taken)
34] SMT call: SAT
35] Processing BB 2 (000082e8)
36] bl 8278
37] seti t1, 0x8278 (33400)
38] + t1 = 0x8278
39] seti ?14, 0x82ec (33516)
40] + ?14 = 0x82ec
41] branch t1
42] - t1 = 0x8278
43] Predicates generated: [?14 = 0x82ec]
44] Processing Edge: BB 2 (000082e8) -> BB 4 (000082ec) (not taken)
45] SMT call: SAT
46] Processing BB 4 (000082ec)
47] b 82f4
48] seti t1, 0x82f4 (33524)
49] + t1 = 0x82f4
50] branch t1
51] - t1 = 0x82f4
    
```

```

162] load ?14, t1, shift1
163] - (?14 = 0x8318 | 9->10)
164] + ?14 = [t1]
165] add t1, t1, t2
166] [t1 - t2 / t1]
167] - ?14 = [t1]
168] + ?14 = [t1 - t2]
169] - ?4 = [t1 - t2]
170] + ?4 = [(t1 - t2) - t2]
171] - t3 - (t1 - t2) = 8
172] + t3 - ((t1 - t2) - t2) = 8
173] - t1 - t2 = ?13
174] + (t1 - t2) - t2 = ?13
175] set ?13, t3
176] - (t1 - t2) - t2 = ?13
177] + ?13 = t3
178] [?13 / t3]
179] - t3 - ((t1 - t2) - t2) = 8
180] + ?13 - ((t1 - t2) - t2) = 8
181] - ?13 = t3
182] [4 / t2]
183] - ?14 = [t1 - t2]
184] + ?14 = [t1 - 4]
185] - ?4 = [(t1 - t2) - t2]
186] + ?4 = [(t1 - 4) - 4]
187] - ?13 - ((t1 - t2) - t2) = 8
188] + ?13 - ((t1 - 4) - 4) = 8
189] - t2 = 4
190] - ?14 = [t1 - 4]
191] - ?4 = [(t1 - 4) - 4]
192] - ?13 - ((t1 - 4) - 4) = 8
193] bx lr
194] branch ?14
195] Predicates generated: [?0 = 0]
196] Processing Edge: BB 10 (00008318) -> EXIT (virtual)
197] EXIT block reached
198] 1 infeasible path found:
199] - [1->3, 5->6]
    
```

Plan

- 1 Introduction
- 2 Problématique et contexte
- 3 Solution
- 4 Ouvertures et conclusion

Extensions

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The logo for CVC4, featuring the letters 'CVC' in a large, blue, stylized font with a red outline, and a red '4' to its right. The logo is superimposed on a background of SMT-LIA code.

```
(and (or (and (= x0 y0) (=
y0 x1)) (and (= x0 z0)
x1 z0)) (and (= x1 y1) (=
y1 z2)) (or (and (= x2 z1)
x2 z1)) (and (= x2 z2)
y2 x2)) (and (= x2 z2) (= z2
x3))) (not (= x0 x3)))
```

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```
x = (unsigned int) y;
```

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 - Appels au solveur SMT plus intelligents
 - Gérer les spécificités des types de données du langage machine
 - Générer des contraintes ILP ne **suffit plus**
⇒ il faudrait faire de la **réécriture de graphe**.

Conclusion

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- À poursuivre en thèse...

