

Enhanced Serial Peripheral Interface (eSPI) ECN

Engineering Change Notice

TITLE	Support for Host & CPU to access an BMC integrated RTC
DATE	11 July 2020
AFFECTED DOCUMENT	eSPI Base Specification (Revision 1.0) eSPI Addendum for Server Platforms (Revision 0.7)
DISCLOSURE RESTRICTIONS	CNDA or eSPI Click to Accept License Agreement



Intel hereby grants you a fully-paid, non-exclusive, non-transferable, worldwide, limited license (without the right to sublicense), under its copyrights to view, download, and reproduce the Enhanced Serial Peripheral Interface (eSPI) Specification ("Specification"). You are not granted any other rights or licenses, by implication, estoppel, or otherwise, and you may not create any derivative works of the Specification.

The Specification is provided "as is," and Intel makes no representations or warranties, express or implied, including warranties of merchantability, fitness for a particular purpose, non-infringement, or title. Intel is not liable for any direct, indirect, special, incidental, or consequential damages arising out of any use of the Specification, or its performance or implementation.

Intel retains ownership of all of its intellectual property rights in the Specification and retains the right to make changes to the Specification at any time. No license is granted to use Intel's name, trademarks, or patents.

If you provide feedback or suggestions on the Specification, you grant Intel a perpetual, non-terminable, fully-paid, non-exclusive, worldwide license, with the right to sublicense, under all applicable intellectual property rights to use the feedback and suggestions, without any notice, consent, or accounting. You represent and warrant that you own, or have sufficient rights from the owner of, the feedback and suggestions, and the intellectual property rights in them, to grant the above license.

This agreement is governed by Delaware law, without reference to choice of law principles. Any disputes relating to this agreement must be resolved in the federal or state courts in Delaware and you consent, and will not object, to the exclusive personal jurisdiction of the courts in Delaware.

This agreement is the entire agreement of the parties regarding the Specification and supersedes all prior agreements or representations.

THIS SPECIFICATION IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION, OR SAMPLE.

Except for a limited copyright license to copy this specification for internal use only, no license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

Intel Corporation and the authors of this specification disclaim all liability, including liability for infringements of proprietary rights, relating to implementation of information in this document and the specification. Intel Corporation and the authors of this specification also do not warrant or represent that such implementation(s) will not infringe such rights.

Implementations developed using the information provided in this specification may infringe the patent rights of various parties including the parties involved in the development of this specification. Except as expressly granted hereunder, no license, express or implied, by estoppel or otherwise, to any intellectual property rights (including without limitation rights under any party's patents) is granted.

All suggestions or feedback related to this specification become the property of Intel Corporation upon submission.

Intel may make changes to the specifications, product descriptions, and plans at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

This document is an intermediate draft for comment only and is subject to change without notice. Do not finalize a design based on this document.

Intel and the Intel logo are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

* Other names and brands may be claimed as the property of others.

Copyright 2020, Intel Corporation. All rights reserved.



ECN Motivation

As the manufacturing process is optimize, integrating a real time clock (RTC) on Intel's silicon will no longer be possible on future platform generations. The RTC clock and the RTC RAM content cannot be active for an extended length of time (which varies per platform segment, between 180 days to 7 years), due to the reduction of number of nodes on the optimize manufacturing process.

The eSPI Base Specification (revision 1.0) describes bit 29 of the General Capabilities and Configuration register (offset 08h) as reserved. This ECN provides a description and details of this bit 29 update.



ECN Description

Intel's next generation platforms facilitates the use of the RTC in the Baseboard Management Controller (BMC).

Note: consult with your BMC vendor of choice about support for the following bit configuration update.

Current eSPI Base Specification (revision 1.0):

7.2.1.3 Offset 08h: General Capabilities and Configurations

This register is also reset by the In-band RESET command.

Bit	Type	Default	Description
29	RO	0	Reserved.

Update to eSPI Base Specification (revision 1.0):

eSPI master will read bit[29] of the general capabilities and configurations register (offset 0x8).

Offset 08h: General Capabilities and Configurations

Bit	Type	Default	Description
29	RO	0	RTC-integrated-BMC 1: BMC supports an integrated RTC to which eSPI master can forward RTC targeting IO cycles 0: BMC does not support an integrated RTC

When bit 29 is set (1), RTC cycles are sent downstream as IO Read or IO Write cycles. Please see platform specific eSPI compatibility spec for more details.