RISC-V ACPI Platform Requirements Specification

Sunil V L, RISC-V Platform HSC Group

Version 0.2, 1/27/2022: This document is in Development state. Change should be expected.

Table of Contents

Preamble

This document is in the Development state

Assume everything can change. This draft specification will change before being accepted as standard, so implementations made to this draft specification will likely not conform to the future standard.

Copyright and license information

Contributors

This RISC-V specification has been contributed to directly or indirectly by:

- Sunil V L <sunilvl@ventanamicro.com>
- Anup Patel <apatel@ventanamicro.com>
- Atish Patra <atishp@atishpatra.org>
- Kumar Sankaran <ksankaran@ventanamicro.com>
- Jessica Clarke <jrtc27@jrtc27.com>

Chapter 1. Introduction

RISC-V server class platforms need to support Advanced Configuration and Power Interface (ACPI) as the hardware discovery and configuration mechanism. This document describes the mandatory ACPI tables and objects for RISC-V server platforms. All other ACPI tables not mentioned in this document can be implemented as needed adhering to the ACPI specification.

Chapter 2. Revision History

Date	Revision	Change
01/27/2022	0.2 Draft	New documentation template
01/10/2022	0.1 Draft	Initial Draft

Chapter 3. ACPI Namespace

In ACPI namespace, processors are required to be defined under the System Bus **(_SB)** name space.

Chapter 4. ACPI System Description Tables

The required ACPI System Description Tables, Device Objects and Methods are listed below.

Table 1. Required ACPI System Description Tables

ACPI Table	ACPI Section	Note
Root System Description Pointer (RSDP)	5.2.5	
Extended System Description Table (XSDT)	5.2.8	
Fixed ACPI Description Table (FADT)	5.2.9	
Differentiated System Description Table (DSDT)	5.2.11.1	
Multiple APIC Description Table (MADT)	5.2.12	
RISC-V Hart Capabilities Table (RHCT)	New	To communicate information about hart capabilities like extensions supported etc.
RISC-V Timer Description Table (RTDT)	New	timebase-frequency
Processor Properties Topology Table (PPTT)	5.2.29	CPU and Cache topology information
Memory-mapped Configuration space (MCFG)	See Links to ACPI-Related Documents (uefi.org/acpi) under the heading "PCI Sig"	Required for PCIe support
Debug Port Table 2 (DBG2)	See Links to ACPI-Related Documents (uefi.org/acpi) under the heading “Debug Port Table 2”	
Serial Port Console Redirection (SPCR)	See Links to ACPI-Related Documents (uefi.org/acpi) under the heading “Serial Port Console Redirection Table”	
System Resource Affinity Table (SRAT)	5.2.16	Required if the platform supports NUMA
System Locality Information Table (SLIT)	5.2.17	Required if the platform supports NUMA
Boot Error Record Table (BERT)	18.3.1	RAS APEI
Error Injection Table (EINJ)	18.6.1	RAS APEI

ACPI Table	ACPI Section	Note
Error Record Serialization Table (ERST)	18.5	RAS APEI
Hardware Error Source Table (HEST)	18.3.2	RAS APEI

Chapter 5. ACPI Device Objects and Methods

Table 2. Required Device Objects and Methods

Object/Method	ACPI Section	Note
_AEI	5.6.5.2	Required for GPIO-signalled events
_EVT	5.6.5.3	Required for interrupt-signalled events
_ADR	6.1.1	Required for PCI
_HID	6.1.5	
_UID	6.1.12	
_CRS	6.2.2	
_CCA	6.2.17	Required for DMA capable devices
_STA	6.3.7/7.2.4	Device status

References

- ACPI Specification version 6.4