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- 欢迎在开始的前5分钟进行自我介绍
- 日常八卦在东亚时区RISC-V双周同步微信群中，欢迎加入
- 东亚时区Slides会公开到：https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync/tree/main/biweekly-meetings仓库，并且默认了CC协议

东亚时区RISC-V双周会

2025年09月18日·第 111 次

https://github.com/cnrv/RISCV-East-Asia-Biweekly-Sync

Host: 张馥媛

Organizer: PLCT Lab plct-oss@iscas.ac.cn

会议议程（15:00 - 16:00）

- 自我介绍、等待参会者接入、非技术话题八卦（没有的话就直接跳过）
- RVI 的更新和八卦（基本上跟东亚双周会群内消息同步）
- 东亚地区小伙伴的项目更新
- 自由讨论

RISC-V International 同步、全球开源社区八卦（陈逸轩）

[tech-vme]讨论了行读取，VME是否应该支持累加器直接从内存中 load/store 行或列。
[tech-vector-ext]讨论了 spike 在 SEW/LMUL 比例变化时不将 vill 设置为1，而是进入“保留”的状态、更新了 Zvabd 扩展v0.1.0草案
[tech-attached-matrix-extesion]开始进行未来技术路线投票，视频回放
[sig-perf-analysis]讨论RISC-V PMU ACPI支持方案
[sig-fp]会议改成一月一次
[privileged-software]讨论了 trace context

RISC-V 中文社区的同步与八卦（聂雨婷）

1. SiFive 推出全新 RISC-V IP，融合标量、向量与矩阵运算，加速从边缘物联网到数据中心的 AI 应用
   这代产品强化了SiFive在 RISC-V AI IP 领域的技术领先优势，SiFive正打造一个既开放又具竞争力的体系
2. Cloud Hypervisor 48 引入对 RISC-V 64 位架构的固件启动支持
   行业主流虚拟化方案正在逐渐接受 RISC-V，贡献来自中科院软件所内一位虚拟化工程师。
3. RISC-V Zalasr扩展的Linux内核支持补丁目前已进入审核阶段
   Zalasr 的 v0.9 版本规范已于两个月前定稿，公测期于 8 月结束。
4. RISC-V校园行项目正式启动，欢迎高校登记
   PLCT实验室诚邀广大高校加入“RISC-V校园行”系列活动，点击链接可查看活动详情、扫码登记高校信息
5. RISC-V在中国的十年（五）：国内资本动向与投融资盘点（近三年）
   汇总贴，对RISC-V市场融资感兴趣的老师欢迎跳转阅读

RISC-V 韩语社区的同步与八卦

RISC-V 德语社区的同步与八卦（罗云翔）

产业

- RISC-V: Shaping the Future of Mobility with Open Standards September 17, 2025

  Andrea Gallo：RISC-V 开放、可定制和协作的指令集架构（ISA）模式，正在彻底改变汽车行业的创新方式，使其成为未来移动出行（Mobility）领域的关键推动力。（慕尼黑 RISC-V Automotive Conference 2025）

- From guesswork to guidance: Mastering processor co-design with Codasip Exploration Framework 11 September, 2025

  Codasip：为特定应用定制处理器是提升性能与效率的关键，但手动评估海量配置选项极其困难。Codasip 的自动化探索框架（Exploration Framework）解决了这一难题，它能快速、精准地找到最优的处理器配置，从而显著降低设计风险并加速产品上市时间

- ELIV 2025 October 15 - 16, 2025 Bonn, World Conference Center

  全球最大的汽车电子、软件及应用大会 日程

  Transforming the RISC-V Landscape: The Path to Ecosystem Alignment，Quintauris

- Andes RISC-V CON Munich October 14 2025

  晶心科技年度技术研讨会，2025年10月14日慕尼黑

RISC-V 德语社区的同步与八卦(罗云翔)

学术

- Introducing Instruction-Accurate Simulators for Performance Estimation of Autotuning Workloads RWTH Aachen University, Germany

  面向自动调优工作负载性能评估的指令级精确模拟器解决方案:加速机器学 习(ML)工作负载因其庞大的优化空间需要高效方法。自动调优已成为系统评估实现方案变体的有效手段。传统自动调优需在目标硬件上执行工作负载，文章提出了一种可在模拟器上运行自动调优任务的接口。该方法在目标硬件资源有限时提供高度可扩展性。实验结果表明:经调优的预测器效果显著，包括RISC-V目标硬件上实际运行时间最优的工作负载方案始终位于预测结果的前3%区间。

- FastPath: A Hybrid Approach for Efficient Hardware Security Verification RPTU Kaiserslautern-Landau, Kaiserslautern, Germany

  FastPath面向高效硬件安全验证的混合方案:针对硬件设计领域安全漏洞激增的 现状，研究者已提出多种微架构信息泄露 检测方法。这些精密方案在防范攻 击者破坏系统机密性方面取得 显著成效，但各自存在固有缺陷:或在可 扩展性方面不足，或缺乏穷尽性验证能力，或难以适应变化的需求与 现有验证流程的整合。文章提出 FastPath混合验证方法，结合仿真的高效性与形式化 验证的穷尽性优势。该方案采用结构分析框架 实现自动化验证流程。实验结果表明，与最先 进的形式化方法相比，FastPath在保持同等 穷尽性验证信心的同时，显著降低了人工成本。

RISC-V 日语社区的同步与八卦

RISC-V 中国峰会进展（吴伟）

Clang/LLVM 上游进展

- [RISCV] Support ZVqdot Codegen and C intrinsics

  https://github.com/llvm/llvm-project/commit/7fb1dc08
- [RISCV] Extend zvqdot matching to handle disjoint or

  https://github.com/llvm/llvm-project/commit/33c9236b
- RVP intrinsics support (draft pr)

  https://github.com/llvm/llvm-project/pull/157044

GCC 进展

- Implemented rvp intrinsics in gcc part

  https://github.com/ruyisdk/riscv-gcc/tree/p-dev

- Supported sdtrig and ssstrict extension

  https://patchwork.sourceware.org/project/gcc/patch/20250913021703.1377145-1-chendongyan@isrc.iscas.ac.cn/

- Allow profiles input in '--with-arch' option

  https://patchwork.sourceware.org/project/gcc/patch/20250908112743.1734061-3-jiawei@iscas.ac.cn/

- Fixed testcases for '--with-arch' and '--with-abi' avaliable for binutils

  https://github.com/riscv-collab/riscv-gnu-toolchain/commit/1faa77ffe8daec705aa1ef266e944c554d838881

  https://patchwork.sourceware.org/project/binutils/patch/20250910120916.1103023-1-jiawei@iscas.ac.cn/

QEMU/Spike 进展（呼唤志愿者）

Sail / ACT 上游进展

https://github.com/riscv/sail-riscv/pull/1067 Add VU and VS privilege level H扩展的一部分，添加了对 VS 和 VU 两个特权等级的基础支持

https://github.com/riscv/sail-riscv/pull/1158 Add support for Zfbfmin extension

添加了两个 bfloat16 转换相关指令 fcvt.bf16.s，fcvt.s.bf16

https://github.com/riscv/sail-riscv/pull/1271 Add html doc bundle to build and release

添加了生成html支持，支持语法高亮和代码跳转

alasdair.github.io/sail-riscv/riscv_insts_base.html

```
function clause execute (ITYPE (imm, rs1, rd, op)) = {
  let immext : xlenbits = sign_extend(imm);
  X(rd) = match op {
    ADDI  => X(rs1) + immext,
    SLTI  => zero_extend(bool_to_bits(X(rs1) <_s immext)),
    SLTIU => zero_extend(bool_to_bits(X(rs1) <_u immext)),
    ANDI  => X(rs1) & immext,
    ORI   => X(rs1) | immext,
    XORI  => X(rs1) ^ immext
  };
  RETIRE_SUCCESS
}
```

V8 for RISC-V 更新（邱吉、陆亚涵）

Upload:

1. 6928701: [riscv] Fix custom-descriptors-inlining.js failed | https://chromium-review.googlesource.com/c/v8/v8/+/6928701
2. 6934203: [riscv] Fix build for v8_enable_external_code_space | https://chromium-review.googlesource.com/c/v8/v8/+/6934203
3. 6955146: [riscv] Add Extension Zimop | https://chromium-review.googlesource.com/c/v8/v8/+/6955146

Port:

1. 6914315: [riscv][wasm, codegen] Add skipped write barrier verification to Liftoff | https://chromium-review.googlesource.com/c/v8/v8/+/6914315
2. 6916617: [riscv] Remove external references for allocation space top/limit | https://chromium-review.googlesource.com/c/v8/v8/+/6916617
3. 6907272: [riscv][sandbox] Bottleneck kUnknownIndirectPointerTag | https://chromium-review.googlesource.com/c/v8/v8/+/6907272

Review:

1. 6873190: [riscv] Use shxadd instruction to calculate address for load & store | https://chromium-review.googlesource.com/c/v8/v8/+/6873190
2. 6916101: [riscv] Don't round to zero when doing an i32x4-mul operation | https://chromium-review.googlesource.com/c/v8/v8/+/6916101
3. 6917460: [riscv][compiler] Support skipped write barrier verification in Turbofan | https://chromium-review.googlesource.com/c/v8/v8/+/6917460
4. 6842160: [riscv] Save vector registers when entering the runtime | https://chromium-review.googlesource.com/c/v8/v8/+/6842160
5. 6907272: [riscv][sandbox] Bottleneck kUnknownIndirectPointerTag | https://chromium-review.googlesource.com/c/v8/v8/+/6907272
6. 6918878: [riscv] Fix more rounding modes for SIMD operations | https://chromium-review.googlesource.com/c/v8/v8/+/6918878

Spidermonkey for RISC-V更新（邱吉、陆亚涵）

OpenJDK on RISC-V (PLCT 杨飞)

- Java 25 / JDK 25: General Availability: https://mail.openjdk.org/pipermail/announce/2025-September/000360.html
- Linux-riscv64 binaries available for download: https://bell-sw.com/pages/downloads/#jdk-25-lts

Timelines

JDK 25.0.1 timeline

- Jul 22 2025 RDP2
- Oct 21 2025 GA

JDK 25.0.2 timeline

- Oct 2025 RDP2
- Mid Jan 2026 GA

JDK 25, the reference implementation of Java 25, is now Generally Available. We shipped build 36 as the second Release Candidate of JDK 25 on 15 August, and no P1 bugs have been reported since then. Build 36 is therefore now the GA build, ready for production use.

GPL-licensed OpenJDK builds from Oracle are available here:

https://jdk.java.net/25

Builds from other vendors will no doubt be available soon.

This release includes eighteen JEPs [1]:

470: PEM Encodings of Cryptographic Objects (Preview)
502: Stable Values (Preview)
503: Remove the 32-bit x86 Port
505: Structured Concurrency (Fifth Preview)
506: Scoped Values
507: Primitive Types in Patterns, instanceof, and switch (Third Preview)
508: Vector API (Tenth Incubator)
509: JFR CPU-Time Profiling (Experimental)
510: Key Derivation Function API
511: Module Import Declarations
512: Compact Source Files and Instance Main Methods
513: Flexible Constructor Bodies
514: Ahead-of-Time Command-Line Ergonomics
515: Ahead-of-Time Method Profiling
518: JFR Cooperative Sampling
519: Compact Object Headers
520: JFR Method Timing & Tracing
521: Generational Shenandoah

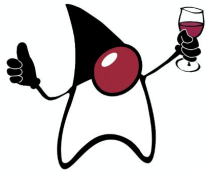
This release also includes, as usual, hundreds of smaller enhancements and thousands of bug fixes.

Thanks to everyone who contributed this release, whether by designing and implementing features or enhancements, by fixing bugs, or by testing the early-access builds!

- Mark

[1] https://openjdk.org/projects/jdk/25/

1. Reviewed JDK-mainline PRs:
- https://github.com/openjdk/jdk/pull/26318 (8362838: RISC-V: Incorrect matching rule leading to improper oop instruction encoding)
- https://github.com/openjdk/jdk/pull/26408 (8357694: RISC-V: Several IR verification tests fail when vlen=128)
- https://github.com/openjdk/jdk/pull/26409 (8362596: RISC-V: Improve _vectorizedHashCode intrinsic)
- https://github.com/openjdk/jdk/pull/26437 (8363898: RISC-V: TestRangeCheckHoistingScaledIV.java fails after JDK-8355293 when running without RVV)
- https://github.com/openjdk/jdk/pull/26481 (8364120: RISC-V: unify the usage of MacroAssembler::instruction_size)
- https://github.com/openjdk/jdk/pull/26719 (8365200: RISC-V: compiler/loopopts/superword/TestGeneralizedReductions.java fails with Zvbb and vlen=128)
- https://github.com/openjdk/jdk/pull/26738 (8365302: RISC-V: compiler/loopopts/superword/TestAlignVector.java fails when vlen=128)
- https://github.com/openjdk/jdk/pull/17413 (8322174: RISC-V: C2 VectorizedHashCode RVV Version)



Go community work update (PLCT 蒙卓)

TL;DR Summary：

- ***zfh/zicond/vector seg load/store，3 more steps to rva23u64 !***
- RVV runtime optimazation reviewing
- RISC-V ELF attributes support upstreaming
- RV Zk asm support upstreaming, runtime/crypto library TBD

1. Authored/Co-authored Go-mainline CLs:
   - 647596: runtime: unify C -> Go ABI transitions on riscv64 | https://go-review.googlesource.com/c/go/+/647596
   - all: add race support for riscv64 | https://github.com/mengzhuo/go/commit/a1b9b0d4faae07a31c599e00ee73aa6b4f882068 https://github.com/golang/go/issues/64345
   - 659175: cmd/link: generate proper attributes for riscv profile | https://go-review.googlesource.com/c/go/+/659175
   - 657036: internal/bytealg: vector implementation of count 1 byte for riscv64 | https://go-review.googlesource.com/c/go/+/657036
   - 663778: cmd/asm, cmd/internal/obj: add zvbb/zvbc/zvkb for riscv64 | https://go-review.googlesource.com/c/go/+/663778
   - 664155: cmd/asm, cmd/internal/obj: add crypto algorithm suites for riscv64 | https://go-review.googlesource.com/c/go/+/664155
   - 664375: cpu: add crypto extensions detection for riscv64 | https://go-review.googlesource.com/c/sys/+/664375
   - 663675: cmd/internal/obj: add crypto extension for riscv64 | https://go-review.googlesource.com/c/go/+/663675
   - 696655:MinimumRequirements: update minimum requirements for riscv64 | https://go-review.googlesource.com/c/wiki/+/696655
   - **697615: cmd/compile: simplify zerorange on riscv64 | https://go-review.googlesource.com/c/go/+/697615 [merged]**
   - **699635: cmd/compile: use generated loops instead of DUFFZERO on riscv64 | https://go-review.googlesource.com/c/go/+/699635 [merged]**
   - **700537: cmd/compile: use generated loops instead of DUFFCOPY on riscv64 | https://go-review.googlesource.com/c/go/+/700537 [merged]**
   - **700538: runtime: remove duff support for riscv64 | https://go-review.googlesource.com/c/go/+/700538 [merged]**
   - 703215: cmd/compile: Const64F by MOVD with const on riscv64 | https://go-review.googlesource.com/c/go/+/703215
   - **702136: cmd/asm: add double precision comparision testcases for riscv64 | https://go-review.googlesource.com/c/go/+/702136【merged】**
   - **702697: cmd/compile: combine doubling with shift on riscv64 | https://go-review.googlesource.com/c/go/+/702697【merged】**
   - **703716: test/codegen: check zerobase for newobject on 0-sized types | https://go-review.googlesource.com/c/go/+/703716【merged】**
   - 702695: cmd/internal/obj: add zfh extensions for riscv64 | https://go-review.googlesource.com/c/go/+/702695
   -

2. Reviewed Go-mainline CLs:
   - 652717: doc, cmd/internal/obj/riscv: document the riscv64 assembler | https://go-review.googlesource.com/c/go/+/652717
   - 646736: internal/bytealg: vector implementation of equal for riscv64 | https://go-review.googlesource.com/c/go/+/646736
   - 646737: internal/bytealg: vector implementation of compare for riscv64 | https://go-review.googlesource.com/c/go/+/646737
   - **670876: riscv64: add support for RVV 1.0 instructions | https://go-review.googlesource.com/c/arch/+/670876 [merged]**
   - 670875: riscv64: fix the path to the RISC-V extensions in spec.go | https://go-review.googlesource.com/c/arch/+/670875
   - cmd/compile: line number debug info regression in go1.25 around literal rewriting | https://github.com/golang/go/issues/74576
   - 348389: cmd/compile: emit classify instructions for infinity tests on riscv64 | https://go-review.googlesource.com/c/go/+/348389
   - 670875: riscv64: fix the path to the RISC-V extensions in spec.go | https://go-review.googlesource.com/c/arch/+/670875
   - 690495: runtime: identify virtual memory layout for riscv64 | https://go-review.googlesource.com/c/go/+/690495
   - **702677: cmd/internal/obj/riscv: add support for Zicond instructions | https://go-review.googlesource.com/c/go/+/702677【merged】**
   - 703715: cmd/compile/internal/ssa: add codegen for Zicond extension on riscv64 | https://go-review.googlesource.com/c/go/+/703715
   - **704775: [release-branch.go1.24] cmd/link: fix cgo on riscv64 when building with gcc-15 | https://go-review.googlesource.com/c/go/+/704775【merege】**
   - **703216: cmd/internal/obj/riscv: improve handling of float point moves | https://go-review.googlesource.com/c/go/+/703216【merged】**
   - **691695: cmd/internal/obj/riscv: implement vector segment load/store instructions | https://go-review.googlesource.com/c/go/+/691695【merged】**
   - **630519: cmd/asm, cmd/internal/obj: add riscv64 generic CSR ops | https://go-review.googlesource.com/c/go/+/630519【merged】**

RuyiSDK (何佩)

本期我们重点优化了发版测试流程，进一步加强了版本发布前的兼容性与文档测试。经过 2 天集中修复，RuyiSDK 0.40 现已正式发布。

包管理器：
RuyiSDK 0.40 对应的包管理器版本也为 0.40.0，已于 9 月 9 日发布。您可移步 GitHub Releases、PyPI 或 ISCAS 镜像源下载体验。

- PyPI：`pip install ruyi`
- GitHub Releases
- ISCAS 镜像源

Note：
RISC-V 用户可以使用 `pip` 安装 `ruyi`，但由于 `ruyi` 依赖的部分 Python 库暂未在 PyPI 上提供 RISC-V 架构的预编译包，安装 `ruyi` 时 Python 包管理器会尝试从源代码编译安装这些依赖，可能非常耗时或编译失败。

本次 RuyiSDK 软件源的更新主要包含了以下内容：

- 完善了设备支持：
  - Sipeed LicheeRV Nano 的 fishwaldo 构建的 Debian：新增了历史版本 1.2.0 与 1.3.0。
  - Milk-V Pioneer 的 RevyOS：更新了 0.20250901.0 版本。
- 工程化迭代：
  - 修复了 `board-image/debian-desktop-sdk-milkv-mars-cm-sd` 的数据结构，并以 CI 形式确保了类似问题不会再发生。

操作系统支持矩阵：

- Dump ArchLinux@Duo_S
- Fix OrangePi-RV metadata

详见RuyiSDK双周进展：https://github.com/ruyisdk/wechat-articles

openEuler RISC-V (周嘉诚)

Status / 20250918

- openEuler 25.09:

  RVA20(Official): Testing in progress

  RVA23(Preview, GCC14.3, Binutils 2.42): Mass-rebuilding
- openEuler 24.03 SP2:

  RVA22+V(Preview, LLVM19): Releasing in progress

- Updates
- RVCK(6.6): Merged DP1000 PCIe driver and dts changes
- RVCK(6.6): Merged backported perf kvm stat support
- Golang: backporting RVA23 changes to 1.21
- xxHash: Merged backported RVV changes
- OpenJDK: add hwprobe Zicboz detection item, pipeline descriptions optimization

Following releases in 2025

- Late Q3 - openEuler 25.09 (RVA20+23*)
- Late Q4 - openEuler 24.03 SP3 (**RVA23**)

Features:

- 6.6-based common kernel for QEMU, Pioneer(SG2042), LPi4A(TH1520), BPi-F3(K1)
- UEFI-supported Hardware & QEMU images

Images:

- UEFI ISO
- UEFI qcow2 Image
- U-Boot Images for devboards

Gentoo for RISC-V 的情况更新（Gentoo 小队）

Arch Linux RISC-V (Felix & PRZ)

- [core] 262 / 273 (95.97%)
- [extra] 14109 / 14513 (97.22%)

- Chromium 140 patches updated.
- Electron 37 patches updated.
- Node.js 24.7 patches updated.
- Sophgo Linux Kernel updated to 6.16.0. Thanks to RevyOS Team!
- GCC 15.1.1 / glibc 2.42 updates still in progress. There are more GCC issues ahead:
  - https://gcc.gnu.org/bugzilla/show_bug.cgi?id=121652
  - https://gcc.gnu.org/bugzilla/show_bug.cgi?id=121534
- ROCm stalled as no builder can build composable-kernel anymore.

Arch Linux RISC-V (Felix & PRZ) - Electron

-

Fedora on RISC-V status update（20250917）

- **RPM packaging (https://www.fedoravforce.com)**
  - Koji Status: F42, GA on Apr 15
    - **F42: 22471 [92.32%] srpm**
    - **F43/rawhide: 6093 [24.90%] srpm**
    - **RVA23**
- **main package version(F43):**
  - Toolchain:
    - gcc-15.1.1-5
    - **glibc-2.42-4**
    - binutils-2.45-1
  - libffi-3.5.1-2
  - **java-25-openjdk-25.0.0.0.36**
  - java-latest-openjdk(24.0.1.0.9-4)
  - perl-5.42.0-520
  - python3.14-3.14.0~rc1-2
  - llvm-20.1.6-1
  - golang-1.24.4-2
  - rust-1.88.0-1

- Desktop support Fedora 43:
  - Building: XFCE/LXDE/GNOME/KDE/Sugar/i3/LXQT/Cinnamon/Sway/Budgie/Mate/Deepin
  - **Key Desktop App**
    - firefox-140.0.4-1
    - libreoffice-25.2.3.1-3
    - Thunderbird-128.12.0-1
    - chromium-137.0.7151.119-1.rv64
- Image and REPOs :
  - https://images.fedoravforce.com
  - Images: rsync://mirror.iscas.ac.cn/fedora-riscv/releases/42/Spins/
  - REOP: rsync://mirror.iscas.ac.cn/fedora-riscv/releases/42/Everything
  -
- ROS/ROS2 upgraded to F42
- Sail for rawhide[UPSTREAMING]
- function testing for F42:
  - **Podman**, **Image**: **fedorariscv/base**
  - Ceph[ONGOING]
  - K8s[ONGOING]

INSTALLATION SUMMARY

FEDORA 42 INSTALLATION

us

LOCALIZATION

Keyboard
English (US)

Time & Date
Restoring hardware time...

SYSTEM

Installation Destination
Automatic partitioning selected

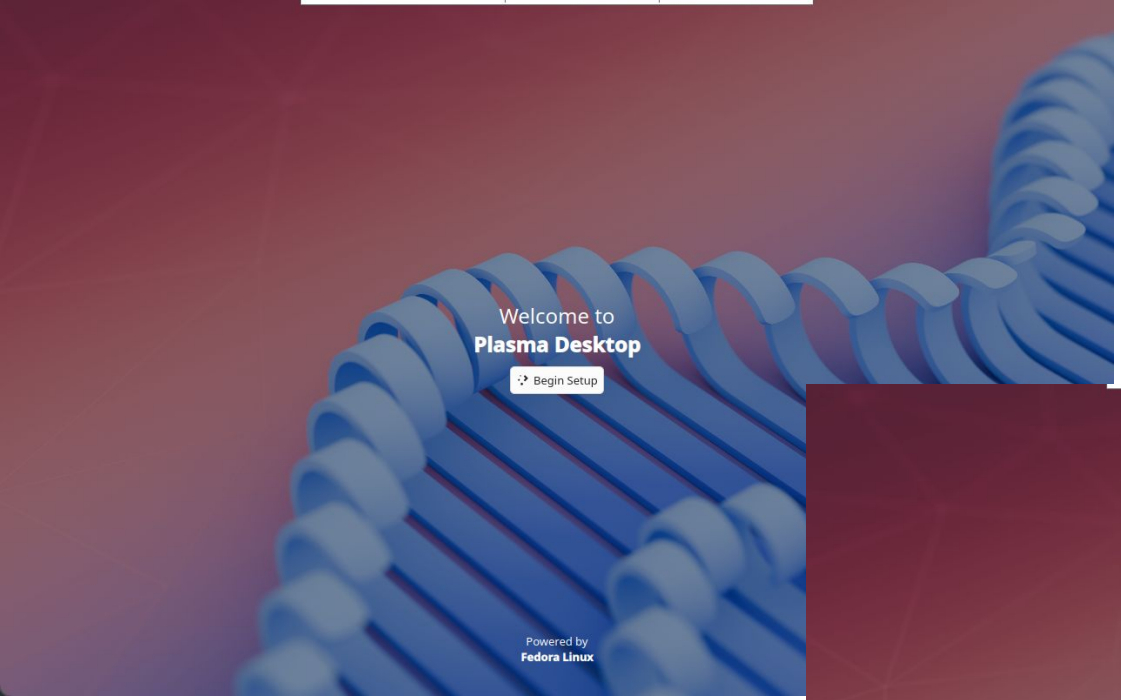
Quit

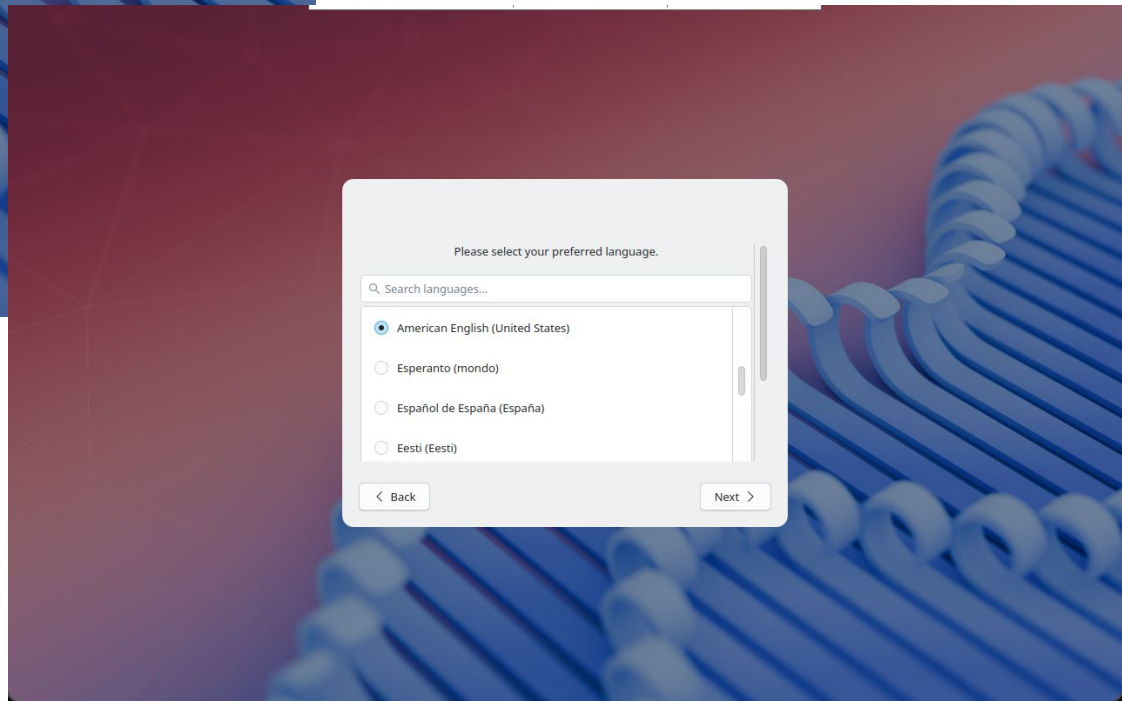
Begin Installation

We won't touch your disks until you click 'Begin Installation'.

Please complete items marked with this icon before continuing to the next step.

Time zone is not set; click here to open Date & Time settings and set one


Welcome to
Plasma Desktop
Begin Setup
Powered by
Fedora Linux


Please select your preferred language.
Search languages...
American English (United States)
Esperanto (mondo)
Español de España (España)
Eesti (Eesti)
Back
Next

CentOS on RISC-V status update（20250918）

- **RPM packaging (https://www.fedoravforce.com)**
  - Koji Status: **working on C10S repo**
    - **C10S: 2200+ [99%] srpm**
    - **EPEL: 3140 [49%] srpm**
    - **RVA23**
- **main package version(C10S):**
  - Toolchain:
    - gcc
    - **glibc**
    - **binutils**
  - libffi
  - **java-21-openjdk**
  - **java-latest-openjdk**
  - **perl**
  - python3.12
  - **llvm**
  - **golang**
  - **rust**
- Desktop support C10S:
  - **DONE: GNOME**
  - **Key Desktop App**
    - **firefox**
    - libreoffice
    - **Thunderbird**
- Image and REPOs :
  - https://openkoji.iscas.ac.cn/pub/temp/c10s-50ffc0f3/
  - https://openkoji.iscas.ac.cn/pub/centos-riscv/10-stream/BaseOS/riscv64/os/
  -
- function testing for C10S:
  - **Podman, Image: fedorariscv/base (ongoing)**
  - **EPEL (ongoing)**

Debian for RISC-V（于波）

- **Official port update**

  0. golang-1.24/1.25 ftbfs on riscv64 due to tsan test which blocks some go packages
- **Debci update**

  0. No update, but prepare for adding more hardwares
- **Reproduce-build**

  reproduced > 95% for riscv64 trixie
- **Some works**

  1.justbuild [review/uplod], chromium [140-1], golang-1.24 [backport cgo patch], cuneiform[fix ftbfs on rv64]

  2. redleafos: trying to boot from nvme


请此页编辑者删除水印
RevyOS

Guix on RISC-V(郑俊杰)

Sophgo Linux Upstream Status Update（汪辰）

https://github.com/sophgo/linux/wiki [Last updated: Sep/17/2025]

Linux Upstream Status updated for Sophgo: Sep/17/2025: https://ruyisdk.cn/t/topic/1485

Details：

- CV18xx
  - USB phy is pulled, expected to be picked by 6.18
- SG2042
  - SPI-nor: DTS part is updated to v2, may need more updated after some discussion.
  - msi controller: Set irq type according to DT configuration, updated to v3.Pulled by irq/drivers, expected to be picked by 6.18.
  - PCIe driver: updated to v3.
  - Add numa id description (v1)
- SG2044
  - N/A

RT-Thread (RISC-V) Upstream Status Update（汪辰）

OpenCloudOS SIG 进展（孙敏）

Box64 RISC-V 进展

-

OpenSBI（王翔）

- 在修改PMP后刷新tlb缓存
  https://lists.infradead.org/pipermail/opensbi/2025-September/008841.html
- 添加VisionFive 2 Lite
  https://lists.infradead.org/pipermail/opensbi/2025-September/008855.html
- 在挂起恢复时添加mideleg保存恢复
  https://lists.infradead.org/pipermail/opensbi/2025-September/008857.html
  https://lists.infradead.org/pipermail/opensbi/2025-September/008858.html
- 添加spacemit k1支持
  https://lists.infradead.org/pipermail/opensbi/2025-September/008886.html

RustSBI团队进展（洛佳）（演讲人不在线）

- 正在维护artinchip-hal系列Rust HAL支持项目
- 超激进路线：大模型可以是引导程序吗？（深圳Rust China Tour演讲）
- K230支持开发中

香山开源RISC-V处理器 - ICT / PCL

- 前端
  - RTL 新特性
  - 支持 resolve 更新 BPU（#4962）
  - 支持 ICache 动态取指块大小，节省功耗，同时为 64B 取指块做准备（#4999）
  - 优化 mbtb、abtb 替换算法，采用 SRAM 实现的 PLRU 以节省面积（#4964）
  - 实现 ITTAGE 接入 V3 BPU（#5000，#5020）
  - 优化 PHR 更新机制（#4995）
  - TAGE-SC 持续开发中，暂未合入（#5001）
  - Bug 修复
  - 修复 resolve 更新触发的一些 bug
  - 修复 IFU 处理跨预测块的、被预测为分支指令的非分支指令 时重定向错误的问题（与 #4962 一起合入）
  - 协助修复后端 branchUnit 计算分支目标地址错误的问题（与 #4962 一起合入）
  - 修复 ubtb 更新条件错误导致多路命中的问题（#5004，#5008）
  - 修复 IBuffer 错误传递 identifiedCfi 的问题（#5019）
  - 模型探索
  - 分析 TAGE 实现，修复两个存在性能问题的方向，实现和 CBP 对齐
  - 代码质量
  - 重构 IFU、IBuffer 使用 V3 前端参数系统（#4975，#5013）
  - 简化 mbtb 参数（#4987）

香山开源RISC-V处理器 - ICT / PCL

- 后端流水线
  - Bug 修复
  - 后端应提供 FTQ 项的起始 PC（#5017）
  - 修复 isRVC 传输逻辑以适应新的 FTQ 设计（#5003）
- 访存与缓存
  - RTL新特性
  - （V2）在 CoupledL2 的 MMIOBridge 中，将 clint 的地址范围从 xstilewrap 的映射中排除并重新配置，以集成私有的 clint ip（CoupledL2 #429）
  - MMU、LoadUnit、StoreQueue、L2 等模块重构持续推进中
  - 重构 NEMU 的访存部分，包括代码整理以及增加 V3 新特性
  - Bug 修复
  - （V2）修复了 ITLB 在特定周期收到 PWT 响应时卡死的问题（#4983）
  - （V2）在 LLTLB 处理 jmp_bitmap_check 请求时初始化 first_s2xlate_fault 信号，以避免 L2TLB 同时处理 allStage 与 noS2xlate 请求时发生问题（#4996）
  - （V2）修复了 prefetch hit 计数器实现错误，导致统计得到的预取命中数目大于预取请求数目的问题（#5005）
  - （V2）修复了 VSegment 中非对齐访存拆分时地址生成错误的问题（#5006）
  - （V2）修复了 LLPTW 中非必要的位图检查逻辑（#0518）
  - 工具
  - tl-test-new 支持 anvil 模式下的噪声生成（tl-test-new #80）
  - 为 CoupledL2 的 TestTop 添加生成二进制格式 CHI log 的功能，用于压缩日志文件大小（CoupledL2 #410）

banshanjdk-8 让你的 java8 程序在 RISC-V 平台极限加速

Chisel and Additional Technology / Sequencer

OpenHW & OpenHW Aisa Working Group

甲辰计划进展(吴伟)

-

自由讨论 / AOB

BACKUP

准备加入更多的国际开源组织进行同步观测

欢迎追加或提议