

NCV7342

High Speed Low Power CAN Transceiver

Description

The NCV7342 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12 V and 24 V systems. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

The NCV7342 is an addition to the CAN high-speed transceiver family complementing NCV734x CAN stand-alone transceivers and previous generations such as AMIS42665, AMIS3066x, etc.

Due to the wide common-mode voltage range of the receiver inputs and other design features, the NCV7342 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

Features

- Compatible with the ISO 11898-2, ISO 11898-5 Standards
- High Speed (up to 1 Mbps)
- V_{IO} Pin on NCV7342-3 Version Allowing Direct Interfacing with 3 V to 5 V Microcontrollers
- V_{SPLIT} Pin on NCV7342-0 Version for Bus Common Mode Stabilization
- Very Low Current Consumption in Standby Mode with Wake-up via the Bus
- Excellent Electromagnetic Susceptibility (EMS) Level Over Full Frequency Range. Very Low Electromagnetic Emissions (EME) Low EME Also Without Common Mode (CM) Choke
- Bus Pins Protected Against >15 kV System ESD Pulses
- Transmit Data (TxD) Dominant Time-out Function
- Bus Dominant Time-out function in Standby Mode
- Under All Supply Condition the Chip Behaves Predictably
- No Disturbance of the Bus Lines with an Unpowered Node
- Thermal Protection
- Bus Pins Protected Against Transients in an Automotive Environment
- Bus Pins Short Circuit Proof to Supply Voltage and Ground
- These are Pb-Free Devices

Quality

- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

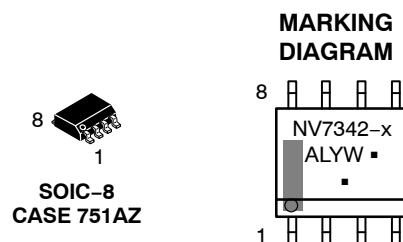
Typical Applications

- Automotive
- Industrial Networks



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NV7342-x= Specific Device Code

x = 0 or 3

A = Assembly Location

L = Wafer Lot

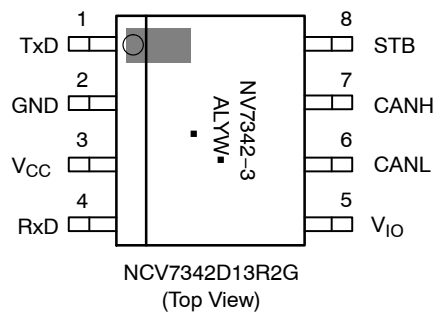
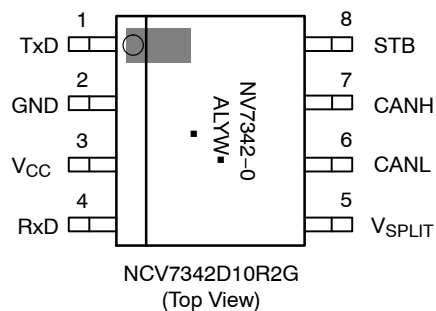
Y = Year

W = Work Week

■ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

Table 1. KEY TECHNICAL CHARACTERISTICS AND OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Power supply voltage		4.5	5.5	V
V_{UVDVCC}	Undervoltage detection voltage on pin V_{CC} (NCV7342–3 only)		3.5	4.5	V
I_{CC}	Supply current	Dominant; $V_{TxD} = 0$ V Recessive; $V_{TxD} = V_{IO}$		75 10	mA
I_{CCS}	Supply current in standby mode including V_{IO} current	$T_J \leq 100^{\circ}\text{C}$, (Note 1)		15	μA
V_{CANH}	DC voltage at pin CANH	$0 < V_{CC} < 5.5$ V; no time limit	–50	+50	V
V_{CANL}	DC voltage at pin CANL	$0 < V_{CC} < 5.5$ V; no time limit	–50	+50	V
$V_{CANH,L}$	DC voltage between CANH and CANL pin	$0 < V_{CC} < 5.5$ V	–50	+50	V
V_{ESD}	Electrostatic discharge voltage	IEC 61000–4–2 at pins CANH and CANL	–15	15	kV
$V_{O(dif)(bus_dom)}$	Differential bus output voltage in dominant state	$45\ \Omega < R_{LT} < 65\ \Omega$	1.5	3	V
CM–range	Input common–mode range for comparator	Guaranteed differential receiver threshold and leakage current	–35	+35	V
C_{load}	Load capacitance on IC outputs			15	pF
t_{pd0}	Propagation delay TxD to RxD (NCV7342–0 version)	See Figure 8	50	230	ns
t_{pd3}	Propagation delay TxD to RxD (NCV7342–3 version)	See Figure 8	50	230	ns
T_J	Junction temperature		–40	150	$^{\circ}\text{C}$

1. Not tested in production. Guaranteed by design and prototype evaluation.

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BLOCK DIAGRAMS

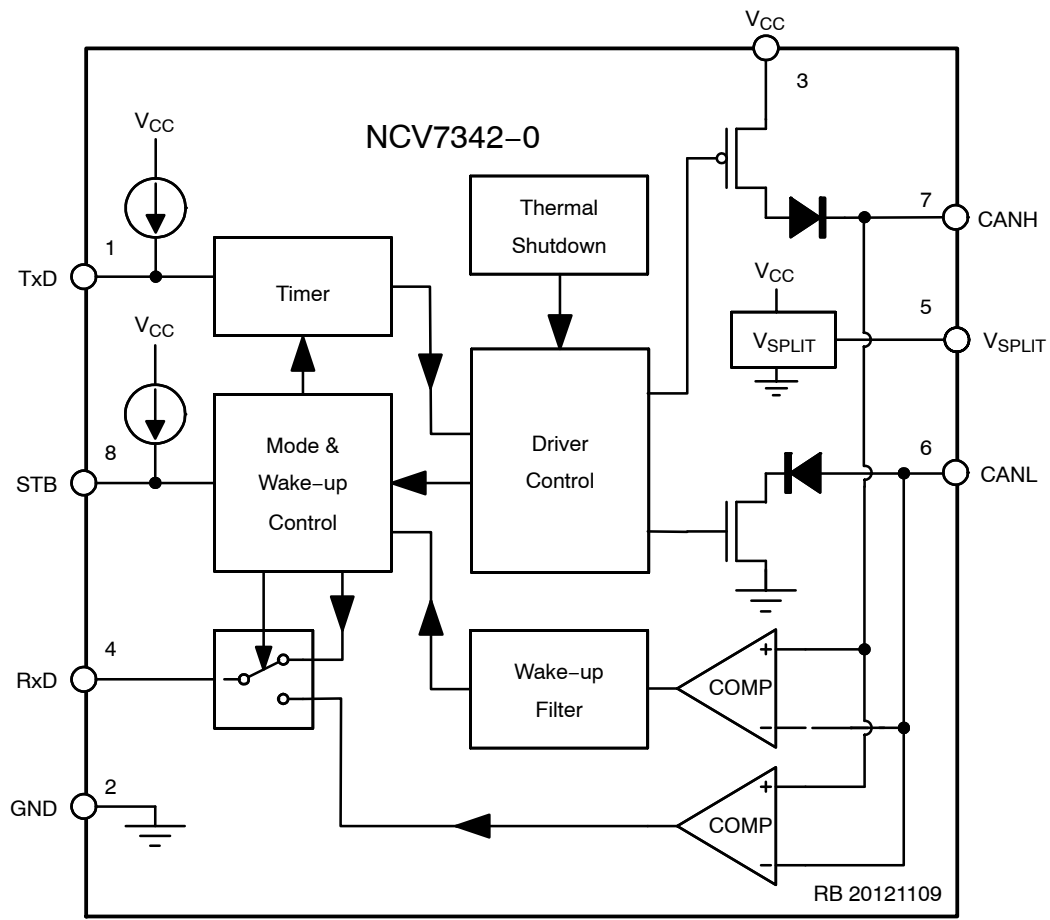


Figure 1. NCV7342-0 Block Diagram

NCV7342

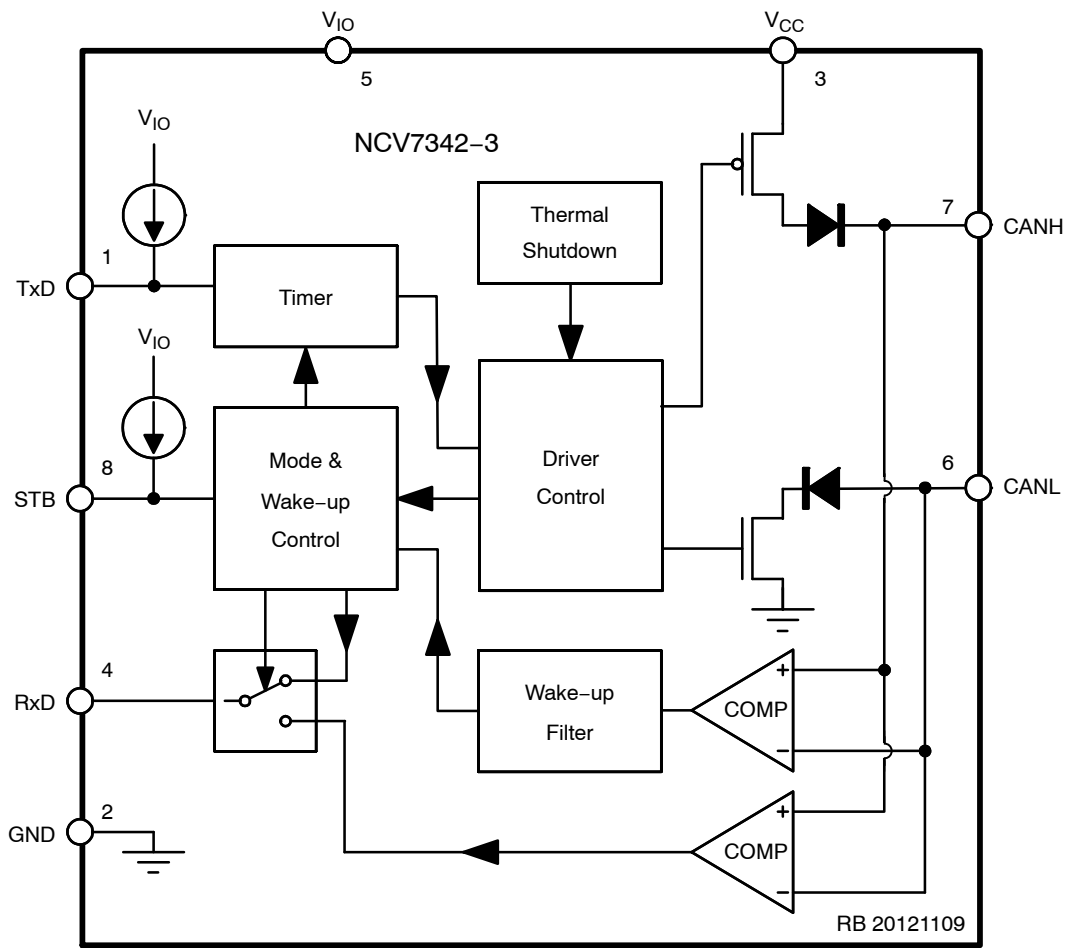


Figure 2. NCV7342-3 Block Diagram

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TYPICAL APPLICATION

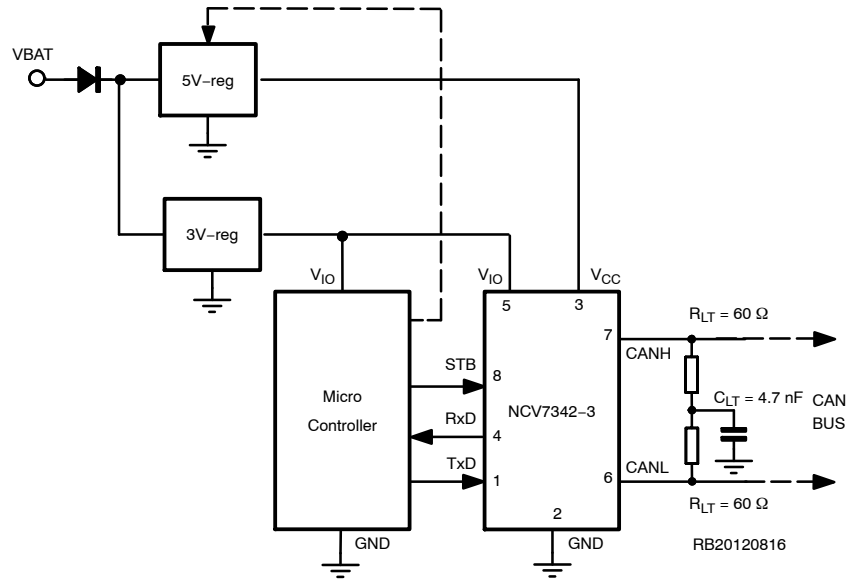


Figure 3. Application Diagram NCV7342-3

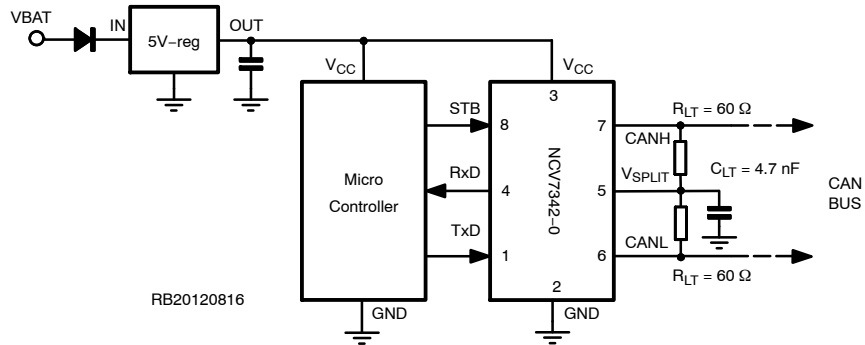


Figure 4. Application Diagram NCV7342-0

Table 2. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	TxD	Transmit data input; Low input → dominant driver; internal pull-up current
2	GND	Ground
3	V _{CC}	Supply voltage
4	RxD	Receive data output; dominant transmitter → Low output
5	V _{IO}	Input/Output pins supply voltage. On NCV7342-3 only
5	V _{SPLIT}	Common-mode stabilization output. On NCV7342-0 only
6	CANL	Low-level CAN bus line (Low in dominant mode)
7	CANH	High-level CAN bus line (High in dominant mode)
8	STB	Standby mode control input

FUNCTIONAL DESCRIPTION

NCV7342 has two versions which differ from each other only by function of pin 5.

NCV7342-0: Pin 5 is common mode stabilization output V_{SPLIT} . (see Figure 4) This version is full replacement of NCV7340.

NCV7342-3: Pin 5 is V_{IO} pin, which is supply pin for transceiver digital inputs/output (supplying pins TxD, RxD, STB) The V_{IO} pin should be connected to microcontroller supply pin. By using V_{IO} supply pin shared with microcontroller, the I/O levels between microcontroller and transceiver are properly adjusted. This adjustment allows communication between 3 V microcontroller and the transceiver. (See Figure 3)

Operating Modes

NCV7342 provides two modes of operation as illustrated in Table 3. These modes are selectable through pin STB.

Table 3. OPERATING MODES

Pin STB	Mode	Pin RxD	
		Low	High
Low	Normal	Bus dominant	Bus recessive
High	Standby	Wake-up request detected	No wake-up request detected

Normal Mode

In normal mode, the transceiver is able to communicate via the bus lines. The signals are transmitted and received to the CAN controller via the pins TxD and RxD. The slopes on the bus lines outputs are optimized to give extremely low EME.

Standby Mode

In standby mode both the transmitter and receiver are disabled and a very low-power differential receiver

monitors the bus lines for CAN bus activity. The bus lines are terminated to ground and supply current is reduced to a minimum, typically 10 μ A. When a wake-up request is detected by the low-power differential receiver, the signal is first filtered and then verified as a valid wake signal after a time period of $t_{dwakerd}$. The RxD pin is driven Low by the transceiver to inform the controller of the wake-up request.

V_{IO} Supply Pin

The V_{IO} pin (available only on NCV7342-3 version) should be connected to microcontroller supply pin. By using V_{IO} supply pin shared with microcontroller the I/O levels between microcontroller and transceiver are properly adjusted. See Figure 3. Pin V_{IO} also provides the internal supply voltage for low-power differential receiver of the transceiver. This allows detection of wake-up request even when there is no supply voltage on Pin V_{CC} .

Split Circuit

The V_{SPLIT} pin (available on NCV7342-0 version) is operational only in normal mode. In standby mode this pin is floating. The V_{SPLIT} can be connected as shown in Figure 4 or, if it's not used, can be left floating. Its purpose is to provide a stabilized DC voltage of $0.5 \cdot V_{CC}$ to the bus reducing possible steps in the common-mode signal, therefore reducing EME. These unwanted steps could be caused by an unpowered node on the network with excessive leakage current from the bus that shifts the recessive voltage from its nominal $0.5 \cdot V_{CC}$ voltage.

Wake-up

When a valid wake-up (dominant state longer than t_{Wake}) is received during the standby mode, the RxD pin is driven Low after $t_{dwakerd}$. The wake-up detection is not latched: RxD returns to High state after $t_{dwakedr}$ when the bus signal is released back to recessive – see Figure 5.

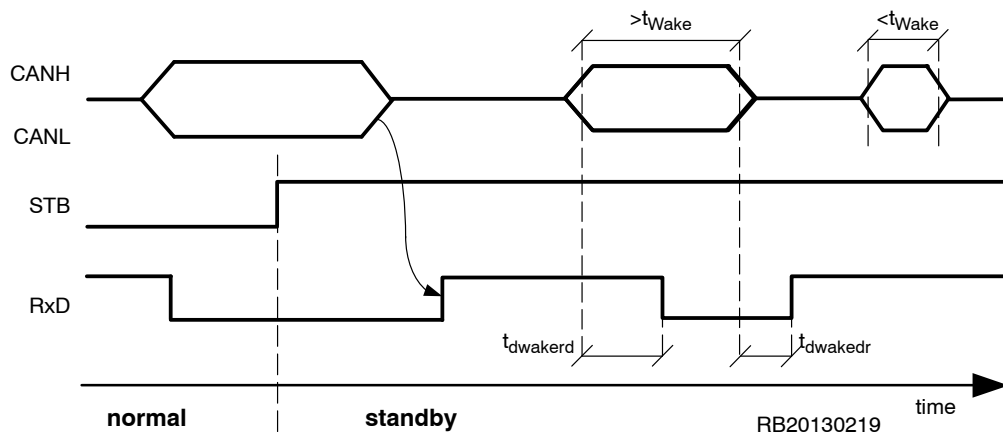


Figure 5. NCV7342 Wake-up behavior

Over-temperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 180°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC is reduced. All other IC functions continue to operate. The transmitter off-state resets when the temperature decreases below the shutdown threshold and pin TxD goes High. The thermal protection circuit is particularly needed in case of a bus line failure.

TxD Dominant Time-out Function

A TxD dominant time-out timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication), if pin TxD is forced permanently Low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low-level on pin TxD exceeds the internal timer value $t_{\text{dom(TxD)}}$, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on pin TxD.

This TxD dominant time-out time ($t_{\text{dom(TxD)}}$) limits the minimum possible bit rate to 8 kbps.

Bus Dominant Time-out Function

Bus dominant time-out timer is started in the standby mode when CAN bus changes from recessive to dominant

state. If the dominant state on the bus is kept for longer time than $t_{\text{dom(bus)}}$, the RxD pin is released to High level. The timer is reset when CAN bus changes from dominant to recessive state. This feature prevents generating permanent wake-up request by the bus clamped to the dominant level.

Fail Safe Features

A current-limiting circuit protects the transmitter output stage from damage caused by an accidental short circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

V_{CC} supply dropping below V_{UVDVCC} undervoltage level will force transceiver to switch into the standby mode. The logic level on pin STB will be ignored as long as undervoltage condition is not recovered. (NCV7342-3 version only)

V_{IO} supply dropping below V_{UVDVIO} undervoltage detection level will cause the transceiver to disengage from the bus (no bus loading) until the V_{IO} voltage recovers. (NCV7342-3 version only)

The pins CANH and CANL are protected against automotive electrical transients (according to ISO 7637; see Figure 6). Pins TxD and STB are pulled High internally should the input become disconnected. Pins TxD, STB and RxD will be floating, preventing reverse supply should the V_{CC} supply be removed.

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (pin 2). Positive currents flow into the IC. Sinking current means the current is flowing into the pin; sourcing current means the current is flowing out of the pin.

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min	Max	Unit
V _{SUP}	Supply voltage V _{CC} , V _{IO}		-0.3	6	V
V _{CANH}	DC voltage at pin CANH	0 < V _{CC} < 5.5 V; no time limit	-50	50	V
V _{CANL}	DC voltage at pin CANL	0 < V _{CC} < 5.5 V; no time limit	-50	50	V
V _{CANH,Lmax}	DC voltage at pin CANH and CANL during load dump condition	0 < V _{CC} < 5.5 V; less than one second	-	58	V
V _{SPLIT}	DC voltage at V _{SPLIT} pin (On NCV7342-0 version only)	0 < V _{CC} < 5.5 V; no time limit	-50	50	V
V _{IO}	DC voltage at pin TxD, RxD, STB		-0.3	6	V
V _{esd}	Electrostatic discharge voltage at all pins according to EIA-JESD22	Note 2	-4	4	kV
	Standardized charged device model ESD pulses according to ESD-STM5.3.1-1999		-750	750	V
	Electrostatic discharge voltage at CANH,CANL, V _{SPLIT} pins according to EIA-JESD22	Note 2	-8	8	kV
	Electrostatic discharge voltage at CANH, CANL pins According to IEC 61000-4-2	Note 3	-15	15	kV
V _{schaff}	Transient voltage at CANH, CANL pins, See Figure 6	Note 4	-150	100	V
Latch-up	Static latch-up at all pins	Note 5		150	mA
T _{stg}	Storage temperature		-55	+150	°C
T _{amb}	Ambient temperature		-40	+125	°C
T _J	Maximum junction temperature		-40	+170	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

- Standardized human body model electrostatic discharge (ESD) pulses in accordance to EIA-JESD22. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
- System human body model electrostatic discharge (ESD) pulses. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor referenced to GND. Verified by external test house
- Pulses 1, 2a,3a and 3b according to ISO 7637 part 3. Verification by external test house.
- Static latch-up immunity: Static latch-up protection level when tested according to EIA/JESD78.

Table 5. THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
R _{θJA_1}	Thermal Resistance Junction-to-Air, 1S0P PCB (Note 6)	Free air	125	K/W
R _{θJA_2}	Thermal Resistance Junction-to-Air, 2S2P PCB (Note 7)	Free air	75	K/W

- Test board according to EIA/JEDEC Standard JESD51-3, signal layer with 10% trace coverage.
- Test board according to EIA/JEDEC Standard JESD51-7, signal layers with 10% trace coverage.

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Table 6. CHARACTERISTICS

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$; $V_{IO} = 2.8\text{ V to }5.5\text{ V}$ (Note 8); $T_J = -40\text{ to }+150^\circ\text{C}$; $R_{LT} = 60\ \Omega$ unless specified otherwise. On chip versions without V_{IO} pin reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO} .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY (Pin V_{CC})						
I_{CC}	Supply current	Dominant; $V_{TxD} = 0\text{ V}$ Recessive; $V_{TxD} = V_{IO}$		50 6.8	75 10	mA
I_{CCS0}	Supply current in standby mode for NCV7342-0	$T_J \leq 100^\circ\text{C}$ (Note 9)		8	15	μA
I_{CCS3}	Supply current in standby mode for NCV7342-3 including current into V_{IO}	$T_J \leq 100^\circ\text{C}$ (Note 9)			17	μA
V_{CC}	Undervoltage detection voltage on V_{CC} pin (NCV7342-3 only)		3.5		4.5	V
TRANSMITTER DATA INPUT (Pin TxD)						
V_{IH}	High-level input voltage	Output recessive	2.0		6	V
V_{IL}	Low-level input voltage	Output dominant	-0.3		0.8	V
I_{IH}	High-level input current	$V_{TxD} = V_{IO}$	-5	0	5	μA
I_{IL}	Low-level input current	$V_{TxD} = 0\text{ V}$	-385	-200	-45	μA
C_i	Input capacitance	Not tested		5	10	pF
TRANSMITTER MODE SELECT (Pin STB)						
V_{IH}	High-level input voltage	Standby mode	2.0		$V_{IO}+0.3$ (Note 10)	V
V_{IL}	Low-level input voltage	Normal mode	-0.3		0.8	V
I_{IH}	High-level input current	$V_{STB} = V_{IO}$	-5	0	5	μA
I_{IL}	Low-level input current	$V_{STB} = 0\text{ V}$	-10	-4	-1	μA
C_i	Input capacitance	Not tested		5	10	pF
RECEIVER DATA OUTPUT (Pin RxD)						
I_{OH}	High-level output current	Normal mode $V_{RxD} = V_{IO} - 0.4\text{ V}$	-1.2	-0.4	-0.1	mA
I_{OL}	Low-level output current	$V_{RxD} = 0.4\text{ V}$	1.5	6	12	mA
V_{OH}	High-level output voltage	Standby mode $I_{RxD} = -100\ \mu\text{A}$	$V_{IO} - 1.1$	$V_{IO} - 0.7$	$V_{IO} - 0.4$	V
BUS LINES (Pins $CANH$ and $CANL$)						
$V_{o(\text{reces})}$ (norm)	Recessive bus voltage on pins $CANH$ and $CANL$	$V_{TxD} = V_{IO}$; no load; normal mode	2.0	2.5	3.0	V
$V_{o(\text{reces})}$ (stby)	Recessive bus voltage on pins $CANH$ and $CANL$	$V_{TxD} = V_{IO}$; no load; standby mode	-100	0	100	mV
$I_{o(\text{reces})}$ ($CANH$)	Recessive output current at pin $CANH$	$-30\text{ V} < V_{CANH} < 35\text{ V}$; $0\text{ V} < V_{CC} < 5.5\text{ V}$	-2.5		2.5	mA
$I_{o(\text{reces})}$ ($CANL$)	Recessive output current at pin $CANL$	$-30\text{ V} < V_{CANL} < 35\text{ V}$; $0\text{ V} < V_{CC} < 5.5\text{ V}$	-2.5		2.5	mA
$I_{LI}(\text{CANH})$	Input leakage current to pin $CANH$	$0\ \Omega < R(V_{CC} \text{ to GND}) < 1\text{ M}\Omega$ $0\ \Omega < R(V_{IO} \text{ to GND}) < 1\text{ M}\Omega$ $V_{CANL} = V_{CANH} = 5\text{ V}$ (Note 8)	-10	0	10	μA
$I_{LI}(\text{CANL})$	Input leakage current to pin $CANL$		-10	0	10	μA
$V_{o(\text{dom})}$ ($CANH$)	Dominant output voltage at pin $CANH$	$V_{TxD} = 0\text{ V}$	3.0	3.6	4.25	V

8. Only version NCV7342-3 has V_{IO} supply pin. In NCV7342-0 this supply is provided from V_{CC} pin.

9. Not tested in production. Guaranteed by design and prototype evaluation.

10. In case $V_{IO} > V_{CC}$, the limit is $V_{IO} + 0.3\text{ V}$

Table 6. CHARACTERISTICS

$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$; $V_{IO} = 2.8 \text{ V to } 5.5 \text{ V}$ (Note 8); $T_J = -40 \text{ to } +150^\circ\text{C}$; $R_{LT} = 60 \Omega$ unless specified otherwise. On chip versions without V_{IO} pin reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO} .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BUS LINES (Pins CANH and CANL)						
$V_{o(dom)} (CANL)$	Dominant output voltage at pin CANL	$V_{TxD} = 0 \text{ V}$	0.5	1.4	1.75	V
$V_{o(dif)} (bus_dom)$	Differential bus output voltage ($V_{CANH} - V_{CANL}$)	$V_{TxD} = 0 \text{ V}$; dominant; $45 \Omega < R_{LT} < 65 \Omega$	1.5	2.25	3.0	V
$V_{o(dif)} (bus_rec)$	Differential bus output voltage ($V_{CANH} - V_{CANL}$)	$V_{TxD} = V_{IO}$; recessive; no load	-120	0	50	mV
$V_{o(sym)} (bus_dom)$	Bus output voltage symmetry $V_{CANH} + V_{CANL}$	$V_{TxD} = 0 \text{ V}$	0.9		1.1	V_{CC}
$I_{o(sc)} (CANH)$	Short circuit output current at pin CANH	$V_{CANH} = 0 \text{ V}$; $V_{TxD} = 0 \text{ V}$	-90	-70	-40	mA
$I_{o(sc)} (CANL)$	Short circuit output current at pin CANL	$V_{CANL} = 36 \text{ V}$; $V_{TxD} = 0 \text{ V}$	40	70	100	mA
$V_{i(dif)} (th)$	Differential receiver threshold voltage	$-12 \text{ V} < V_{CANL} < 12 \text{ V}$; $-12 \text{ V} < V_{CANH} < 12 \text{ V}$; $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$	0.5	0.7	0.9	V
$V_{ihcm(dif)} (th)$	Differential receiver threshold voltage for high common-mode	$-30 \text{ V} < V_{CANL} < 35 \text{ V}$; $-30 \text{ V} < V_{CANH} < 35 \text{ V}$; $V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$	0.40	0.7	1.0	V
$V_{i(dif)} (th)_{STDBY}$	Differential receiver threshold voltage in standby mode	$-12 \text{ V} < V_{CANL} < 12 \text{ V}$; $-12 \text{ V} < V_{CANH} < 12 \text{ V}$; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.4	0.8	1.15	V
$R_{i(cm)} (CANH)$	Common-mode input resistance at pin CANH		15	26	37	k Ω
$R_{i(cm)} (CANL)$	Common-mode input resistance at pin CANL		15	26	37	k Ω
$R_{i(cm)} (m)$	Matching between pin CANH and pin CANL common mode input resistance	$V_{CANH} = V_{CANL}$	-0.8	0	0.8	%
$R_{i(dif)}$	Differential input resistance		25	50	75	k Ω
$C_{i(CANH)}$	Input capacitance at pin CANH	$V_{TxD} = V_{IO}$; not tested		7.5	20	pF
$C_{i(CANL)}$	Input capacitance at pin CANL	$V_{TxD} = V_{IO}$; not tested		7.5	20	pF
$C_{i(dif)}$	Differential input capacitance	$V_{TxD} = V_{IO}$; not tested		3.75	10	pF

COMMON-MODE STABILIZATION (Pin V_{SPLIT}) Only for NCV7342-0 version

V_{SPLIT}	Reference output voltage at pin V_{SPLIT}	Normal mode; $-500 \mu\text{A} < I_{SPLIT} < 500 \mu\text{A}$	0.3		0.7	V_{CC}
V_{SPLITo}	Reference output voltage at pin V_{SPLIT}	$R_{load} V_{split} > 1 \text{ M}\Omega$	0.45		0.55	V_{CC}
$I_{SPLIT(l)}$	V_{SPLIT} leakage current	Standby mode	-5		5	μA
$I_{SPLIT(lim)}$	V_{SPLIT} limitation current	Normal mode	1.3		5	mA

V_{IO} SUPPLY VOLTAGE (Pin V_{IO}) Only for NCV7342-3 version

V_{IO}	Supply voltage on pin V_{IO}		2.8		5.5	V
I_{IOS}	Supply current on pin V_{IO}	Standby mode			14	μA
I_{IONM}	Supply current on pin V_{IO}	Normal mode Dominant; $V_{TxD} = 0 \text{ V}$ Recessive; $V_{TxD} = V_{IO}$	0.30 0.29	0.70 0.44	1.10 0.68	mA

8. Only version NCV7342-3 has V_{IO} supply pin. In NCV7342-0 this supply is provided from V_{CC} pin.

9. Not tested in production. Guaranteed by design and prototype evaluation.

10. In case $V_{IO} > V_{CC}$, the limit is $V_{IO} + 0.3 \text{ V}$

Table 6. CHARACTERISTICS

$V_{CC} = 4.5\text{ V to }5.5\text{ V}$; $V_{IO} = 2.8\text{ V to }5.5\text{ V}$ (Note 8); $T_J = -40\text{ to }+150^\circ\text{C}$; $R_{LT} = 60\ \Omega$ unless specified otherwise. On chip versions without V_{IO} pin reference voltage for all digital inputs and outputs is V_{CC} instead of V_{IO} .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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V_{IO} SUPPLY VOLTAGE (Pin V_{IO}) Only for NCV7342–3 version

V_{UVDVIO}	Undervoltage detection voltage on V_{IO} pin		1.3		2.7	V
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THERMAL SHUTDOWN

$T_{J(SD)}$	Shutdown junction temperature	junction temperature rising	160	180	200	$^\circ\text{C}$
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TIMING CHARACTERISTICS (See Figure 7 and 8)

$t_{d(TxD-BUSon)}$	Delay TxD to bus active	$C_i = 100\text{ pF}$ between CANH to CANL		60		ns
$t_{d(TxD-BUSoff)}$	Delay TxD to bus inactive	$C_i = 100\text{ pF}$ between CANH to CANL		30		ns
$t_{d(BUSon-RxD)}$	Delay bus active to RxD	$C_{RxD} = 15\text{ pF}$		60		ns
$t_{d(BUSoff-RxD)}$	Delay bus inactive to RxD	$C_{RxD} = 15\text{ pF}$		70		ns
t_{pd_dr}	Propagation delay TxD to RxD dominant to recessive transition	$C_i = 100\text{ pF}$ between CANH to CANL, $C_{RxD} = 15\text{ pF}$	50	100	230	ns
t_{pd_rd}	Propagation delay TxD to RxD recessive to dominant transition	$C_i = 100\text{ pF}$ between CANH to CANL, $C_{RxD} = 15\text{ pF}$	50	120	230	ns
$t_{d(stb-nm)}$	Delay standby mode to normal mode				47	μs
t_{Wake}	Dominant time for wake-up via bus		0.5		5	μs
$t_{dwakerd}$	Delay to flag wake event (recessive to dominant transitions) See Figure 5	Valid bus wake-up event, $C_{RxD} = 15\text{ pF}$	1		10	μs
$t_{dwakedr}$	Delay to flag end of wake event (dominant to recessive transition) See Figure 5	Valid bus wake-up event, $C_{RxD} = 15\text{ pF}$	0.5		5	μs
$t_{dom(TxD)}$	TxD dominant time for time out	$V_{TxD} = 0\text{ V}$	1.3		3	ms
$t_{dom(bus)}$	Bus dominant time out	Standby mode	1.3		3	ms

8. Only version NCV7342–3 has V_{IO} supply pin. In NCV7342–0 this supply is provided from V_{CC} pin.

9. Not tested in production. Guaranteed by design and prototype evaluation.

10. In case $V_{IO} > V_{CC}$, the limit is $V_{IO} + 0.3\text{ V}$

MEASUREMENT SET-UPS AND DEFINITIONS

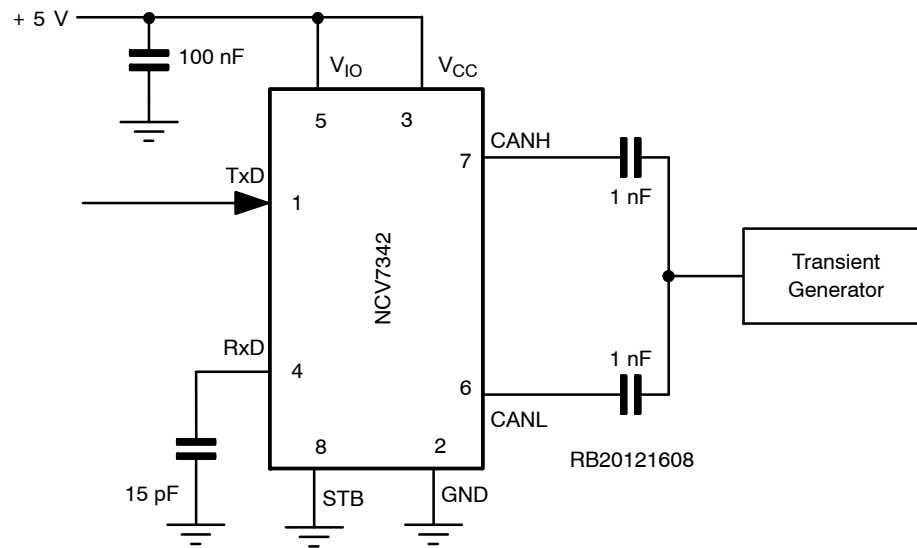


Figure 6. Test Circuit for Automotive Transients

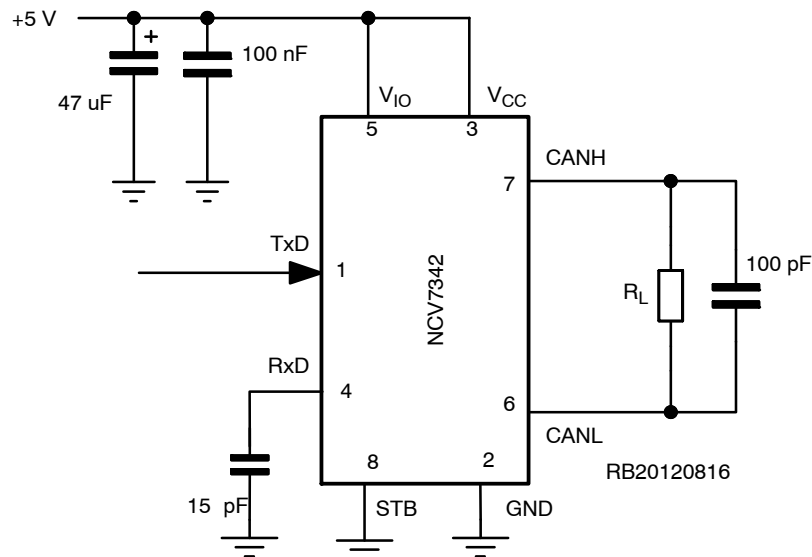


Figure 7. Test Circuit for Timing Characteristics

NCV7342

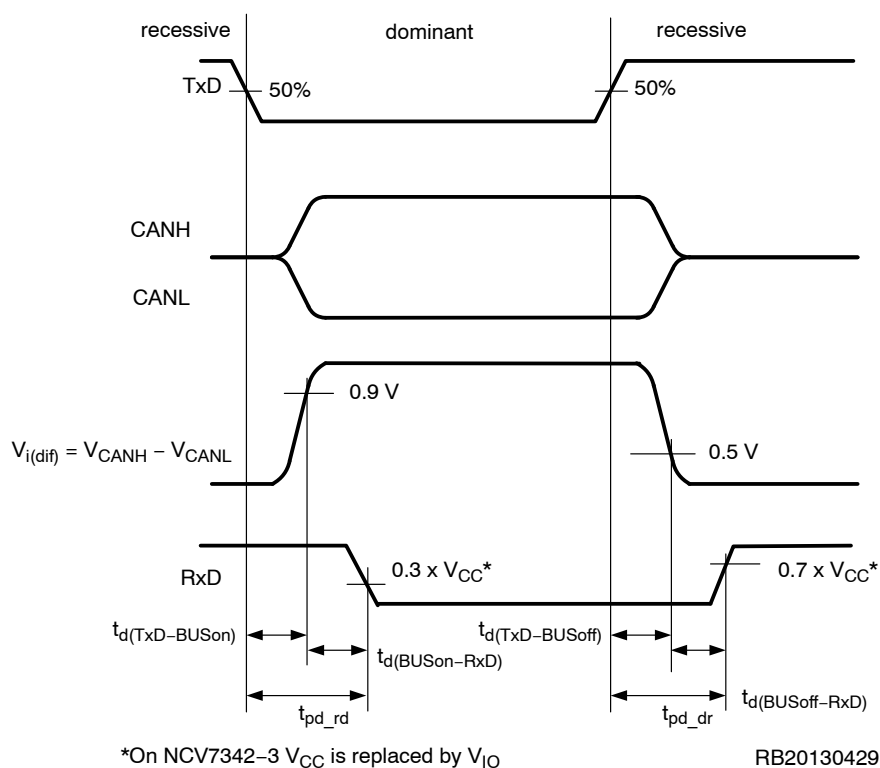


Figure 8. Transceiver Timing Diagram

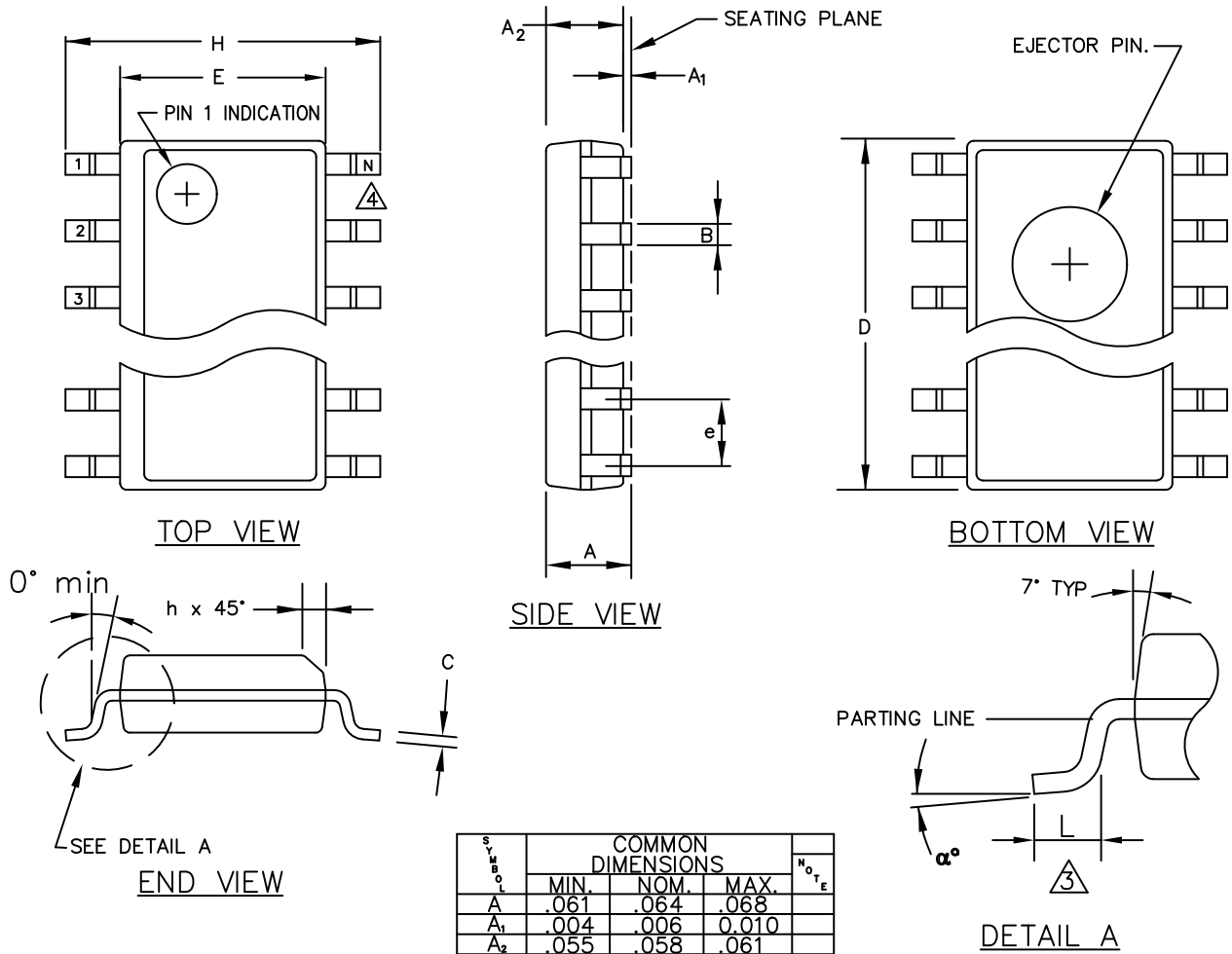
DEVICE ORDERING INFORMATION

Part Number	Description	Package	Shipping [†]
NCV7342D10R2G	High Speed CAN Transceiver with Standby and V_{SPLIT} pin	SOIC 150 8 GREEN (Matte Sn, JEDEC MS-012) (Pb-Free)	3000 / Tape & Reel
NCV7342D13R2G	High Speed CAN Transceiver with Standby and V_{IO} pin (available in 2014)		


[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

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CASE 751AZ
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