

HO CHI MINH UNIVERSITY OF TECHNOLOGY
FACULTY OF COMPUTER SCIENCE AND ENGINEERING



LOGIC DESIGN PROJECT

REPORT

Design of a Sports Stopwatch on ArtyZ7 FPGA

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Contents

| | | |
|----------|--|-----------|
| 1 | Introduction | 3 |
| 2 | Requirements | 4 |
| 2.1 | Functional Requirements | 4 |
| 2.1.1 | Count-Up Mode | 4 |
| 2.1.2 | Countdown Mode | 4 |
| 2.1.3 | Time Point Storage | 4 |
| 2.1.4 | Pause,Resume, Adjust and Reset Functionality | 4 |
| 2.2 | Additional contents | 4 |
| 2.2.1 | Alarm Mode | 4 |
| 2.2.2 | Setup Mode | 4 |
| 3 | Devices | 5 |
| 3.1 | ArtyZ7 | 5 |
| 3.2 | 4x7-segment LEDs | 6 |
| 3.3 | Breadboard, Wires | 7 |
| 4 | Design | 8 |
| 4.1 | Block Diagram | 8 |
| 4.2 | Functional Block Descriptions | 9 |
| 4.2.1 | Sport Watch | 9 |
| 4.2.2 | Signal Controller | 9 |
| 4.2.3 | Count-up, count-down mode | 9 |
| 4.2.4 | Alarm, Setup mode | 9 |
| 4.2.5 | Utility Module | 10 |
| 4.3 | Flowchart | 11 |
| 5 | Simulation | 12 |
| 5.1 | Simulation of display 4x7 LED | 12 |
| 5.2 | Simulation of alarm mode | 12 |
| 5.3 | Simulation of setup mode | 13 |
| 5.4 | Simulation of normal clock mode | 14 |
| 5.5 | Simulation of count up mode | 15 |
| 5.6 | Simulation of count down mode | 16 |
| 5.7 | Simulation of sportwatch module | 17 |
| 6 | Conclusion | 18 |
| 6.1 | Overview of Results | 18 |
| 6.2 | Summary of the Team's Work | 18 |
| 6.3 | Future Directions | 18 |
| 6.4 | Challenges Encountered | 18 |



| | | |
|----------|--|-----------|
| 6.5 | Breakdown of Work | 18 |
| 7 | Link to demonstration video and source code | 20 |
| 7.1 | Demonstration video: | 20 |
| 7.2 | Source code: | 20 |
| 8 | Work distribution | 20 |

1 Introduction

In the realm of sports and competitive events, accurate timekeeping is crucial. Sports watches, particularly stopwatches, play a vital role in training and competitions, providing athletes and coaches with the precise measurements they need to evaluate performance. The increasing demand for reliable timing solutions has driven the development of advanced electronic systems capable of managing time effectively. This project focuses on the design and implementation of a sports stopwatch system utilizing the Arty Z7 FPGA development kit.

Through this project, we aim to explore the integration of digital components, such as 7-segment displays and control buttons, to enhance the functionality of the sports stopwatch. The successful implementation of this system will demonstrate the effectiveness of FPGA technology in real-world applications, showcasing its potential to revolutionize the way athletes monitor their progress and improve their performance.



Figure 1: Sport watch in real life

2 Requirements

2.1 Functional Requirements

2.1.1 Count-Up Mode

- Allowing users to start timing from zero and record elapsed time
- Maximum time unit displayed should be minutes
- Minimum time unit should be hundredths of a second
- Represented on two 7-segment LEDs

2.1.2 Countdown Mode

- Allowing users to set a specific countdown time
- Same time unit structure as the count-up mode
- LED effect should be activated to signal the end of the timer

2.1.3 Time Point Storage

- Allow users to separate and save up to three different time points during count-up operations
- Enable users to track multiple segments or laps effectively

2.1.4 Pause, Resume, Adjust and Reset Functionality

- Ability to pause the timer at any point
- Option to resume from the exact paused time
- Include a reset function to return the timer to its initial state
- Support adjusting time for count-down operations

2.2 Additional contents

2.2.1 Alarm Mode

- Set a specific time at which an alarm will trigger
- Ability to configure the alarm by setting hours, minutes, and seconds using the interface controls

2.2.2 Setup Mode

- Able to set the hour, minute of clock through the interface controls

3 Devices

3.1 ArtyZ7

- The Arty Z7 is a versatile FPGA development board from Digilent, designed for embedded and digital logic design. This architecture enables a wide range of applications, from hardware acceleration to real-time processing, making it an ideal platform for educational projects, prototyping, and digital system design.
- By using the Vivado app, we can make use of its GPIO pins, switches, buttons as well as LEDs to represent a real life sport watch. Using this board, the project can leverage the FPGA's flexibility to build custom logic circuits and the ARM processors for complex data processing, enhancing both the performance and functionality of the stopwatch system.

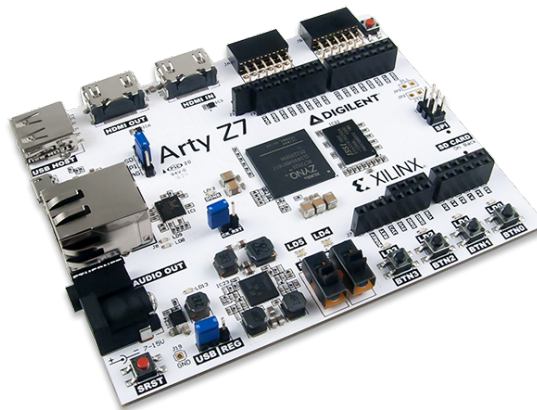


Figure 2: ArtyZ7

3.2 4x7-segment LEDs

- The sports watch system utilizes 4 seven-segment LEDs to display time, with each LED representing a single digit to show the digit. This arrangement provides users with a clear and precise view of time. Additionally, there is one common pin, which is common anode.

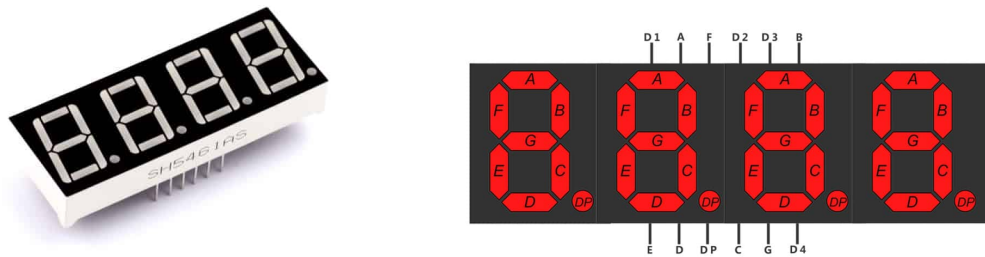


Figure 3: 4x7 Segment Display and Pinout Diagram

3.3 Breadboard, Wires

- A breadboard is an essential tool for prototyping electronic circuits without needing to solder components. It consists of a grid of holes into which electronic components and wires can be inserted. Internally, the breadboard has metal strips that connect certain holes in rows or columns, allowing components to be easily connected and disconnected. In the context of FPGA development or projects like a sports watch, the breadboard helps arrange and test connections among LEDs, resistors, and other necessary components to quickly modify the circuit before moving to a more permanent setup.
- Wires are fundamental in connecting electronic components on the breadboard or linking the breadboard to external devices like an FPGA board.

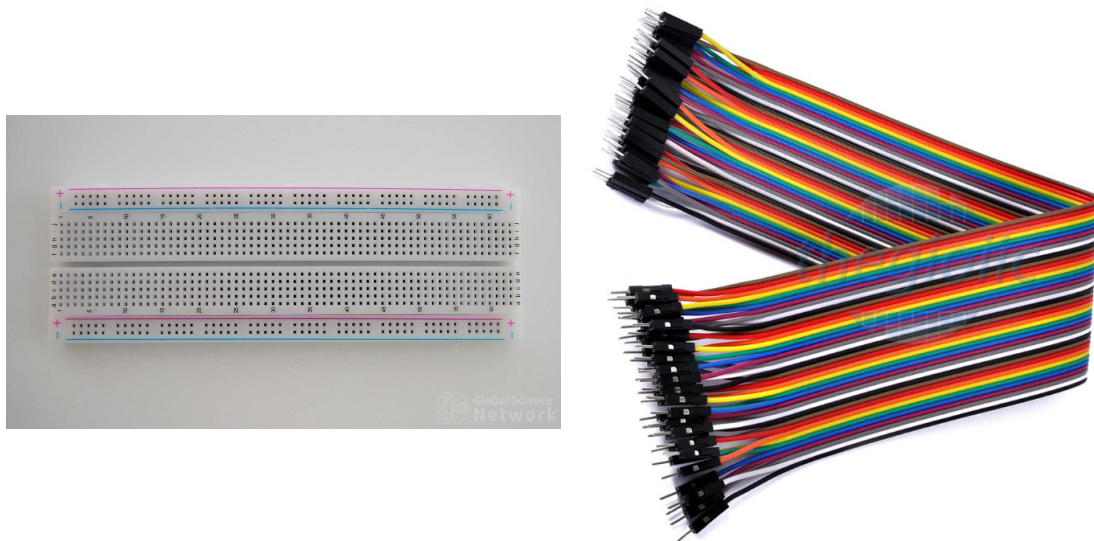


Figure 4: Breadboard and wires

4 Design

4.1 Block Diagram

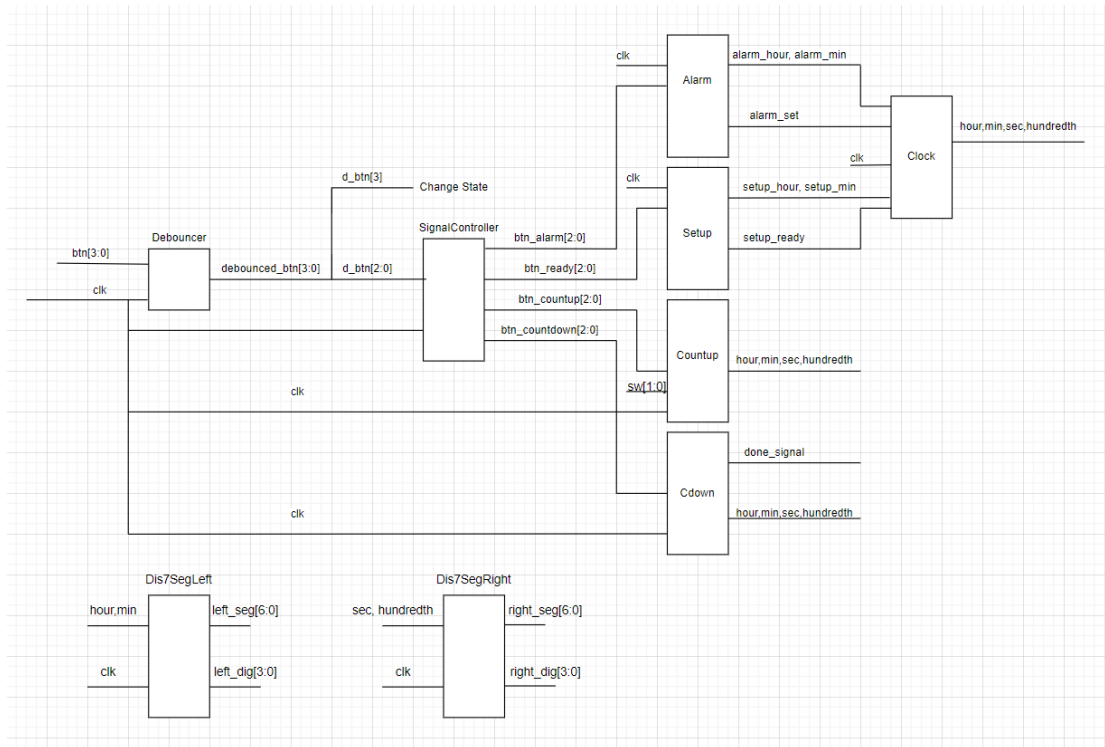


Figure 5: Block Diagram of the system

The block diagram provides an overview of the system architecture and outlines how each primary component interacts to achieve the desired functionalities of the sports stopwatch. This sports stopwatch system is designed with various functional blocks that handle specific operations, including time counting, display management, control operations, and alarm notifications.

4.2 Functional Block Descriptions

4.2.1 Sport Watch

- The Sport Watch serves as the top-level module and the primary interface of the system. This module manages all interactions with the GPIO ports on the Arty Z7, allowing it to control outputs to external displays and components effectively. Additionally, it is responsible for implementing the control logic needed to switch between operating modes, ensuring that the stopwatch can smoothly transition between functions like counting up, counting down, and alarm notifications. This central role makes the Sport Watch module essential for coordinating signals and synchronizing all other components of the system.
- In this module, the digit respective to each mode will be handled also.

4.2.2 Signal Controller

- The Signal Controller module processes signals from buttons and switches within Vivado, interpreting each input to generate the correct control signals for the selected mode. This module plays a crucial role in ensuring that each button press or switch toggle results in a smooth, accurate transition between modes, enabling responsive and intuitive interaction with the stopwatch's features.

4.2.3 Count-up, count-down mode

- In count-up mode, the stopwatch supports standard operations like start and pause, along with additional save and load features. Using the switches on the Arty Z7 as index selectors, users can save specific time points and easily reload them as needed, providing flexible time management options during training or timed activities.
- In count-down mode, users can start and pause the timer as well as adjust the countdown by adding minutes and seconds. When the countdown reaches zero, the RGB LED on the Arty Z7 illuminates, providing a clear visual signal that the timer has ended

4.2.4 Alarm, Setup mode

- The Alarm Mode enhances the functionality of the stopwatch by allowing users to set a specific time for alerts. Once the alarm time is reached, a visual indication is provided through the RGB LED, which illuminates to notify the user.
- The Setup Mode allows users to configure the current time for the normal clock function. In this mode, users can adjust the hours and minutes easily using the designated buttons on the Arty Z7.

4.2.5 Utility Module

- **Debouncer module:** This module to handle the debounce problem on 4 buttons on ArtyZ7. The debounce problem arises due to the unstable contact of mechanical components when they are activated. When a button is pressed, the contacts do not immediately close or open cleanly; instead, they may bounce on and off rapidly for a brief moment before settling into a stable state. As a result, without appropriate handling, a single press can be registered multiple times.

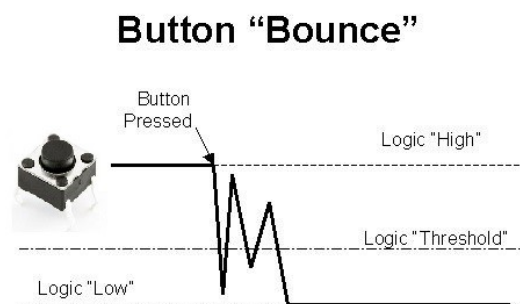


Figure 6: Button Bounce Problem

- **Display 7-segment module:** Comprise of led scanning process and display on each led. To display, we have a function which receives a numerical input and produces a 7-bit string as output, which is used to configure the pins of the 7-segment display, corresponding to segments A through G. LED scanning, also known as multiplexing, is a technique used to control multiple 7-segment displays using fewer pins than would be required if each segment was controlled individually.

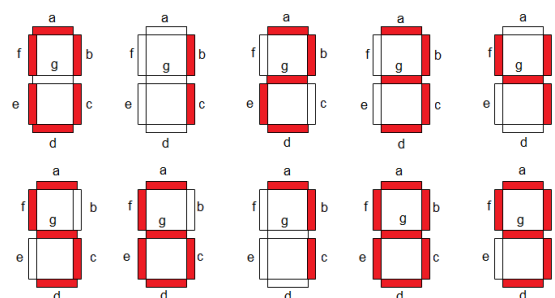


Figure 7: How to display on 7-Segment

4.3 Flowchart

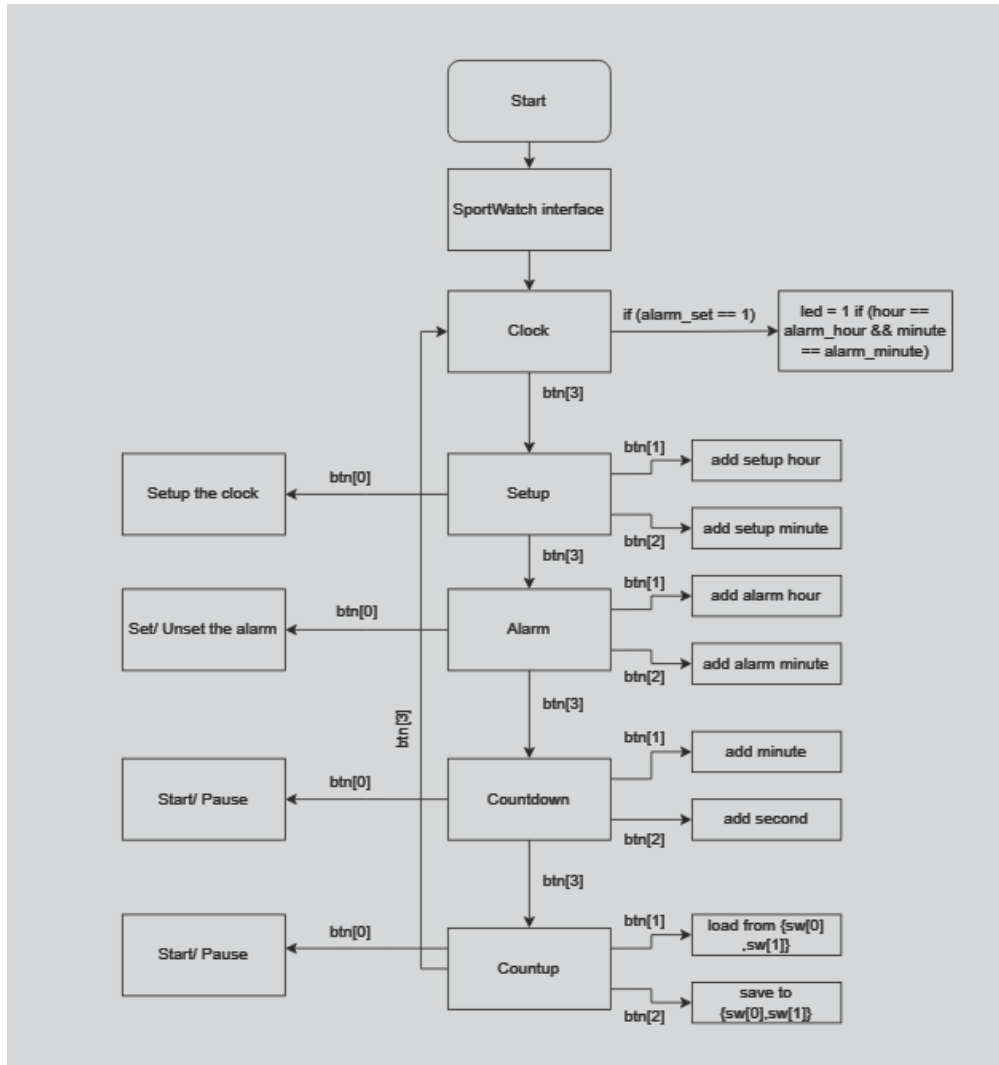


Figure 8: Flowchart

5 Simulation

5.1 Simulation of display 4x7 LED

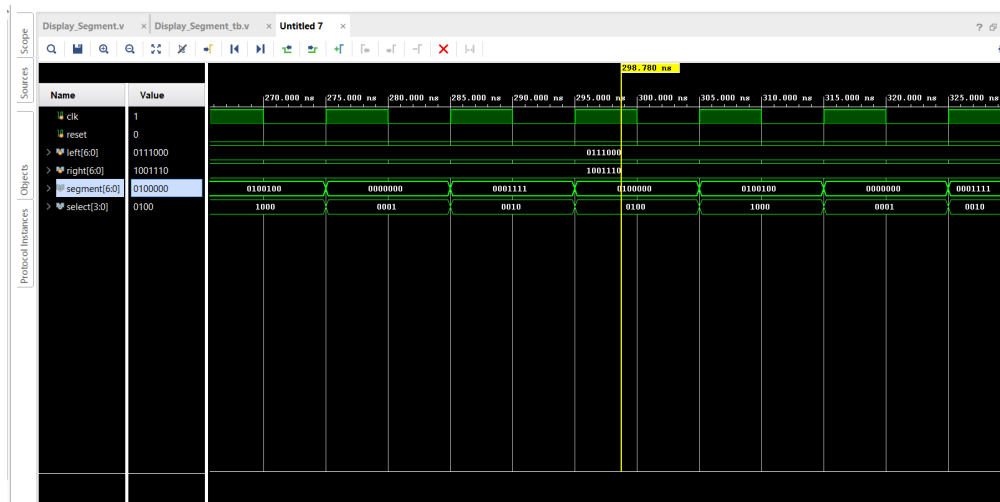


Figure 9: display 4x7 LED

The leftmost two LEDs display the digits '56,' while the rightmost two LEDs display '78,' forming the complete number '5678' across the 4x7 segment LED module. The select variable is used to control and activate each individual LED for proper display.

5.2 Simulation of alarm mode

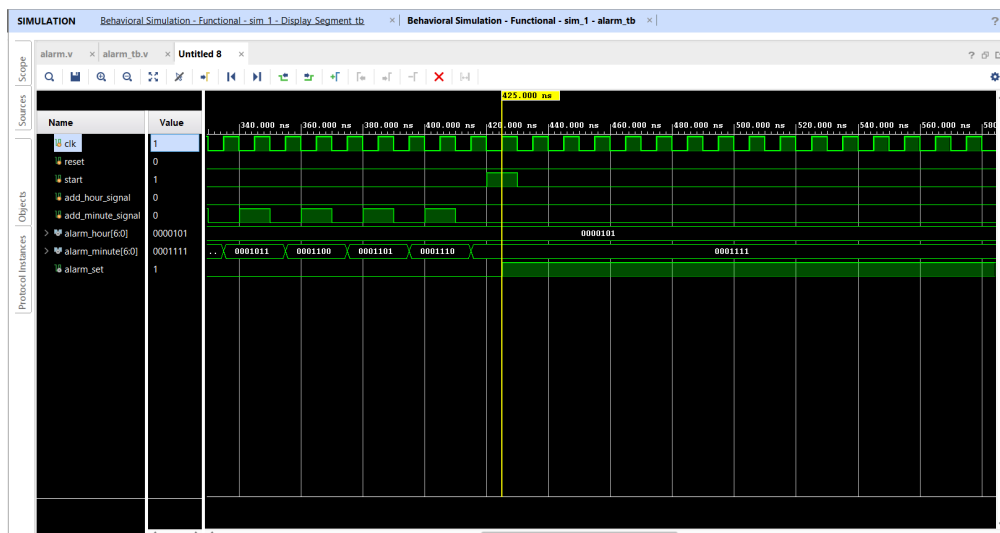


Figure 10: alarm simulation

After incrementing the alarm minutes and hours to the desired time, pressing the 'start' button will set the alarm.

5.3 Simulation of setup mode

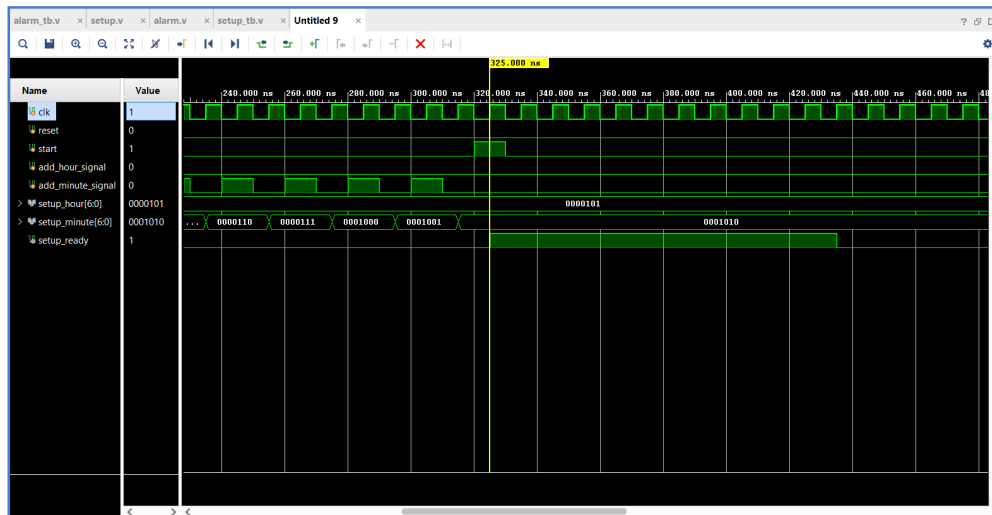


Figure 11: setup simulation

After incrementing the setup minutes and hours to the desired time, pressing the 'start' button will set the setup, successfully configuring the clock.

5.4 Simulation of normal clock mode

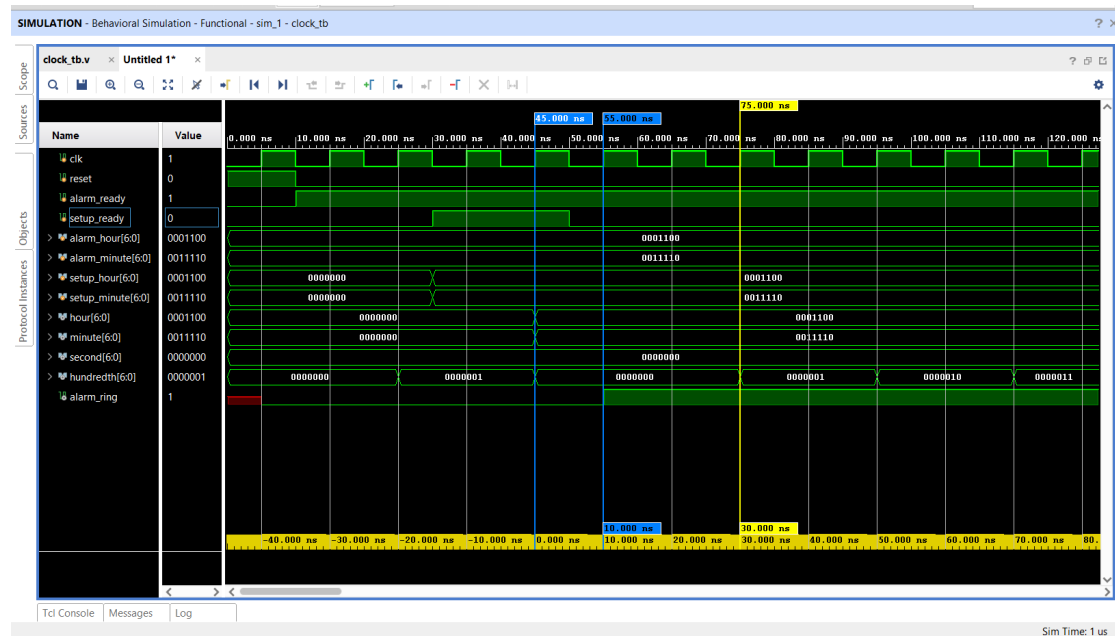


Figure 12: clock simulation

As observed with the two timestamps, when `setup_ready == 1`, it indicates that the setup signal is active in setup mode to configure the clock to the desired time. In this instance, the `alarm_time` is set to that specific time. Consequently, on the next rising edge of the clock, `alarm_ring` is asserted (`alarm_ring = 1`), confirming that both the alarm and setup modes are functioning as intended.

5.5 Simulation of count up mode

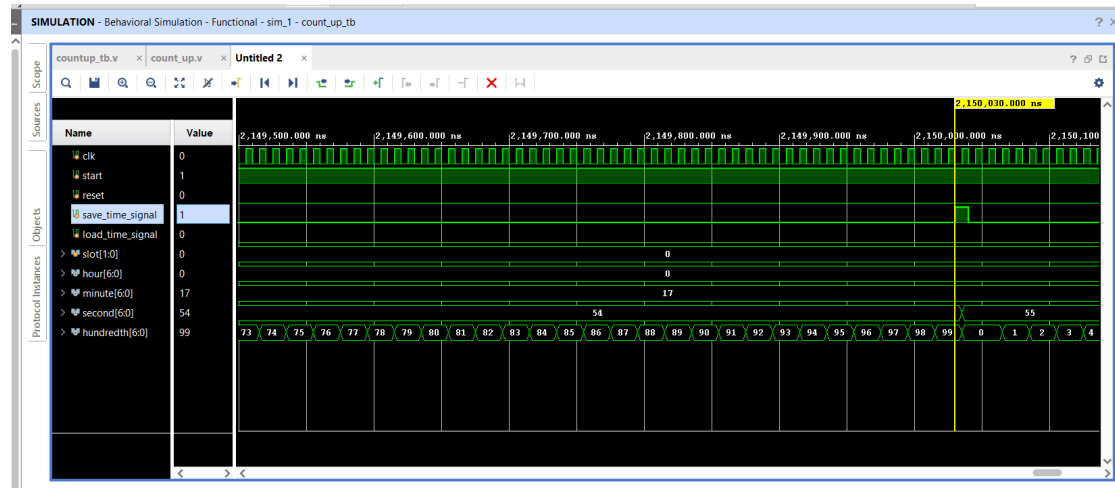


Figure 13: count up simulation

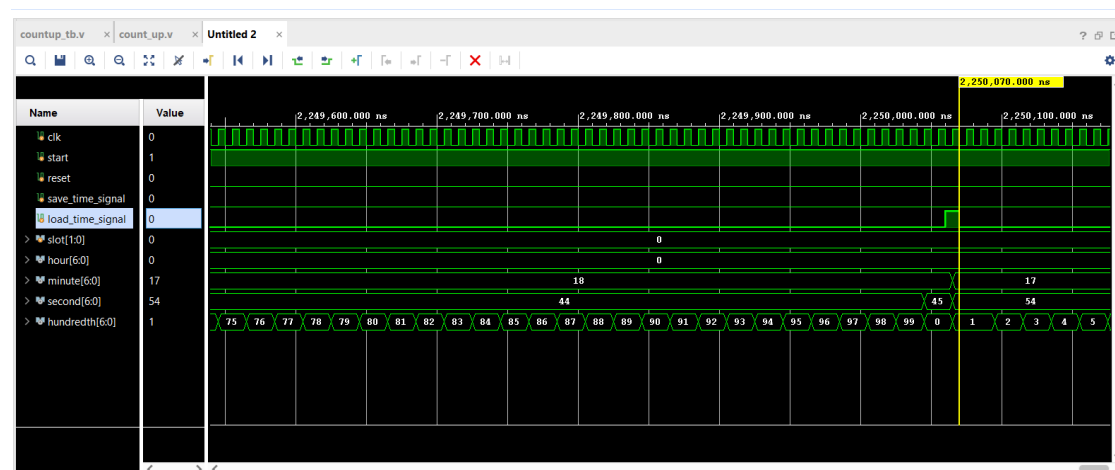


Figure 14: count up simulation

When `save_time_signal == 1`, the current count-up time is successfully saved to a slot. To retrieve and use this saved time, we activate `load_time_signal`, which sets the count-up clock to the previously saved time, as demonstrated above.

5.6 Simulation of count down mode

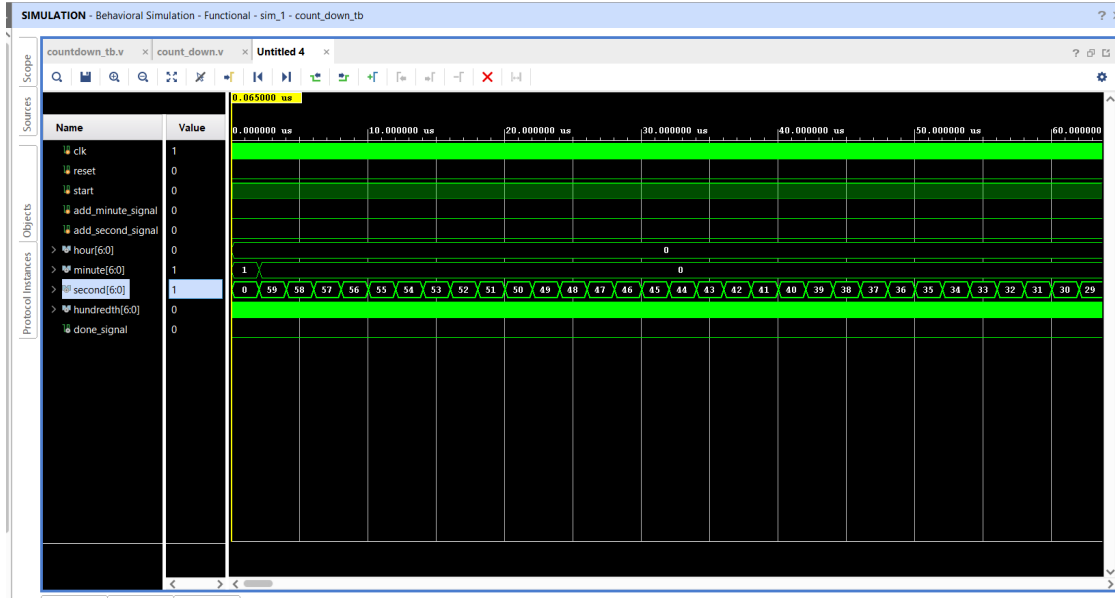


Figure 15: count down simulation

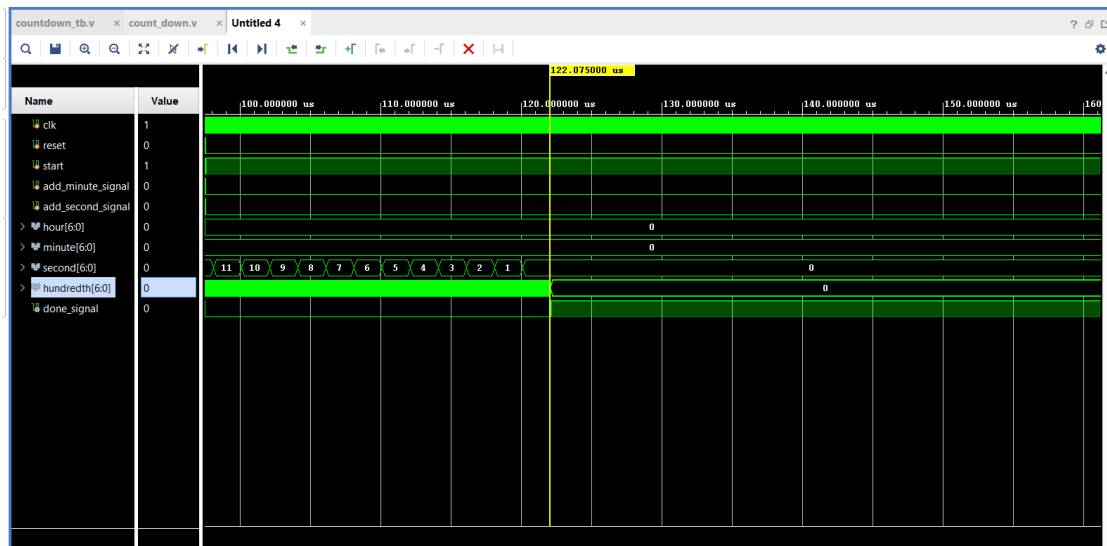


Figure 16: count down simulation

First, the timer is set to 1 minute and 1 second (Figure 15), and it begins counting down normally. When the timer reaches 0 minutes and 0 seconds, the done_signal is asserted, indicating that the countdown has completed.

5.7 Simulation of sportwatch module

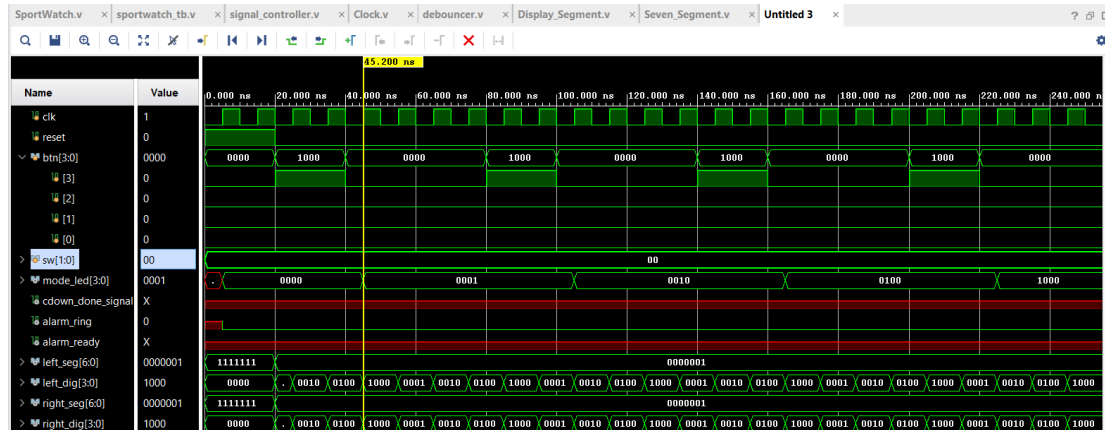


Figure 17: sportwatch simulation

This simulation tests the mode-switching functionality of the top (GUI) module. When button[3] is pressed, the system transitions to a new state. Depending on the selected state, the clock operates according to the corresponding mode, as previously described.

6 Conclusion

6.1 Overview of Results

During the project of developing a sports watch on the Arty Z7 FPGA platform, we successfully designed and implemented a system that meets all the specified requirements. The system supports two operational modes: count-up and count-down, with the ability to display time on two 7-segment LEDs for each time unit. We also integrated functions such as pausing, resuming, and resetting the timer, along with a notification feature at the end of the countdown.

6.2 Summary of the Team's Work

The team clearly assigned tasks and worked collaboratively to complete each phase of the project. Members contributed significantly to circuit design, HDL programming, and creating a user-friendly interface through buttons and switches. Each member took responsibility for a part of the system, from designing functional blocks to testing and refining the software.

6.3 Future Directions

In the future, we plan to expand the system's capabilities by adding features such as the buzzer to the alarm and countdown. This will not only help users manage results easily but also enhance the usability of the sports watch. Additionally, we aim to improve the user interface such as have weather sensor, heart rate sensor or make a real life watch instead of breadboard to provide a better experience when interacting with the device.

6.4 Challenges Encountered

During the project, the team encountered several challenges, particularly in optimizing the HDL code to ensure the stopwatch's performance and accuracy. One notable issue was the need to manage distinct reset, start, and pause signals for each operational mode while being limited to only four buttons on the Arty Z7. This constraint made it challenging to separate signals originating from different always blocks, complicating the code optimization process. Additionally, we faced hardware compatibility issues with the LEDs and switches used in our design. However, through thorough research and experimentation, we were able to identify and implement effective solutions to overcome these obstacles.

6.5 Breakdown of Work

- Idea planning: we have to decide what components to use in this project such as 4x7 segment , wires, breadboard.
- Design from small to larger: First we design and testing how to display on 4x7 segment LED, then we deal with button debouncing and final make other mode.



- HDL Programming: Duong Gia Bao were responsible for writing Verilog code for the watch's functionalities.
- Testing and Refinement: Bui Thai An conducted testing and made necessary adjustments to enhance features.



7 Link to demonstration video and source code

7.1 Demonstration video:

https://drive.google.com/drive/u/1/folders/1aGayJnP_QJ1lnjmDcRf0JuzRk-IVczde

7.2 Source code:

<https://github.com/CoderMongmer/Logic-Design-Project>

8 Work distribution

- Duong Gia Bao: Hardware design
- Bui Thai An: Verilog testing and implementation