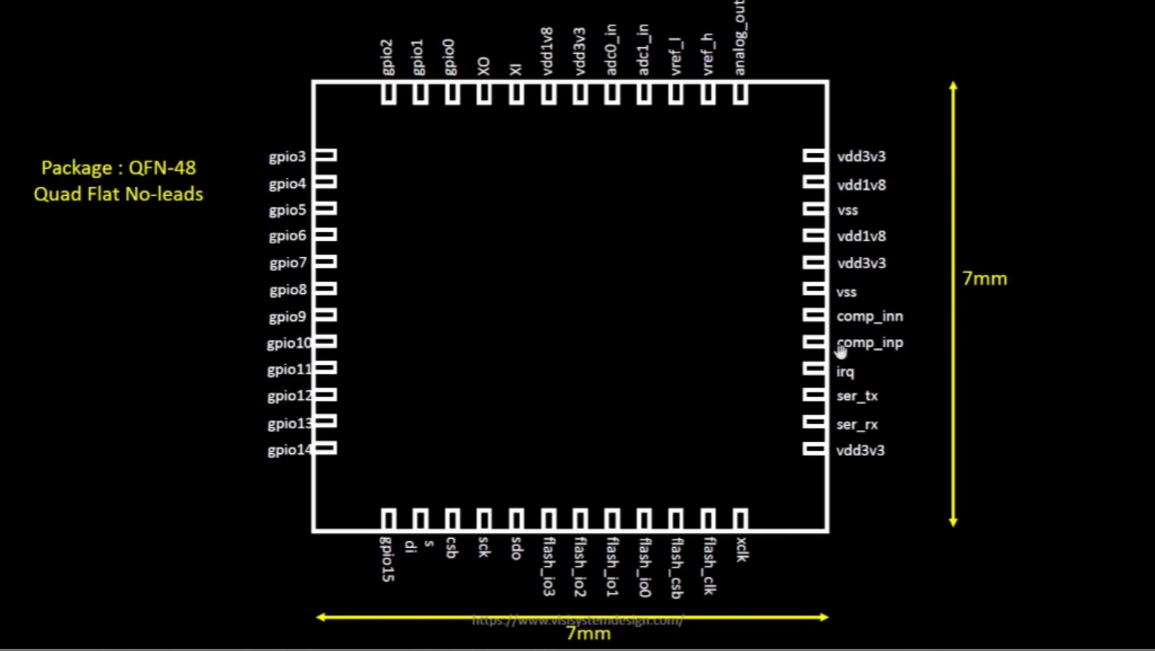
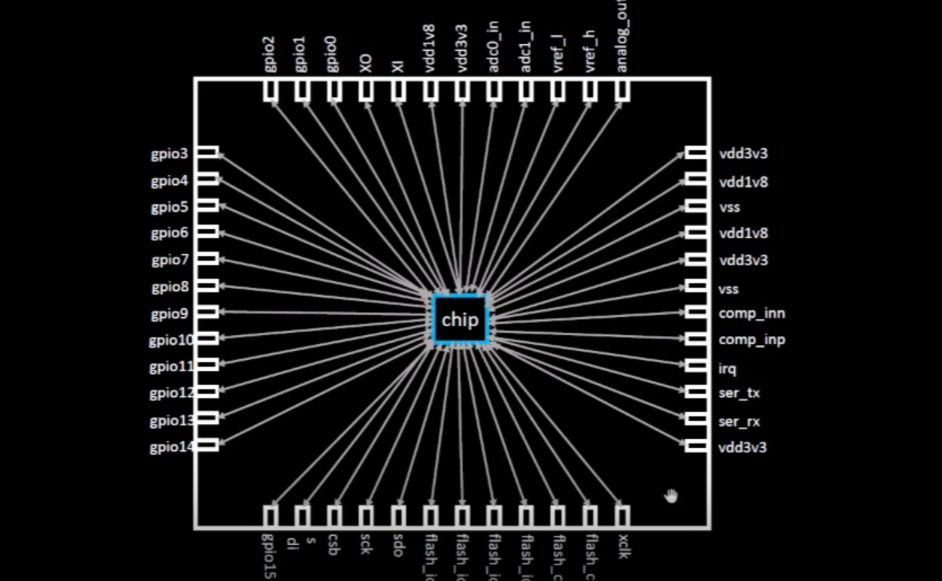
# **Introduction**

These days, you can find the word "chip" in both news stories and social media feeds. The electronics industry is built on these little electronic components. Generally, in order to discover a chip, one must first locate a PCB (Printed Circuit Board), which is easily located in commonplace devices like computers, TVs, air conditioners, cell phones, and more. As an alternative, you might look at the picture of an Arduino PCB board below.

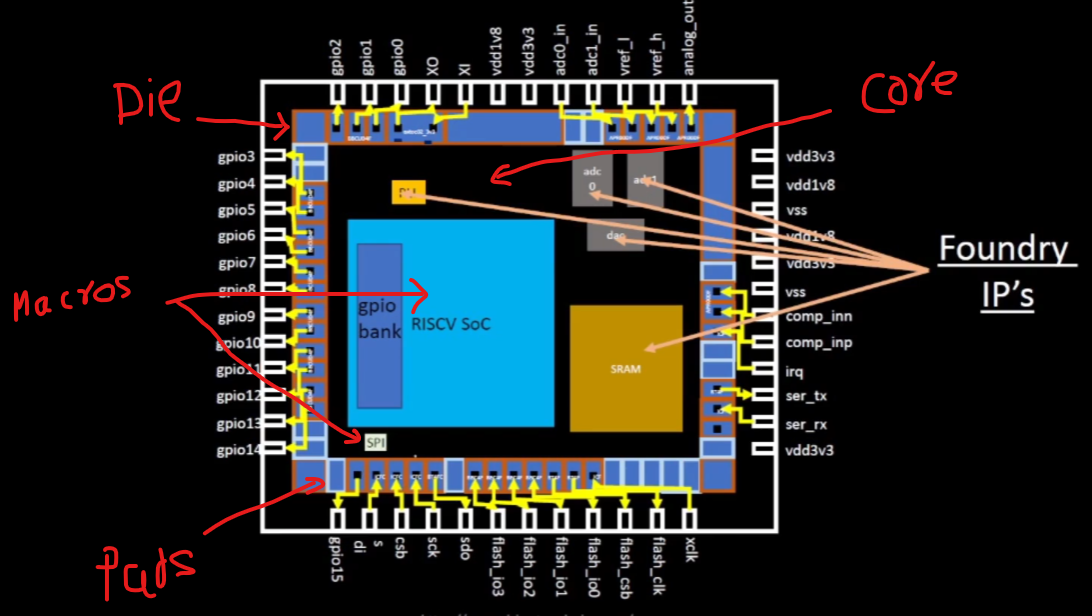


An integrated circuit that is contained within its packaging is indicated by the yellow circle.

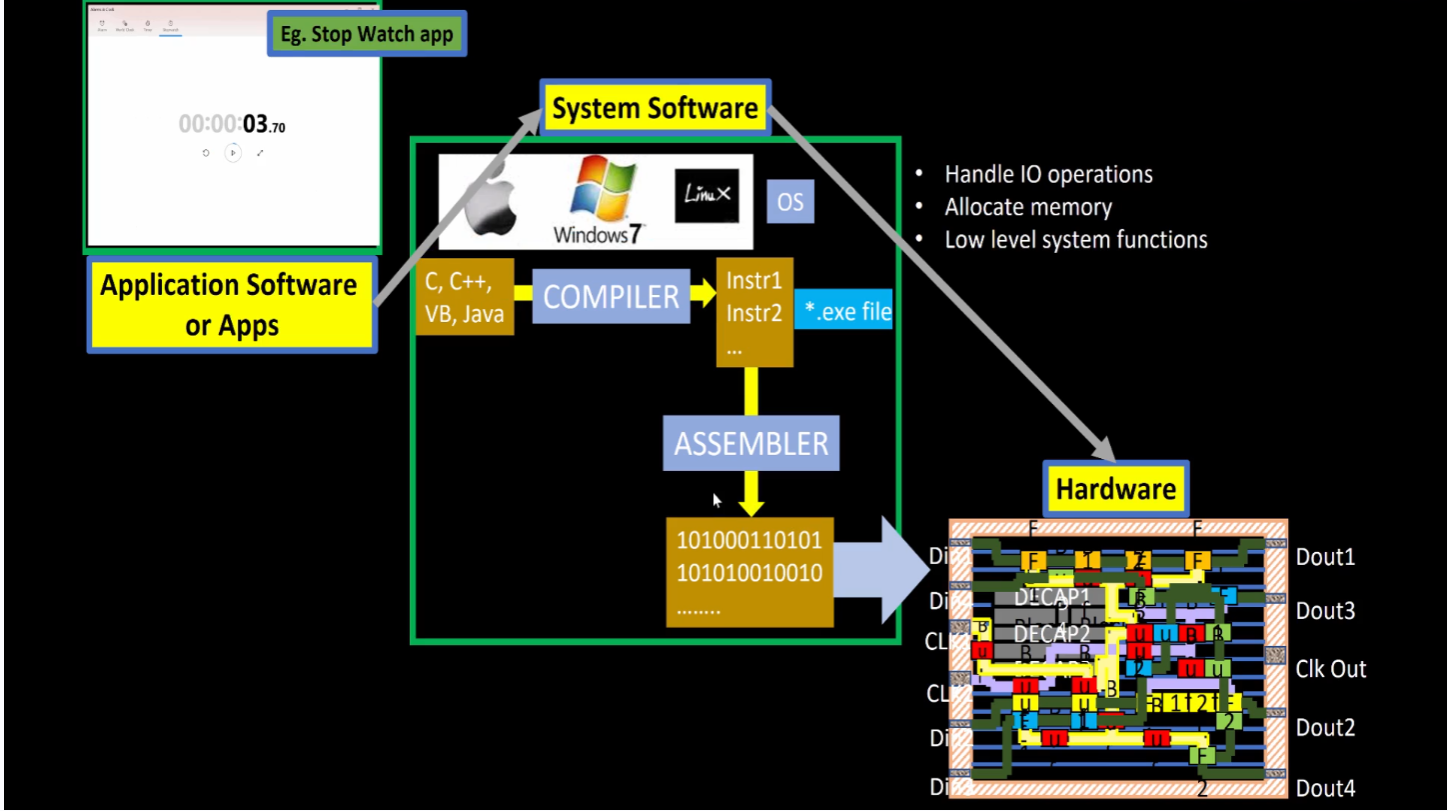


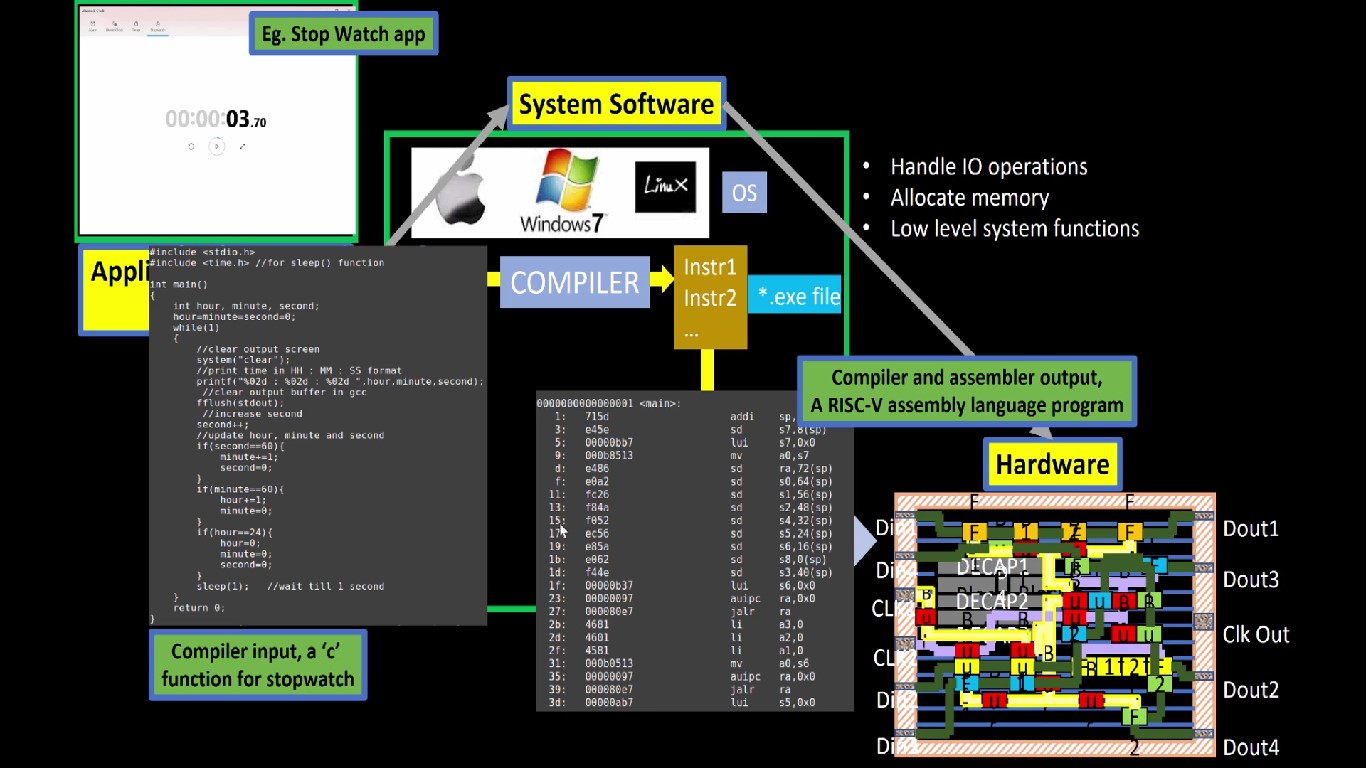
The Size of the package is 7x7 mm. It consists of 48 pins. The package type is QFN (Quad Flat No-leads).There are different packages available such as BGA, SOIC, LGA, QFP, etc. But for our project, we are going to discuss the QFN package.   


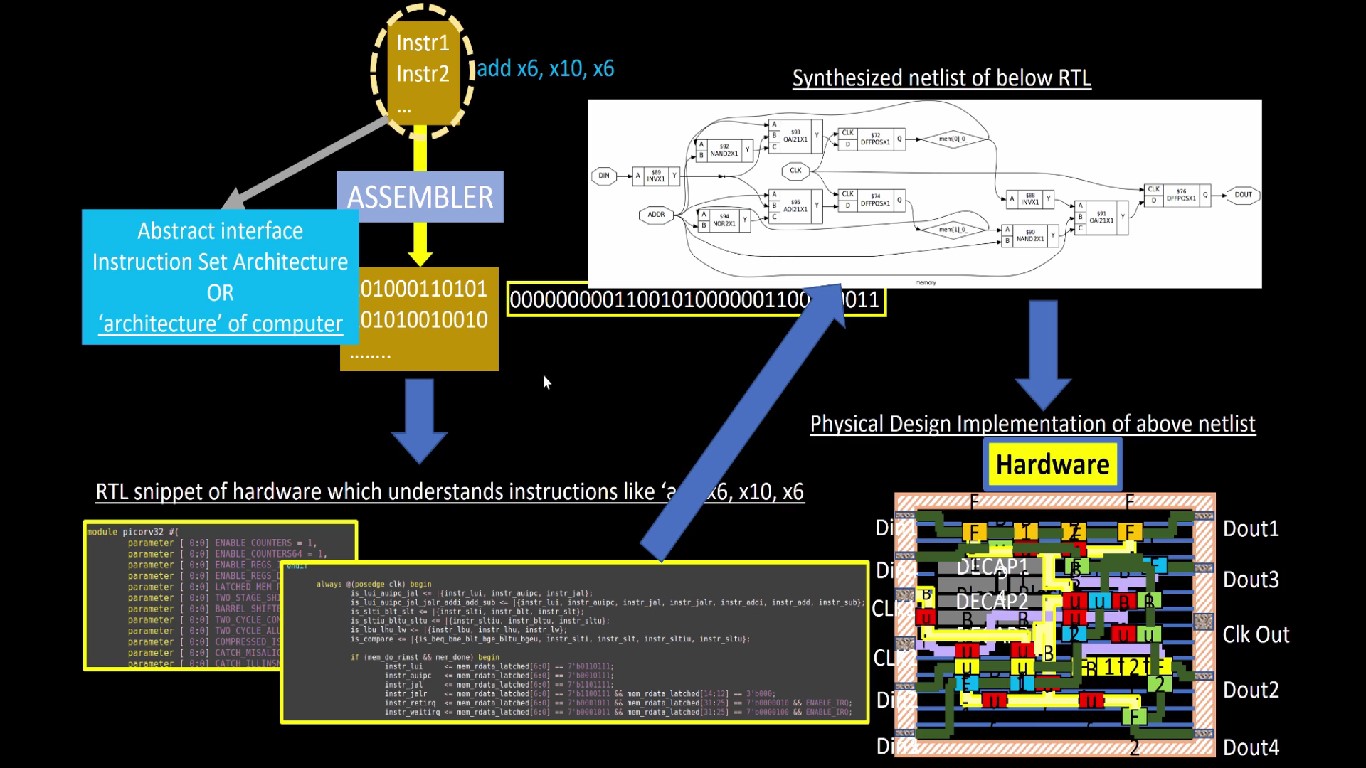
The chip is inside the package. It is connected with the outside world with the help of pads. The pads are the 48pins which are seen in the above figure.



A chip consists of a Die, core area, Pads, IPs, Macros, and standard cells, nets and via’s. So the question arises why do we need chips? Chips do all the computation work and make our lives easy. Let's take an example of a stopwatch.







A programming language, such as C, C++, or Java, is used to write the application or software. These coding statements are transformed into instruction sets by the OS (System Software) with the aid of a compiler. An assembler then translates the instruction sets back into machine language, or binary digits (0s and 1s). The hardware, or chip, will decode the software and generate the result.

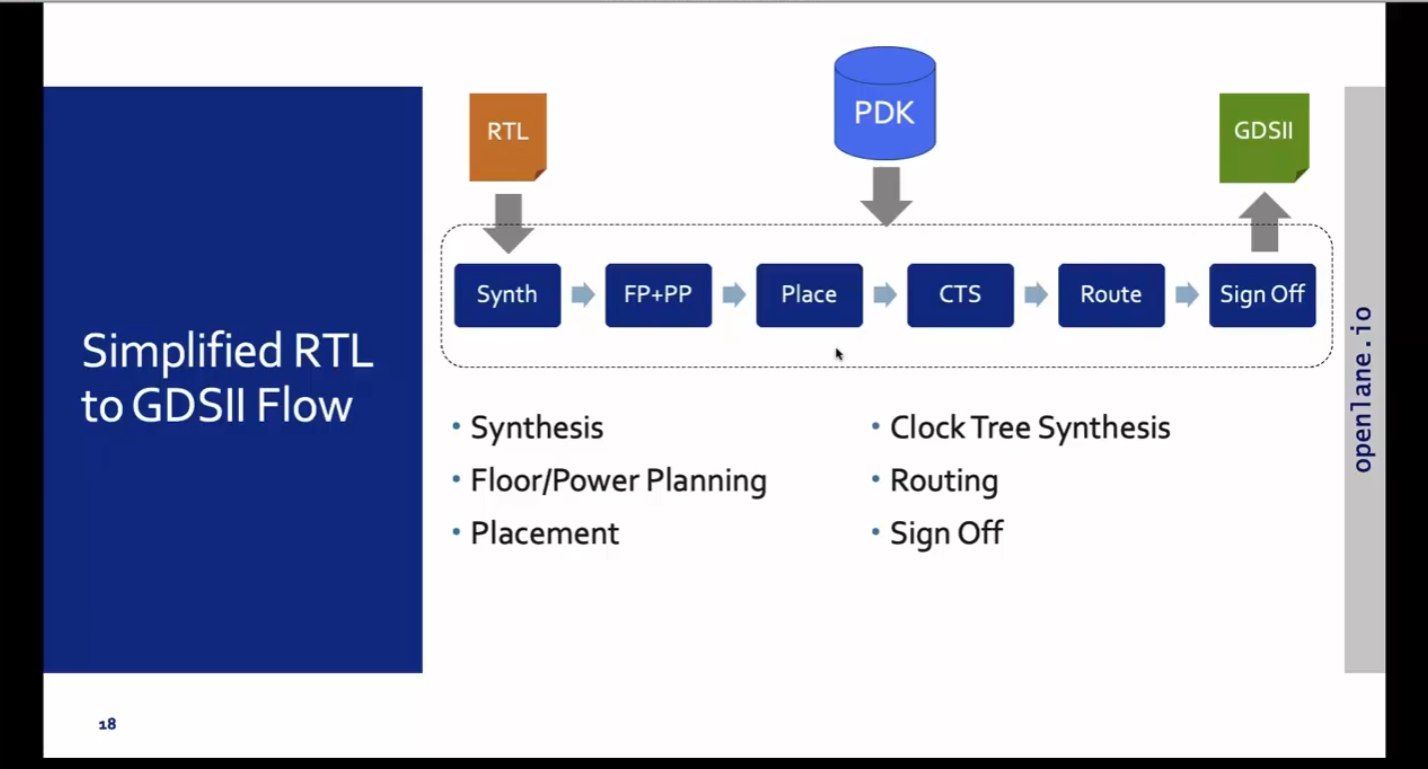
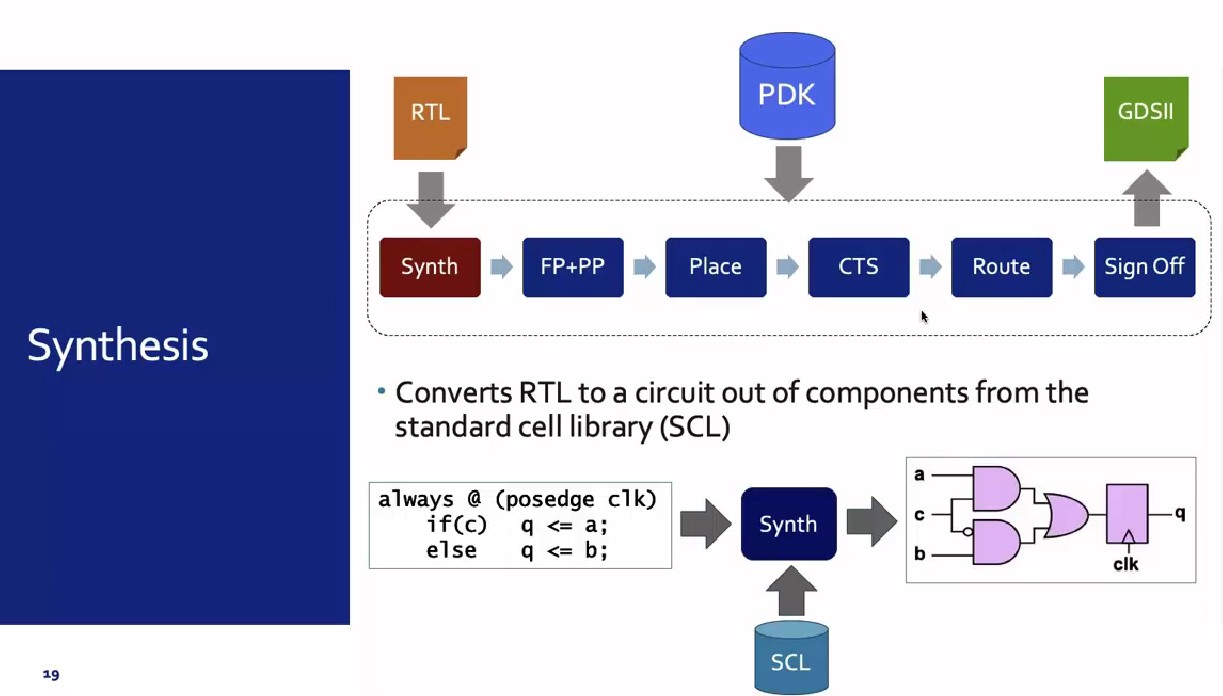
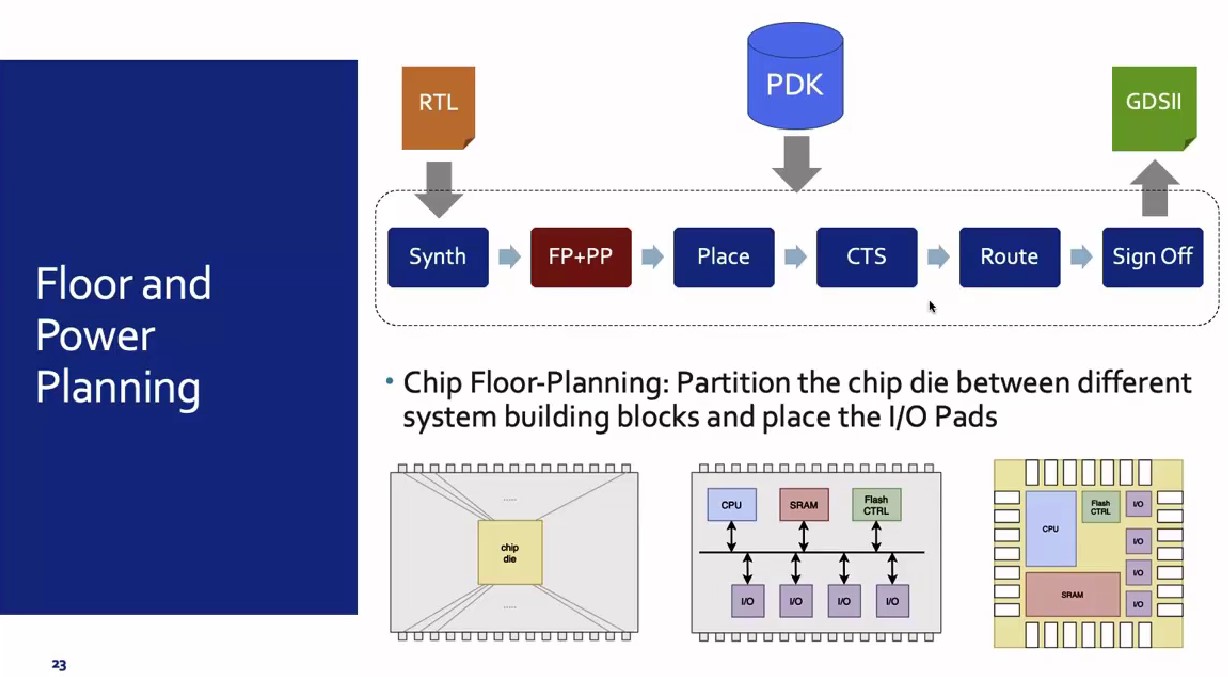
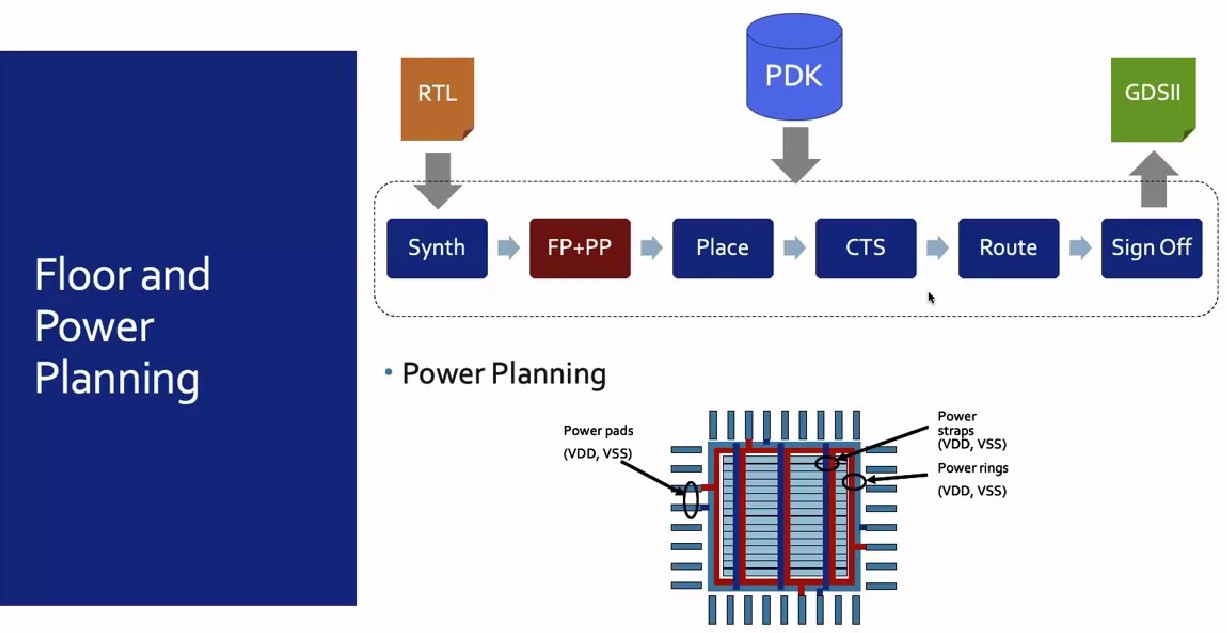
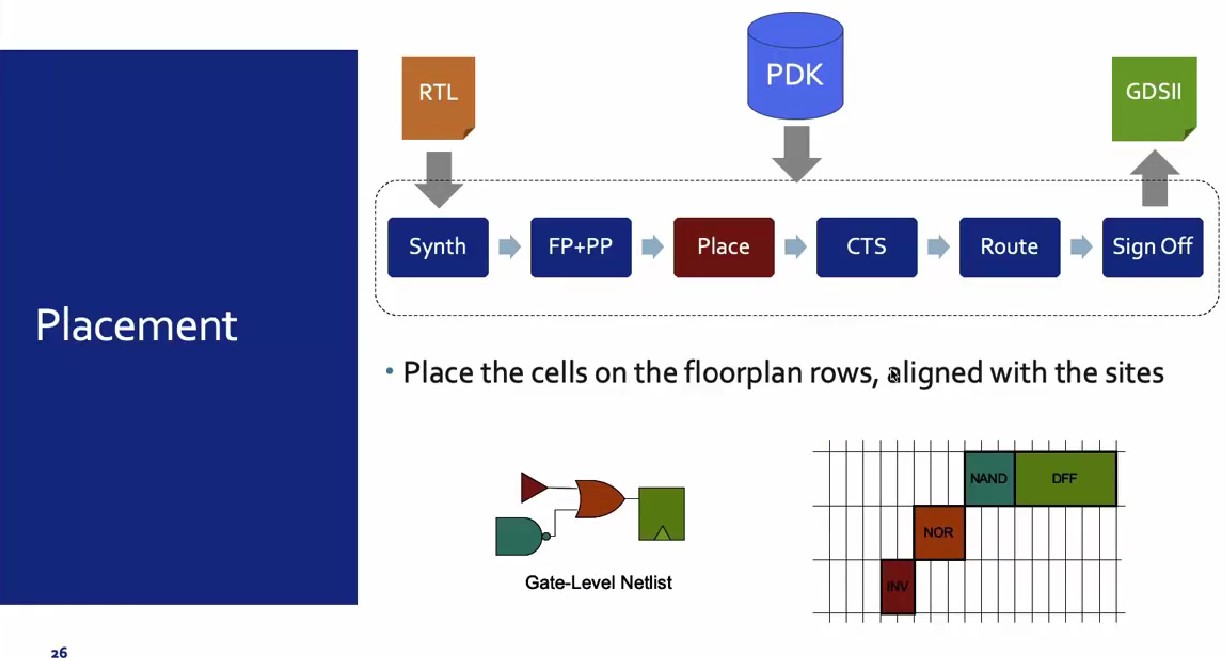


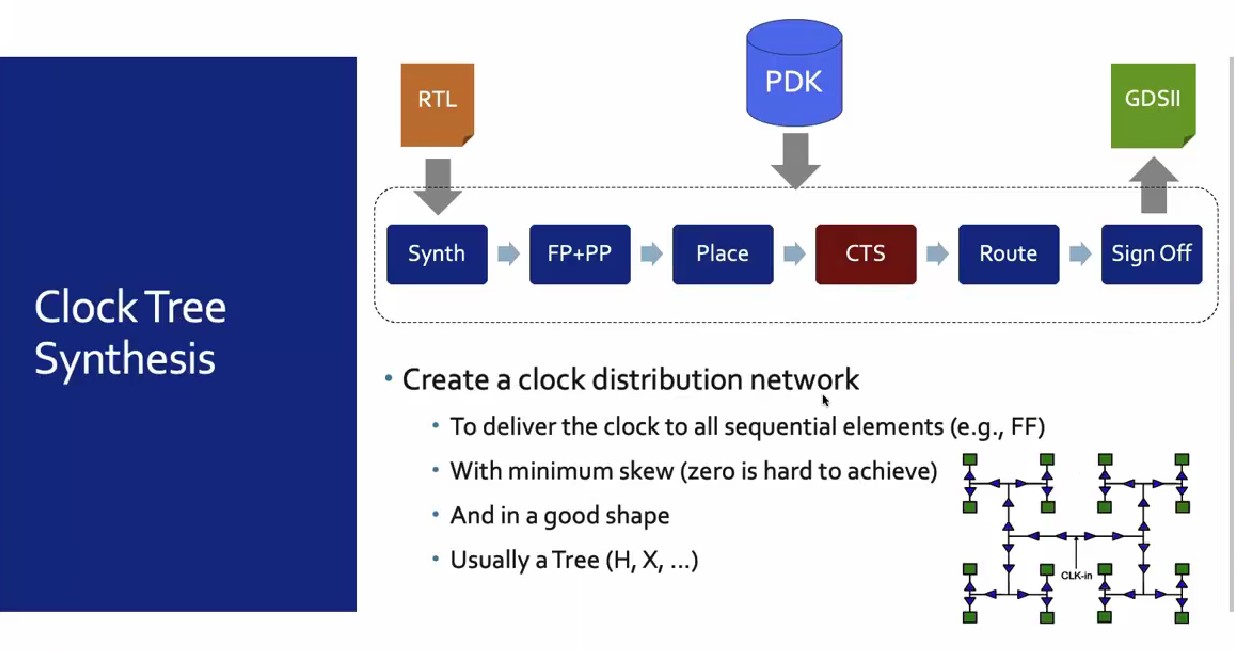
Fig: RTL to GDSII Flow

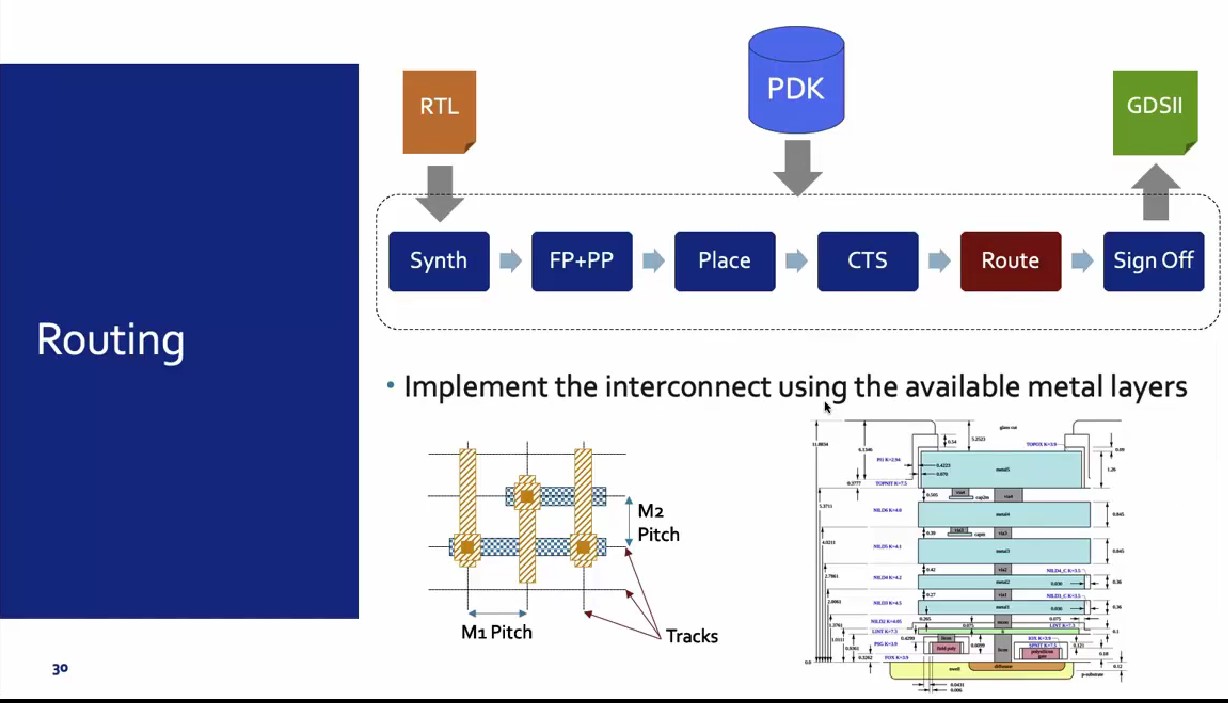


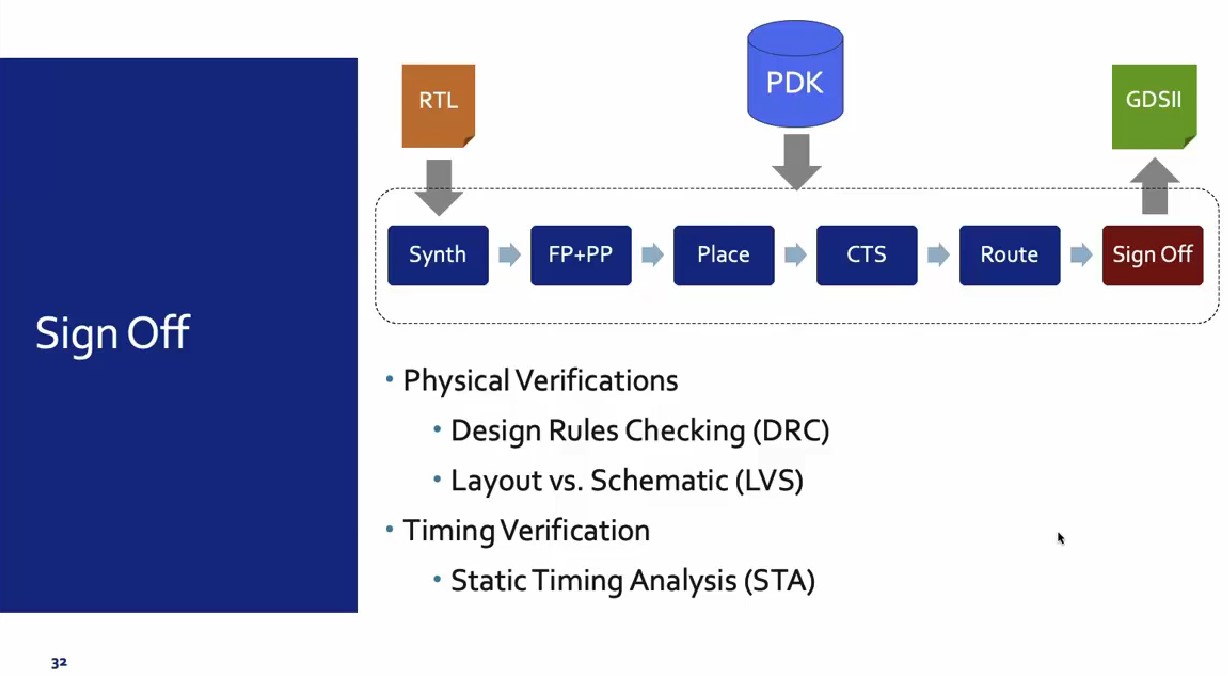




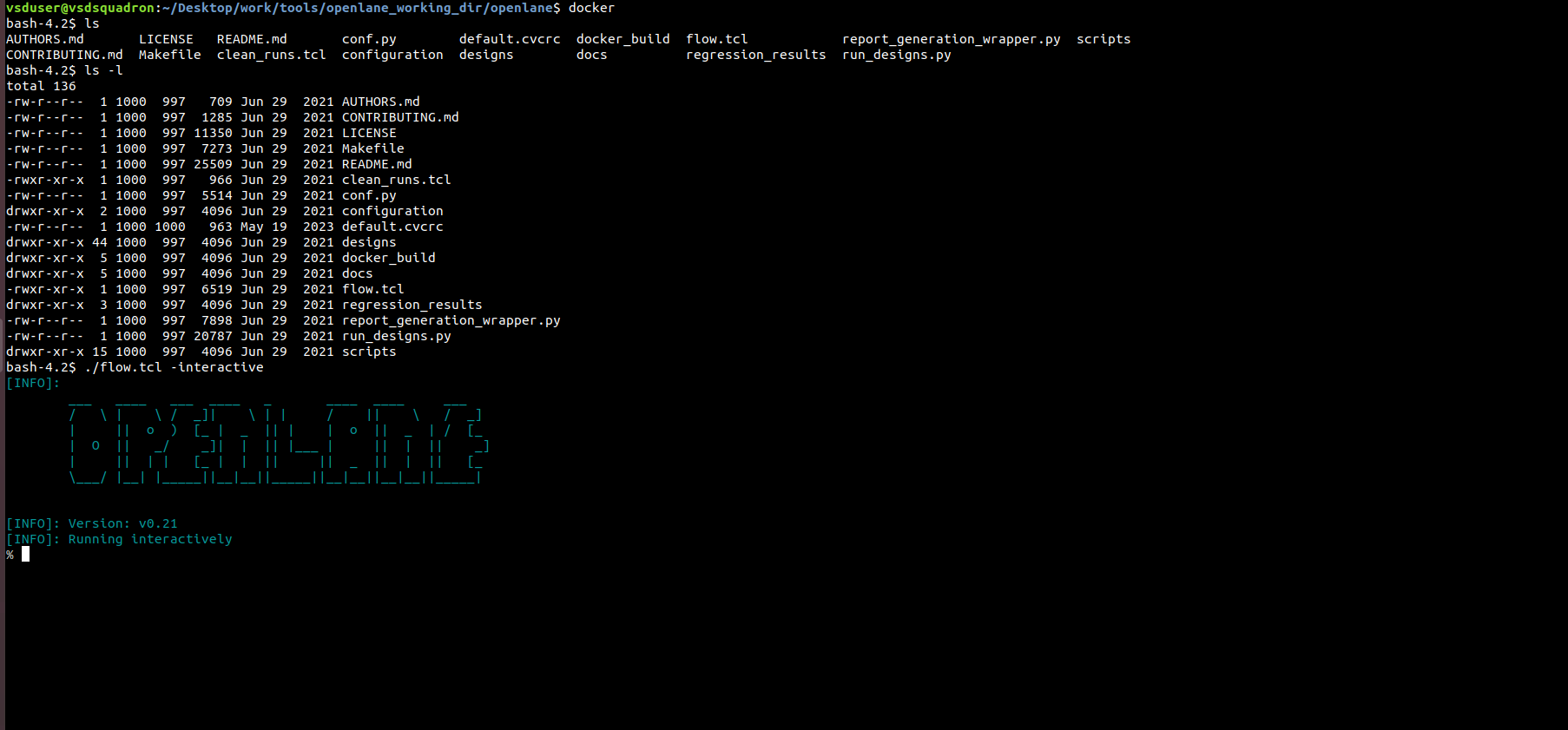








1. Synthesis: Converts RTL to a circuit out of components from the standard cell library (SCL)
2. Floor Planning: Partition the chip die between different system building blocks and place the I/O pads, defining pin locations, macro placements, and power planning by placing Power rings, power straps and power pads.
3. Placement: Place the cells on the rows and align with the sites by using global and detailed method.
4. CTS (Clock Tree Synthesis): Create a clock distribution network to deliver the clock to all sequential elements. It is done by using different types of Tree such as H, X, Fishbone etc.
5. Route: Implement the interconnect using the available metal layers by using global routing (Which generates routing guides) and detailed routing(Uses the routing guide and implements the actual wires).
6. Sign Off: In this step, we will do physical verification which includes DRC(Design Rule Check), LVS(Layout Vs Schematic), and timing verification which includes STA(Static Timing Analysis)



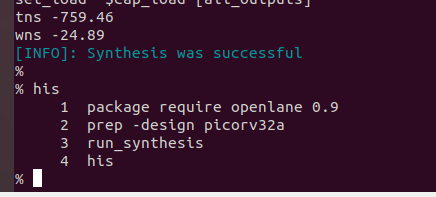
By using docker command and ./flow.tcl – interactive command the open lane tool is opened.



Once the openlane is opened we need to load all the package everytime. By using command package require openlane 0.9

After that we need to do design setup by providing all the input files. By using command prep -design picorv32a.

After run\_synthesis command it will map the all the logic cells to Abs cell after it will generate the gate level netlist.



These are the commands we used in Day1 to understand the tool and get the basic Idea.