United International University
Department of CSE
CSE 313: Computer Architecture
Midterm Examination
Summer 2022

Time: 1 hour and 45 minutes **Full Marks: 30**

[Any examinee found adopting unfair means will be expelled from the trimester / program as per UIU disciplinary rules.]

[N.B.: Answer all the questions. Assume any data if it is not mentioned explicitly.]

1. a) Suppose, there are three classes of instructions A, B, and C in a particular instruction set architecture with CPIs 1.2, 2, and 2.5 respectively. The number of instructions from each class in two separate programs is as follows: [5]

Programs	Instruction classes		
	A	B	C
P1	40	10	16
P2	12	13	40

If both the programs are run on the same device with a clock frequency of 2GHz, then find out which program is faster and by how much.

b) Assume that a processor with a 4GHz clock rate is executing a program that requires the following instruction types.

Instructions	FP	INT	L/S	Branch
Instruction count (10^6)	160	110	10	16
CPI	2	1	5	2

If you want to run the program two times faster than now, then how much should you improve the CPI of FP instructions?

c) Explain Amdahl's law with an example. Also, write in brief about the parameters in Amdahl's law. [2]

2. Consider the following C function that accepts two arguments, **an integer array** and the **length of the array n**. This function doubles the value of the positive integers in the array and returns the sum of the updated positive integers. The starting MIPS assembly instruction address is 1000.

```
int pos_sum(int a[], int n) {

 int sum = 0, i = 0;
 while (i < n) {

  if (a[i] > 0) {
   a[i] = 2 * a[i];
   sum += a[i];
  }

  i++;
 }

 return sum;
}
```

Assume that the variable **sum** corresponds to the register **$s1** and the variable **i** corresponds to **$s2.**

a) Convert the code to the corresponding MIPS assembly instructions. [6]

b) Convert the first 8 lines of your assembly instructions to the corresponding machine code. No need to convert it to binary. [5]

c) Consider an array **A**, whose base address is in **$s3**. The ISA is **double word addressable**, that is the memory can contain double words. What will be the corresponding MIPS assembly code for accessing the **address** of the 9th element of the array, i.e **A[9].** (Write in a **single line**) [2]

3. a) Simulate the division algorithm to divide B by A, where A = 0100 and B = 1110. Show all the iterations and steps required to complete this division. [3]

b) Draw the flowchart of above simulation. [2]

MIPS Machine Codes

Instruction	Opcode	Function Code
add	0	32
sub	0	34
lw	35	
sw	43	
and	0	36
or	0	37
nor	0	39
andi	12	
ori	13	
sll	0	0
srl	0	2
beq	4	
bne	5	
slt	0	42
j	2	
jr	0	8
jal	3	
addi	8	

MIPS Registers

Name	Register Number
$zero	0
$at	1
$v0-$v1	2-3
$a0-$a3	4-7
$t0-$t7	8-15
$s0-$s7	16-23
$t8-$t9	24-25
$k0-$k1	26-27
$gp	28
$sp	29
$fp	30
$ra	31