United International University (UIU)

Dept. of Computer Science & Engineering (CSE)

Mid-Term Exam::Trimester::Fall 2021

Course Code: CSE 425 Course Title: Microprocessor, Microcontroller and Interfacing
Sec: (A, B, C) Total Marks: 30 Duration: 1 hour 45 minutes

Any examinee found adopting unfair means would be expelled from the trimester/ program as per UIU disciplinary rules.

Question 1: There are two parts in this question. Answer any one.		**(6 Marks)**
a.	Draw the diagram of an 16-bit microprocessor with 20 bit address bus and 8 bit data bus interfaced to 128KB RAM system using the full decoding method. Each RAM chip has a 15 bit address bus and 8 bit data bus. Provide the corresponding address range (starting address and end address) for the system.	[4]
b.	Modify the circuit of (a) to address memory range A0000H - BFFFFH	[2]
OR,		
a.	Consider that a RAM chip has the following pins: CS', WE, A0-A9, D0-D7. Draw a block diagram of the RAM chip and briefly explain its operations using a table.	[4]
b.	State the differences between SRAM and DRAM.	[2]
Question 2: Answer all the questions.		**(6 Marks)**
a.	Suppose after execution of an signed additional instruction (5FFFH - A000H). What would be the value of ZF (Zero flag), CF (Carry Flag), PF (Parity Flag), OF (Overflow flag).	[4]
b.	Which address pins and data pins are multiplexed in 8086? Why?	[2]
Question 3: Answer all the questions.		**(6 Marks)**
a.	In programmed I/O, if we set the value of the DDRX register of a particular port to 92H, what does it signify? Why M/IO' Pin is required in standard IO? Explain briefly.	[1+1]
b.	Suppose, transfer of bus control in either direction, from processor to device or vice-versa, takes 150 ns. One of the I/O devices has a data transfer rate of 50KB/sec and employs DMA. If we employ DMA in cycle stealing mode for the first half of the bytes and burst mode for the other half, how long will it take to transfer a block of 1024 bytes?	[4]

Question 4: Answer all the questions.		**(6 Marks)**
a.	If we have a RAM of 64 KB size and a data bus of 4 bits, what should be the size of the address bus?	[1]
b.	Briefly explain memory organization of a microcomputer.	[3]
c.	Differentiate between Data Bus and Address Bus.	[2]
Question 5: Answer all the questions.		**(6 Marks)**
a.	Suppose, the address 7500H: BFD2H has an instruction. To execute the instruction, what should be the value of CS if IP is (i) AB22H (ii) BFDAH	[1+1 =2]
b.	Write in brief about the necessity of memory segmentation.	[2]
c.	Is overlapping segmentation useful? Justify your answer.	[2]