66. Define byte, word, and doubleword.
67. Convert the following words into ASCII-coded character strings:
    (a) FROG
    (b) Arc
    (c) Water
    (d) Well
68. What is the ASCII code for the Enter key and what is its purpose?
69. What is the Unicode?
70. Use an assembler directive to store the ASCII-character string 'What time is it?' in the memory.
71. Convert the following decimal numbers into 8-bit signed binary numbers:
    (a) +32
    (b) −12
    (c) +100
    (d) −92
72. Convert the following decimal numbers into signed binary words:
    (a) +1000
    (b) −120
    (c) +800
    (d) −3212

3–5 QUESTIONS AND PROBLEMS

1. What do the following MOV instructions accomplish?
   (a) MOV AX,BX
   (b) MOV BX,AX
   (c) MOV BL,CH
   (d) MOV ESP,EBP
   (e) MOV RAX,RCX
2. List the 8-bit registers that are used for register addressing.

3. List the 16-bit registers that are used for register addressing.
4. List the 32-bit registers that are used for register addressing in the 80386 through the Core2 microprocessors.
5. List the 64-bit registers available to the 64-bit mode of the Pentium 4 and Core2.
6. List the 16-bit segment registers used with register addressing by MOV, PUSH, and POP.
7. What is wrong with the MOV BL,CX instruction?
8. What is wrong with the MOV DS,SS instruction?

Answers to Questions and Problems

CHAPTER 1

2. Herman Hollerith
4. Konrad Zuse
6. ENIAC
8. Augusta Ada Byron
10. A machine that stores the instructions of a program in the memory system.
12. 200 million
14. 16M bytes
16. 1993
18. 2000
20. Millions of instructions per second
22. A binary bit stores a 1 or a 0.
24. 1024K
26. 1024
28. System area and transient program area
30. 640K
32. 1M
34. 80386, 80486, Pentium, Pentium Pro, PII, PIII, P4, and Core2
36. The basic I/O system
38. The XT was used with the 8088 and 8086 and beginning with the 80286, the AT became the name of the system.
40. 8-bit and 16-bit
42. The advanced graphics port is designed to support video cards.
44. The serial ATA interface is designed to support disk drive memory.
46. 64K
48. See Figure 1–6.
50. Address, data, and control buses.
52. $\overline{\text{MRDC}}$
54. Memory read operation
56. (a) 8-bit signed number (b) 16-bit signed number (c) 32-bit signed number (d) 32-bit floating-point number (e) 64-bit floating-point number
58. (a) 156.625 (b) 18.375 (c) 4087.109375 (d) 83.578125 (e) 58.90625
60. (a) 10111_2, 27_8, and 17_{16} (b) 1101011_2, 153_8, and 6B (c) 1001101011_2, 2326_8, and $4D6_{16}$ (d) 1011100_2, 134_8, and $5C_{16}$ (e) 10101101_2, 255_8, and AD
62. (a) 0010 0011 (b) 1010 1101 0100 (c) 0011 0100 . 1010 1101 (d) 1011 1101 0011 0010 (e) 0010 0011 0100 . 0011
64. (a) 0111 0111 (b) 1010 0101 (c) 1000 1000 (d) 0111 1111
66. Byte is an 8-bit binary number, word is a 16-bit binary number, doubleword is a 32-bit binary number.
68. Enter is a 0DH and it is used to return the cursor/print head to the left margin of the screen or page of paper.
70. LINE1 DB 'What time is it?'
72. (a) 0000 0011 1110 1000 (b) 1111 1111 1000 1000 (c) 0000 0011 0010 0000 (d) 1111 0011 0111 0100
74. char Fred1 = –34
76. Little endian numbers are stored so the least significant portion is in the lowest numbered memory location and big endian numbers are stored so the most significant part is stored in the lowest numbered memory location.
78. (a) packed = 00000001 00000010 and unpacked 00000001 00000000 00000010 (b) packed = 01000100 and unpacked 00000100 00000100 (c) packed = 00000011 00000001 and unpacked 00000011 00000000 00000001 (d) packed = 00010000 00000000 and unpacked 00000001 00000000 00000000 00000000
80. (a) 89 (b) 9 (c) 32 (d) 1
82. (a) +3.5 (b) −1.0 (c) +12.5

Chapter One

1. Charles Babbage
3. Herman Hollerith
5. To decode the Enigma code during World Was II
7. Intel Corporation
9. Grace Hopper
11. 8080
13. 8086/8088
15. 4G bytes
17. 1995
19. 80486 through the Core2
21. Complex Instruction Set Computer
23. 1024
25. 1024
27. 1,000,000
29. 2G or 3G for 32-bit mode and currently 8G for 64-bit mode
31. 1G
33. Currently 1T byte using a 40-bit address
35. Protected memory or extended memory
37. An early operating system called the Disk Operating System
39. Video Electronics Standards Association
41. Universal Serial Bus
43. Extended Memory System
45. System Area
47. The BIOS controls the computer at its most basic level and provides for compatibility between computers.
49. The microprocessor is the controlling element in a computer system.
51. Address bus
53. The I/O read signal causes an I/O device to be read.
55. (a) defines a byte or bytes of memory (b) defines a quadword or quadwords of memory (c) defines a word or words of memory (d) defines a doubleword or doublewords of memory
57. (a) 13.25 (b) 57.1875 (c) 43.3125 (d) 7.0625
59. (a) 163.1875 (b) 297.75 (c) 172.859375 (d) 4011.1875 (e) 3000.05078125
61. (a) 0.101 0.5 0.A (b) 0.0000101 0.024 0.0A (c) 0.10100001 0.502 0.A1 (d) 0.11 0.6 0.C (e) 0.1111 0.74 0.F
63. (a) C2 (b) 10FD (c) BC (d) 10 (e) 8BA
65. (a) 0111 1111 (b) 0101 0100 (c) 0101 0001 (d) 1000 0000
67. (a) 46 52 4F 47, (b) 41 72 63, (c) 57 61 74 65 72, and (d) 57 65 6C 6C
69. The Unicode is the 16-bit alphanumeric code used with Windows
71. (a) 0010 0000 (b) 1111 0100 (c) 0110 0100 (d) 1010 0100
73. DB -34

CHAPTER 2

2. 16
4. EBX
6. Holds the offset address of the next step in the program.
8. No, if you add +1 and −1 you have zero, which is a valid number.
10. The I-flag.
12. The segment register addresses the lowest address in a 64K memory segment.
14. (a) 12000H (b) 21000H (c) 24A00H (d) 25000H (e) 3F12DH
16. DI
18. SS plus either SP or ESP
20. (a) 12000H (b) 21002H (c) 26200H (d) A1000H (e) 2CA00H
22. All 16M bytes
24. The segment register is a selector that selects the descriptor from a descriptor table. It also sets privilege level of the request and chooses either the global or local table.
26. A00000H–A01000H
28. 00280000H–00290FFFH
30. 3
32. 64K
34.

0000 0011	1101 0000
1001 0010	0000 0000
0000 0000	0000 0000
0010 1111	1111 1111

36. Through a descriptor stored in the global table
38. The program invisible registers are the cache portions of the segment registers and also the GDTR, LDTR, and IDTR registers.
40. 4K
42. 1024
44. Entry zero or the first entry
46. The TLB caches the most recent memory accesses through the paging mechanism.
50. 1T

CHAPTER 3

2. AL, AH, BL, BH, CL, CH, DL, and DH
4. EAX, EBX, ECX, EDX, ESP, EBP, EDI, and ESI
6. CS, DS, ES, SS, FS, and GS
8. You may not specify mixed register sizes.
10. (a) MOV AL,12H (b) MOV AX,123AH
    (c) MOV CL,0CDH (d) MOV RAX,1000H
    (e) MOV EBX,1200A2H

Chapter Two

1. Program visible register are the registers that are directly used in an instruction.
3. The 80386 through the Core2
5. CL, CX, ECX, or RCX
7. INC and DEC
9. Odd
11. The 80386 through the Core2
13. (a) 10000H—1FFFFH (b) 12340H—2233FH (c) 23000H—32FFFH
    (d) E0000H—EFFFFH (e) AB000H—BAFFFH
15. 100000H
17. EAX, EBX, ECX, EDX, EBP, ESI, and EDI
19. Stack
21. (a) 23000H (b) 1C000H (c) CA000H (d) 89000H (e) 1CC90H
23. Any location in the memory system
25. 8,192
27. 01000000H—0100FFFFH
29. 4
31. Descriptor 20H, local table, a privilege ring 1
35. GDTR
37. The internal cache is loaded with the base address, offset address, and access rights byte
39. The GDTR address the Global Descriptor Table
41.4,096
43. 4M
45. 30000000H
49. The flat mode memory system is used with 64-bit operation of the Core2

Chapter Three

1. (a) the contents of BX is copied into AX (b) The contents of AX are copied into BX (c) the contents of CH are copied into BL (d) the contents of EBP are copied into ESP (e) the contents of RCX are copied into RAX
3. AX, BX, CX, DX, SP, BP, SI, DI, CS, DS, ES, SS, FS, and GS
5. RAX, RBX, RCX, RDX, RSP, RBP, RSI, RDI and R8—R15
7. The register sizes must be equal, 16-bit cannot be fit into 8-bits
9. (a) MOV EDX,EBX (b) MOV CL,BL (c) MOV BX,SI (d) MOV AX,DS (e) MOV AH,AL (f) MOV R10,R8
11. #
13. .CODE
15. Opcode
17. It ends the program by exiting to the operating system
19. The .STARTUP directive loads the DS register
21. Indirect addressing
23. Memory to memory transfers are not allowed with the MOV instruction
25. INC WORD PTR [EDI]
27. DEC QWORD PTR [RAX]
29. (a) 21110H (b) 10100H (c) 21000H
31. (a) 12100H (b) 12350H (c) 12220H
33. (a) 11750H (b) 11950H (c) 11700H
35. (a) 15700H (b) 05100H (c) 07100H
39. 5, the first byte is the opcode, followed by a two byte segment address, followed by a two byte offset address
41. ±32K
43. A far jump always a jump to any location in the memory map
45. (a) short (b) near (c) short (d) far
47. JMP NEAR
49. PUSH [DI] places the 16-bit contents of the location addressed by DS and DI onto the stack.
51. Places the 32-bit contents of he register array onto the stack
53. no

Chapter Four

1. Opcode
3. The MOD field specifies the type of access for the R/M field and the size of the displacement.
5. If operated in the 16-bit mode, a register-size and/or address-size prefix is used to specify a 32-bit register.
7. (a) SS (b) DS (c) DS (d) SS (e) DS
9. MOV BX,[BP+4C00H]
11. 67 66 8B 30
13. The contents of CS will change causing an unpredictable jump
15. 32