CPE 186 Computer Hardware Design

66MHz Implementation

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66MHz Uses 3.3V Signaling Environnent

- 66MHz components only operate correctly in a 3.3V signaling environment. The 5V environment is not supported. This means that 66MHz add-in cards are keyed to install only in 3.3V connectors and cannot be installed in 5V card connectors .

How Components Indicate 66MHz Support

- The 66MHz PCI component or add-in card indicates its support in two fashions: programmatically and electrically.

66MHz-Capable Bit

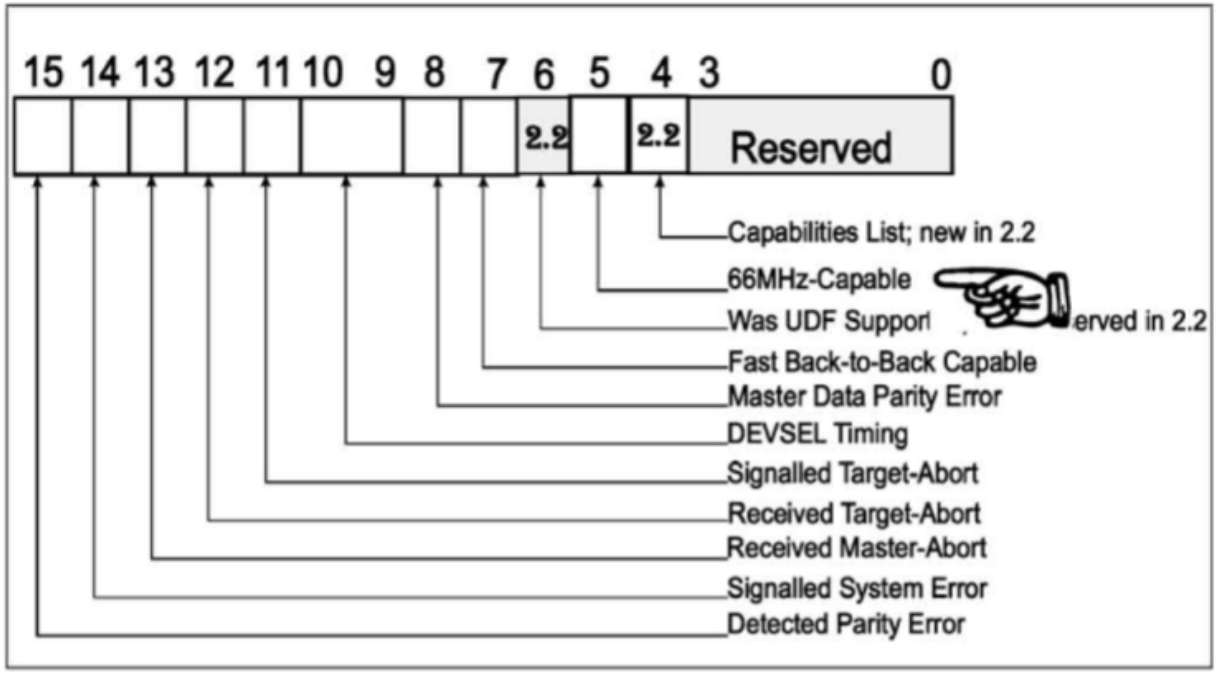
- The 66MHz-Capable bit has been added to the Status register

Bridge's 66MHz-Capable Bit	Device's 66MHz-Capable Bit	Description
0	0	Bus is a 33MHz bus, so all devices operate at 33MHz.
0	1	66MHz-capable device located on 33MHz bus. Bus and all devices operate at 33MHz. If the device is an add-in device and requires the throughput available on a 66MHz bus, the configuration software may prompt the user to install the card in an add-in connector on a different bus.
1	0	33MHz device located on 66MHz-capable bus. Bus and all devices operate at 33MHz. The configuration software should prompt the user to install the card in an add-in connector on a different bus.
1	1	66MHz-capable device located on 66MHz-capable bus. If status check of all other devices on the bus indicates that all of the devices are 66MHz-capable, the bus and all devices operate at 66MHz.

M66EN

- A 66MHz PCI bus includes a newly-defined signal, M66EN. This signal must be bussed to the M66EN pin on an 66MHz-capable devices embedded on the system board and to a redefined pin (referred to as M66EN) on any 3.3V connectors that reside on the bus.

Configuration Status Register



Does Clock Have to be 64MHz?

- As defined in revision 1.0 and 2.0 of the specification, the PCI bus does not have to be Implemented at its top rated speed of 33MHz. Lower speeds are acceptable.
- The same is true of the 66MHz PCI bus description found in revision 2.x of the specification.
- All 66MHz-rated components are required to support operation from 0 through 66.66MHz. The system designer may choose to implement a 50MHz PCI bus, a 60MHz PCI bus, etc.

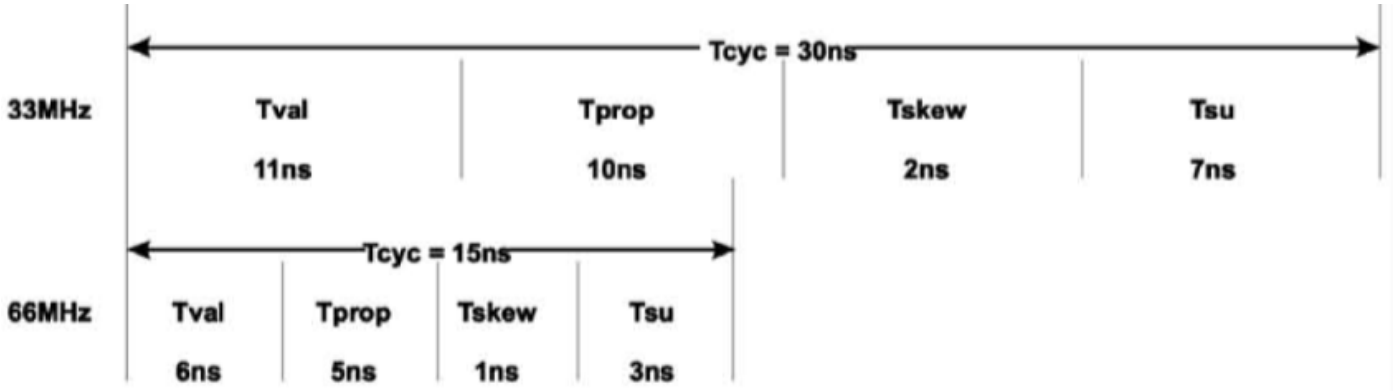
How 66MHz Components Determine Bus Speed

- When a 66MHz-capable device senses M66EN deasserted (at reset time). this automatically disables the device's ability to perform operations at speeds above 33MHz. If M66EN is sensed asserted, this indicates that no 33MHz devices are installed on the bus and the clock circuit is supplying a high-speed PCI clock.

Maximum Achievable Throughput

- The theoretical maximum achievable throughput on a 66MHz PCI bus would be:
- 4 bytes per data phase * 66 million data phases per second = 264MB/second for a 32-bit bus master bursting with a 32-bit target.
- 8 bytes per data phase * 66 million data phases per second = 528MB/second for a 64-bit bus master bursting with a 64-bit target.

33 versus 66MHz Timing



Latency Rule

- Common sense says that devices siding on the 66MHz PCI bus should all be fast access devices.
- The PCI 2.1 specification requires that on a read transaction, the time from assertion of FRAME# to the completion of the first data phase not exceed 16 PCI docks.