CPE 186 Computer Hardware Design

Configuration Address Space

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Introduction

When the machine is first powered on, the configuration software must scan the various buses in the system (PCI and others) to determine what devices exist and what configuration requirements they have. This process is commonly referred to as:

- scanning the bus walking the bus
- walking the bus
- probing the bus
- the discovery process
- bus enumeration

In order to facilitate this process, each PCI function must implement a base set of configuration registers defined by the PCI specification.

PCI Device vs. PCI Function

- A PCI device that contains only one function is referred to as a single-function device. A PCI device that contains more than one function is referred to as a multi-function device

Three Address Spaces: I/O, Memory and Configuration

- PCI bus masters (including the host/PCI bridge) use PCI IO and memory transactions to access PCI IO and memory locations, respectively.
- In addition, a third access type, the configuration access, is used to access a device's configuration registers.
- A function's configuration registers must be initialized at startup time to configure the function to respond to memory and/or IO address ranges assigned to it by the configuration software.

PCI Memory Space & PCI IO Space

- The PCI memory space is either 4GB or 2^64 locations in size (if 64-bit addressing is utilized).
- PCI IO space is 4GB in size (although Intel x86 processors cannot generate I0 addresses above the first 64KB of IO space).

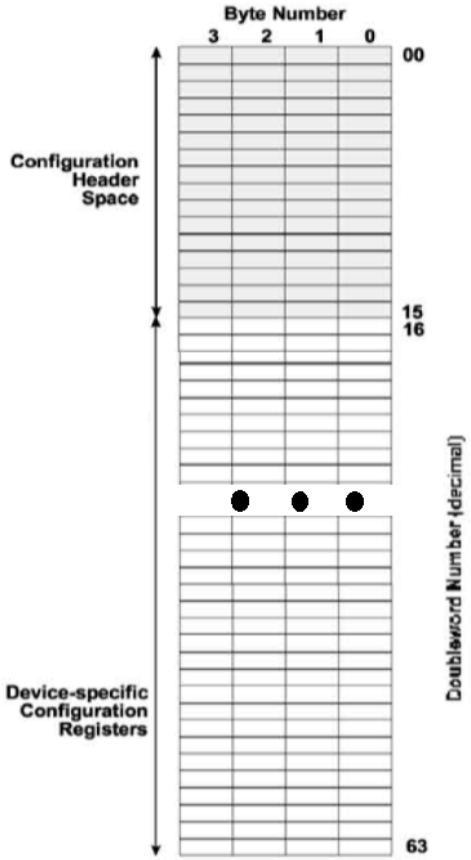
PCI Configuration Space

- PCI configuration space is divided into a separate, dedicated configuration address space for each function contained within a PCI device (i.e.. in a chip or on a card).
- Host Bridge Needn't Implement Configuration Space

PCI Configuration Space

- The first 16 dwords of a function's configurations pace is referred to as the function's configuration Header space. The format and usage of this area are defined by the specification. Three Header formats are currently defied:
- Header Type Zero for all devices other than PCI-to-PCI bridges. Header Type One for PCI-to-PCI bridges.
- Header Type Two for CardBus bridges (defined in the CardBus spec).

PCI Function's Basic Configuration Address Space Format



System with Single PCI Bus

- The interface between the host processor bus and the PCI bus is referred to as the host/PCI bridge.
- The bus directly on the other side of the bridge is always designated (for configuration purposes) as PCI Bus 0.
- If one or more of the functions on PCI Bus 0 are PCI-to-PC1 bridges, the two PCI buses connected to a PCI-to-PCI bridge are referred to as the bridge's primary (the PCI bus closer to the host processor) and secondary buses (the bus further away from the host processor).