120

CpE 151 and EEE 234 CMOS and VLSI Design

Quiz – 3

For CpE 151, 5 lowest grade questions will be dropped. For EEE234 2 questions will be dropped.

Name: _ _____

1. DC Analysis is used to evaluate which of the following information?
   a. Noise Analysis
   b. Band width
   c. Slew-Rate
   (d) Bias Conditions/Operating point

2. AC Analysis is used to evaluate which of the following information?
   (a.) Noise Analysis
   (b.) Band width
   (c.) Slew-Rate
   d. Bias Conditions/Operating point

3. Transient Analysis is used to evaluate which of the following information?
   a. Noise Analysis
   b. Band width
   (c.) Slew-Rate
   d. Bias Conditions/Operating point

4. RC delay model approximates a transistor as a switch / resistor in series with a resistor / switch.

5. A unit nMOS transistor (M1) with L_{min} and W_{min} dimensions has a resistance of R and a Capacitance of C. What would be the resistance of an pMOS (M2) with twice the width of M1? 2R / R.

6. What would be the diffusion cap of a pMOS (M3) with k-times the width of M1? KC.

7. The Capacitance of a MOS transistor is directly (directly/inversely) proportional to its width.

8. The Capacitance of a MOS transistor is directly (directly/inversely) proportional to its length.

9. By increasing the W of a MOS transistor, its resistance is decreased (increased/decreased)?

10. In Elmore-delay estimation, the effect of the largest Resistance is felt closest to the source/load?
Load

11. The Figure – 1 shown below, represents a fanout-of-1 inverter. What is its total delay in terms of R and C defined in problem 5? 3RC + 3RC.

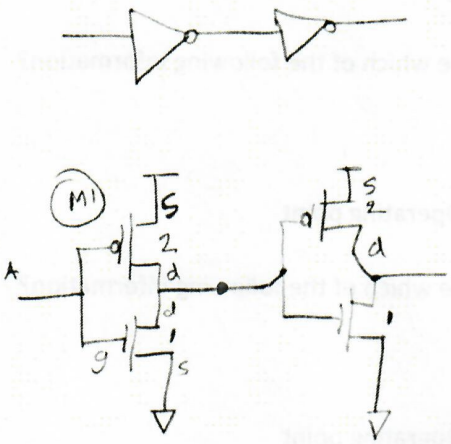

Figure – 1. Fanout – of – 1 inverter

12. In figure – 1: if the fanout of the first inverter is 4 instead of 1, what would be its delay? 15RC.

12RC + 3RC = 15RC

13. In figure – 1, what percentage of the delay is from self-loading (parasitic and internal capacitances) of a fanout – of – 1 inverter? 50 % (25% / 50% / 75% / 100%)

14. What is the relationship between tpd and tcd? tpd ≥ tcd.

15. In linear delay model, the relationship between d, g, h and p is given by d = gh + p, where:

d: delay (Normalized to units of delay of a parasitic free fanout-of-1 inverter)

f: effort component of the delay

p: parasitic component of the delay

g: logical effort

h: fanout (electrical effort)