CPE 186 Computer Hardware Design

Interrupts

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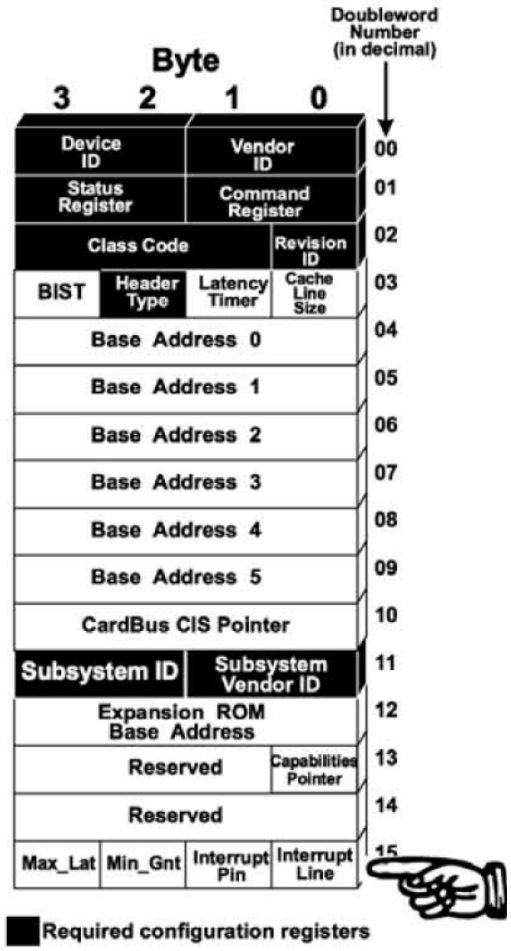
Interrupt Methods

- Method 1: delivers interrupt requests to the processor by asserting its INTR input pin.
- Method 2: delivers Interrupt message packets to the array of processors by APIC (Advanced Programmable Interrupt Controller)
- Method 3: delivers interrupt requests to the processor by performing memory write transactions - MESSAGE SIGNALED INERRUPTS (MSI)

Single-Function PCI Device

- A single-function PCI device must only use INTA# (never INTB#, INTC# or INTD#) to generate interrupt.
- The designer must hardwire this bonding information into the device's read-only interrupt pin configuration register (01h for lNTA# for a single-function PCI device) interrupt requests.
- The interrupt pin register resides in the second byte of configuration dword number 15d in the device's configuration header space.



Interrupt Signal Bonded To	Value Hardwired In Pin Register
Device doesn't generate interrupts.	00h
INTA# pin	01h
INTB# pin	02h
INTC# pin	03h
INTD# pin	04h

Multi-Function PCI Device

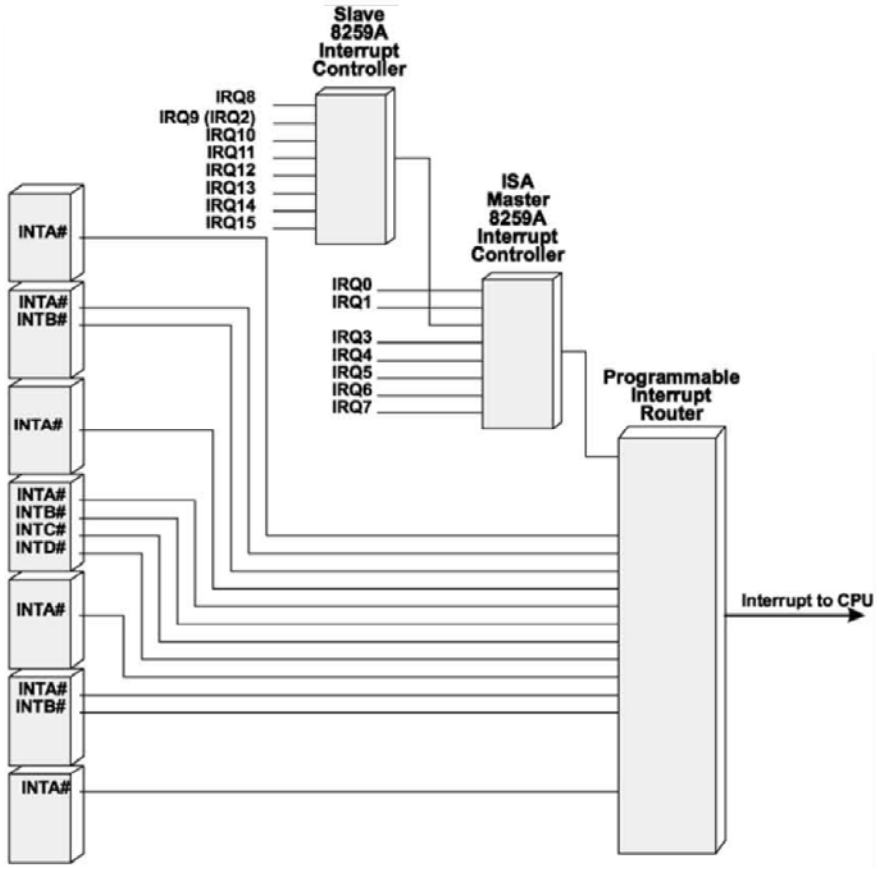
- May implement up to four interrupt pins on a multi-function device: INTA#, INTB#, INTC# and INTD#. Each function within the package is only permitted to use one of these interrupt pins to generate requests.
- Each function's Interrupt Pin register indicates which of the package's interrupt pins the device's internal interrupt request signal is bonded to.
- If a package implements one pin, it must be called INTA#. If it implements two pins, they must be called INTA# and INTB#, etc.

Multi-Function PCI Device

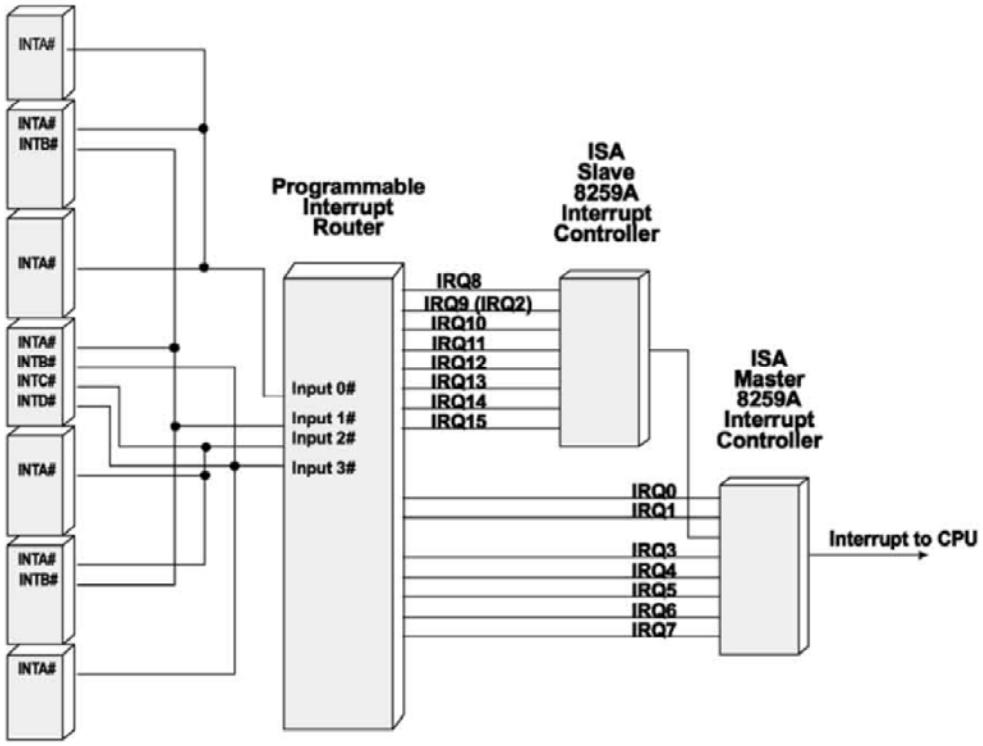
Groups of functions within the package may share the same pin. As some examples, a package embodying eight functions could bond their interrupt request signals in any of the following combinations:

- all eight bonded to the INTA# pin.
- four bonded to INTA# and four to INTB#.
- two bonded to INTA#, two to INTB#, two to INTC# and two to INTD#.
- seven to INTA# and one to INTB#, etc.

Preferred Interrupt Design



Recommended PCI Interrupt Line Routing (when muter only has four input pins)



Interrupt Line Register Values for x86 PC Platforms

System IRQ Line Interrupt Routed To	Value To Be Written In Line Register
IRQ0	0d
IRQ1	1d
IRQ2	2d
IRQ3	3d
IRQ4	4d
IRQ5	5d
IRQ6	6d
IRQ7	7d
IRQ8	8d
IRQ9	9d
IRQ10	10d
IRQ11	11d
IRQ12	12d
IRQ13	13d
IRQ14	14d
IRQ15	15d