



# SACRAMENTO STATE

CPE 151/EEE 234  
Digital IC Design

Project No. 1

Student Name:  
Email ID:  
Date of Submission:

## Table of Contents

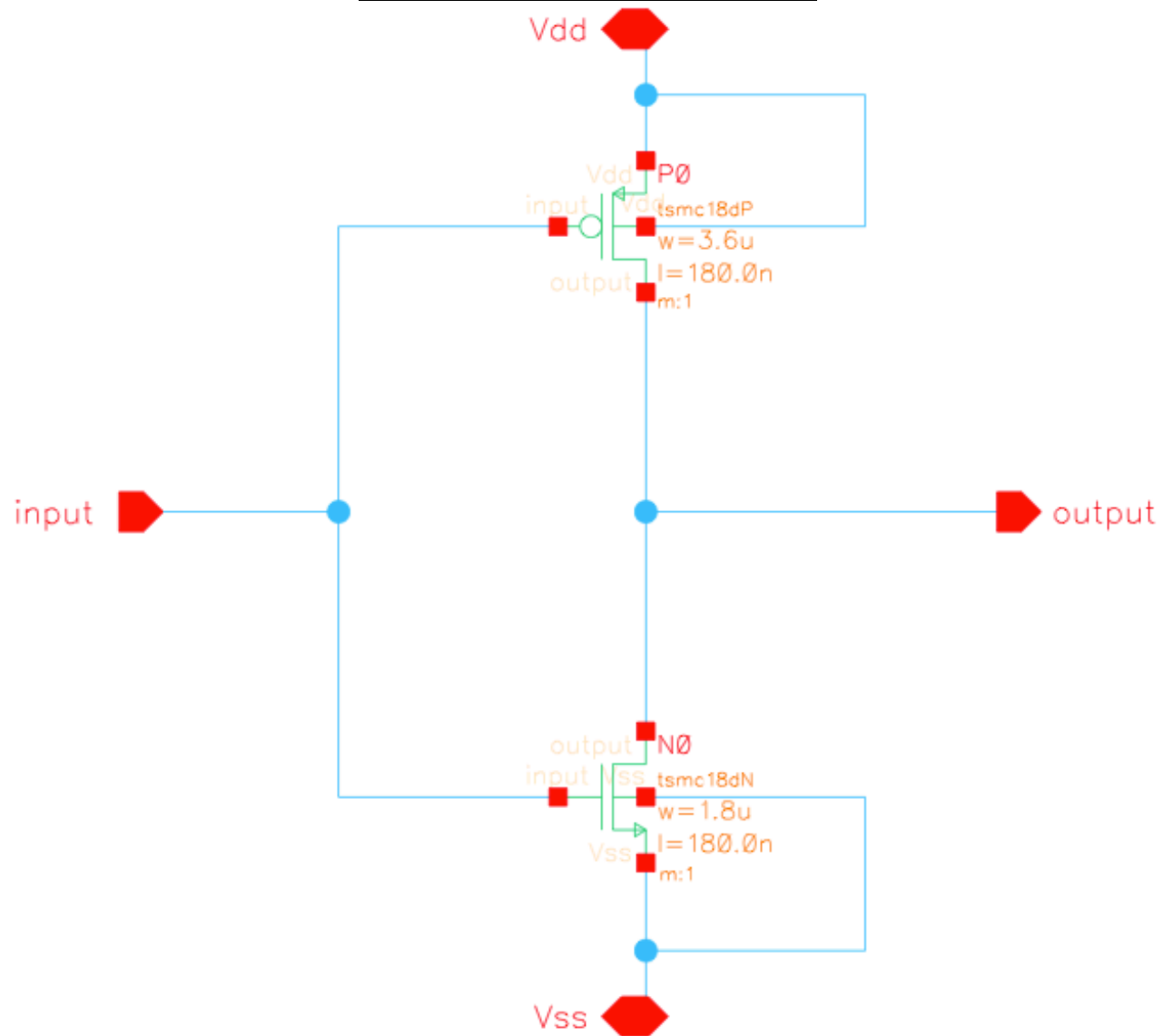
<b>Inverter .....</b>	<b>3</b>
<b>Inverter Schematic .....</b>	<b>4</b>
<b>Inverter Testbench .....</b>	<b>6</b>
<b>Inverter Testbench Waveform .....</b>	<b>7</b>
<b>Inverter Layout.....</b>	<b>8</b>
<b>Inverter DRC.....</b>	<b>9</b>
<b>Inverter Extract .....</b>	<b>10</b>
<b>Inverter LVS.....</b>	<b>11</b>
<b>Inverter Post Layout Simulation.....</b>	<b>13</b>
<b>3-Input NAND Gate .....</b>	<b>14</b>
<b>3-Input NAND Gate Schematic .....</b>	<b>15</b>
<b>3-Input NAND Gate Symbol.....</b>	<b>16</b>
<b>3-Input NAND Gate Testbench .....</b>	<b>17</b>
<b>3-Input NAND Gate Testbench Waveform .....</b>	<b>18</b>
<b>2-Input NOR Gate.....</b>	<b>19</b>
<b>2-Input NOR Gate Schematic.....</b>	<b>20</b>
<b>2-Input NOR Gate Symbol .....</b>	<b>21</b>
<b>2-Input NOR Gate Testbench.....</b>	<b>22</b>
<b>2-Input NOR Gate Testbench Waveform.....</b>	<b>23</b>
<b>Transmission Gate.....</b>	<b>24</b>
<b>Transmission Gate Schematic .....</b>	<b>25</b>
<b>Transmission Gate Symbol .....</b>	<b>26</b>
<b>Transmission Gate Testbench .....</b>	<b>27</b>
<b>Transmission Gate Testbench Waveform.....</b>	<b>28</b>
<b>2:1 MUX .....</b>	<b>29</b>
<b>2:1 MUX Schematic .....</b>	<b>30</b>
<b>2:1 MUX Symbol.....</b>	<b>31</b>
<b>2:1 MUX Testbench .....</b>	<b>32</b>
<b>2:1 MUX Testbench Waveform .....</b>	<b>33</b>
<b>Conclusion.....</b>	<b>34</b>

# Inverter

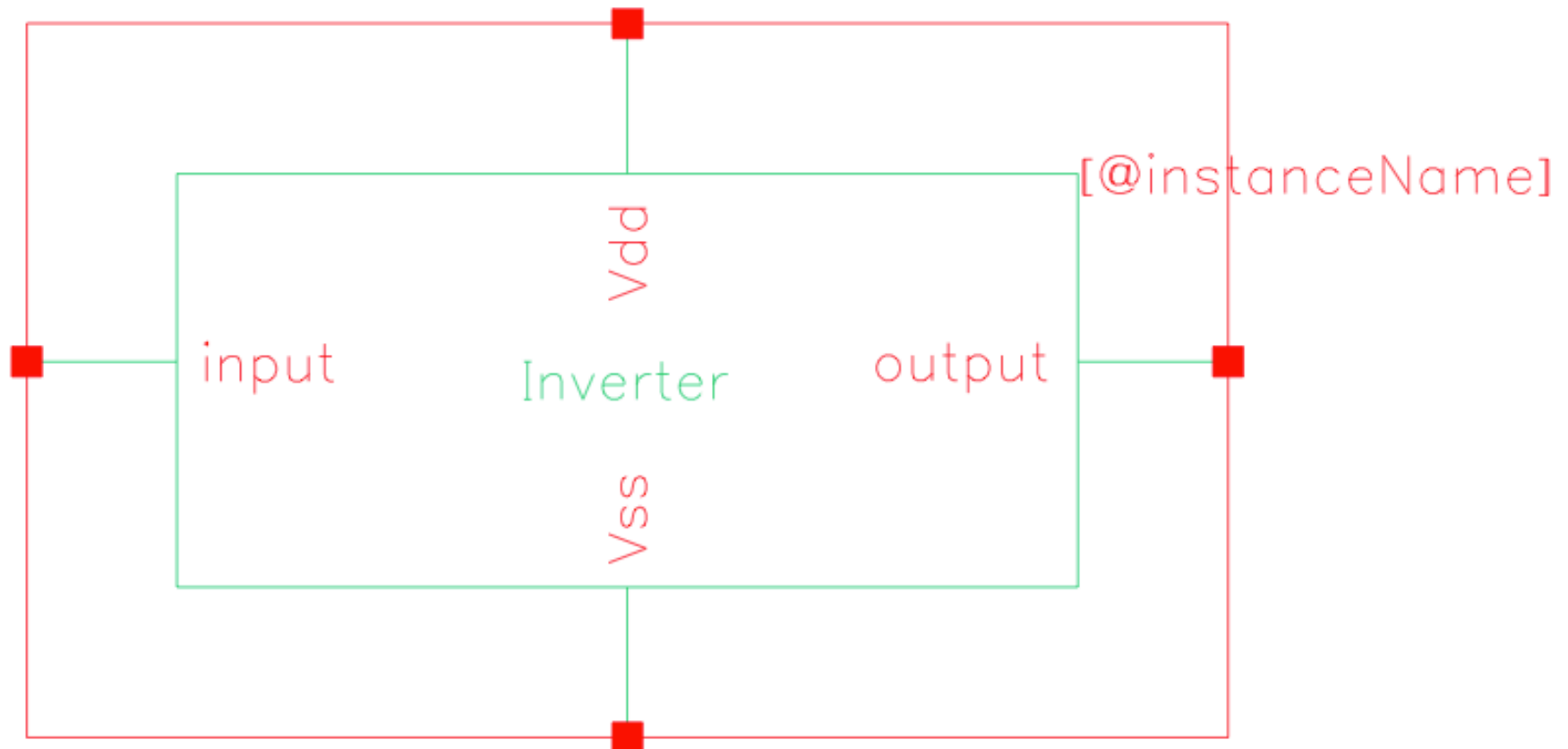
$$(W/L)_n = 1.8/0.18$$

$$(W/L)_p = 3.6/0.18$$

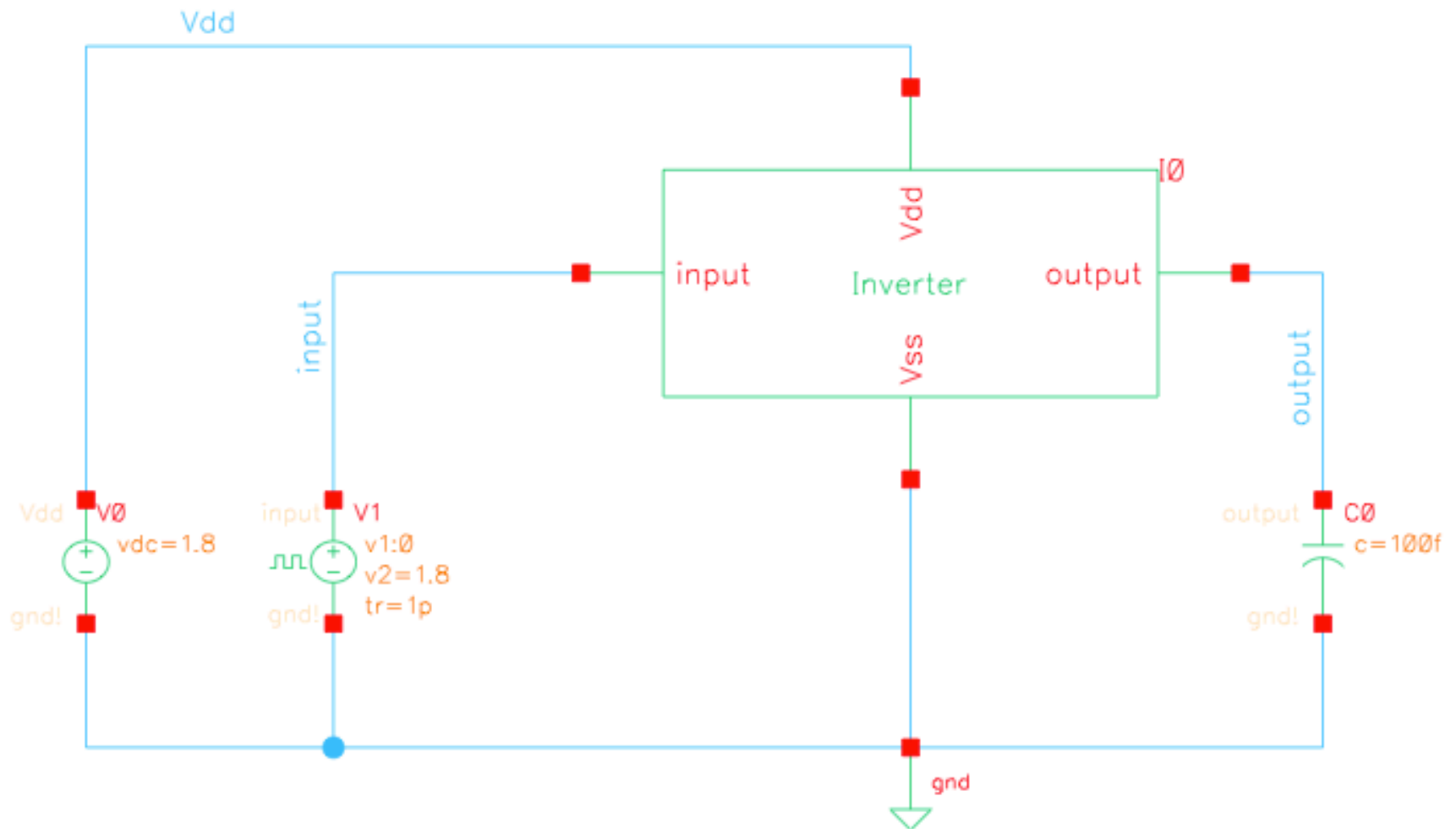
# Inverter Schematic



## Inverter Symbol



## Inverter Testbench



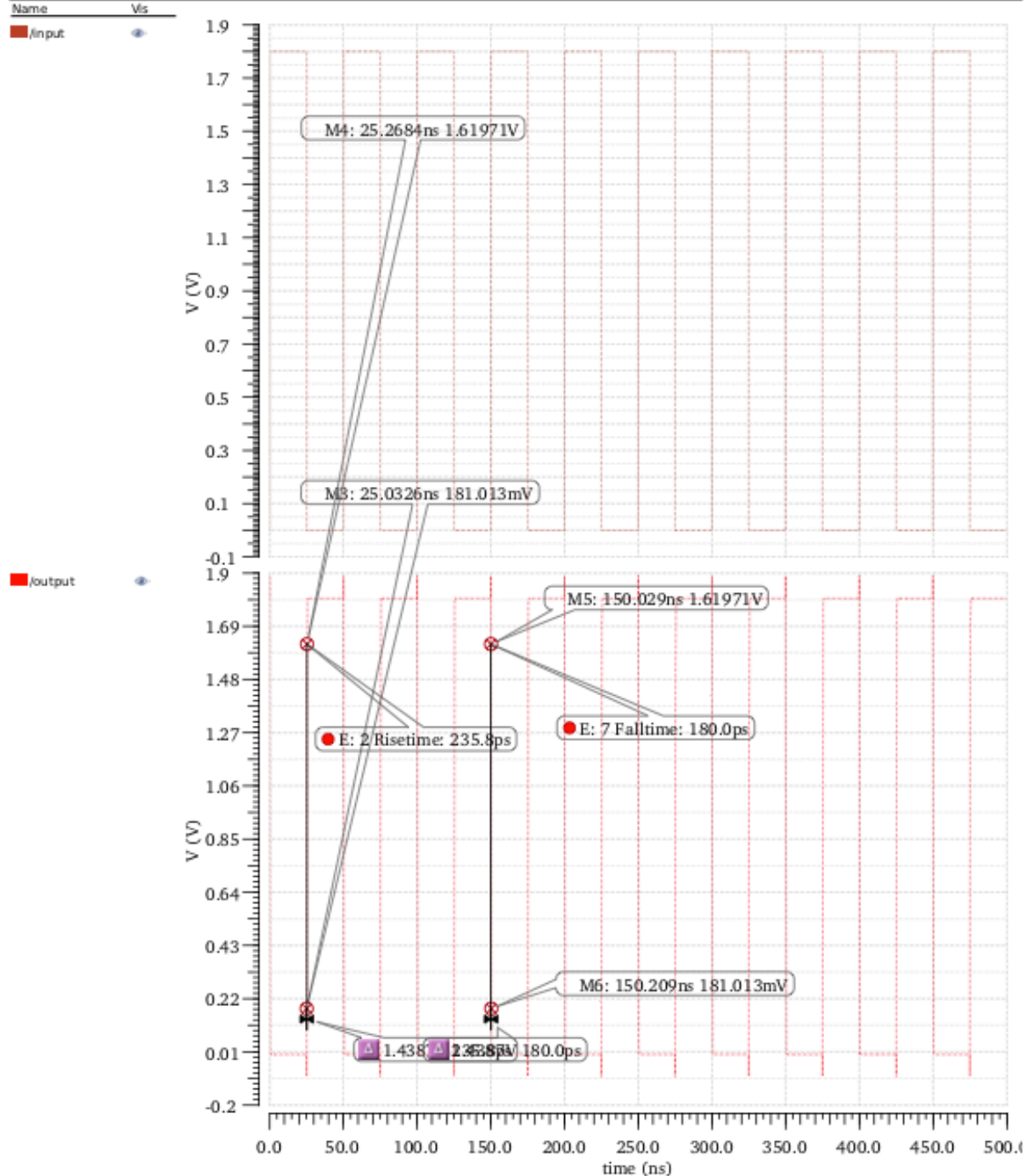
# Inverter Testbench Waveform

Project1:Inverter\_testbench:1 : Project1 Inverter\_testbench schematic

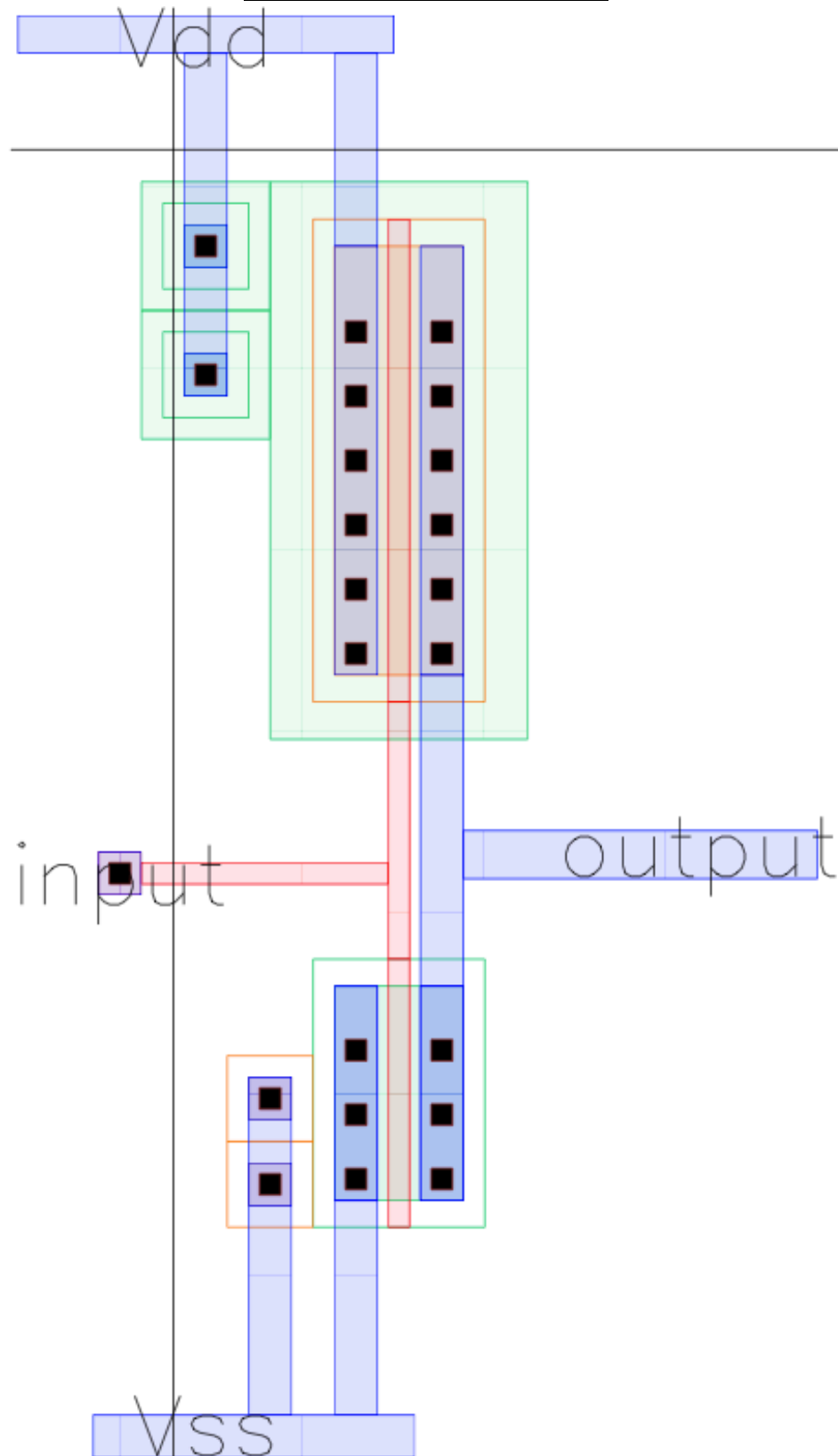
19:20:40 Wed Feb 28 2018

## Transient Response

Wed Feb 28 19:14:42 2018



## Inverter Layout



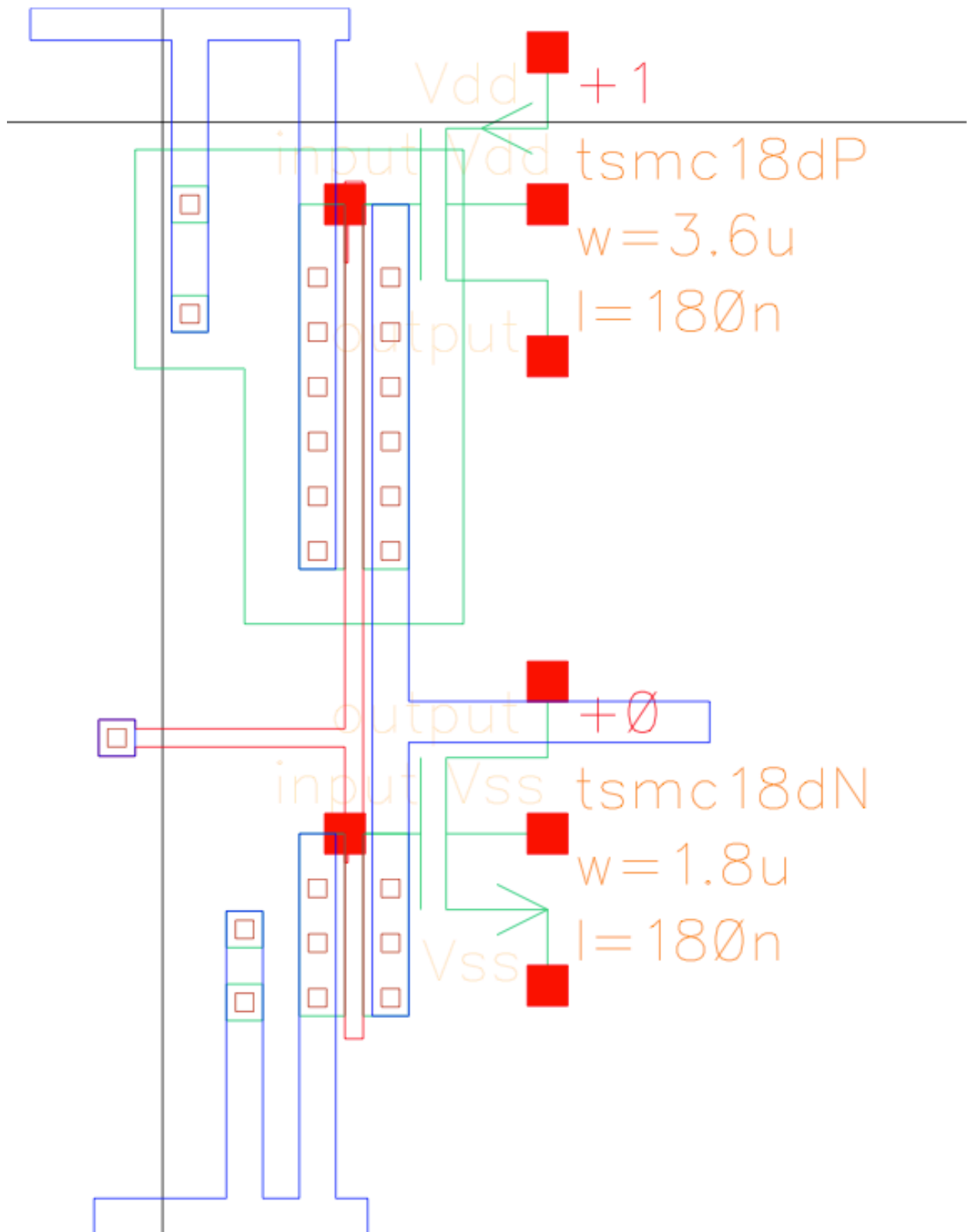


## Inverter DRC

```
Getting layout propt bag
DRC started at Thu Mar  1 22:07:09 2018

Validating hierarchy instantiation for:
library: Project1
cell:    Inverter_Layout
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Thu Mar  1 22:07:09 2018
  completed ....Thu Mar  1 22:07:09 2018
  CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
***** Summary of rule violations for cell "Inverter_Layout layout" *****
  Total errors found: 0
```

## Inverter Extract



# Inverter LVS

@(#)CDSD: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) \$

Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/  
64bit/LVS -dir /gaia/class/student/ /CPE151/LVS -l -s -t /gaia/  
class/student/PE151/LVS/layout /gaia/class/student/  
CPE151/LVS/schematic  
Like matching is enabled.  
Net swapping is enabled.  
Using terminal names as correspondence points.  
Compiling Diva LVS rules...

Net-list summary for /gaia/class/student/PE151/LVS/layout/  
netlist

count	
4	nets
0	terminals
1	pmos
1	nmos

Net-list summary for /gaia/class/student/PE151/LVS/  
schematic/netlist

count	
4	nets
4	terminals
1	pmos
1	nmos

Devices in the rules but not in the netlist:  
cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	2	2
total	2	2
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	4	4
total	4	4
	terminals	
un-matched	0	0

matched but		
different type	0	0
total	0	4

Probe files from /gaia/class/student [REDACTED] CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student [REDACTED] CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

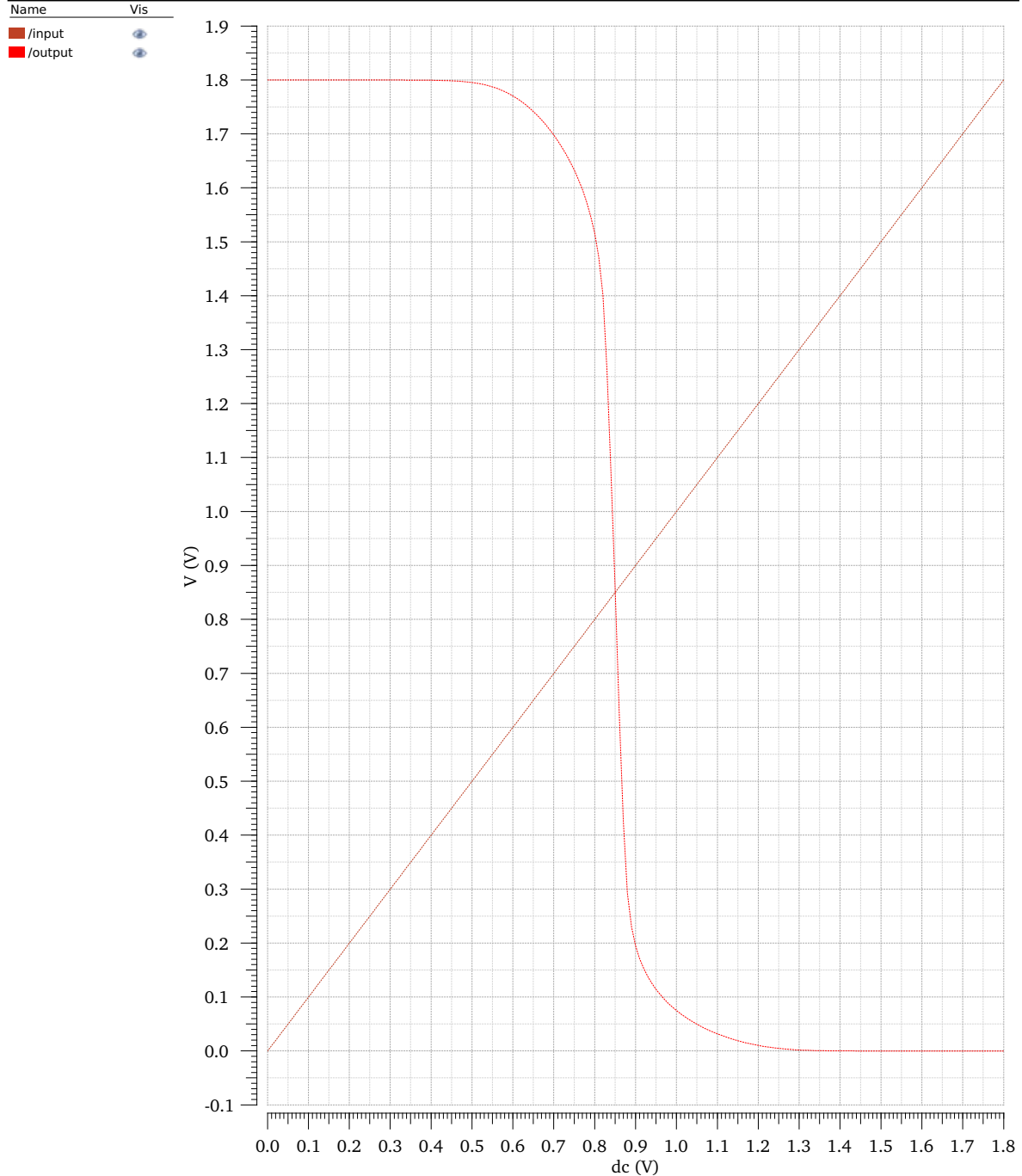
# Inverter Post Layout Simulation

Project1:Inverter\_testbench:1 : Project1 Inverter\_testbench schematic

22:09:15 Thu Mar 1 2018

## DC Response

Thu Mar 1 22:05:08 2018

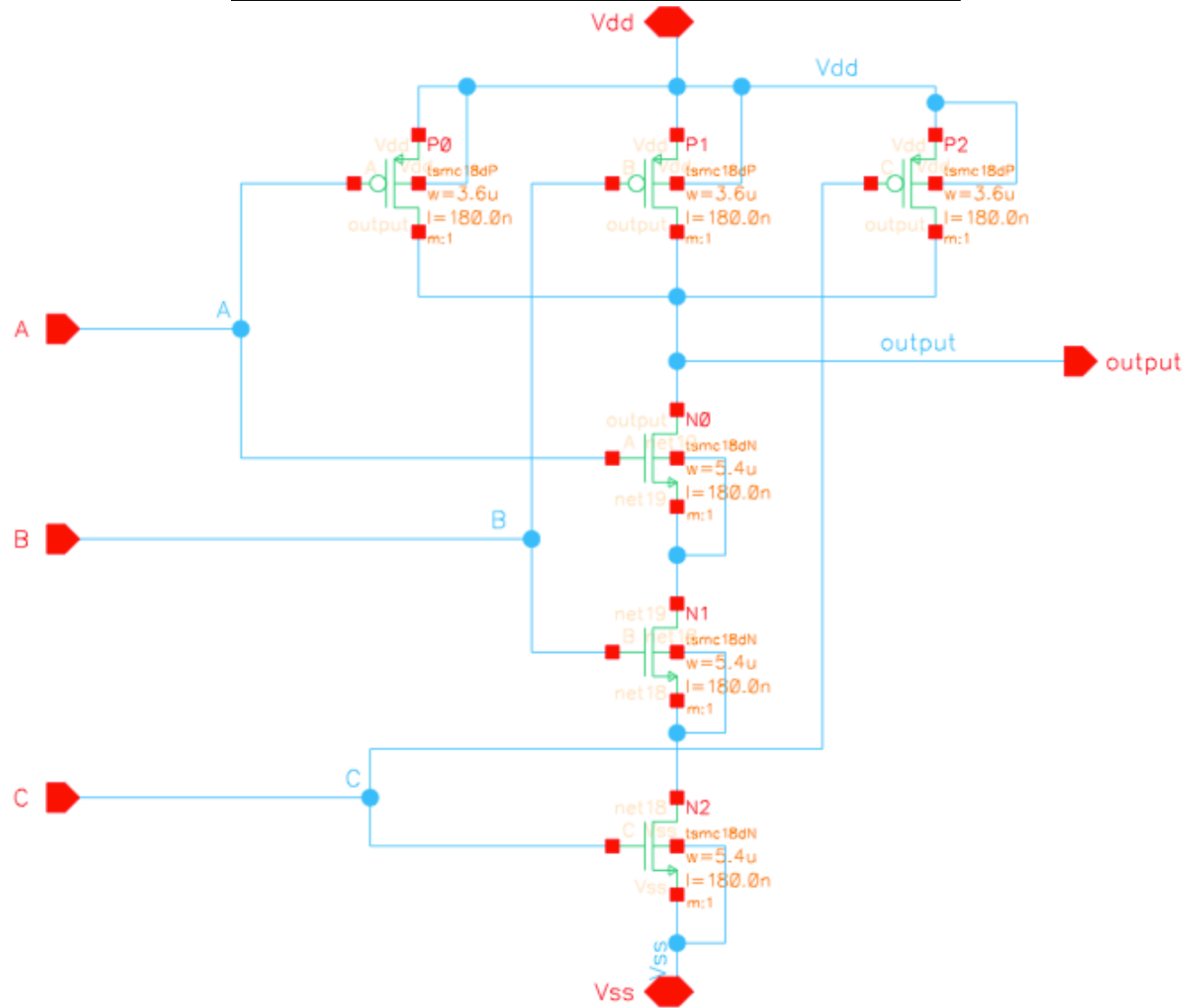


## 3-Input NAND Gate

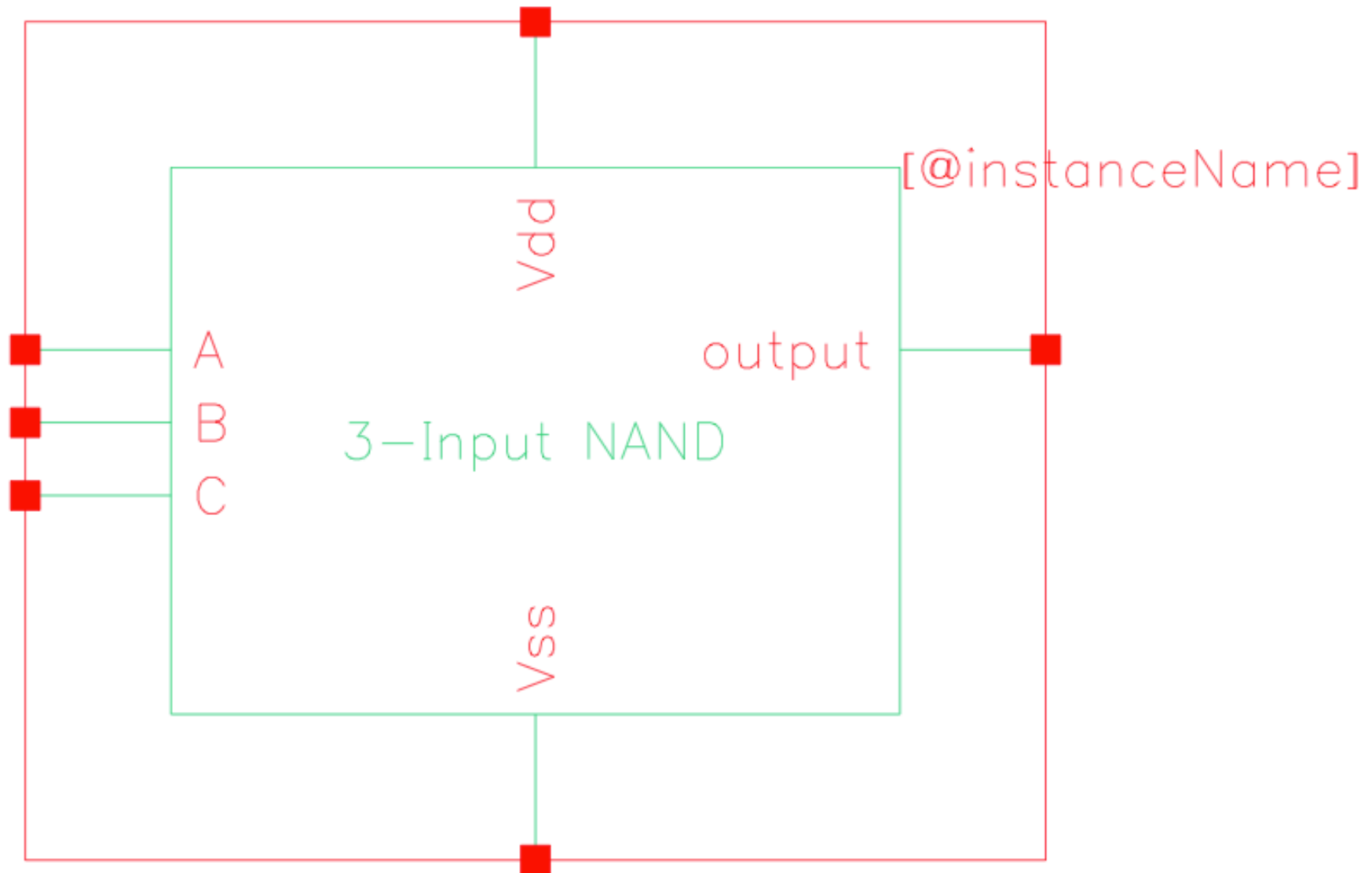
$$(W/L)_n = 5.4/0.18$$

$$(W/L)_p = 3.6/0.18$$

## 3-Input NAND Gate Schematic

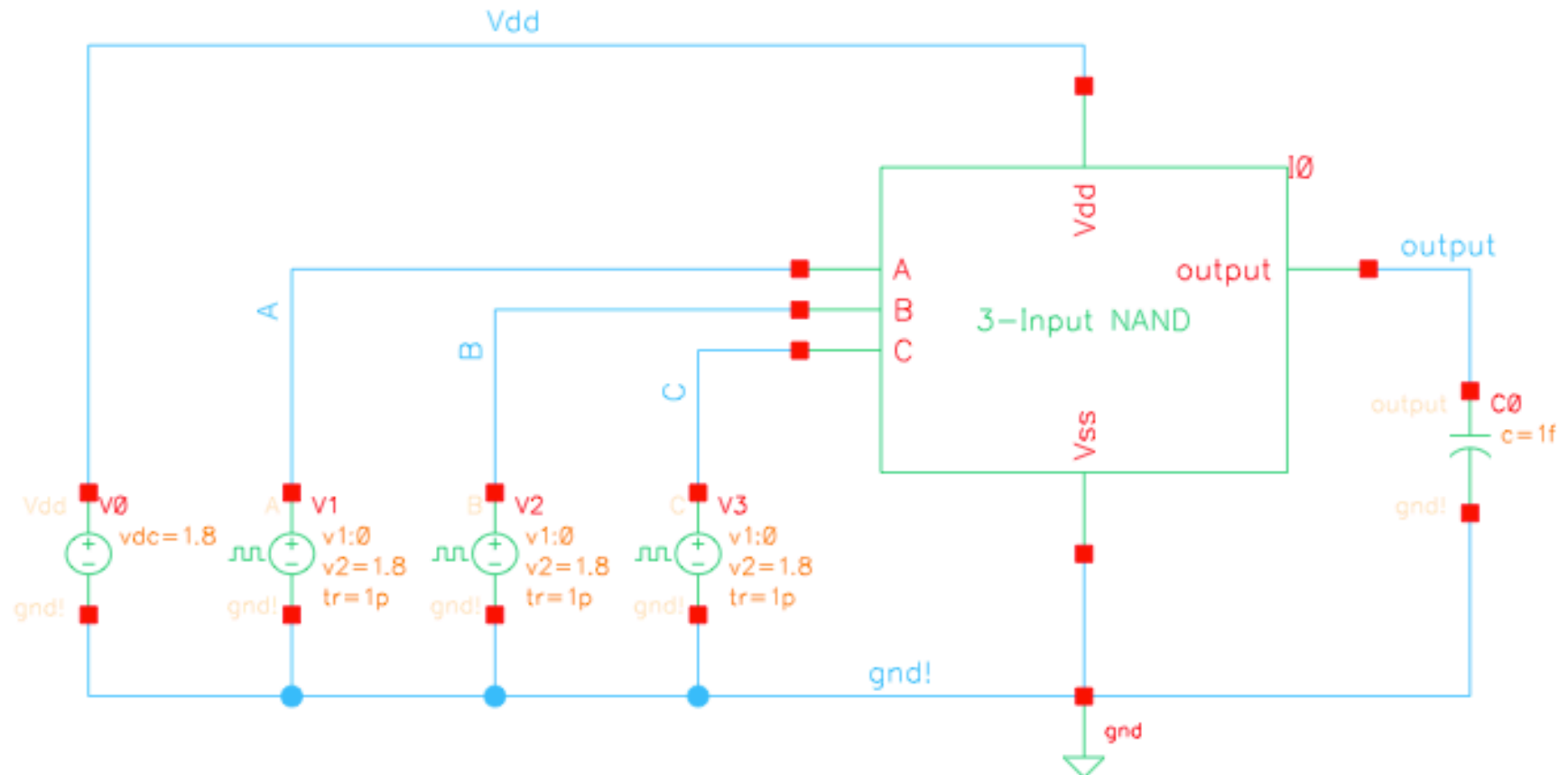


## 3-Input NAND Gate Symbol





## 3-Input NAND Gate Testbench



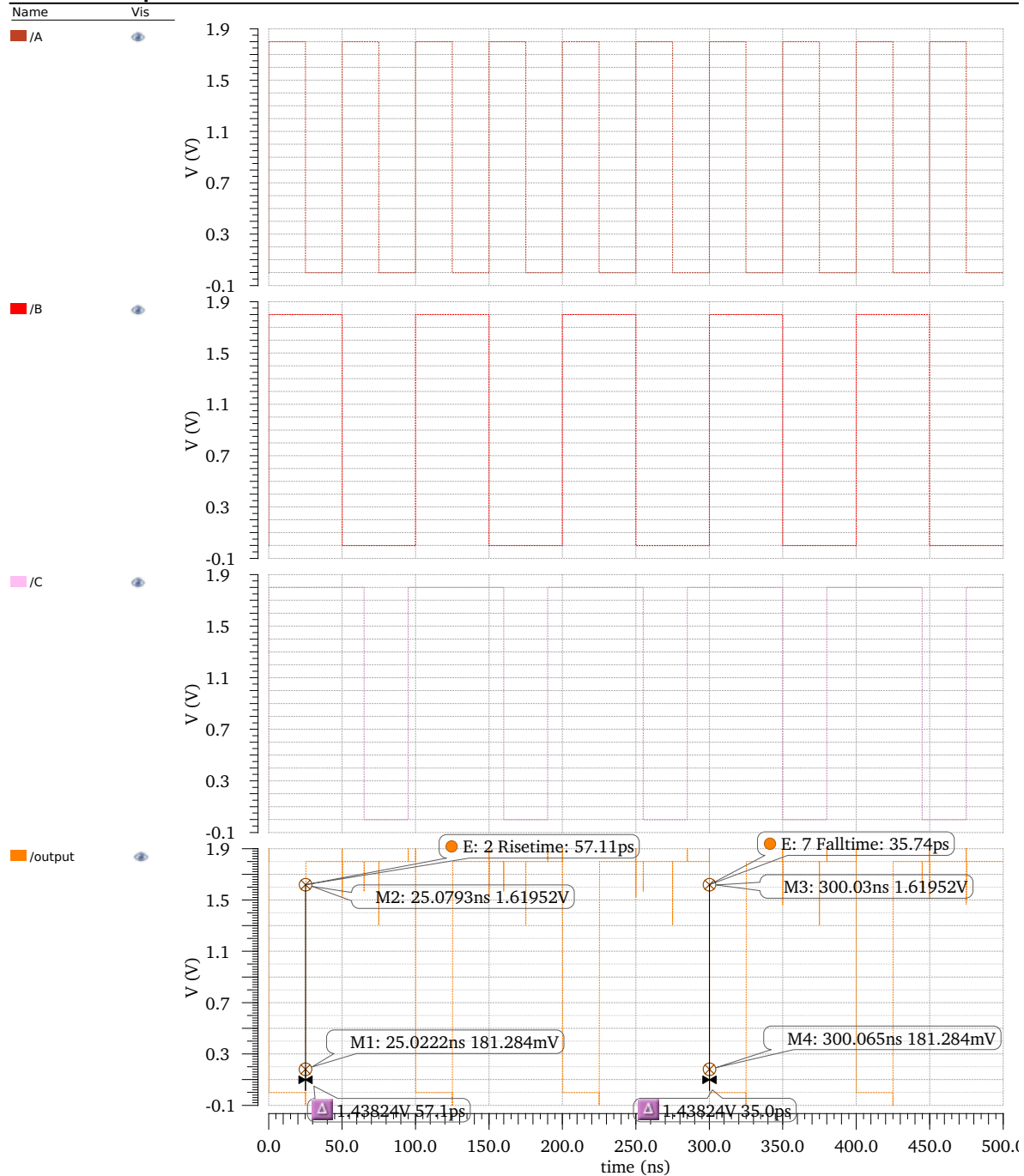
# 3-Input NAND Gate Testbench Waveform

NAND:NAND\_testbench:1 : NAND NAND\_testbench schematic

20:32:12 Thu Mar 1 2018

## Transient Response

Thu Mar 1 20:25:32 2018

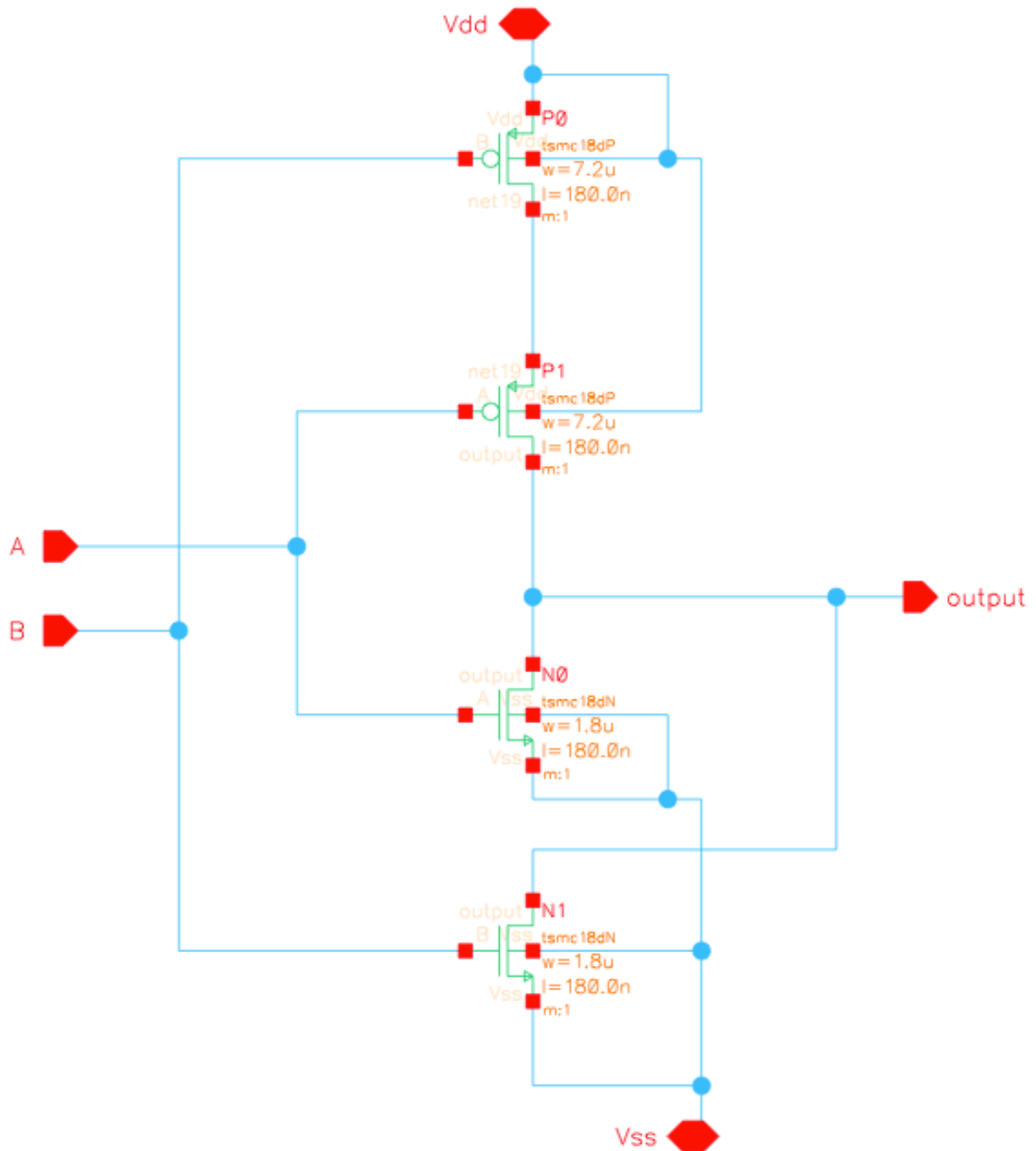


## 2-Input NOR Gate

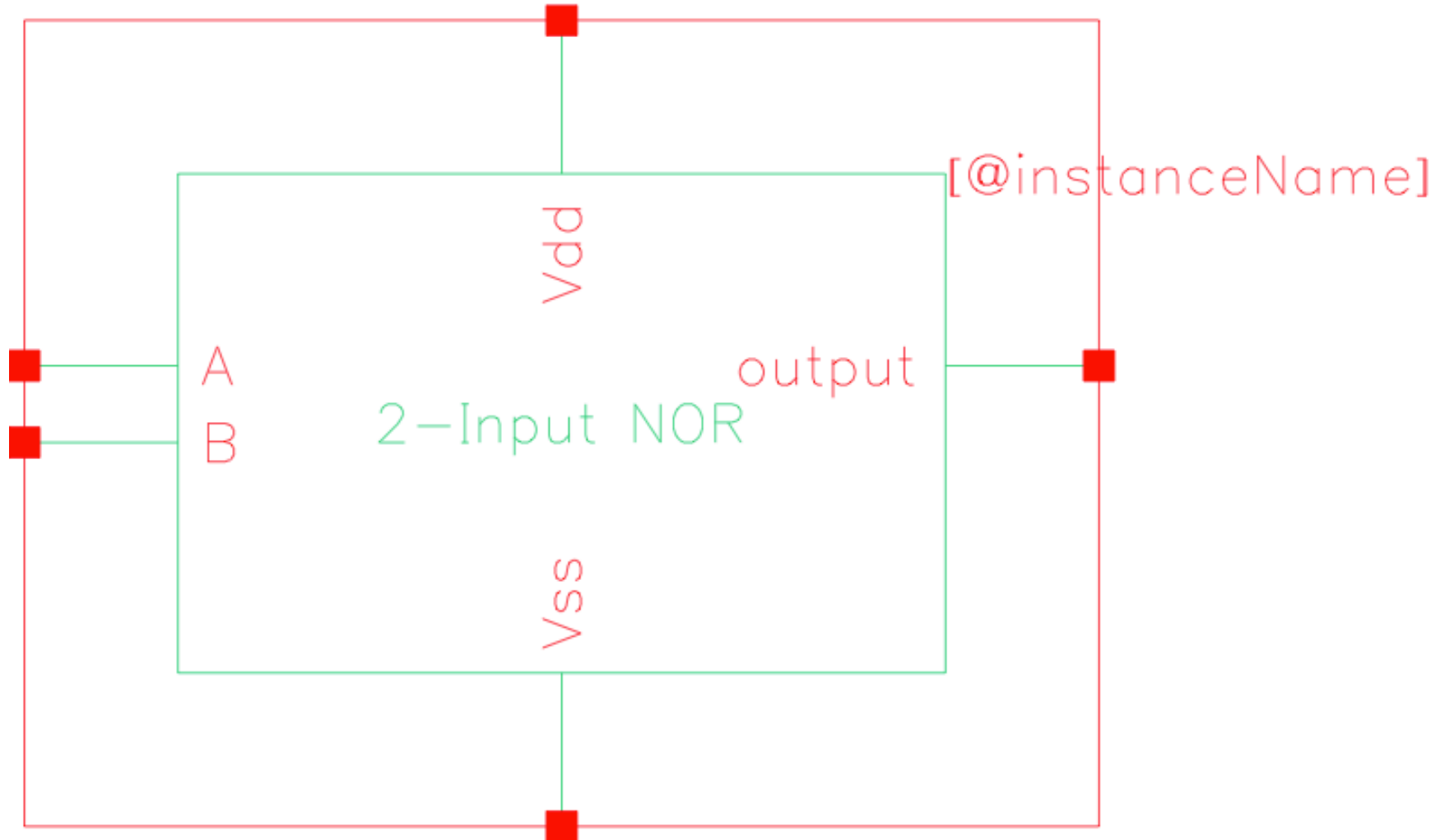
$$(W/L)_n = 1.8/0.18$$

$$(W/L)_p = 7.2/0.18$$

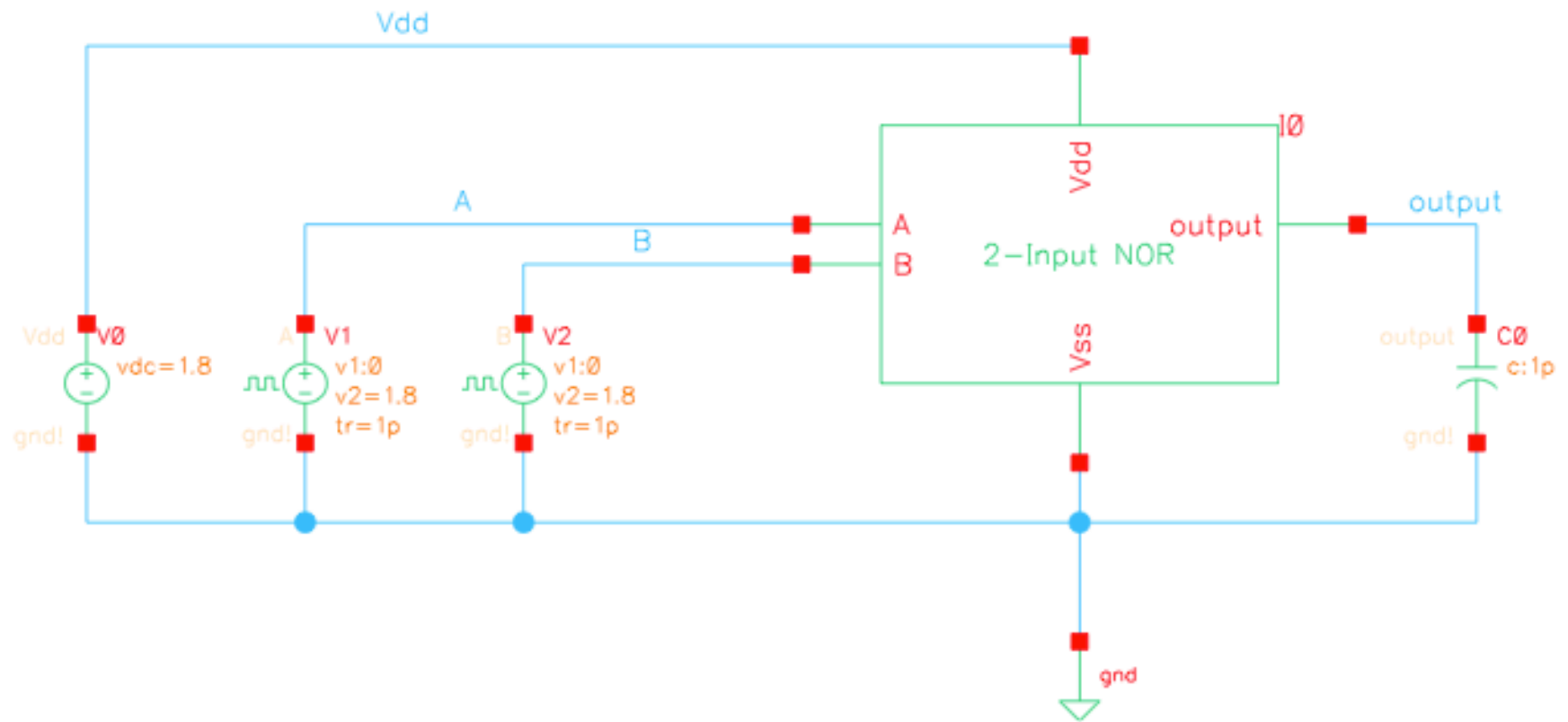
## 2-Input NOR Gate Schematic



## 2-Input NOR Gate Symbol



## 2-Input NOR Gate Testbench



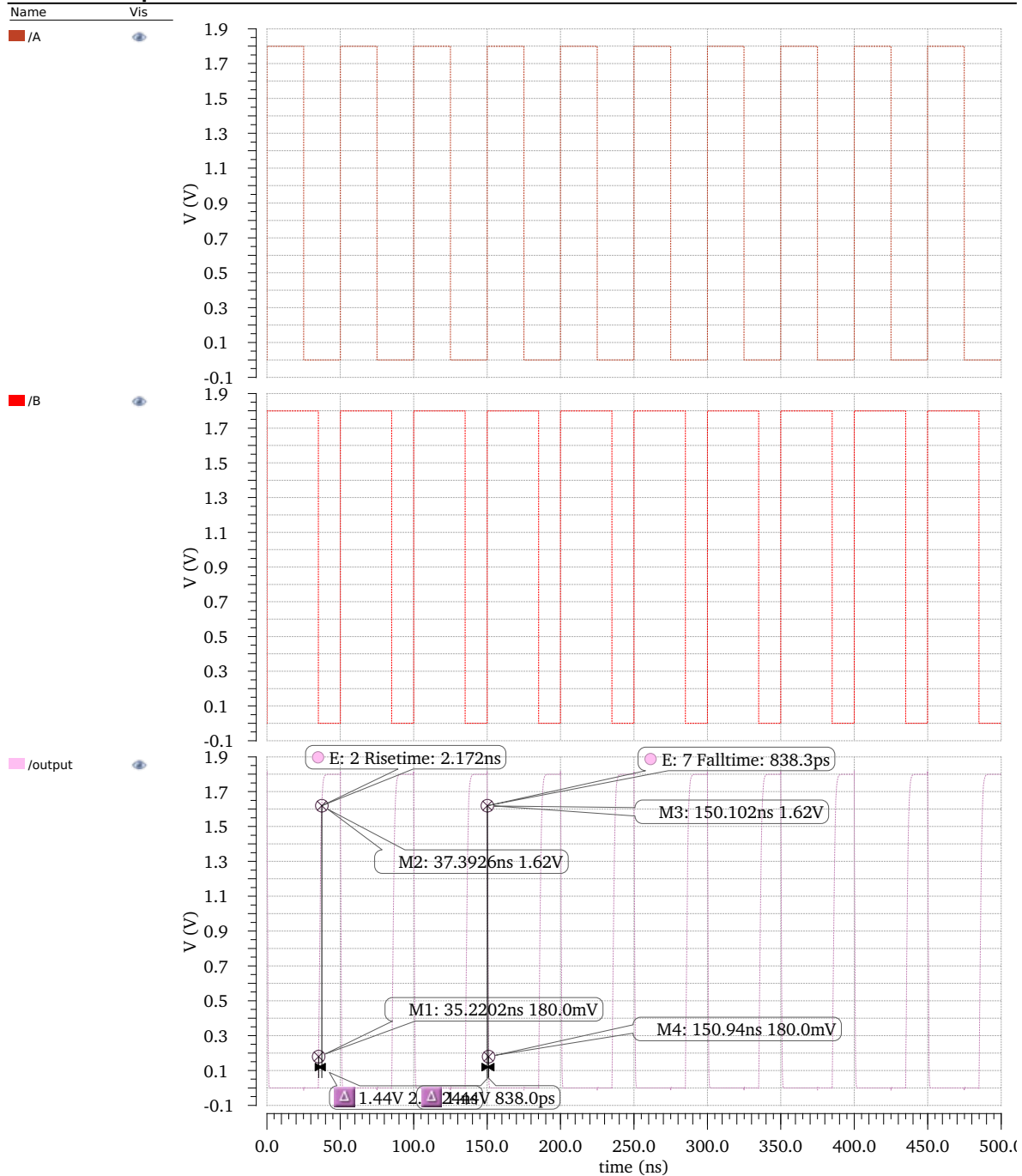
# 2-Input NOR Gate Testbench Waveform

NOR:NOR\_testbench:1 : NOR NOR\_testbench schematic

20:51:44 Thu Mar 1 2018

## Transient Response

Thu Mar 1 20:47:23 2018



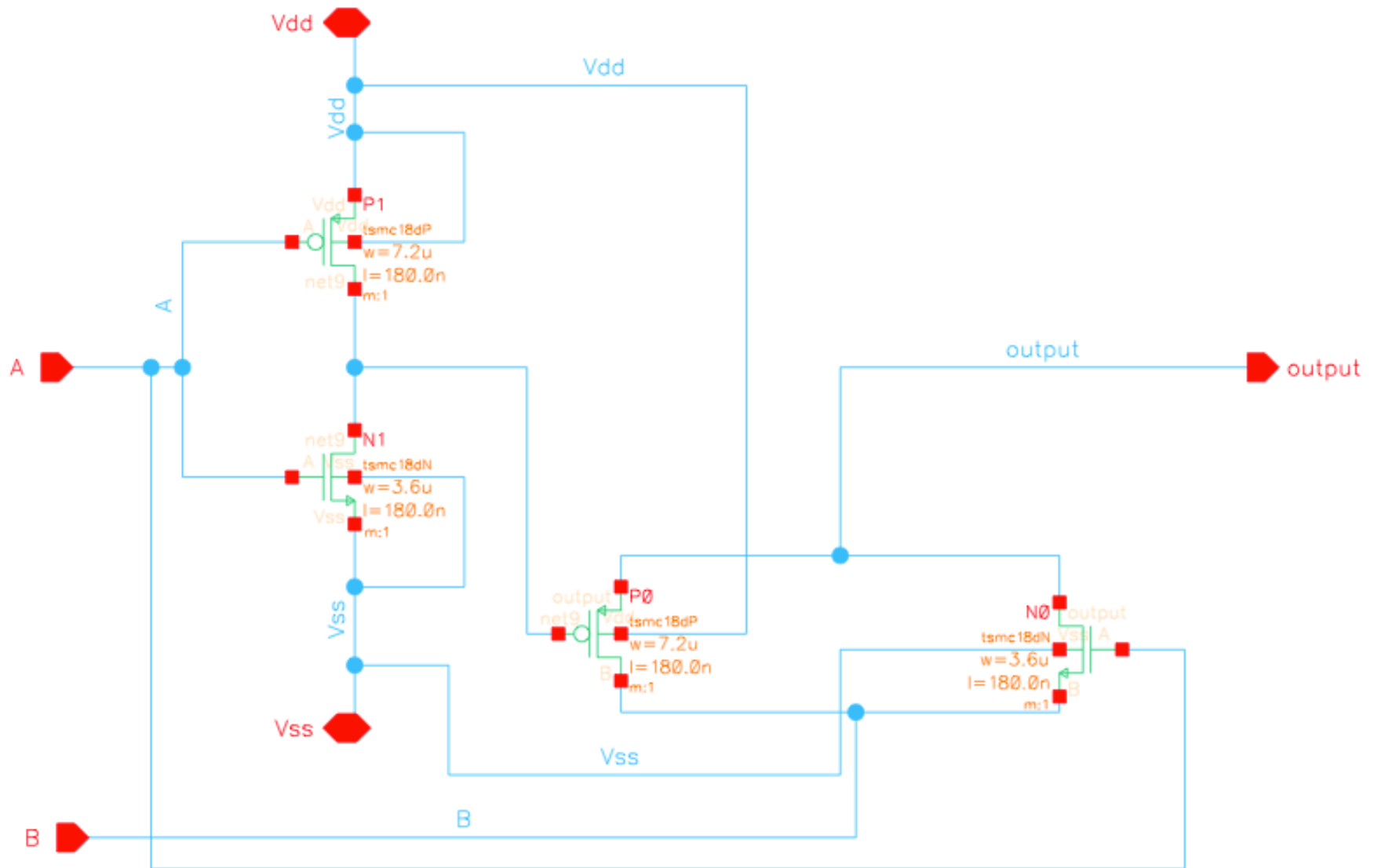
## Transmission Gate

$$(W/L)_n = 3.6/0.18$$

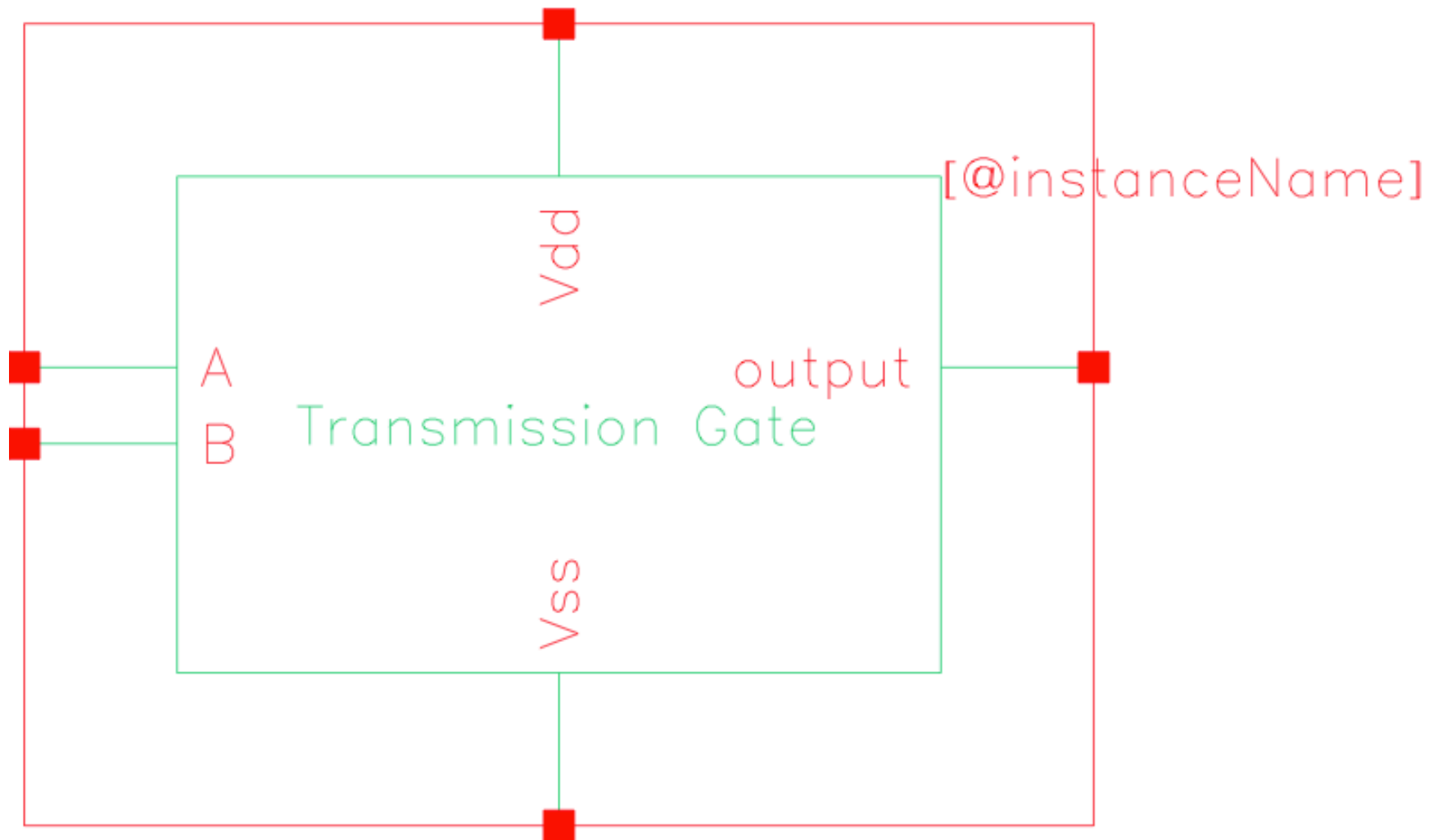
$$(W/L)_p = 7.2/0.18$$



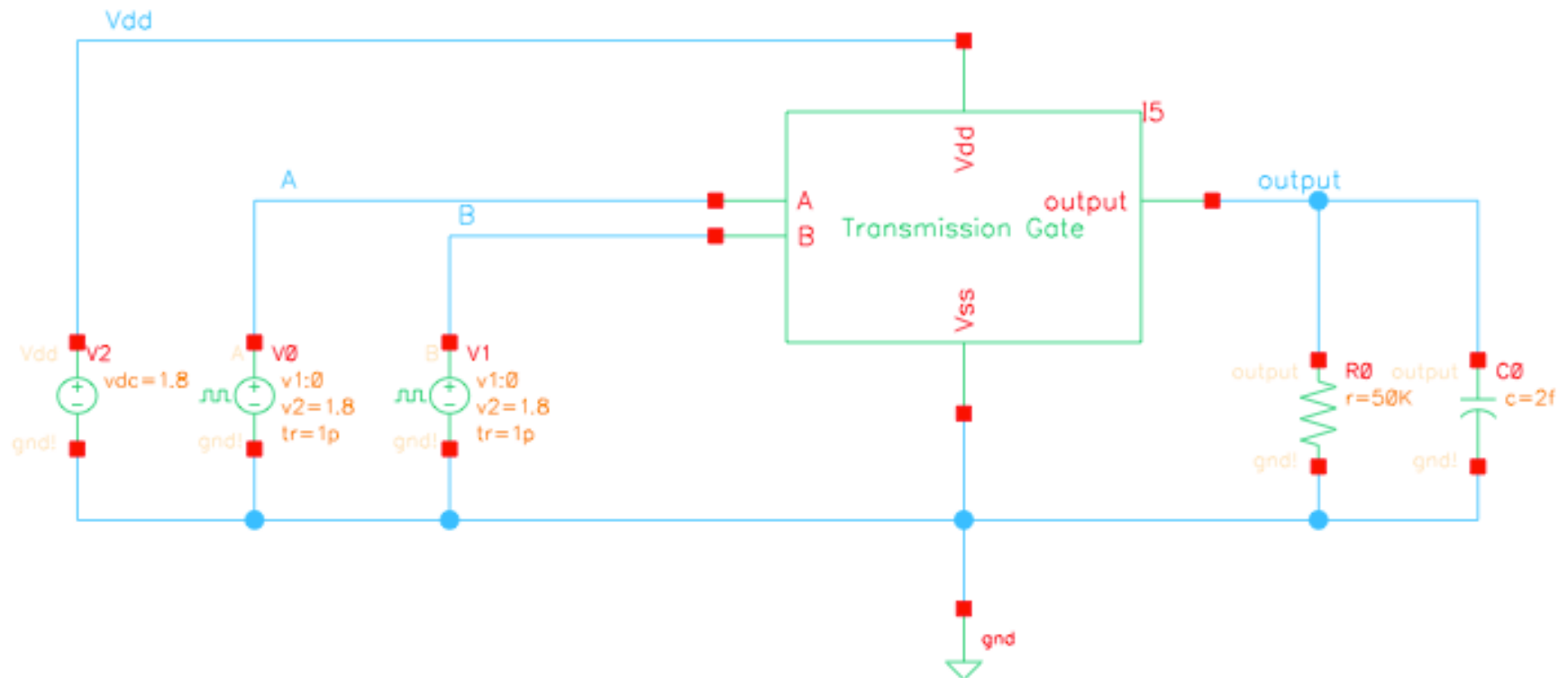
# Transmission Gate Schematic



## Transmission Gate Symbol



## Transmission Gate Testbench

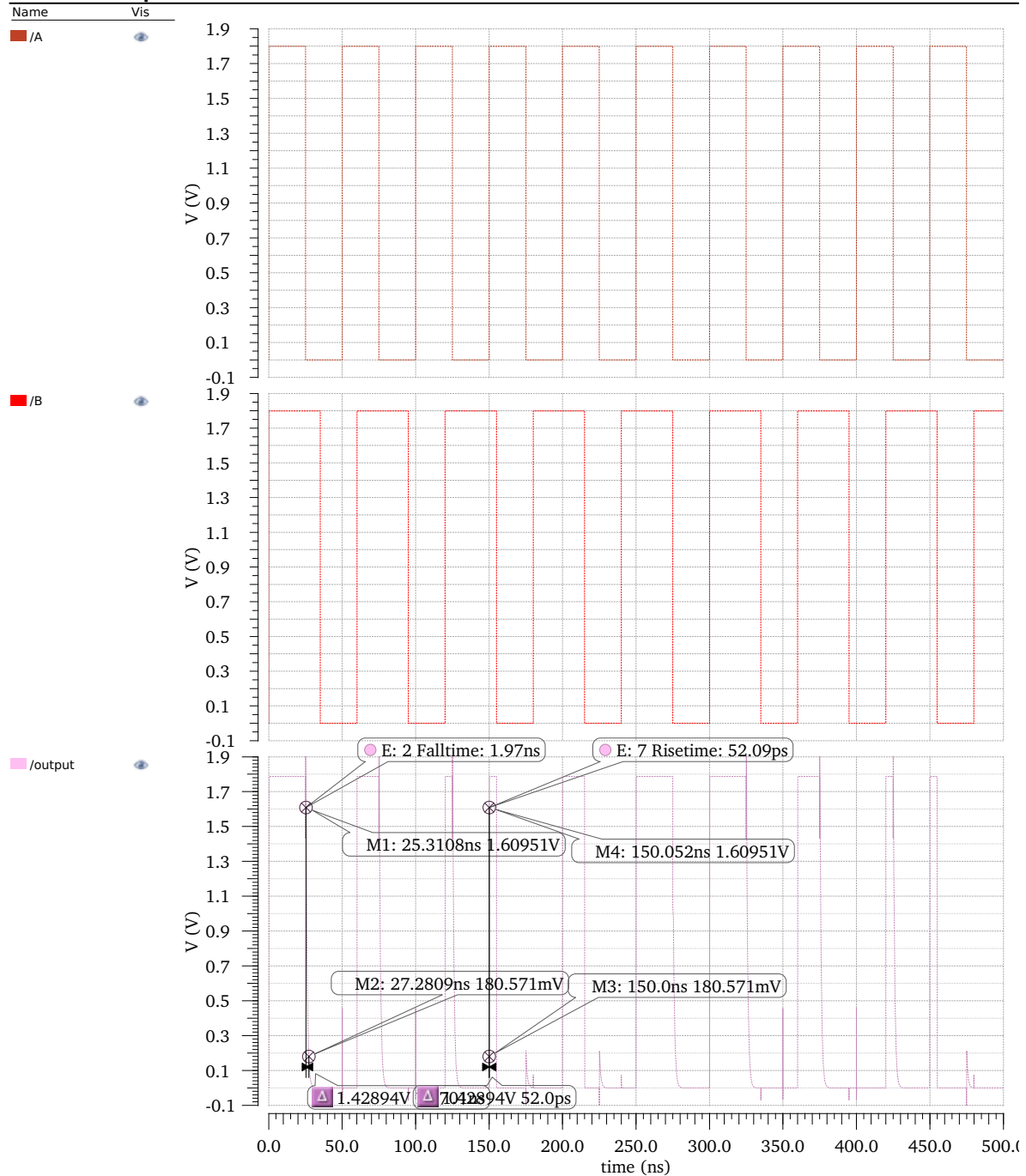


# Transmission Gate Testbench Waveform

Transmission\_Gate:Transmission\_Gate\_testbench:1 : Transmission\_Gate Transmission\_Gate\_testbench schematic 20:59:00 Thu Mar 1 2018

## Transient Response

Thu Mar 1 20:55:26 2018



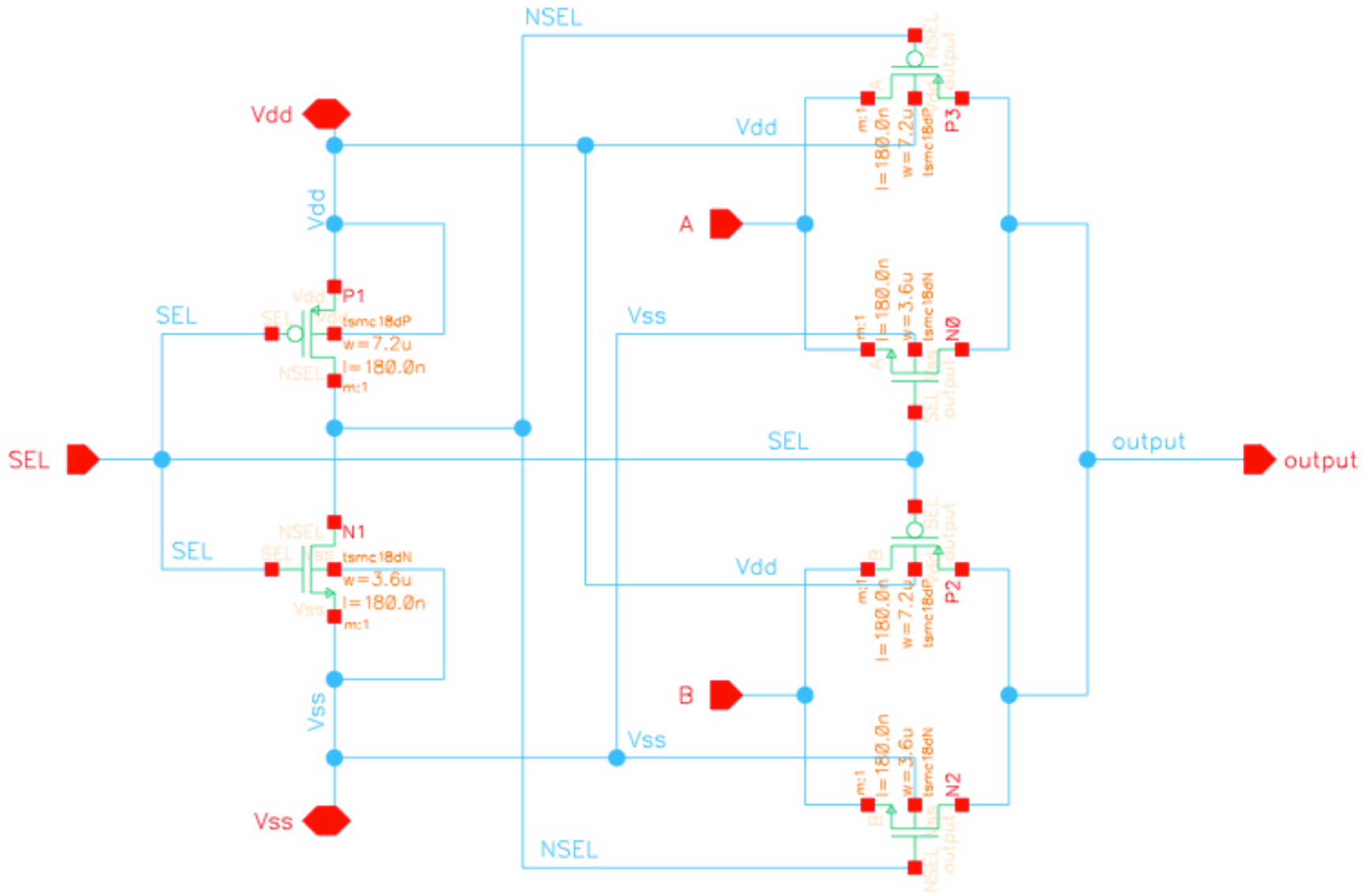
## 2:1 MUX

From Transmission Gate

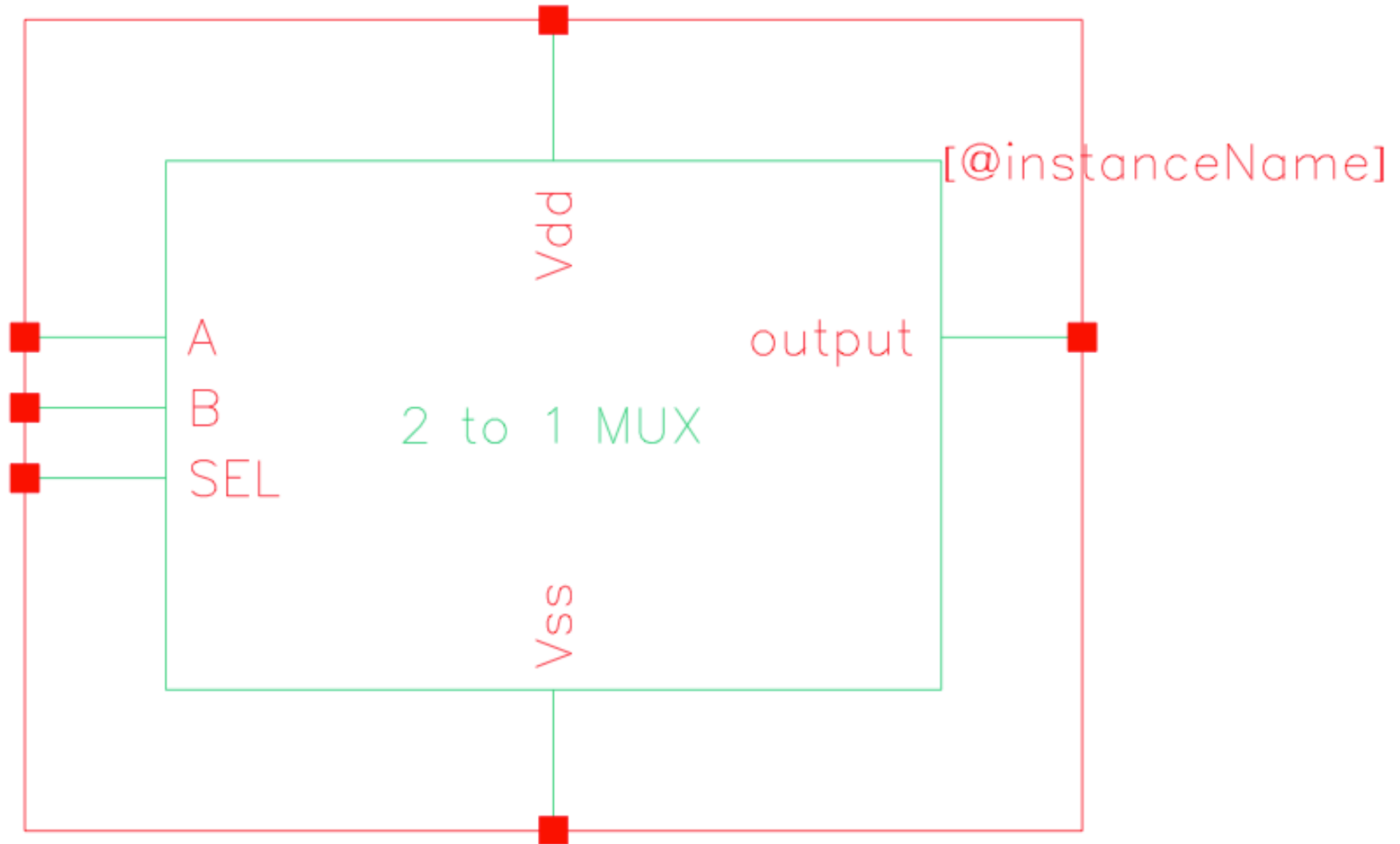
$$(W/L)_n = 3.6/0.18$$

$$(W/L)_p = 7.2/0.18$$

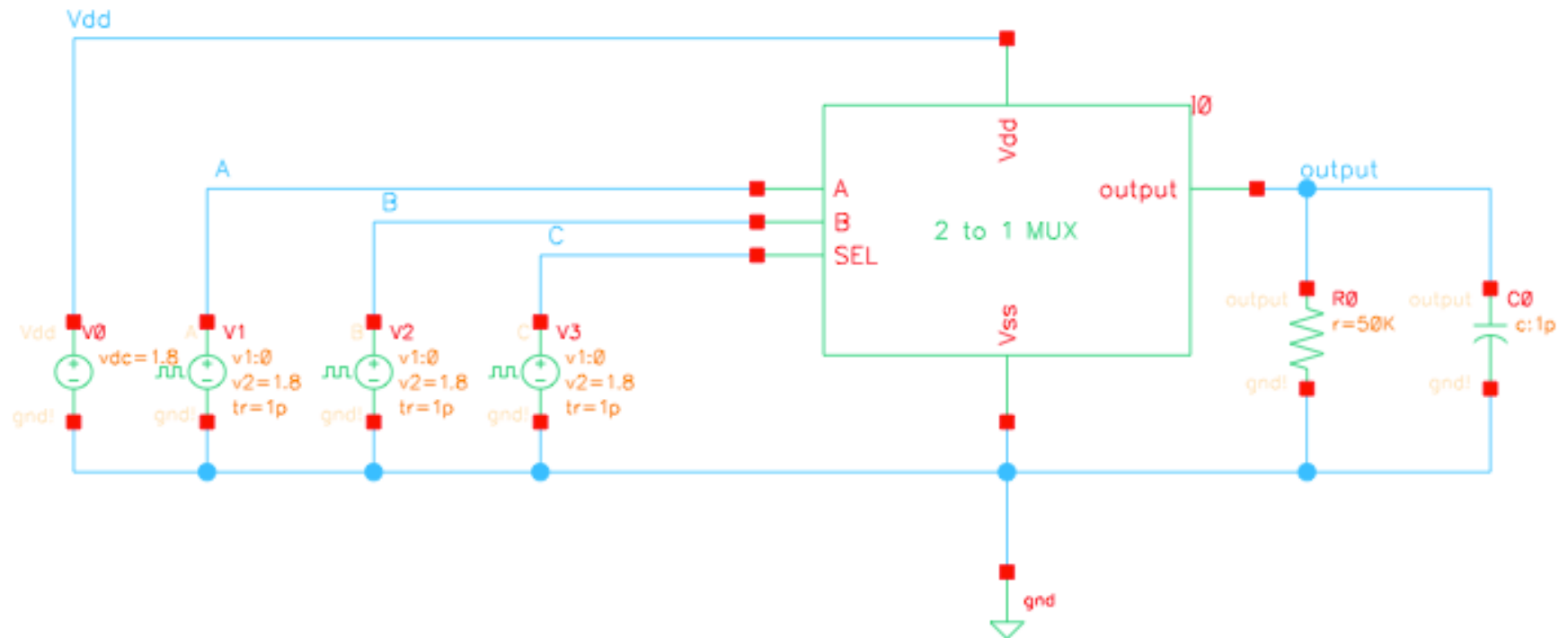
## 2:1 MUX Schematic



## 2:1 MUX Symbol



## 2:1 MUX Testbench





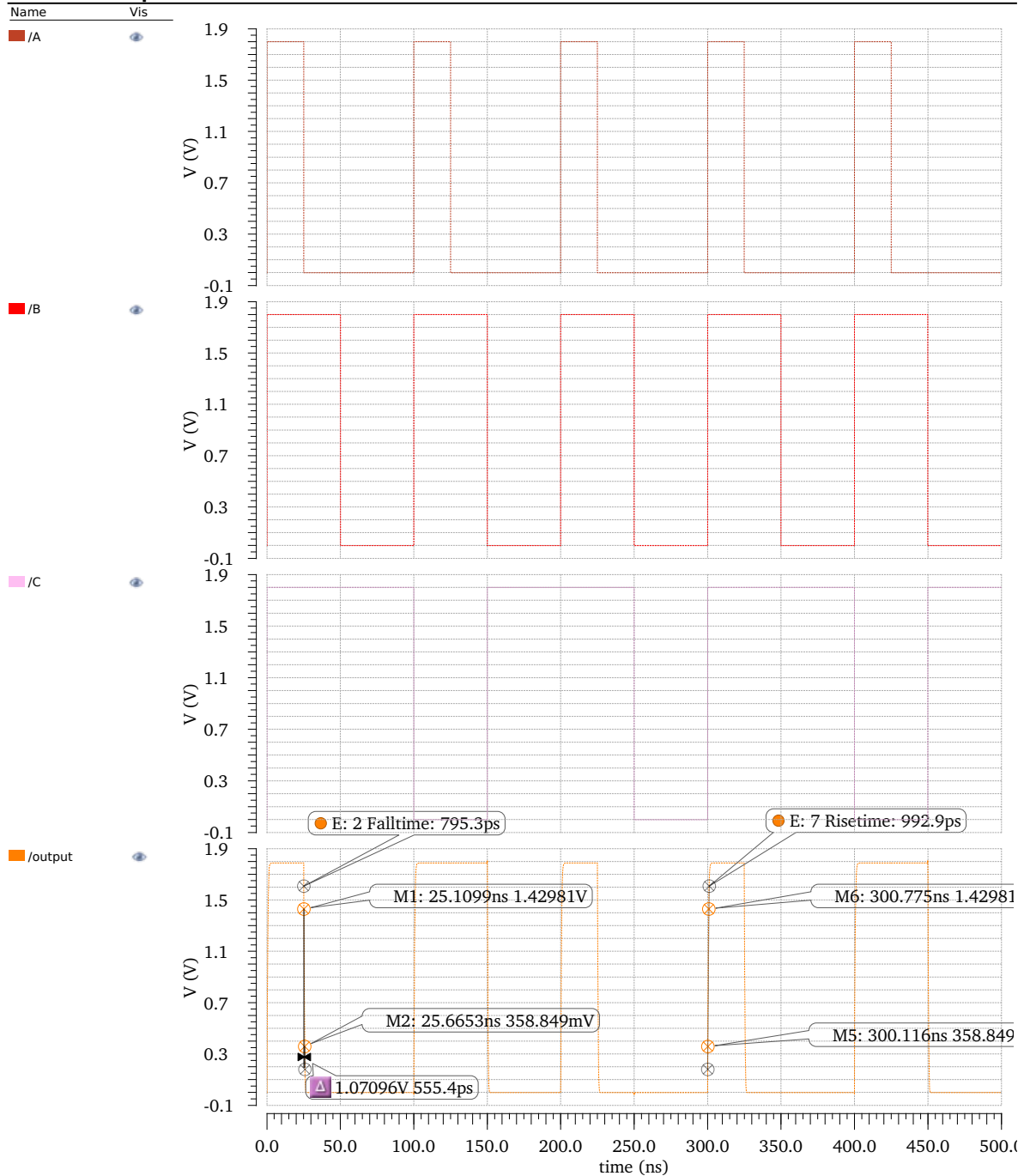
# 2:1 MUX Testbench Waveform

MUX:MUX\_testbench:1 : MUX MUX\_testbench schematic

20:46:33 Thu Mar 1 2018

## Transient Response

Thu Mar 1 20:44:25 2018



## Conclusion

S. No.	Description	Rise Time ( $\mu$ s)	Fall Time ( $\mu$ s)	Delay Time ( $\mu$ s)
1	Inverter	0.000236	0.00018	-0.000056
2	3-Input NAND Gate	0.000057	0.000036	-0.000021
3	2-Input NOR Gate	0.002172	0.000838	-0.001334
4	Transmission Gate	0.000052	0.00197	0.001918
5	2:1 MUX	0.000993	0.000795	-0.000198