81.25

CpE 151 and EEE 234 CMOS and VLSI Design
Quiz – 5

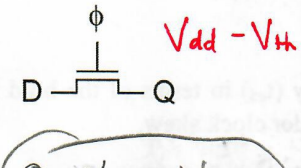
For CpE 151, 2 lowest grade questions will be dropped.

1. Why is t_{pdq} not relevant for Flip-Flops?

Because Flip-Flops are edge-triggered so D=Q at the posedge of the clk only, otherwise Q = previous value
t_{pd} not relavent because Flip-Flops are edge-triggered.

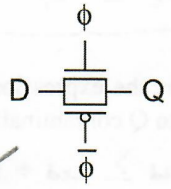
6.25

2. Figure below shows two implementations of a conventional CMOS latch. Annotate the maximum output voltage at the Q of each of the figures. Assume the input is driven by V_{DD}.



$V_{dd} - V_{th}$

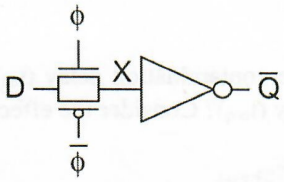
(a) $Q = V_{DD} - V_{th}$



V_{dd}

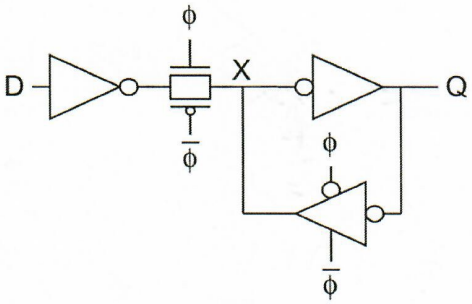
(b) $Q = V_{DD}$

3. Identify the drawback of using the latch below from figure (c)
   a. Output does not swing from rail-to-rail
   b. The signal 'D' drives the diffusion input of the transistor, as a result, noise issues
   c. State node is exposed, as a result, noise on the output can corrupt the state
   d. None of the above



(c)

4. From the figure (d) below, identify the drawback:
   a. Output does not swing from rail-to-rail
   b. The signal 'D' drives the diffusion input of the transistor, as a result, noise issues
   c. State node is exposed, as a result, noise on the output can corrupt the state
   d. None of the above

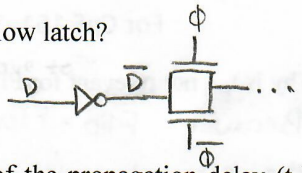


(d)

Static

5. The latch shown in the figure (d) above is Dynamic (Static/Dynamic).

6. How can you convert an active – high latch into an active – low latch?
Place an inverter after the input.



7. What is the expression for clock frequency (T_c) in terms of the propagation delay (t_p), and the sequential overhead, **not** including the clock skew? (Max-Delay constraint)

$t_p \leq T_c - (t_{setup} + t_{cd})$

$T_c \geq t_p + t_{setup} + t_{cd}$

$T_c \geq t_{pcq} + t_{pd} + t_{setup}$

8. What is the expression for the contamination delay (t_{cd}) in terms of the hold time (t_{hold}) and the clock to Q contamination delay (t_{ccq})? Do not consider clock skew.

$t_{hold} \geq t_{cd} + t_{ccq}$

$t_{cd} \geq t_{hold} - t_{ccq}$

9. What is the expression for t_{pd} in terms of the clock period (T_C) and the sequencing overhead in the presence of clock skew?

$t_{pd} \leq T_c - (t_{setup} + t_{skew} + t_{cd})$

10. What is the expression for the contamination delay (t_{cd}) in terms of the hold time (t_{hold}) and the clock to Q contamination delay (t_{ccq})? Consider the effect of clock skew.

$t_{hold} \geq t_{cd} + t_{ccq} + t_{skew}$

$t_{cd} \geq t_{hold} - t_{ccq} + t_{skew}$