

## Lab4. Simplified Microprocessor Design

Figure below shows simplified microprocessor diagram having M0, M1, M2 and Cin inputs, one input switch SW1 and also clock input. The SW1 switch serves as asynchronous reset function.

Your design should finally implement the following operation:

$$R[2] = M0 + (\text{not } M1) + \text{Cin}$$

The R[2] signal is connected with output “dout”.

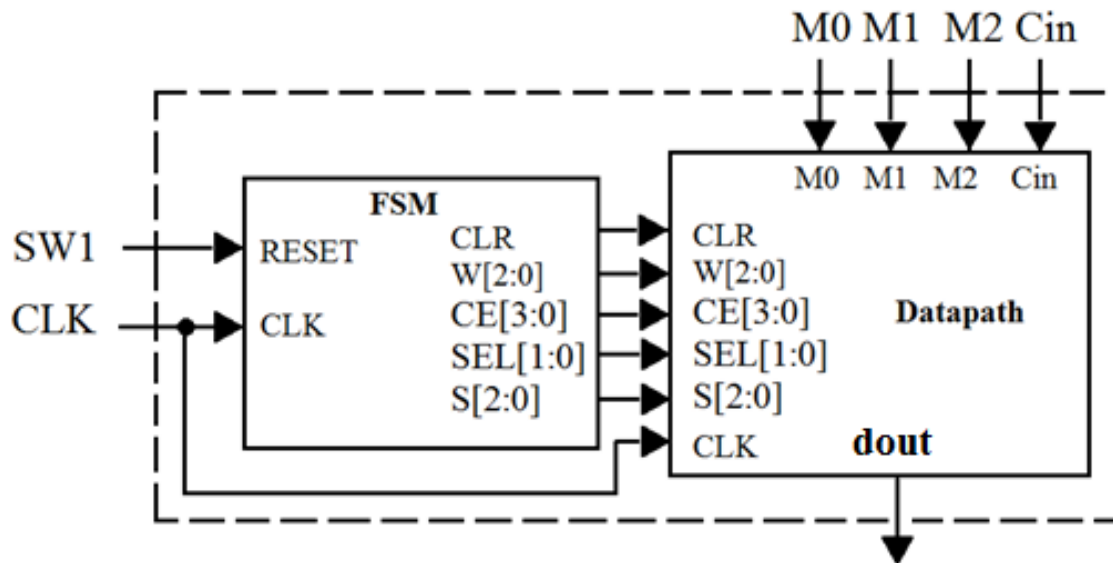


Figure. Simplified microprocessor block diagram

In the above Figure, the “FSM” unit is a finite state machine controller. The logic ‘1’ on “SW1” switch will force the controller to enter its first state. After “SW1” becomes logic ‘0’, the finite state machine will proceed forward automatically into the next state after the rising edge of the clock. The major outputs of different states of the controller are control signals for the datapath circuit.

- (1). Before the final dout result is available, the LED display should be off.
- (2). After the final dout result is available, the LED display should be off when final result is ‘0’ Otherwise the LED display should be on when the final dout result is ‘1’.

The detailed datapath circuit is shown in Figure below.

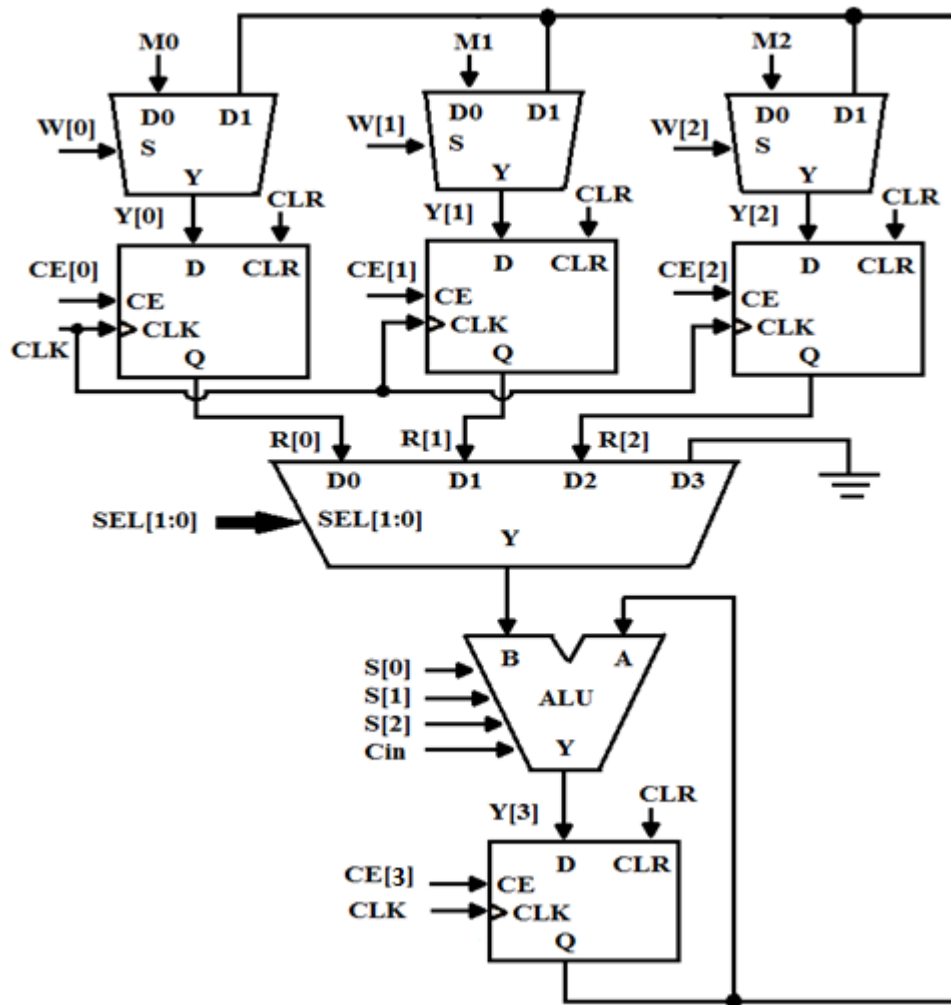


Figure. Datapath circuit diagram

The truth table of the ALU unit inside the datapath circuit is shown in the Table below.

Table. ALU truth table

S2	S1	S0	ALU Output F
0	0	0	$F=A+B+C_{in}$
0	0	1	$F=A+B'+C_{in}$
0	1	0	$F= B$
0	1	1	$F= A \text{ NAND } B$
1	0	0	$F= A \text{ AND } B$
1	0	1	$F= A \text{ OR } B$
1	1	0	$F= A'$
1	1	1	$F= A \text{ XOR } B$

Draw your finite state machine diagram for the “FSM” unit. Use structural hierarchical design method to implement the datapath circuit. Finally, on your top level complete design, you should create two instances: “FSM” and “datapath”, also wire them up to form the simplified microprocessor circuit.

In the lab, demo your testbench simulation for the microprocessor finite state machine control and datapath.

Extra credit of 5 points: Download your complete design of microprocessor system on FPGA. Once microprocessor completes processing of the logic function operation, the following results should be demoed:

- (1). The LED display will be on if the final R[2] result is '1';
- (2). The LED display will be off if the final R[2] result is '0'.