75/100

**CpE 151 and EEE 234 CMOS and VLSI Design**

**Quiz – 1**

For CpE 151, 5 lowest grade questions will be dropped. For EEE234 2 questions will be dropped.

1. MOSFET stands for Metal Oxide Semi-Conductor Field Effect Transistor ~~metal oxide semi-conductor field effect transistor~~ X

2. p-type semiconductor has holes (electrons/holes) as majority charge carriers. ✓

3. n-type semiconductor is built by doping intrinsic Silicon with group V (III/V) element. ✓

4. When a voltage of 5V (High) is applied to the Drain of a NMOS transistor, the transistor is:
   (a) ON (b) OFF (c) Not enough information ✓

5. When a voltage of 0V (Low) is applied to the Gate of a PMOS transistor, the transistor is:
   (a) ON (b) OFF (c) Not enough information ✓

6. Pick one option. A 3-input NAND gate has:
   (a) 3 NMOS transistors in the Pull Up Network
   (b) 3 PMOS transistors in the Pull Down Network
   (c) 3 NMOS transistors in parallel and 3 PMOS transistors in series
   (d) 3 NMOS transistors in series and 3 PMOS transistors in parallel ✓

7. If the NMOS and PMOS transistors switch places in an inverter, the resulting circuit is:
   (a) Weak Inverter
   (b) Strong Inverter
   (c) Weak buffer ✓
   (d) Strong buffer

8. Which of the following is true about NMOS transistor?
   (a) It provides a good '1'
   (b) It provides a good '0' ✓
   (c) It uses p-well
   (d) It uses n-well

9. To properly bias the Source-Bulk and Drain-Bulk diodes, the Bulk (B) terminal of the PMOS transistor should be connected to p-body High-Voltage. X

10. Input dependent phase shift is brought about by which of the following transistor non–ideality?
    a. Channel–charge injection
    b. Clock–feed through
    c. Non–zero ON–resistance X
    d. Negative–bias Temperature Instability (NBTI)

11. Which of the following circuits uses 2-NMOS and 2-PMOS transistors, all in series?
    a. Inverter
    b. 2–input NAND gate
    c. Tri–state inverter
    d. 3–input NOR gate

12. In a transmission gate, when the PMOS is ON, then the NOMS is OFF (ON/OFF).

13. The condition for NMOS transistor to be ON is $V_{gs} > V_t$.

14. The condition for NMOS transistor to be in saturation is high drain voltage $V_{ds} \geq V_{gs} - V_t$.

15. In the Figure – 2 shown below, plot the graph for the equivalent ON-resistance of a transmission gate. The On-resistance of NMOS and PMOS as a function of Vin.

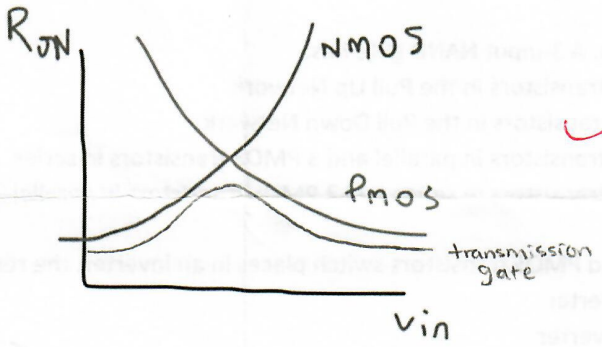


**Figure – 2. On-resistance of NMOS, PMOS and transmission gate**

16. The mobility of electrons is equal than/to that of holes. (greater, smaller or equal).

17. The relation between Q (charge), V (voltage) and C (capacitance) is given by $Q = V \cdot C$.