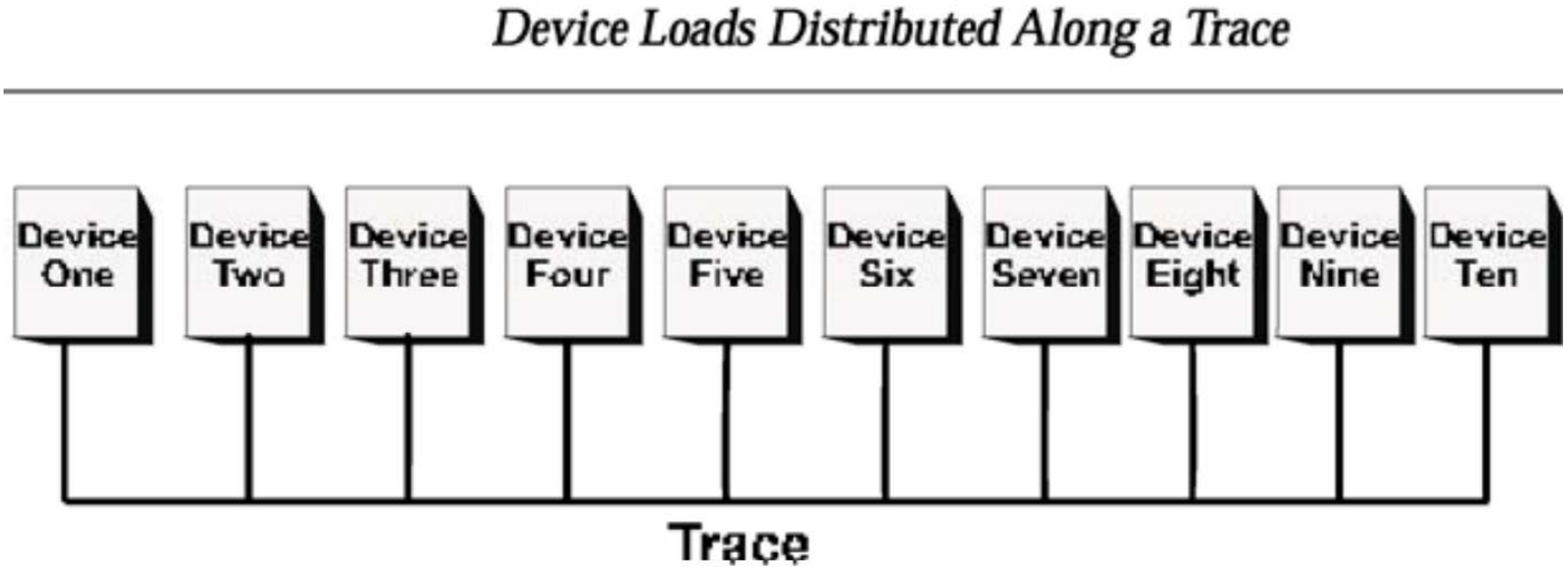
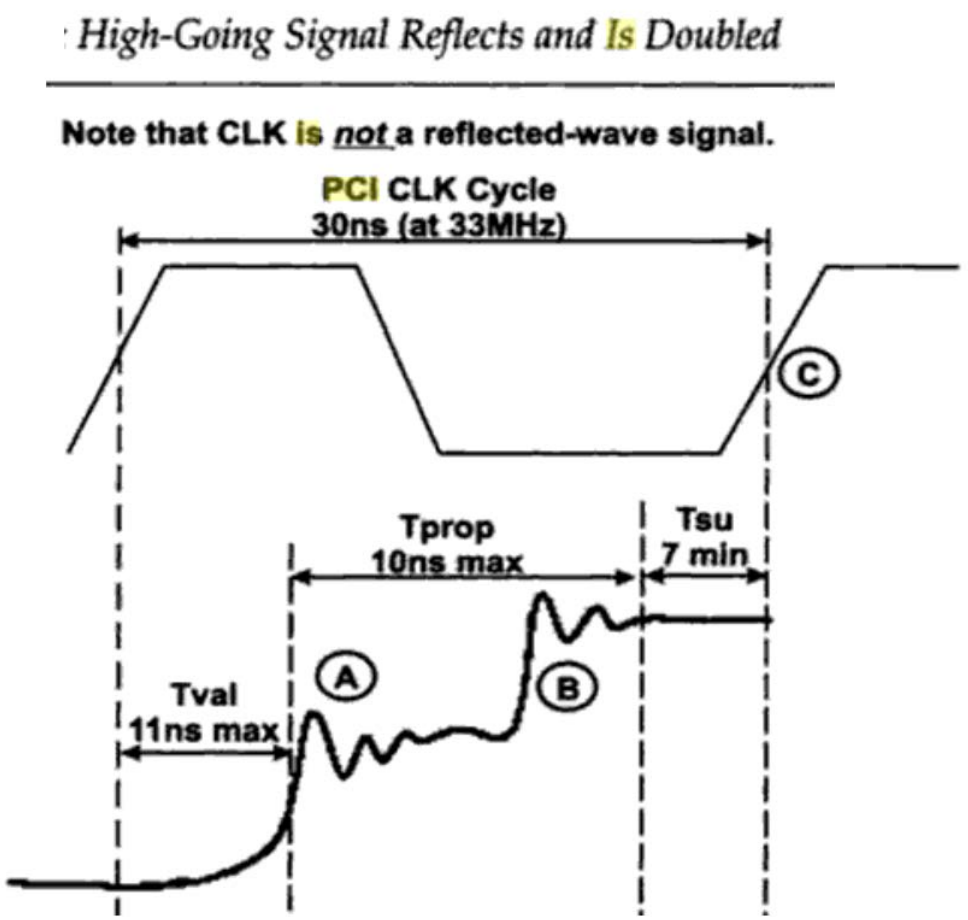
CPE 186 Computer Hardware Design

Intro to Reflected-Wave Switching

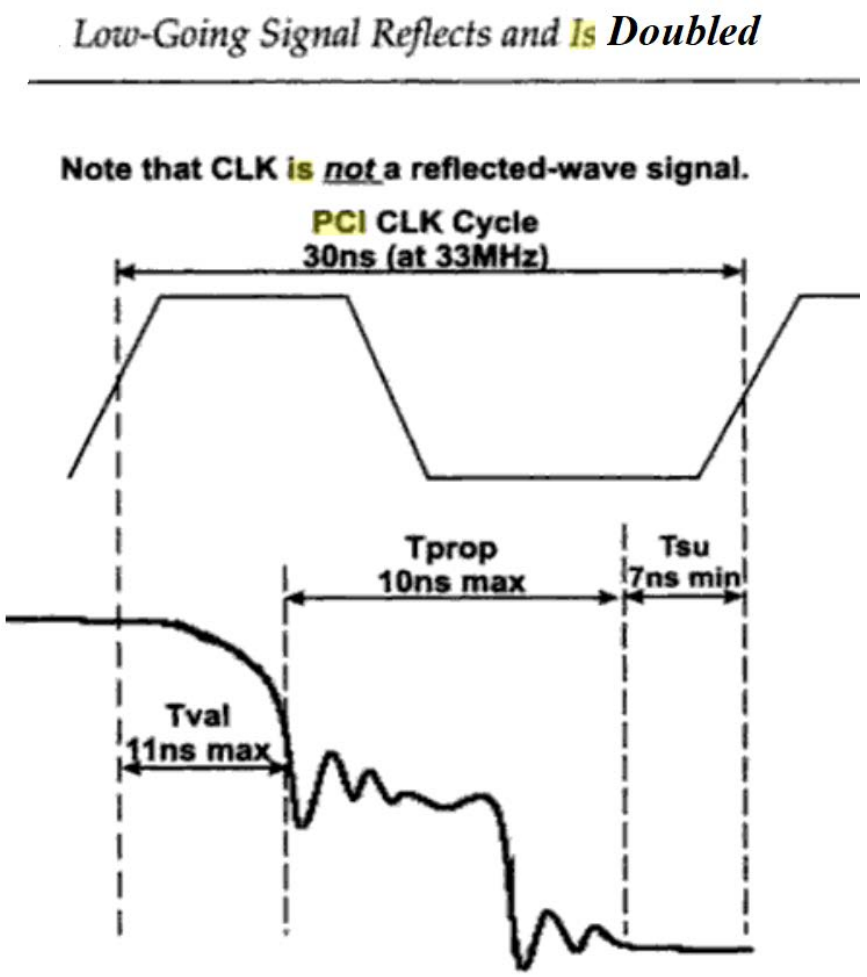
Incident-Wave Switching



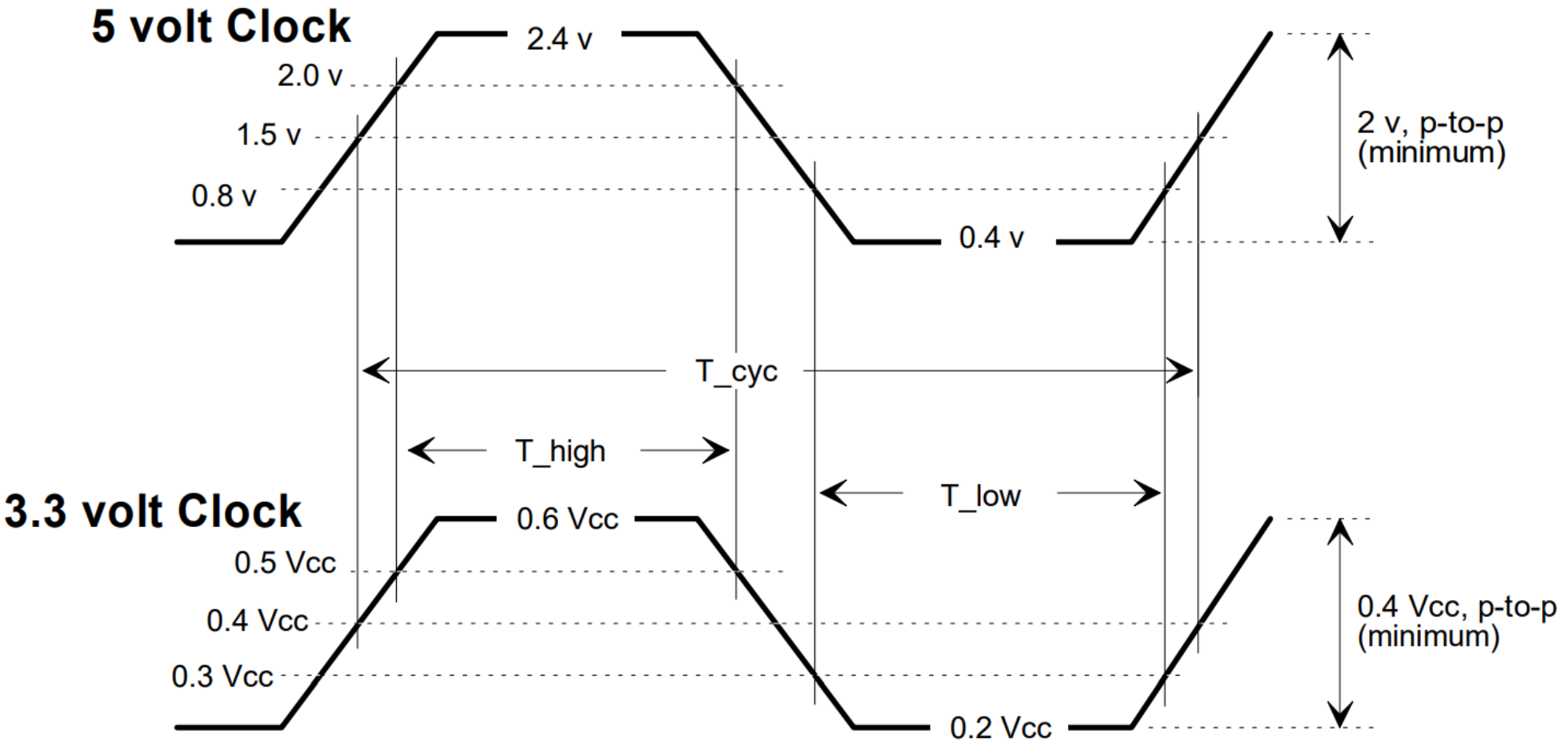
Reflected-Wave Switching



Reflected Wave Switching



PCI Clock Waveform



PCI Clock and Reset Specifications

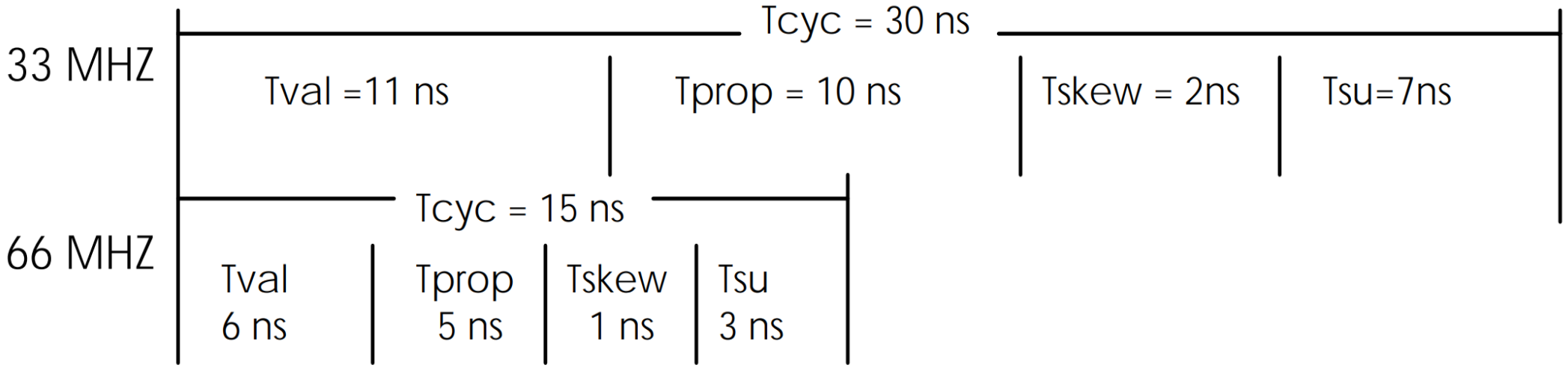
Symbol	Parameter	Min	Max	Units
T_{cyc}	**CLK** Cycle Time	30	∞	ns
T_{high}	**CLK** High Time	11		ns
T_{low}	**CLK** Low Time	11		ns
-	**CLK** Slew Rate	1	4	V/ns
-	**RST#** Slew Rate	50	-	mV/ns

PCI Timing Parameters

Symbol	Parameter	Min	Max	Units	Notes
T_{val}	**CLK** to Signal Valid Delay - bused signals	2	11	ns	1, 2, 3
$T_{val}(ptp)$	**CLK** to Signal Valid Delay - point to point	2	12	ns	1, 2, 3
T_{on}	Float to Active Delay	2		ns	1, 7
T_{off}	Active to Float Delay		28	ns	1, 7
T_{su}	Input Setup Time to **CLK** - bused signals	7		ns	3, 4, 8
$T_{su}(ptp)$	Input Setup Time to **CLK** - point to point	10, 12		ns	3, 4
T_{h}	Input Hold Time from **CLK**	0		ns	4
T_{rst}	Reset active time after power stable	1		ms	5
$T_{rst-clk}$	Reset active time after **CLK** STABLE	100		µs	5
$T_{rst-off}$	Reset Active to Output Float delay		40	ns	5, 6,7
T_{rrsu}	**REQ64#** to **RST#** Setup time	$10*T_{cyc}$		ns	
T_{rrh}	**RST#** to **REQ64#** Hold time	0	50	ns	
T_{rhfa}	**RST#** High to First configuration Access	2^{25}		clocks	
T_{rhff}	**RST#** High to First **FRAME#** assertion	5		clocks	

33 MHz vs. 66 MHz PCI Timing

$$T_{cyc} \geq T_{val} + T_{prop} + T_{skew} + T_{su}$$



Clock Skew

Symbol	5V Signaling	3.3V Signaling	Units
V_{test}	1.5	0.4 V_{cc}	V
T_{skew}	2 (max)	2 (max)	ns