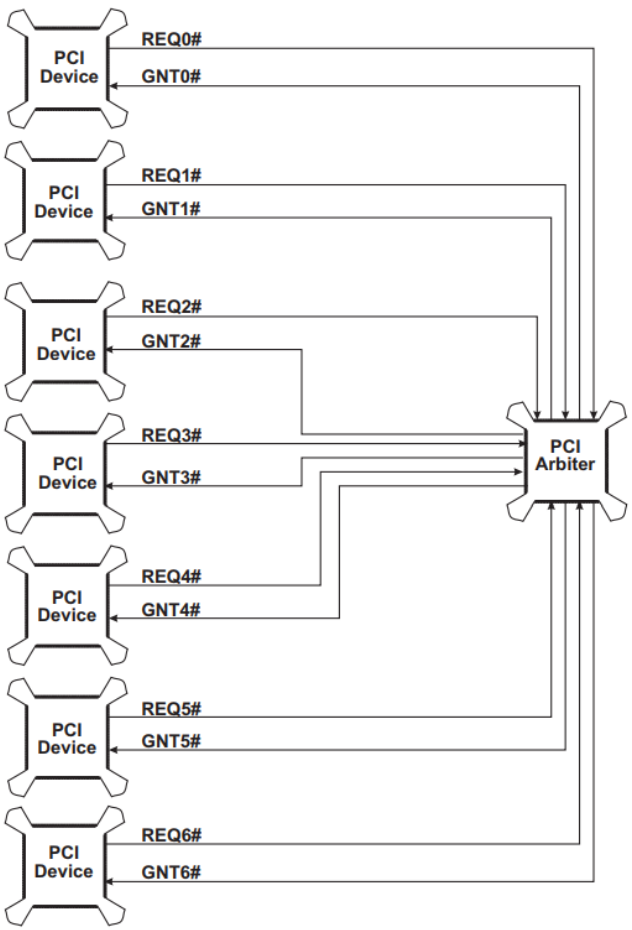
The PCI Bus Arbitration

CPE 186 Handout

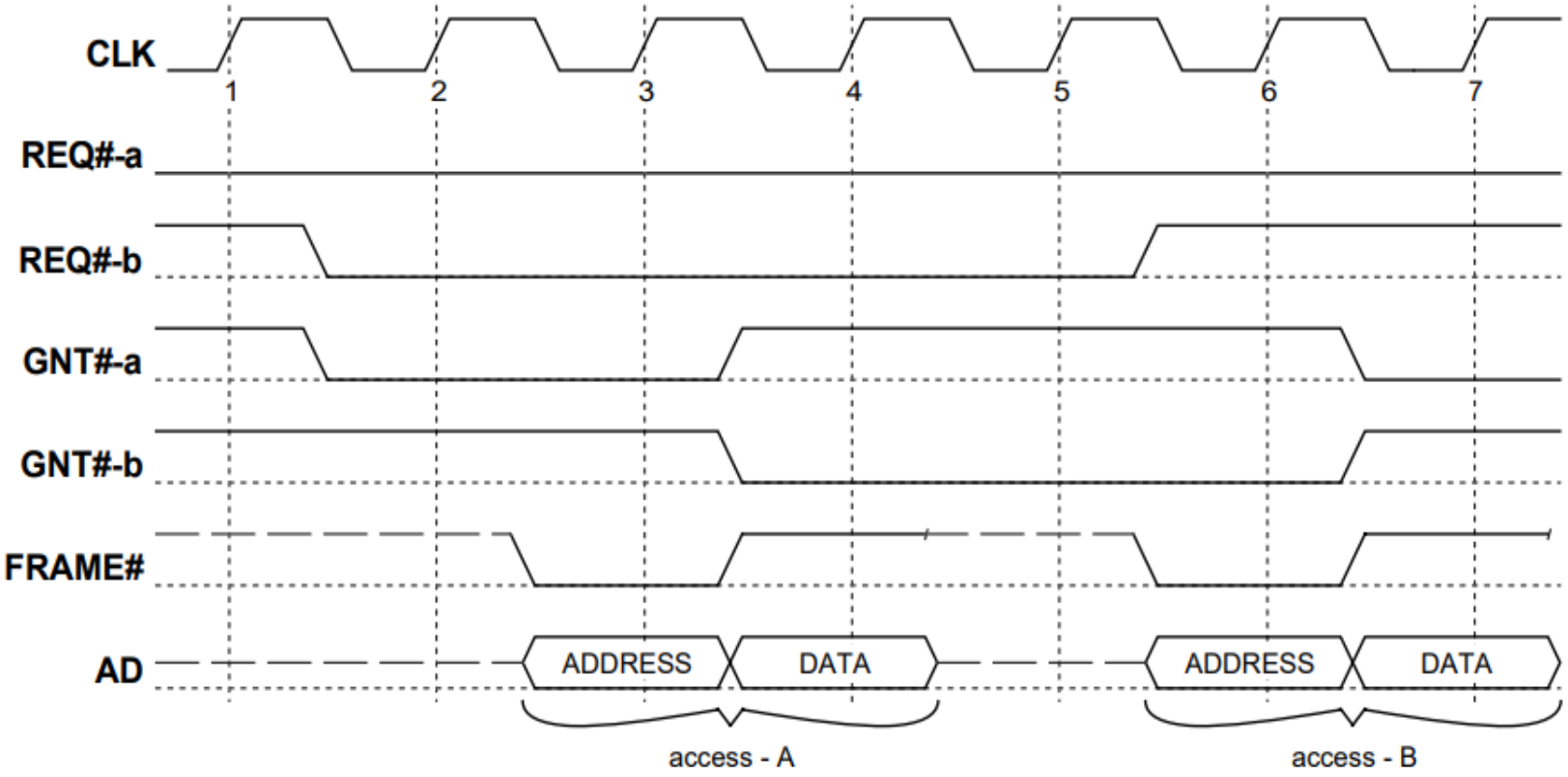
PCI Bus Arbiter



PCI Bus Arbiter

- Uses Centralized Arbitration
  - Independent grant and request lines
    - REQ# and GNT# lines for each device
    - One or more PCI master devices may require use of the PCI bus to perform a data transfer with another PCI device.
  - Does not specify a particular policy
    - Mandates the use of a fair policy

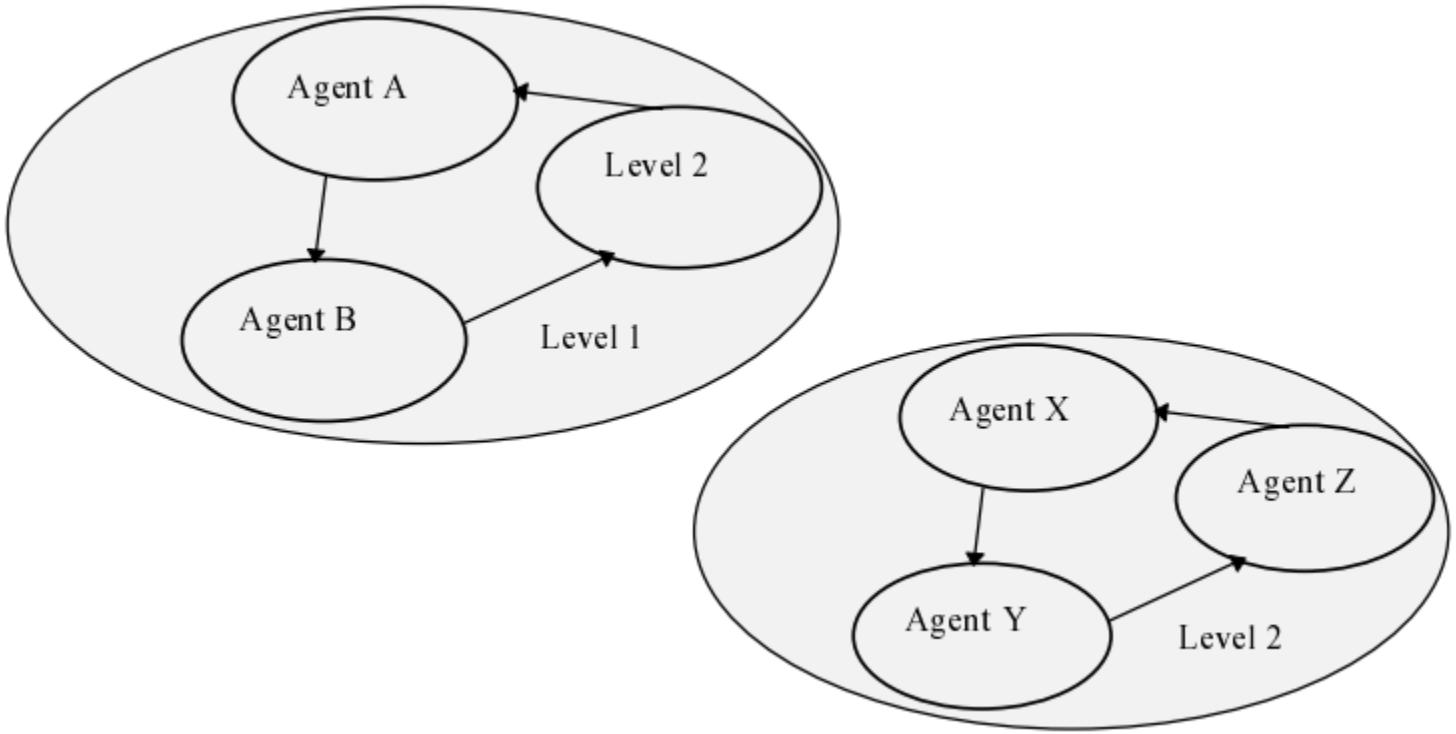
Basic PCI Arbitration



Fairness

The central arbiter is required to implement a fairness algorithm to avoid deadlocks. Fairness means that each potential bus master must be granted access to the bus independent of other requests. Fairness is defined as a policy that ensures that high-priority masters will not dominate the bus to the exclusion of lower-priority masters when they are continually requesting the bus. However, this does not mean that all agents are required to have equal access to the bus.

PCI Bus Arbitration Example (1)



PCI Bus Arbitration Example (2)

Assume the following conditions:

- Master A is the next to receive the bus in the first group.
- Master X is the next to receive it in the second group.
- A master in the first group is the next to receive the bus.

PCI Bus Arbitration Example (3)

If all agents on level 1 and 2 have their **REQ#** lines asserted and continue to assert them, and if Agent A is the next to receive the bus for Level 1 and Agent X is the next for Level 2, then the order of the agents accessing the bus would be:

A, B, Level 2 (this time it is X)

A, B, Level 2 (this time it is Y)

A, B, Level 2 (this time it is Z)

and so forth.

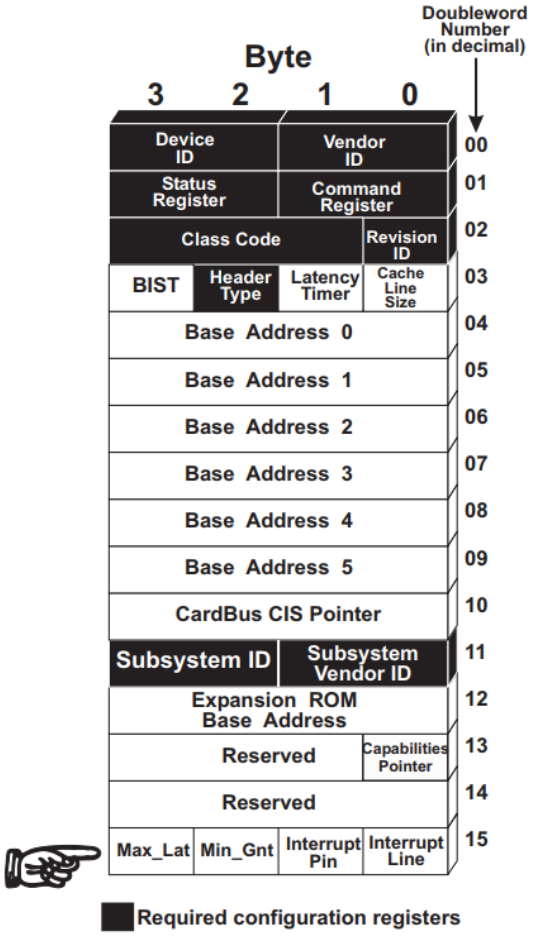
PCI Bus Arbitration Example (4)

If only Agent B and Agent Y had their **REQ#**s asserted and continued to assert them, the order would be:

B, Level 2 (Y),

B, Level 2 (Y).

Maximum Latency Configuration Register



In increments of 250 ns.

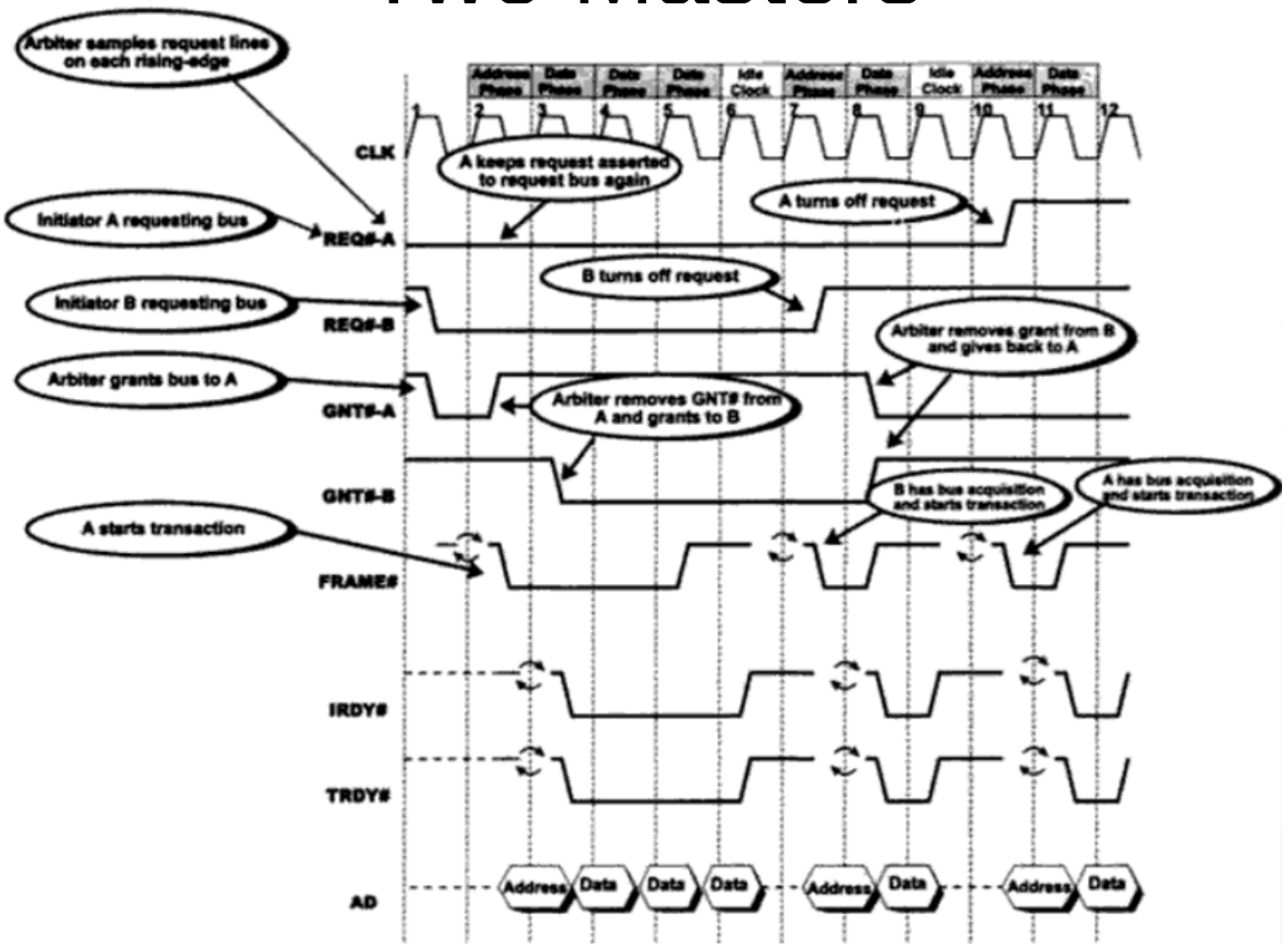
Maximum Latency Configuration Register

Ideally, the bus arbiter should be programmable by the system. If it is, the start-up configuration software can determine the priority to be assigned to each member of the bus master community by reading from the Maximum Latency (Max_Lat) configuration register associated with each bus master (see Figure 5-2 on page 62). The bus master designer hardwires this register to indicate, in increments of 250ns, how quickly the master requires access to the bus in order to achieve adequate performance.

PCI Bus State

FRAME#	IRDY#	Description
deasserted	deasserted	Bus Idle.
deasserted	asserted	Initiator is ready to complete the last data transfer of a transaction, but it has not yet completed.
asserted	deasserted	A transaction is in progress and the initiator is not ready to complete the current data phase.
asserted	asserted	A transaction is in progress and the initiator is ready to complete the current data phase.

PCI Bus Arbitration Between Two Masters



PCI Bus Parking

- A master must only assert its REQ# to signal a current need for the bus.
- If a system designer implements a bus parking scheme, a default bus owner should be defined when no other masters request bus.
- The choice of which master to park the bus on is defined by the designer of the bus arbiter.