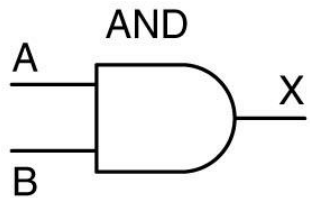


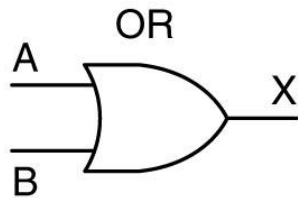
# The Digital Logic Level

## Chapter 3

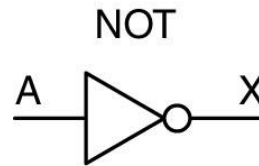
# Gates and Boolean Algebra



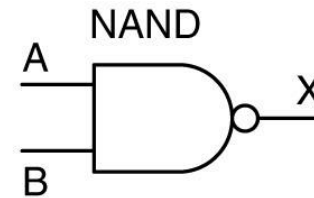
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1



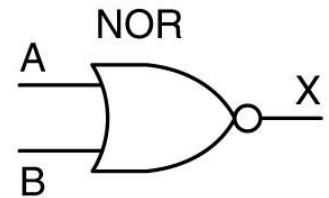
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1



A	X
0	1
1	0

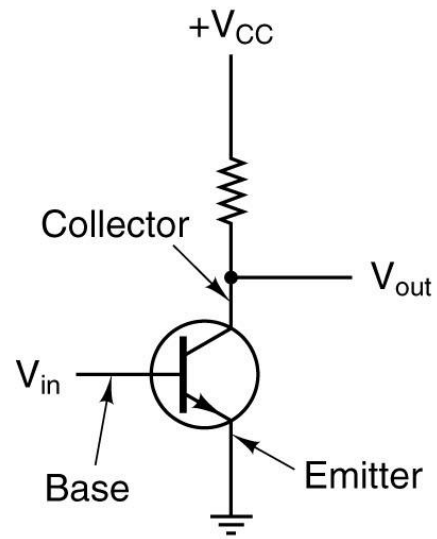


A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

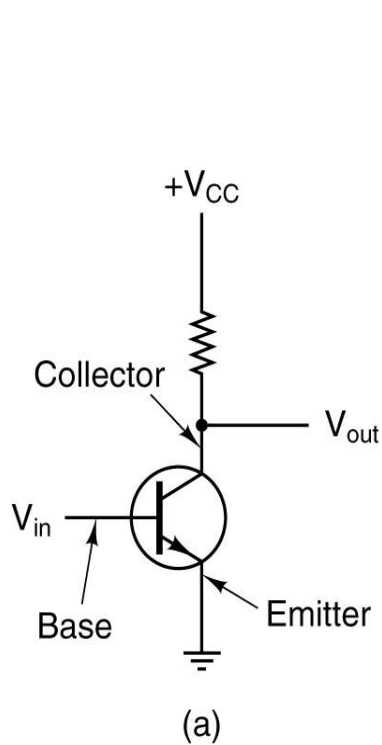


A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

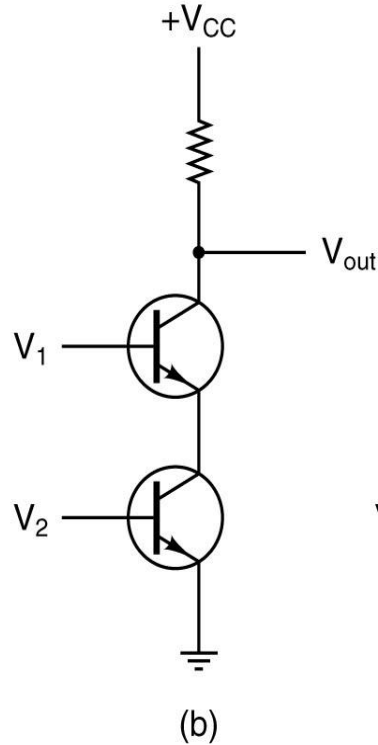
# Transistor



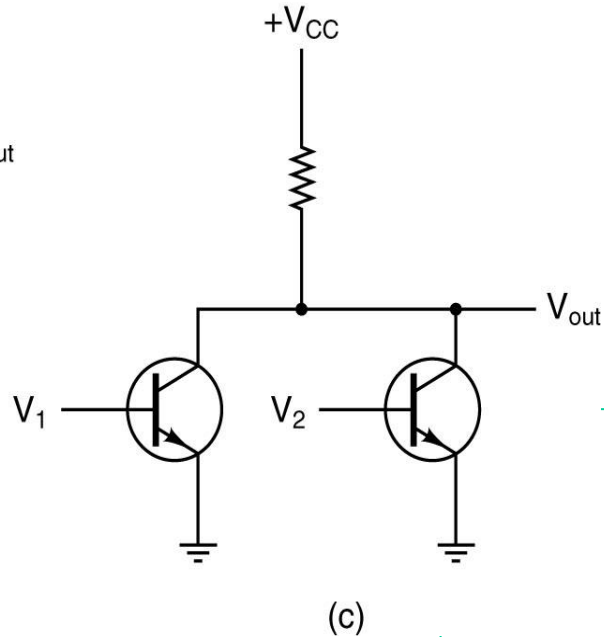
# Gates and Boolean Algebra (1)



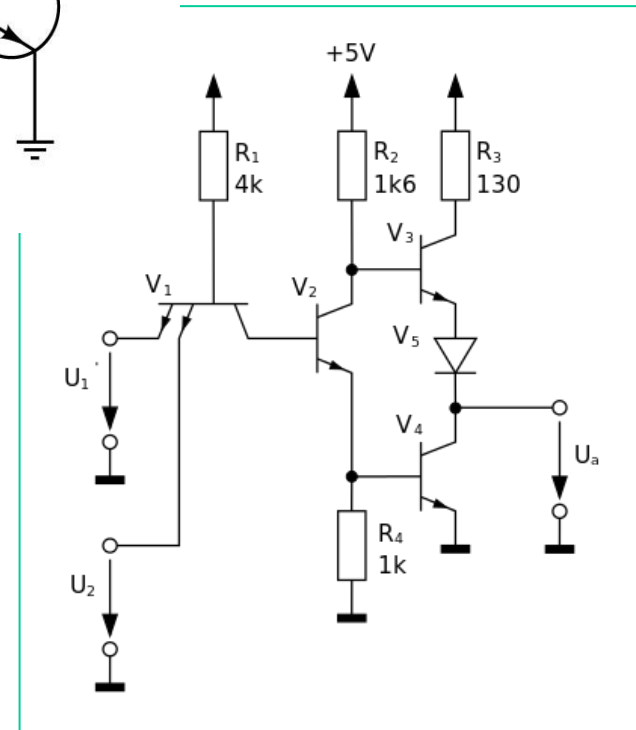
(a) A NOT gate (inverter)



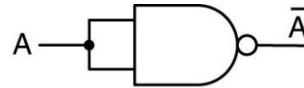
(b) A NAND gate



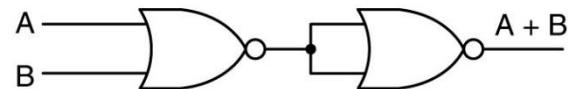
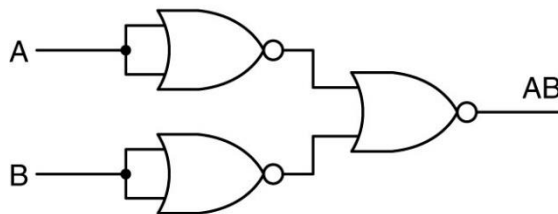
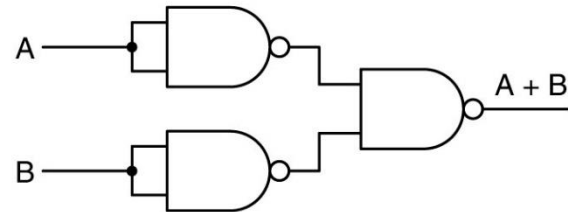
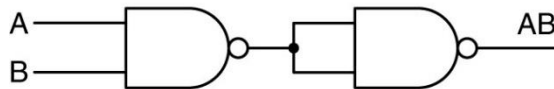
(c) A NOR gate



# Circuit Equivalence



(a)



(b)

(c)

Construction of (a) NOT, (b) AND, and (c) OR gates using only NAND gates or only NOR gates.

# Positive & Negative Logic

<b>A</b>	<b>B</b>	<b>F</b>
0 <sup>V</sup>	0 <sup>V</sup>	0 <sup>V</sup>
0 <sup>V</sup>	5 <sup>V</sup>	0 <sup>V</sup>
5 <sup>V</sup>	0 <sup>V</sup>	0 <sup>V</sup>
5 <sup>V</sup>	5 <sup>V</sup>	5 <sup>V</sup>

(a)

<b>A</b>	<b>B</b>	<b>F</b>
0	0	0
0	1	0
1	0	0
1	1	1

(b)

<b>A</b>	<b>B</b>	<b>F</b>
1	1	1
1	0	1
0	1	1
0	0	0

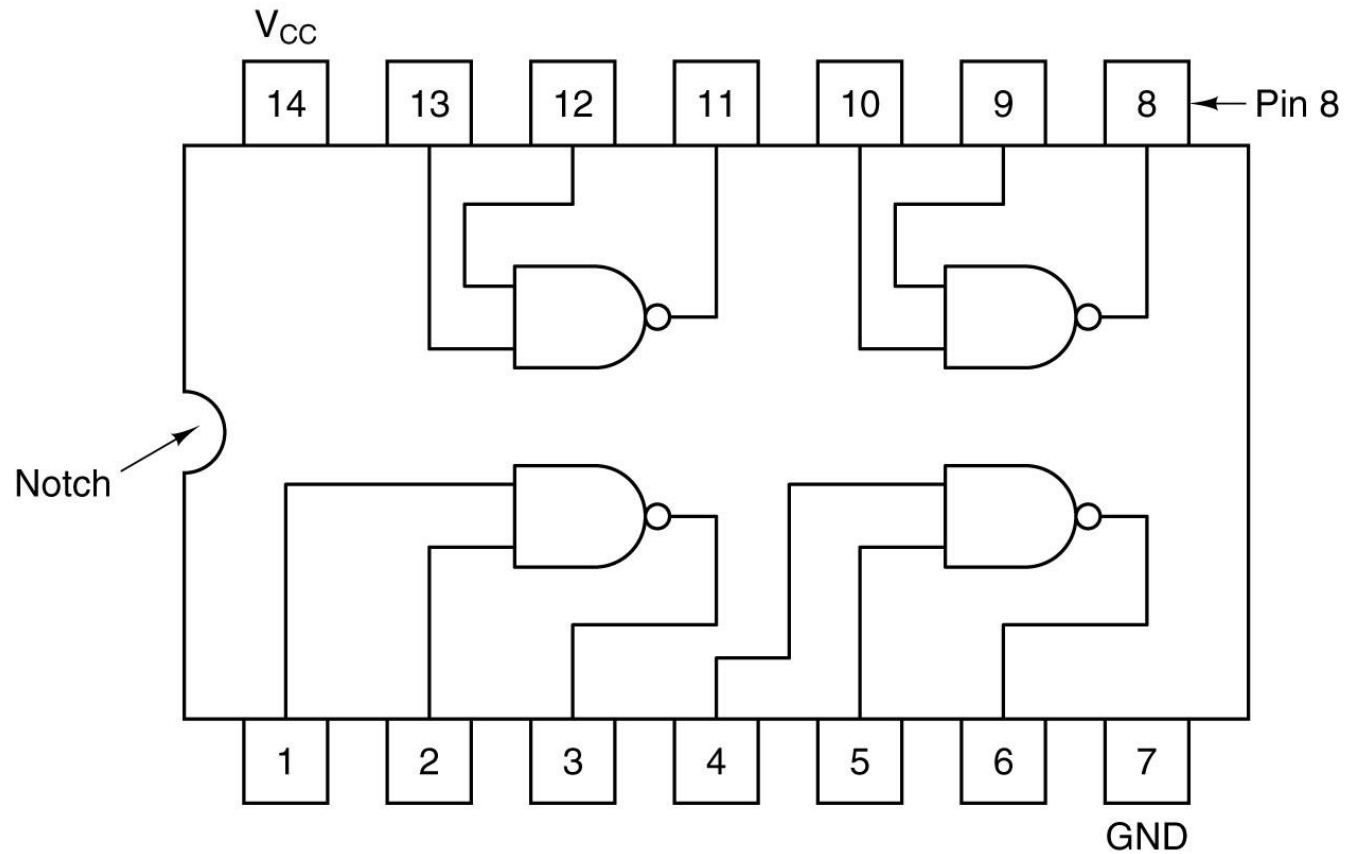
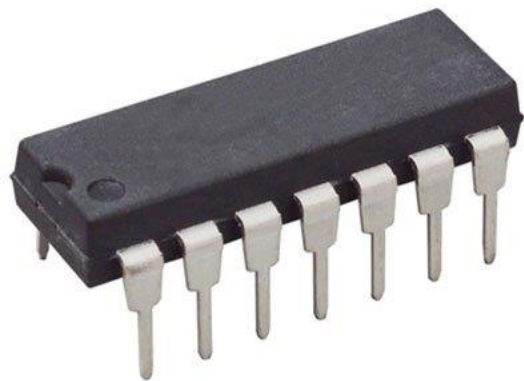
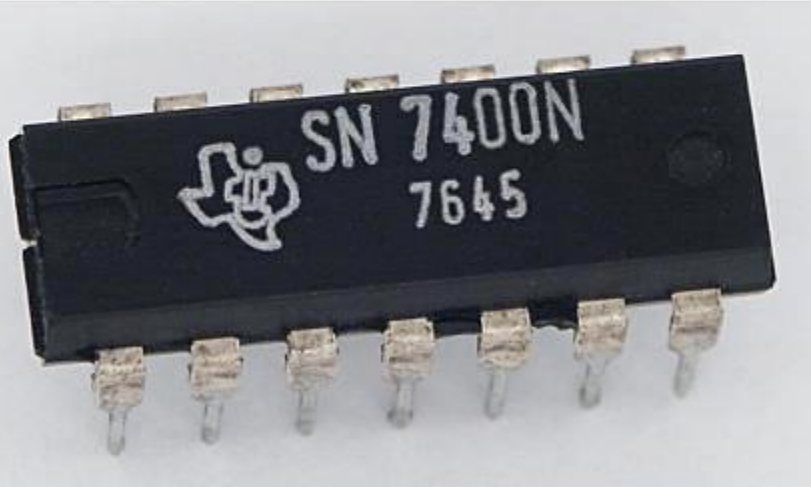
(c)

(a) Electrical characteristics of a device.

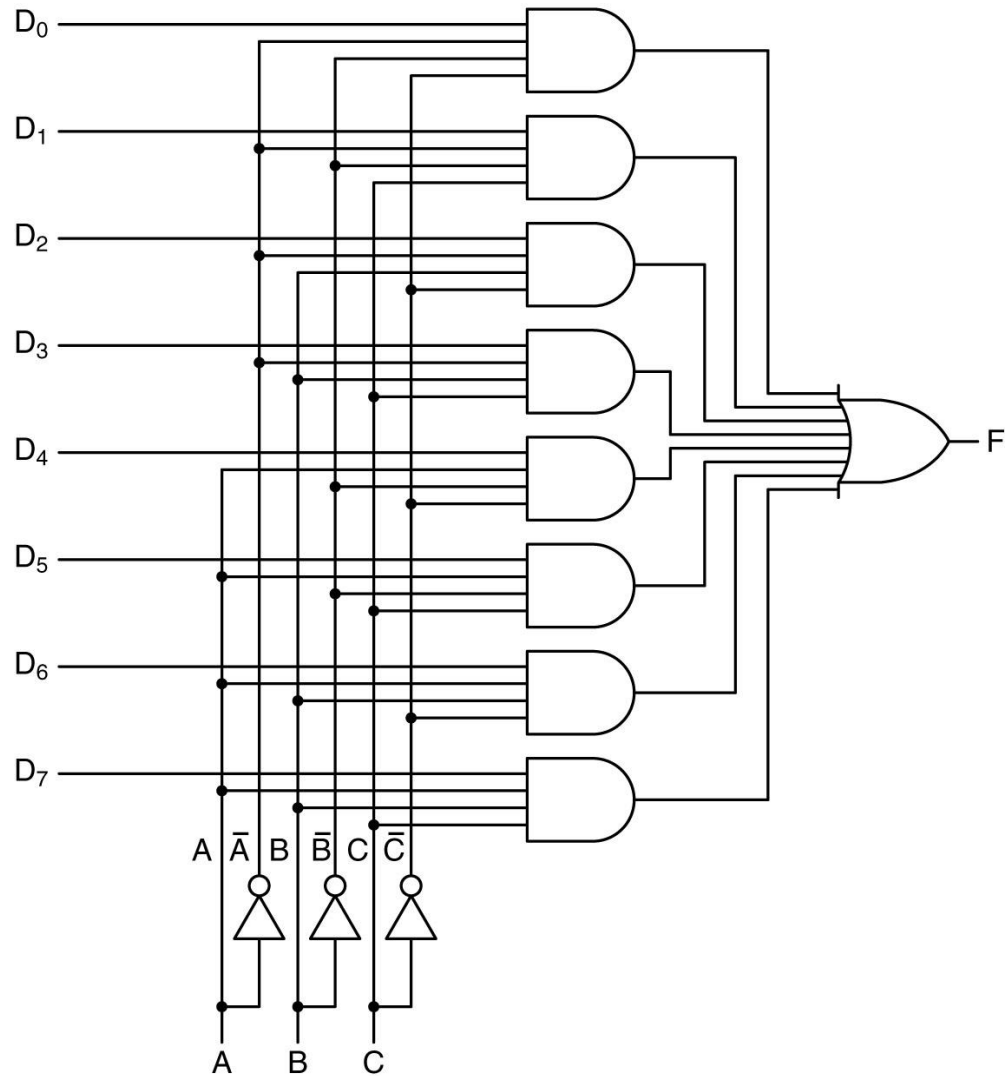
(b) Positive logic.

(c) Negative logic.

# Integrated Circuits

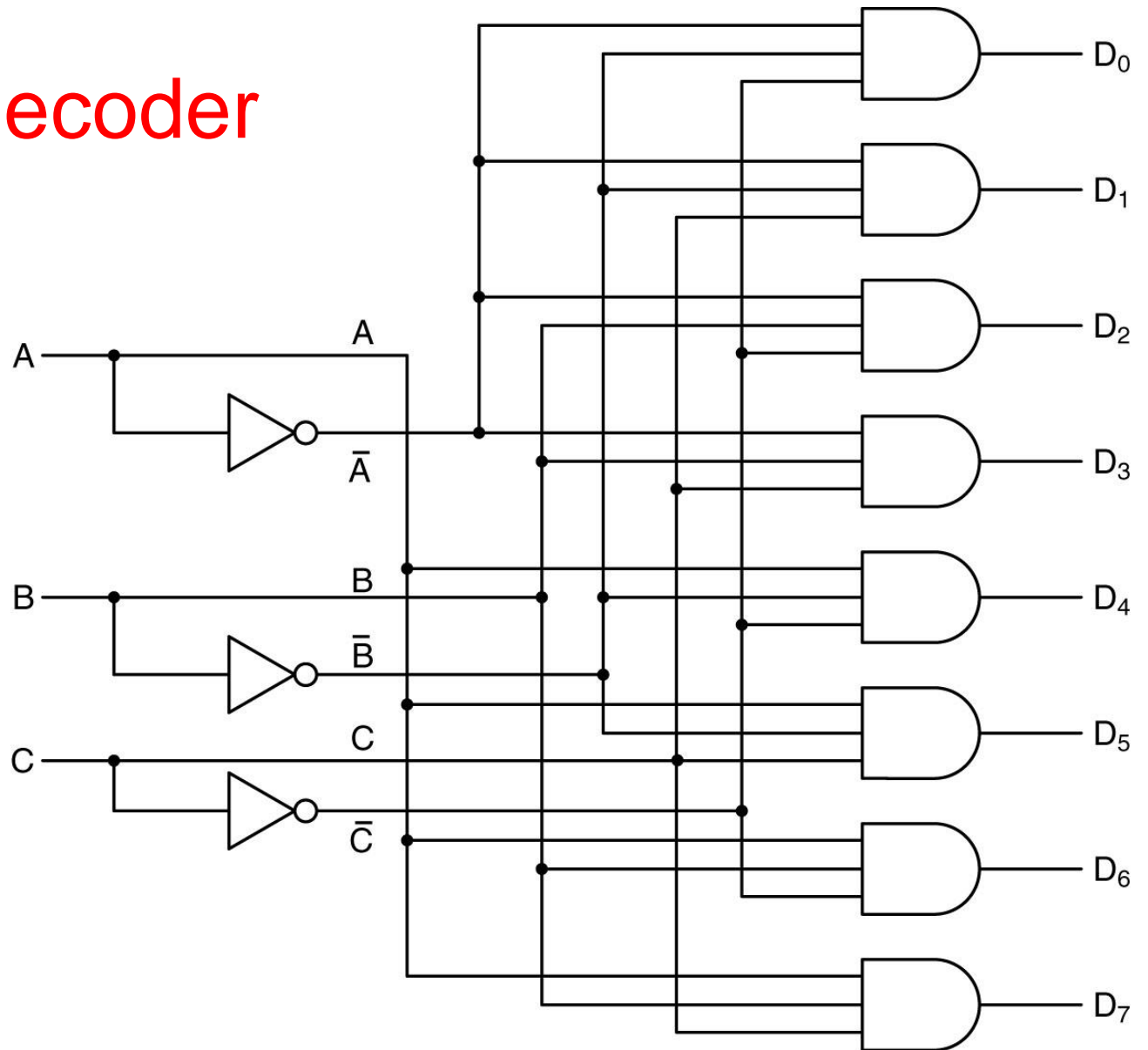


# 8-to-1 Multiplexer

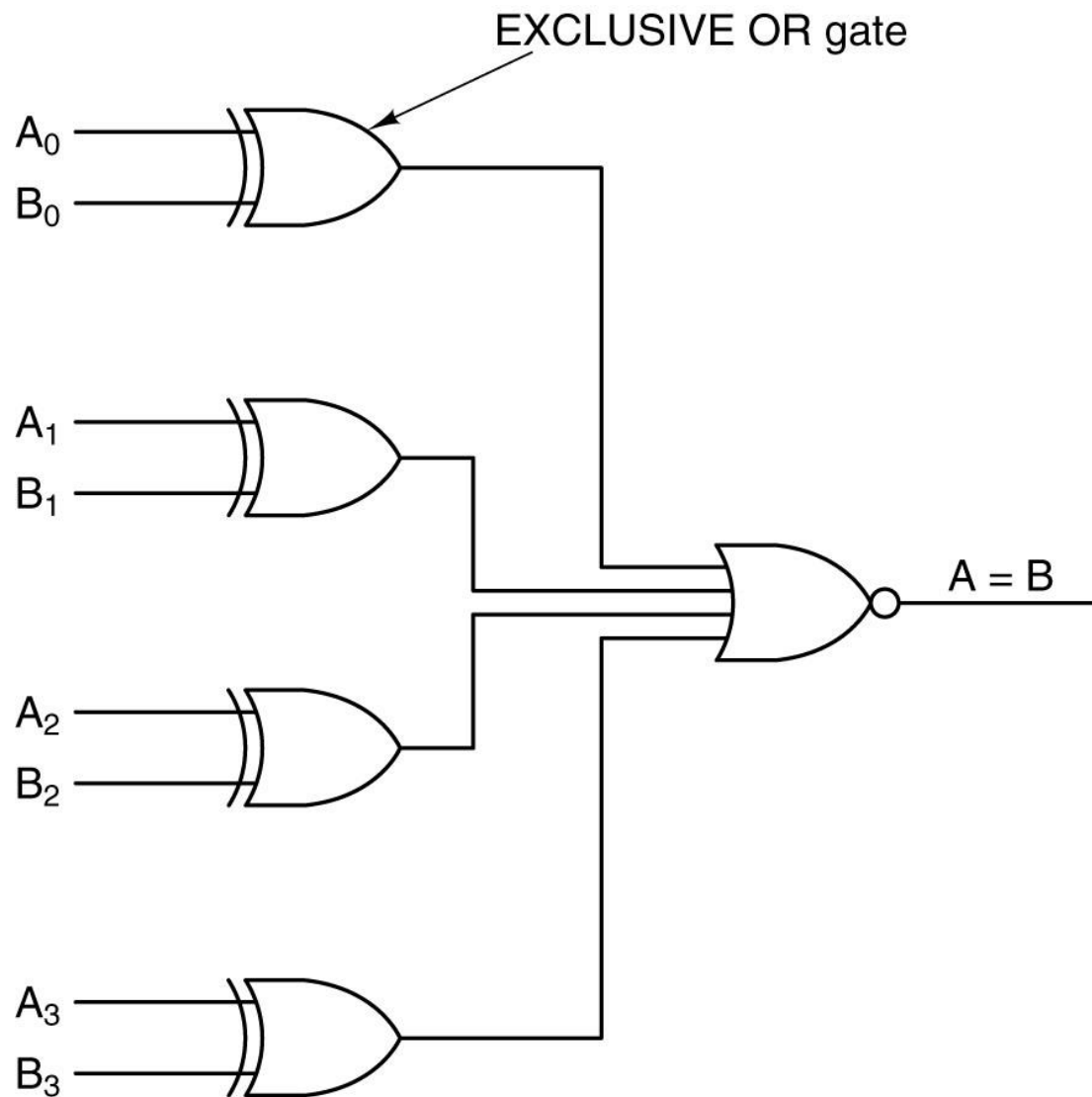




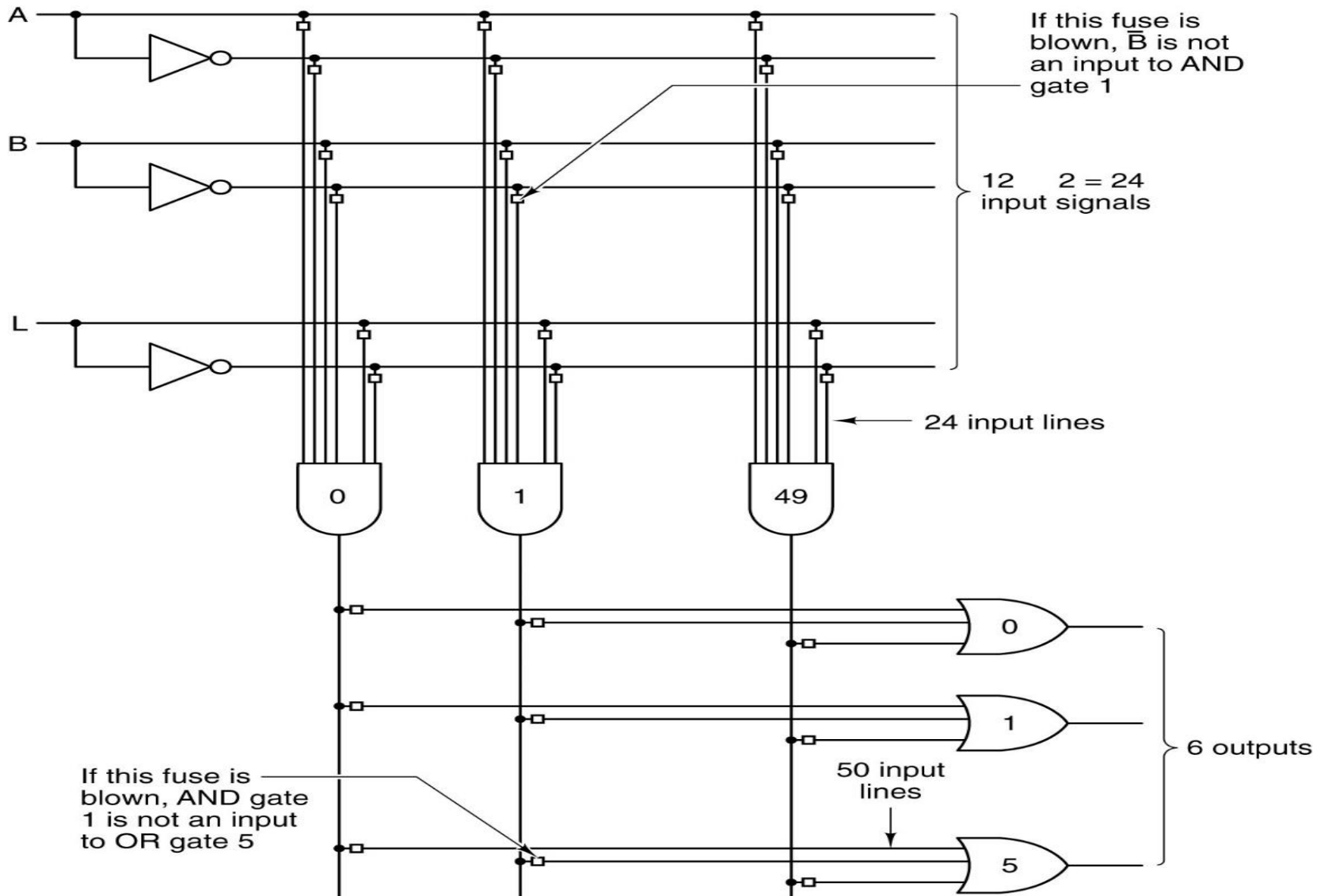
# 3-to-8 Decoder



# 4-bit Comparator



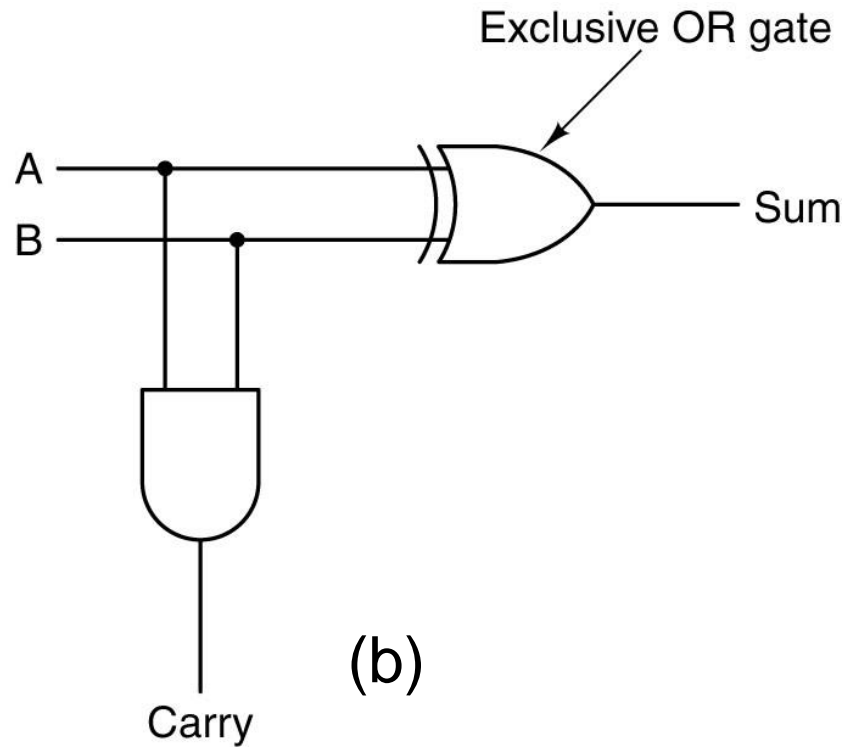
# 12-to-6 Programmable Logic Array (PLA)



# 1-bit Adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(a)

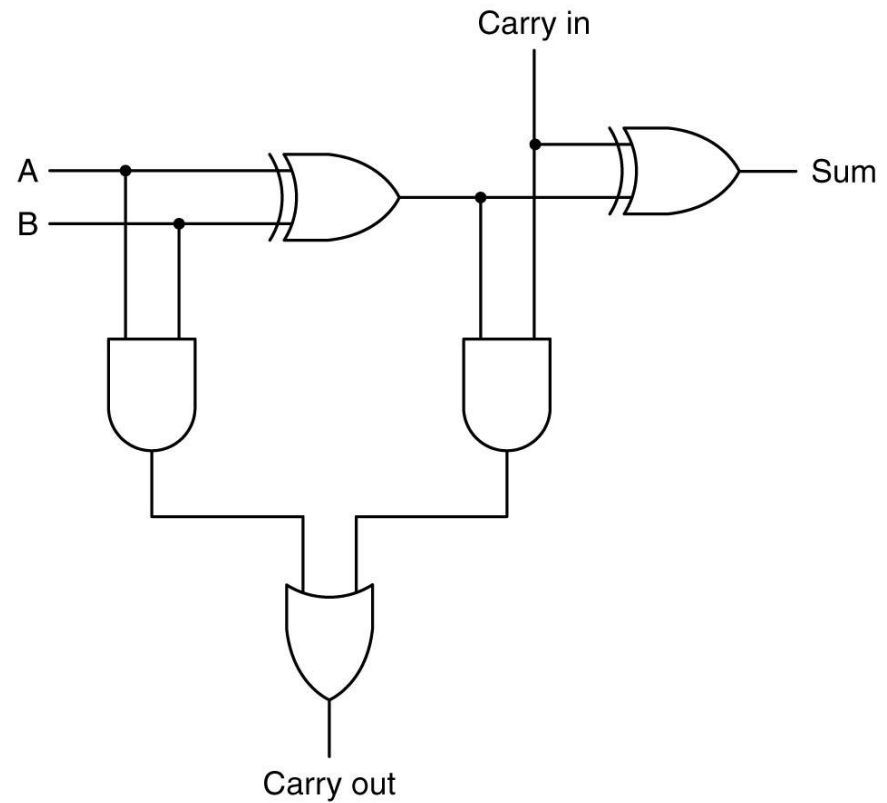


(b)

# 1-bit Full Adder

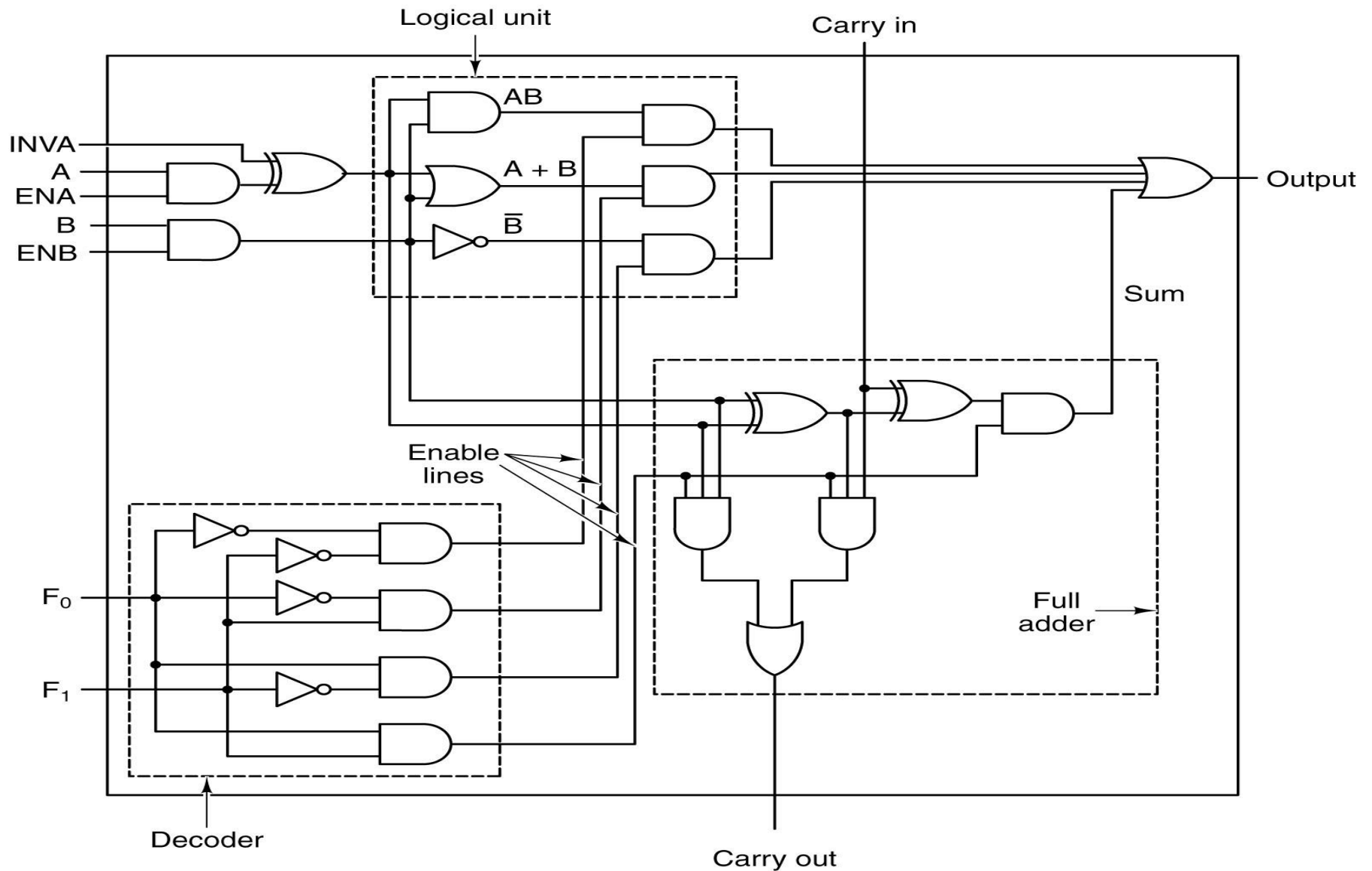
A	B	Carry in	Sum	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a)

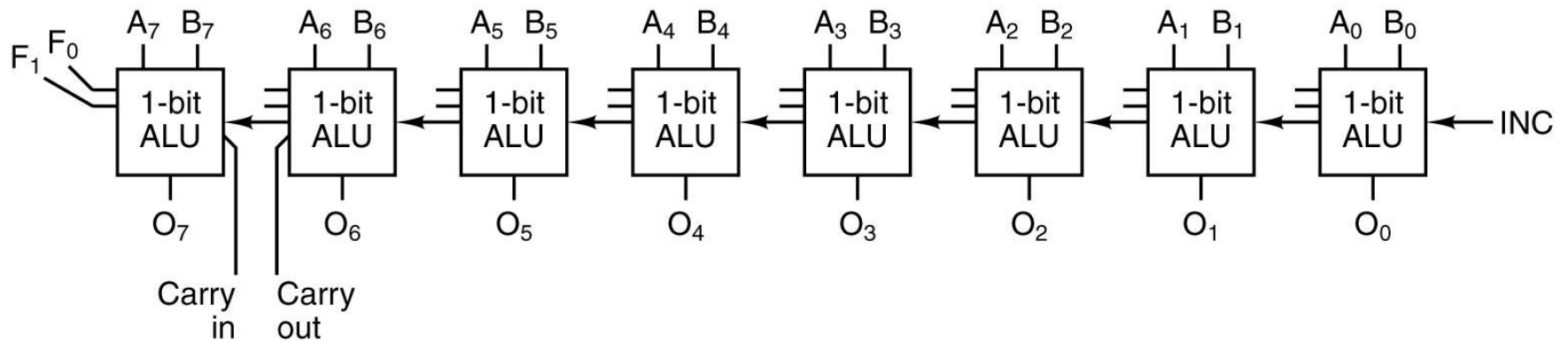


(b)

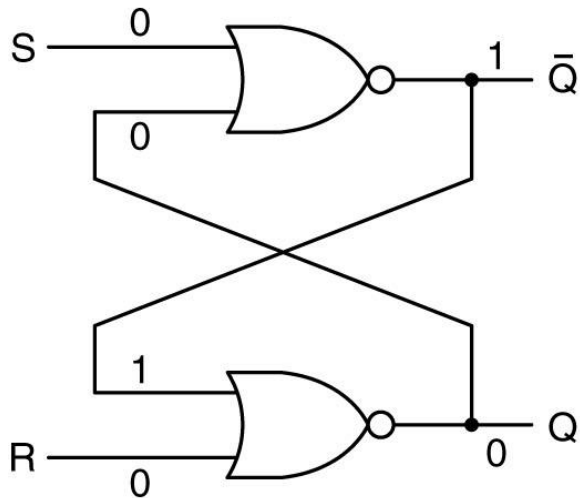
# 1-bit Arithmetic Logic Units (ALU)



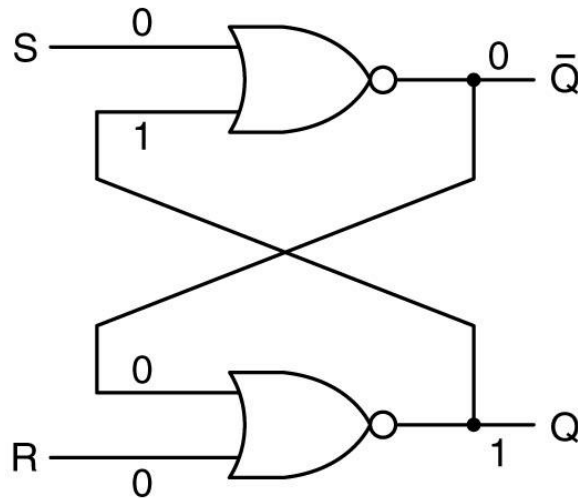
# Arithmetic Logic Unit (ALU)



# Latch



(a)



(b)

A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

(c)

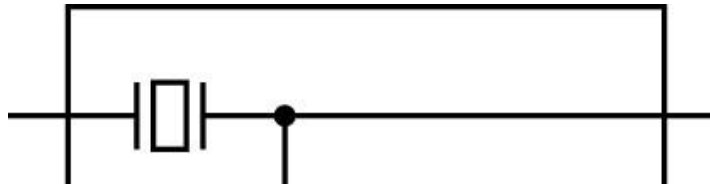
(a) NOR latch in state 0

(b) NOR latch in state 1

(c) Truth table for NOR latch



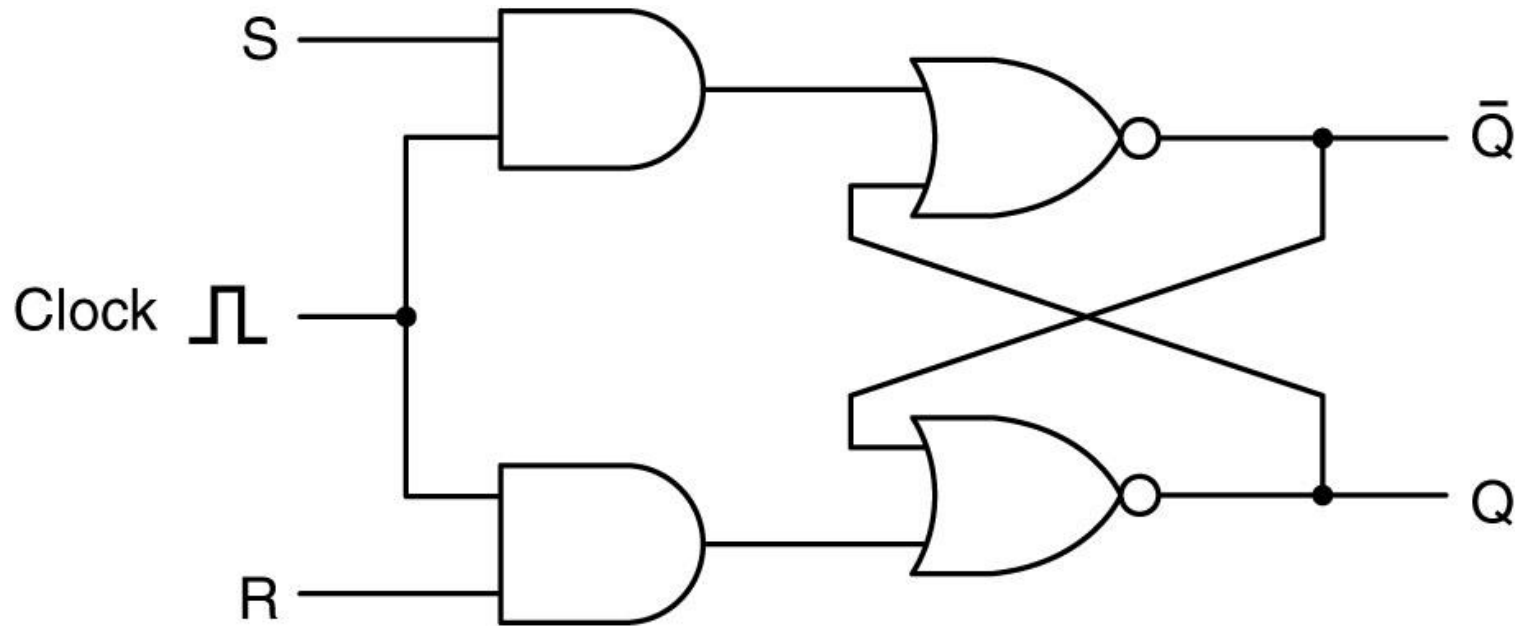
# Clock



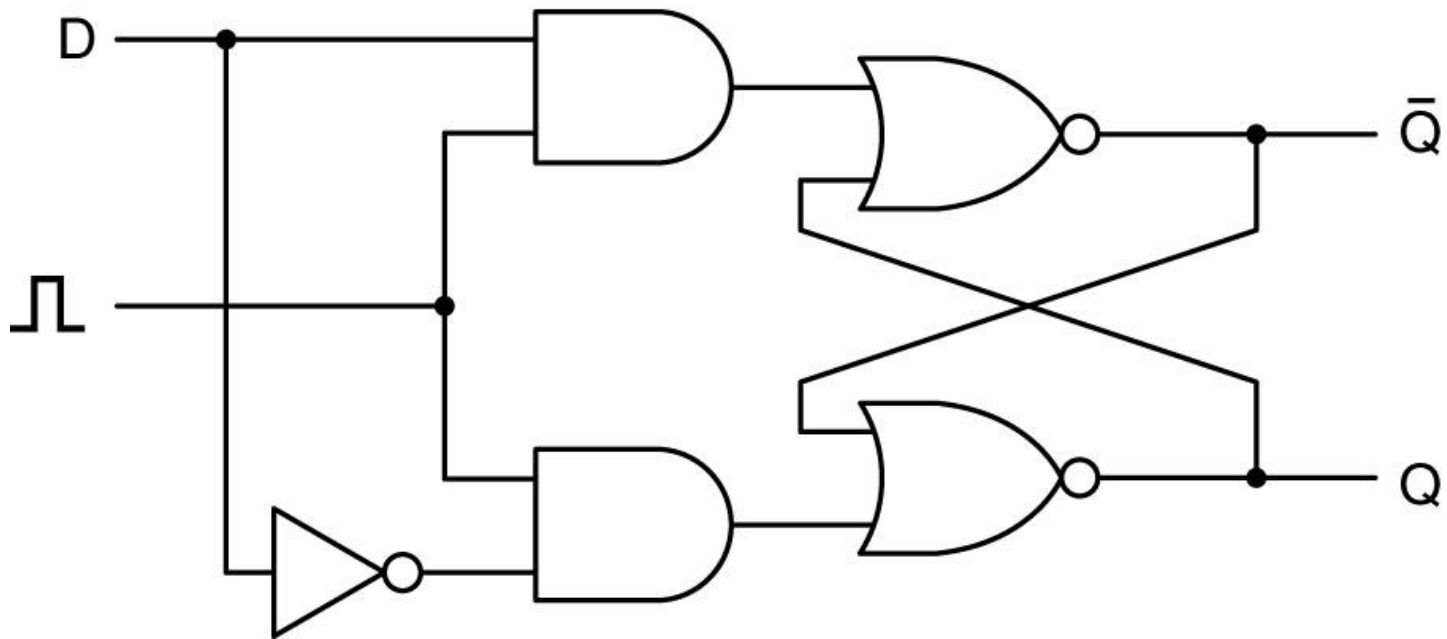
C1



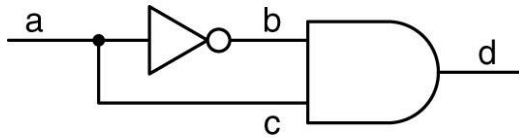
# Clocked SR Latch



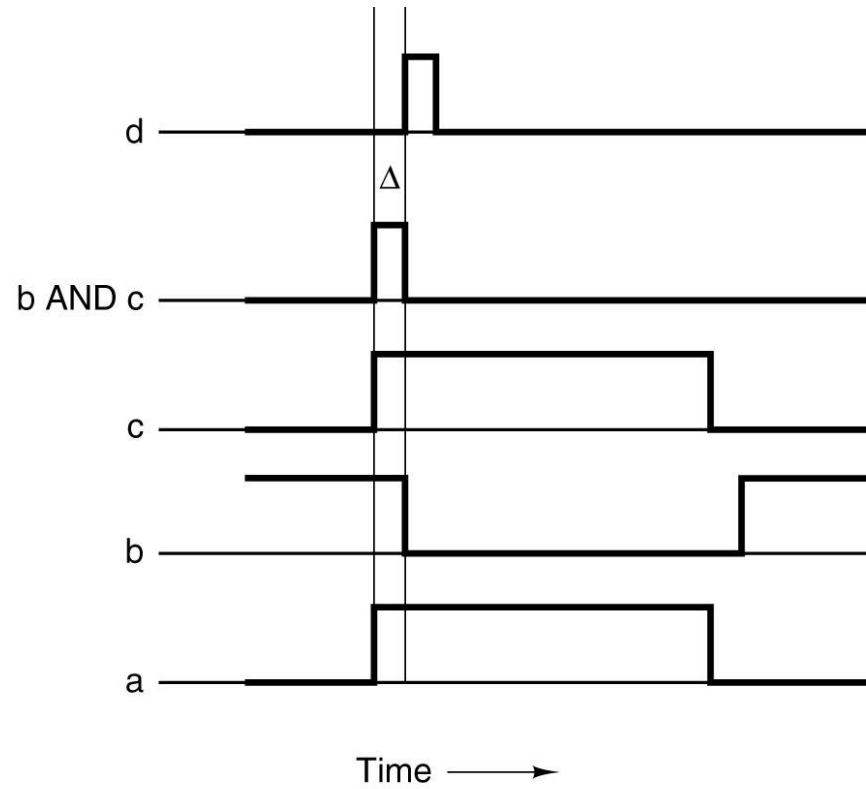
# D Latch



# Pulse Generator

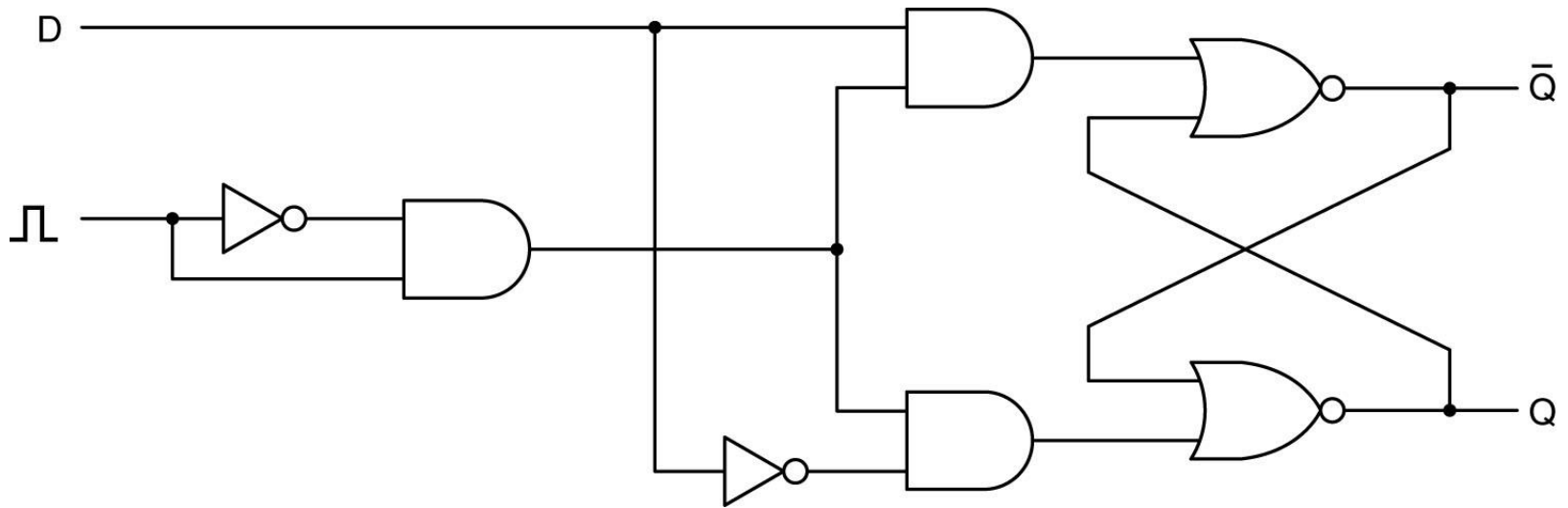


(a)

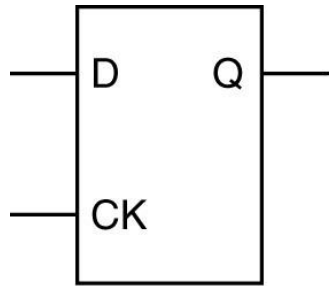


(b)

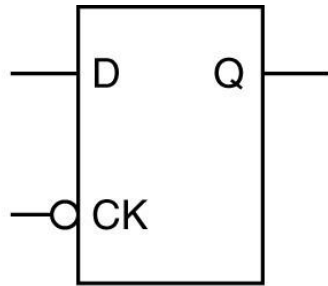
# D Flip-Flop



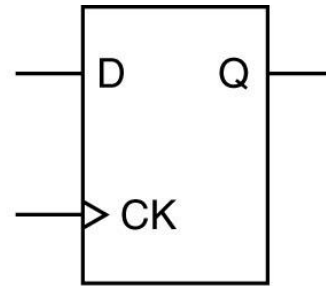
# Logic Notations for D Latch & D Flip-Flop



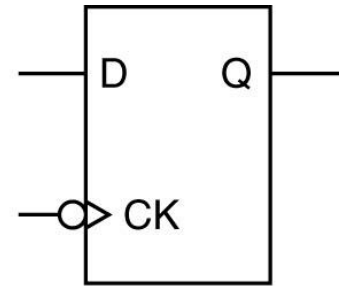
(a)



(b)

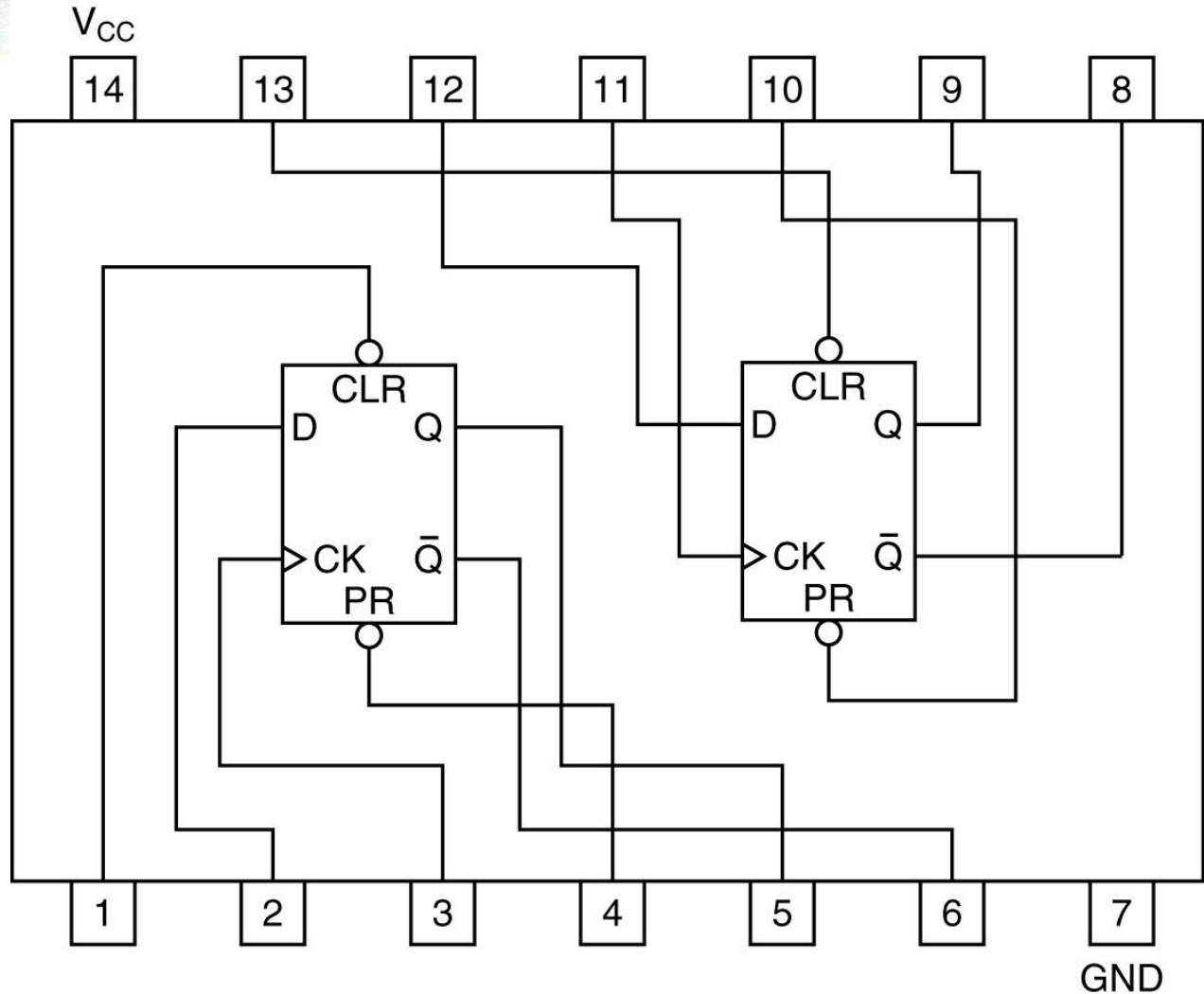
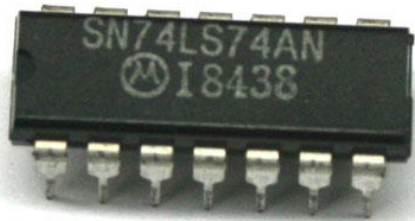


(c)



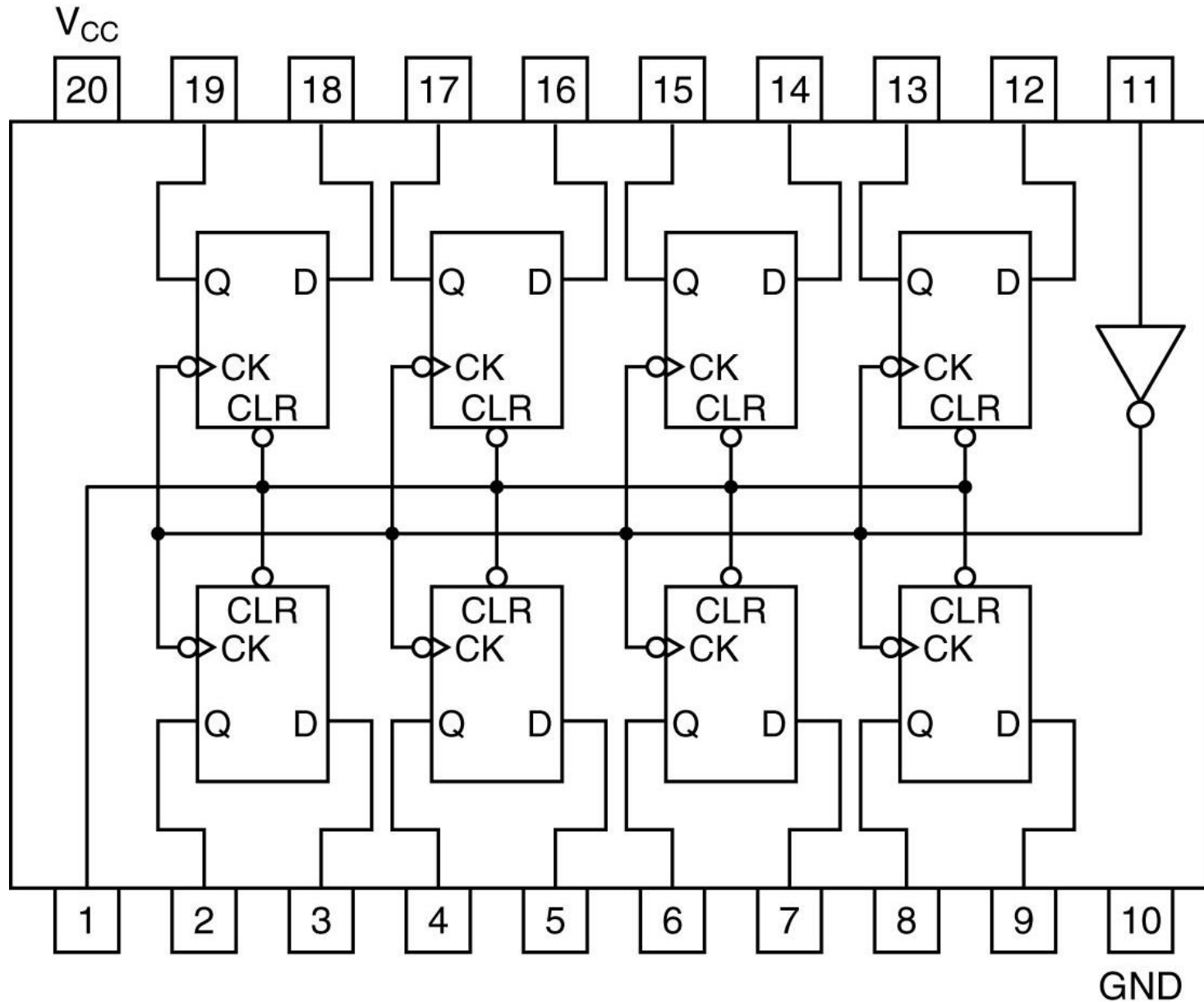
(d)

# Dual D Flip-Flop Chip with Preset/Clear



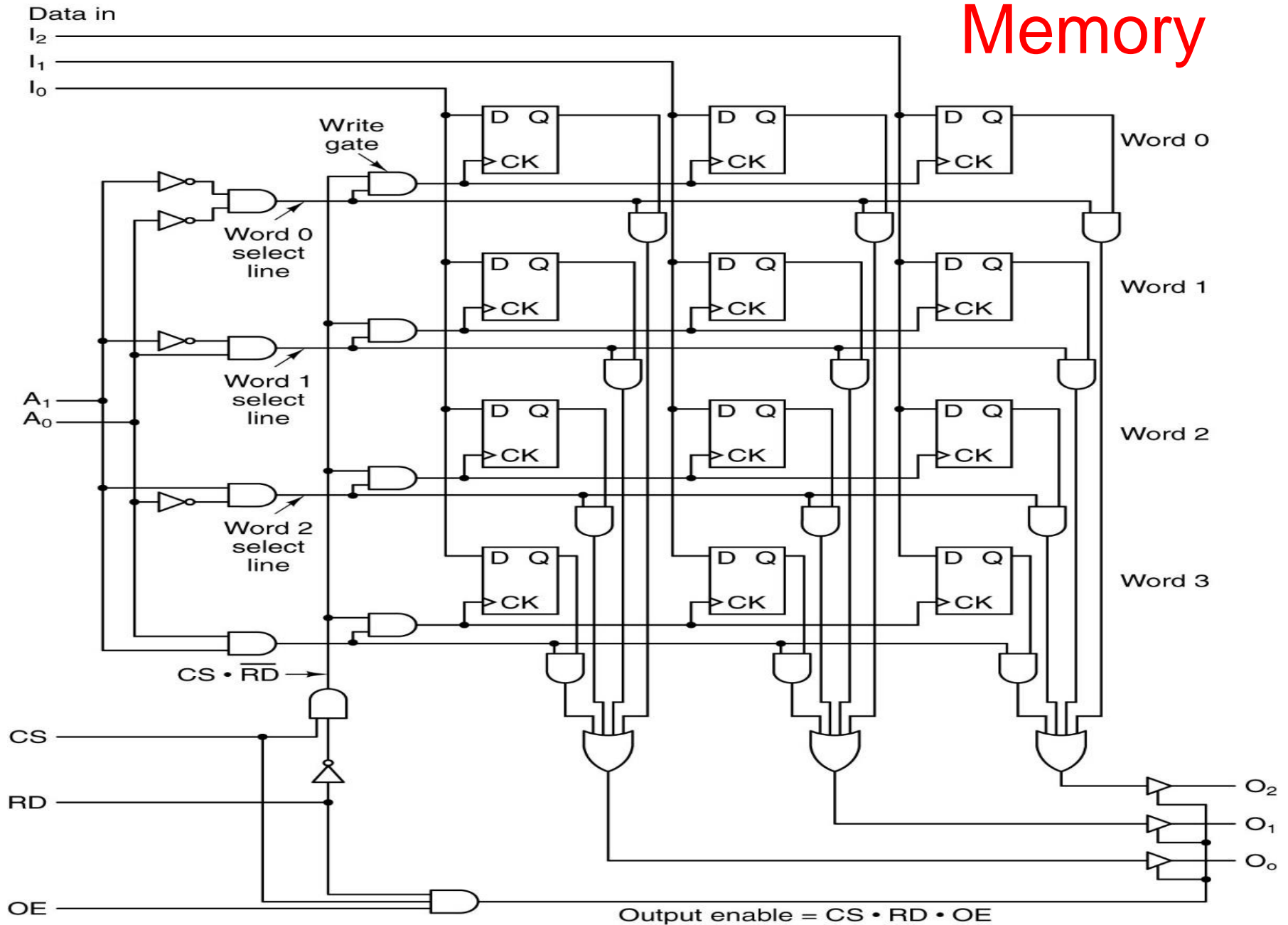
(a)

# Octal D Flip-Flops with Clear

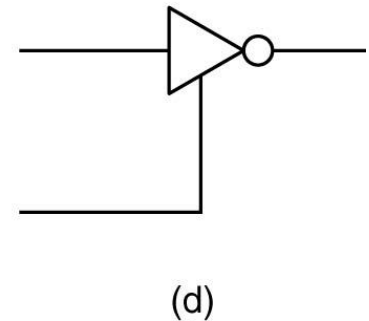
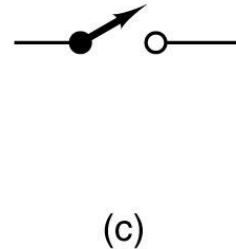
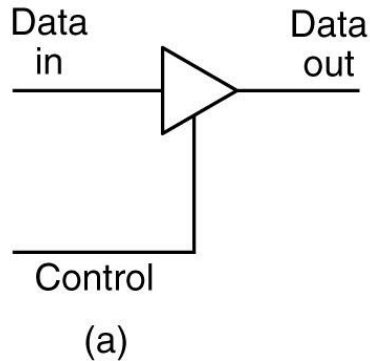




# Memory



# Buffer



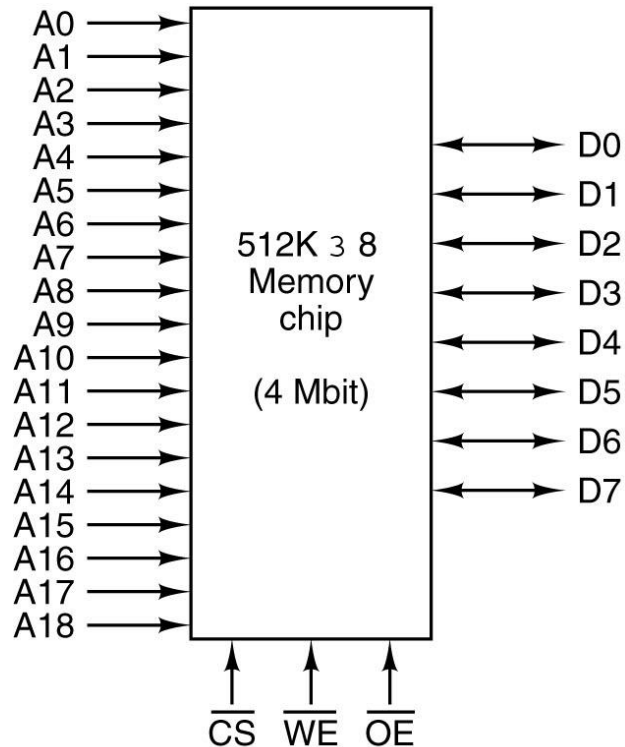
(a) A noninverting buffer.

(b) Effect of (a) when control is high.

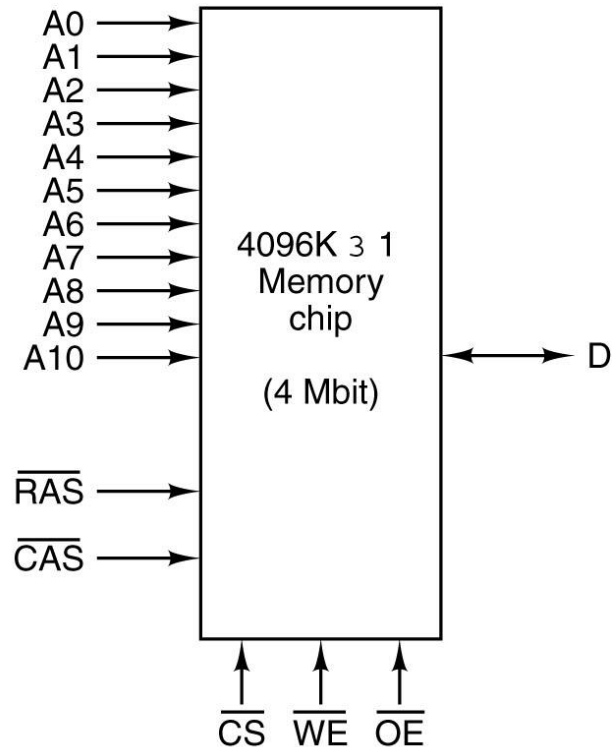
(c) Effect of (a) when control is low.

(d) An inverting buffer.

# Memory Chips (1)



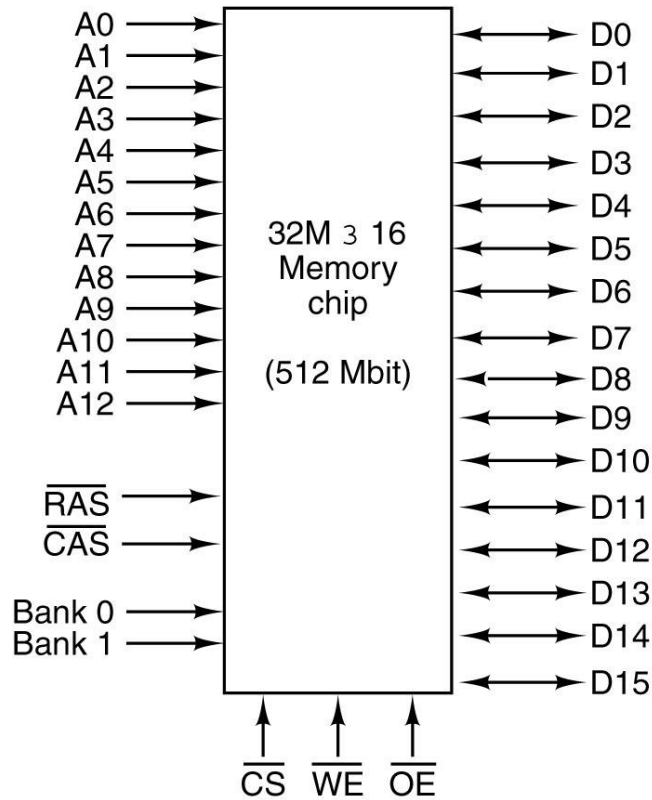
(a)



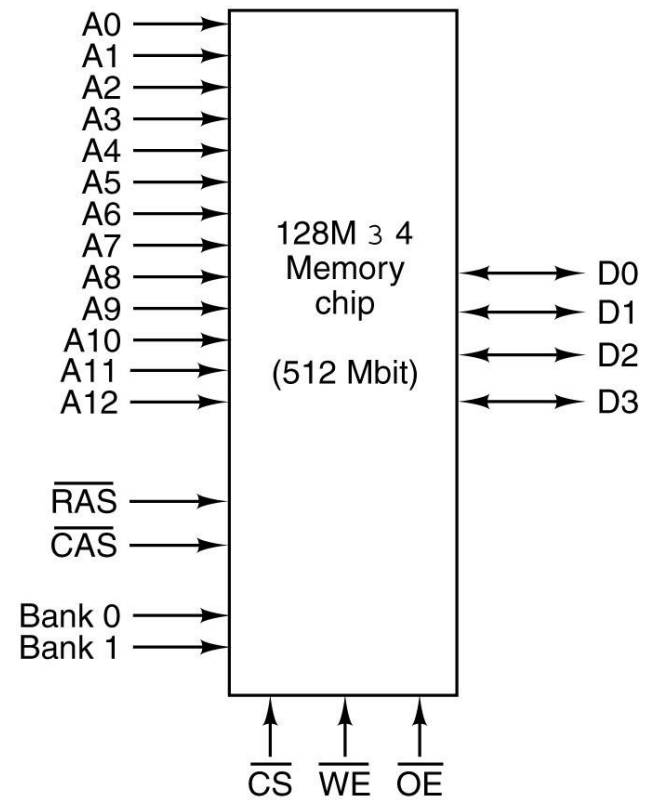
(b)

Two ways of organizing a 4-Mbit memory chip.

# Memory Chips (2)



(a)

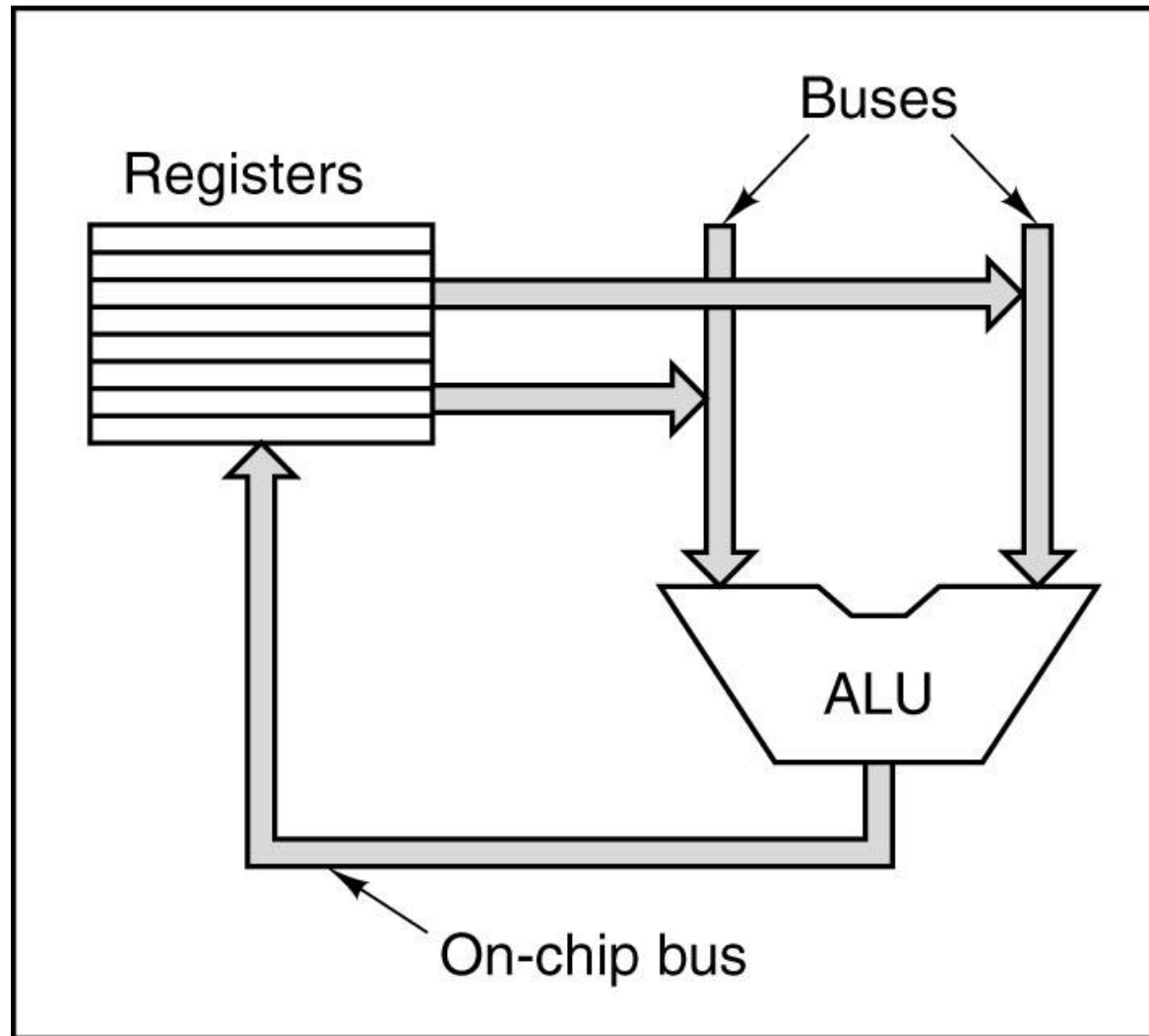


(b)

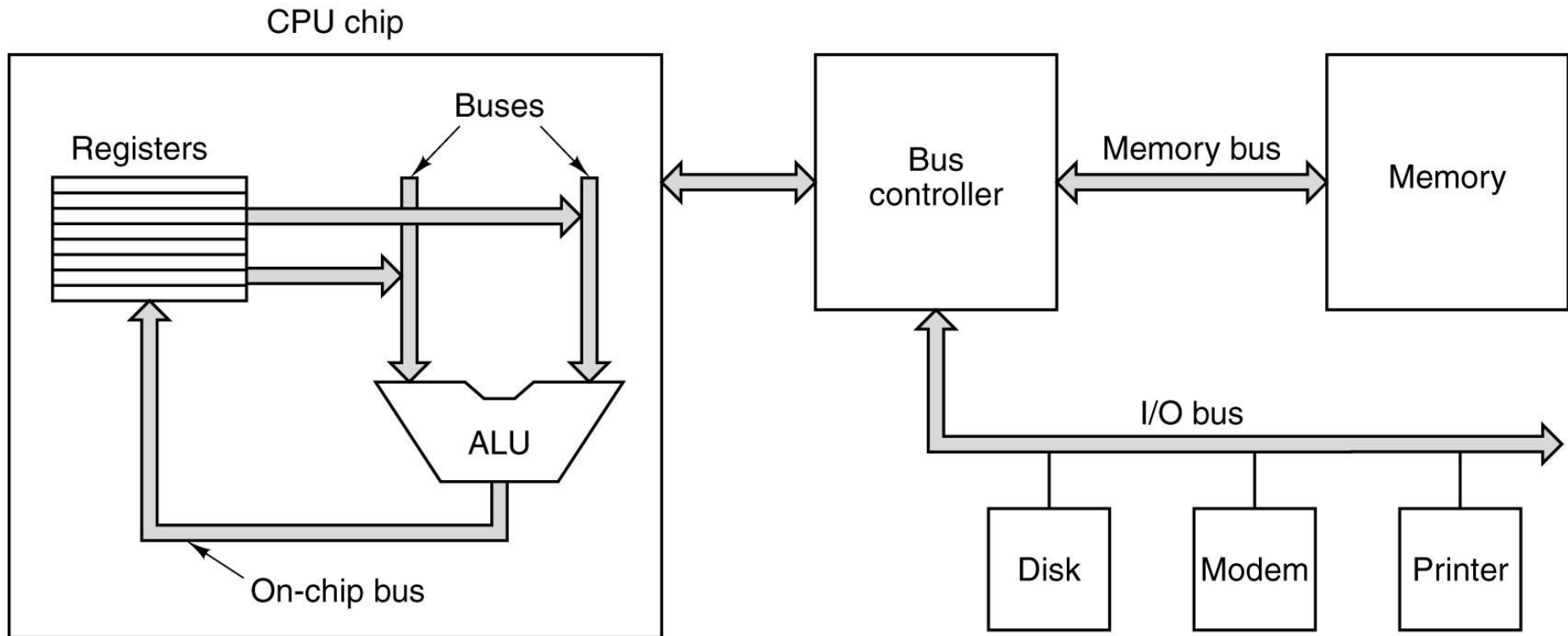
Two ways of organizing a 512 Mbit memory chip.

# Typical CPU

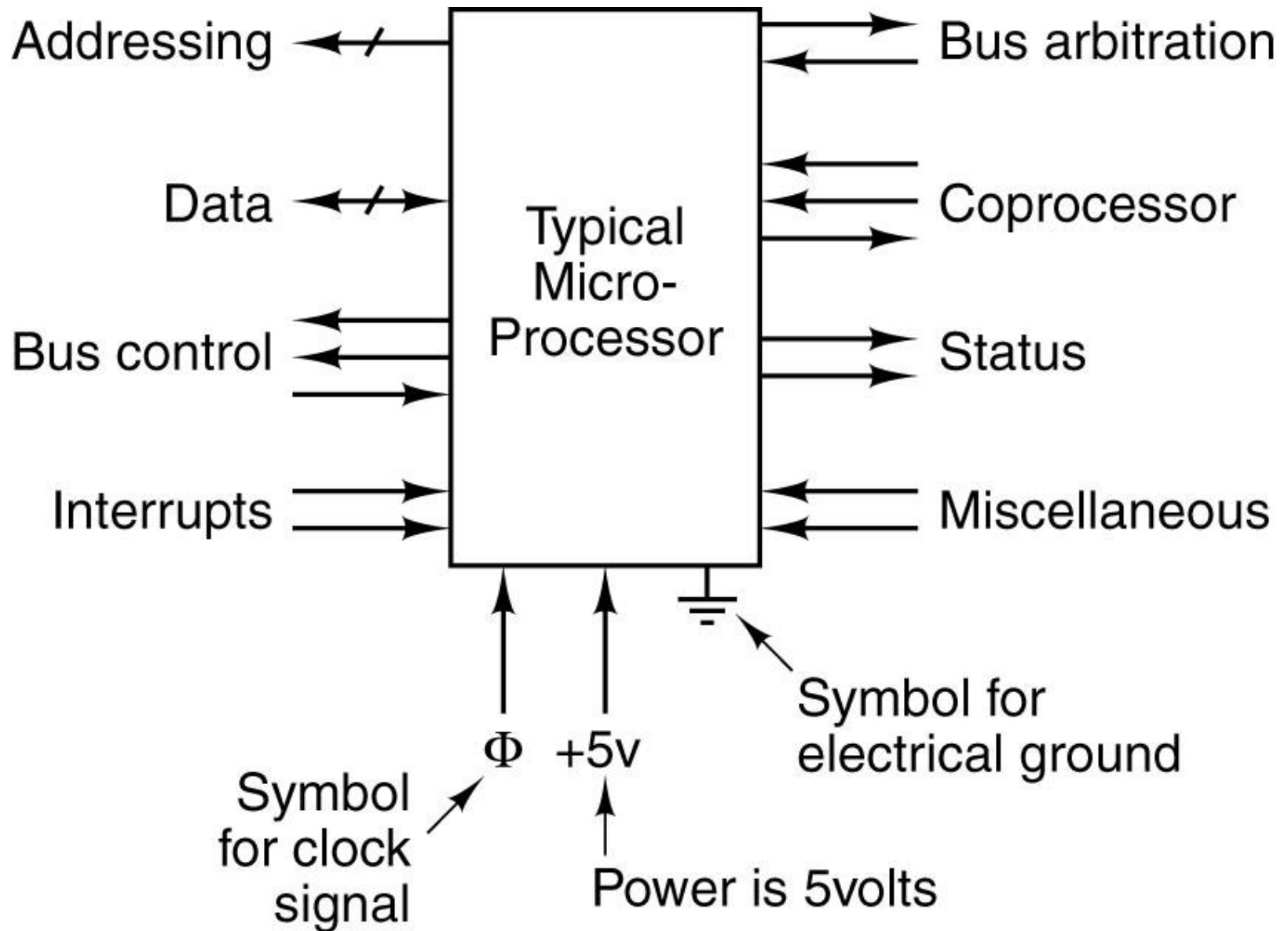
CPU chip



# Typical Computer System



# Microprocessor Chips

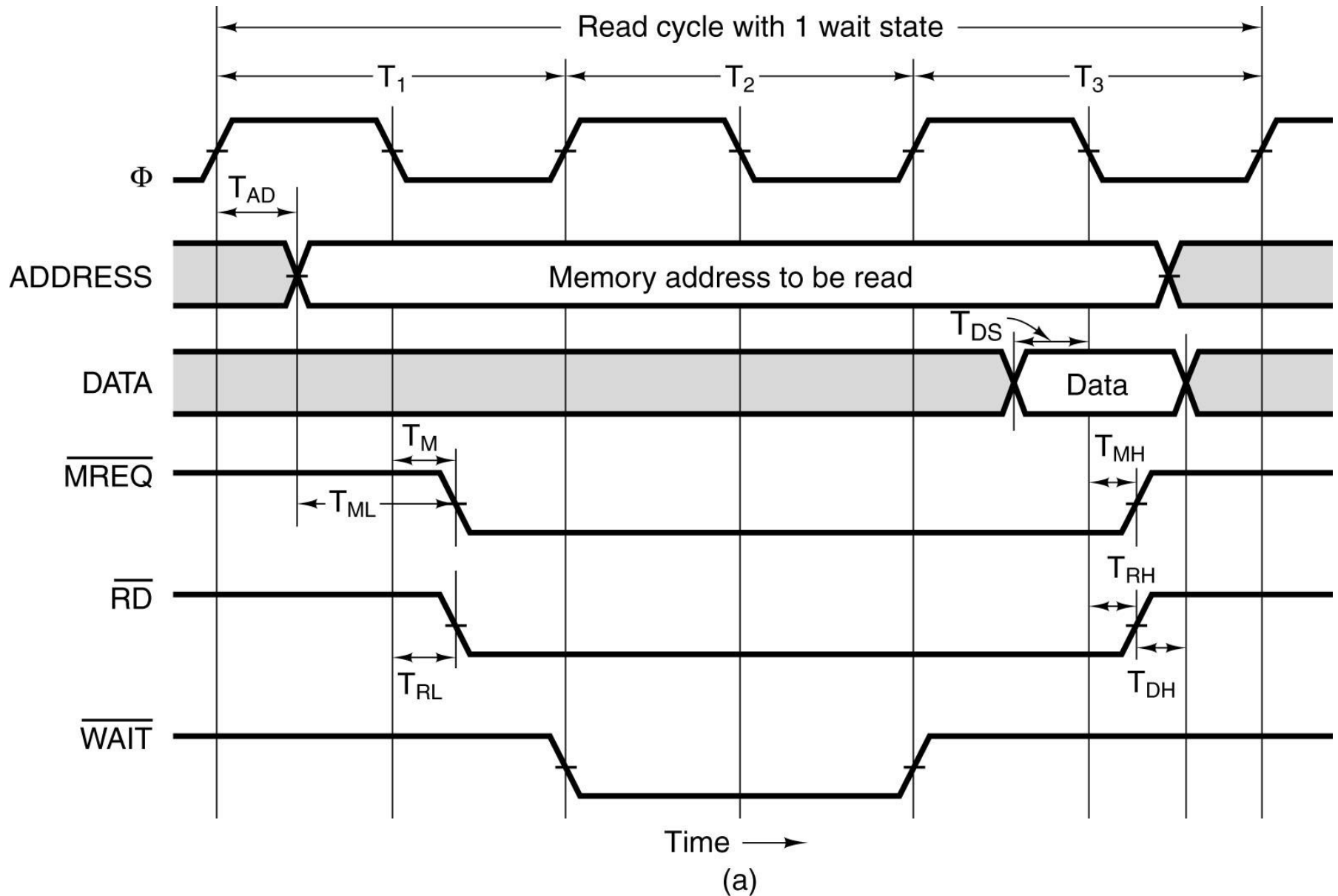


# Bus

Master	Slave	Example
CPU	Memory	Fetching instructions and data
CPU	I/O device	Initiating data transfer
CPU	Coprocessor	CPU handing instruction off to coprocessor
I/O	Memory	DMA (Direct Memory Access)
Coprocessor	CPU	Coprocessor fetching operands from CPU



# Synchronous Bus Timing

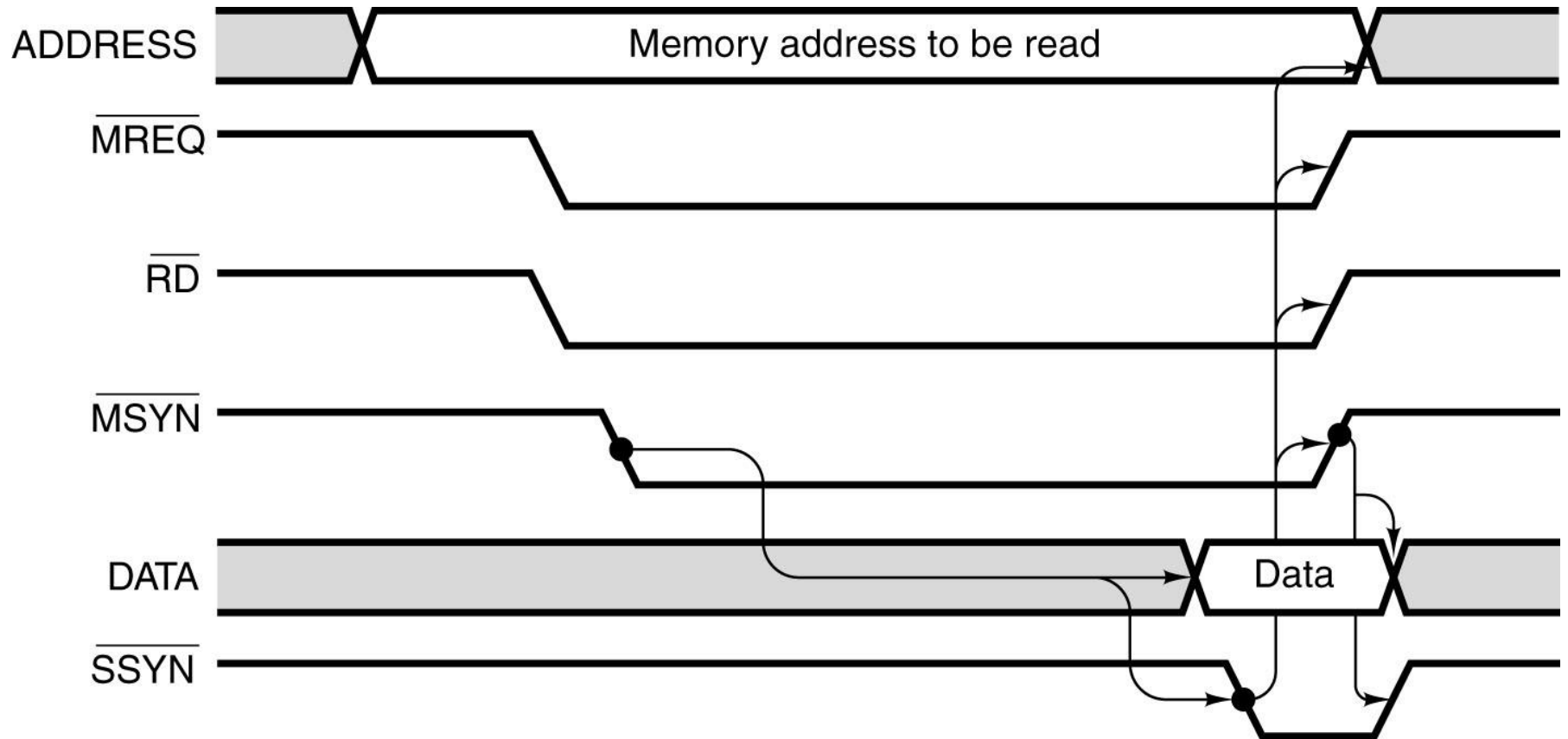


# Critical Times

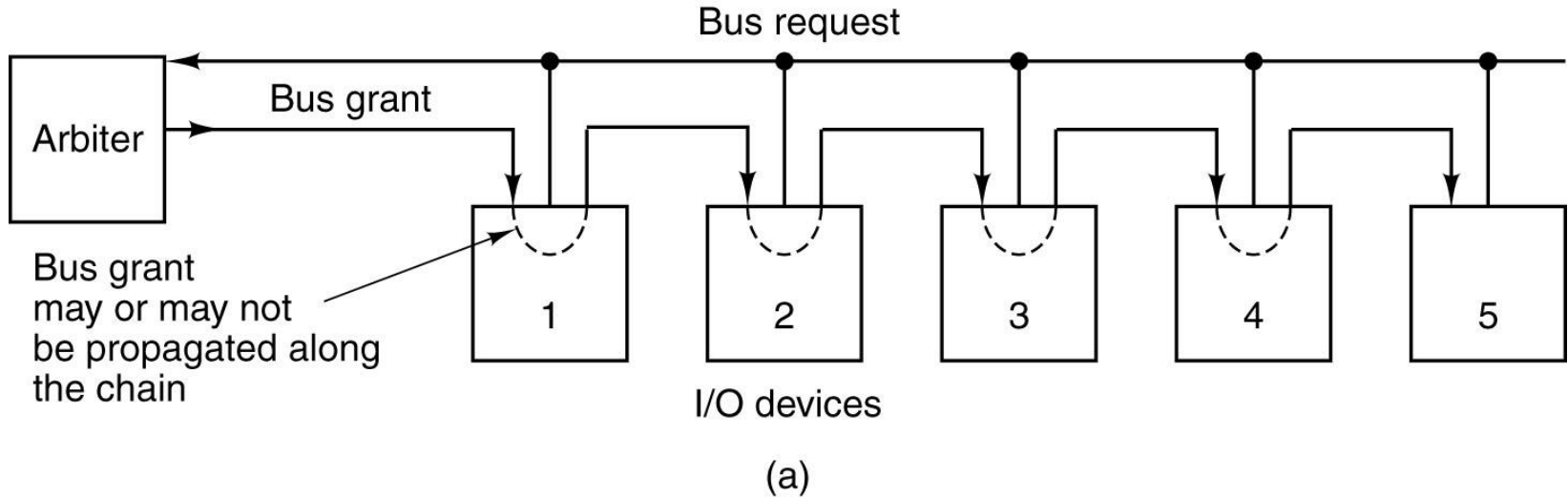
Symbol	Parameter	Min	Max	Unit
$T_{AD}$	Address output delay		4	nsec
$T_{ML}$	Address stable prior to $\overline{MREQ}$	2		nsec
$T_M$	$\overline{MREQ}$ delay from falling edge of $\Phi$ in $T_1$		3	nsec
$T_{RL}$	RD delay from falling edge of $\Phi$ in $T_1$		3	nsec
$T_{DS}$	Data setup time prior to falling edge of $\Phi$	2		nsec
$T_{MH}$	$\overline{MREQ}$ delay from falling edge of $\Phi$ in $T_3$		3	nsec
$T_{RH}$	$\overline{RD}$ delay from falling edge of $\Phi$ in $T_3$		3	nsec
$T_{DH}$	Data hold time from negation of $\overline{RD}$	0		nsec

(b)

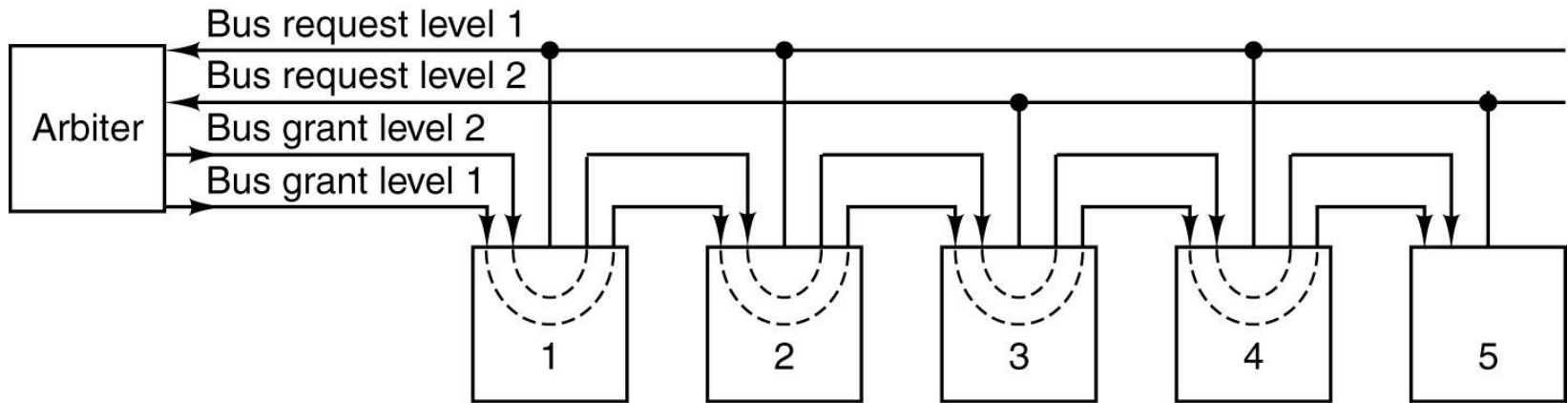
# Asynchronous Bus Timing



# Centralized Bus Arbitration (1 level)

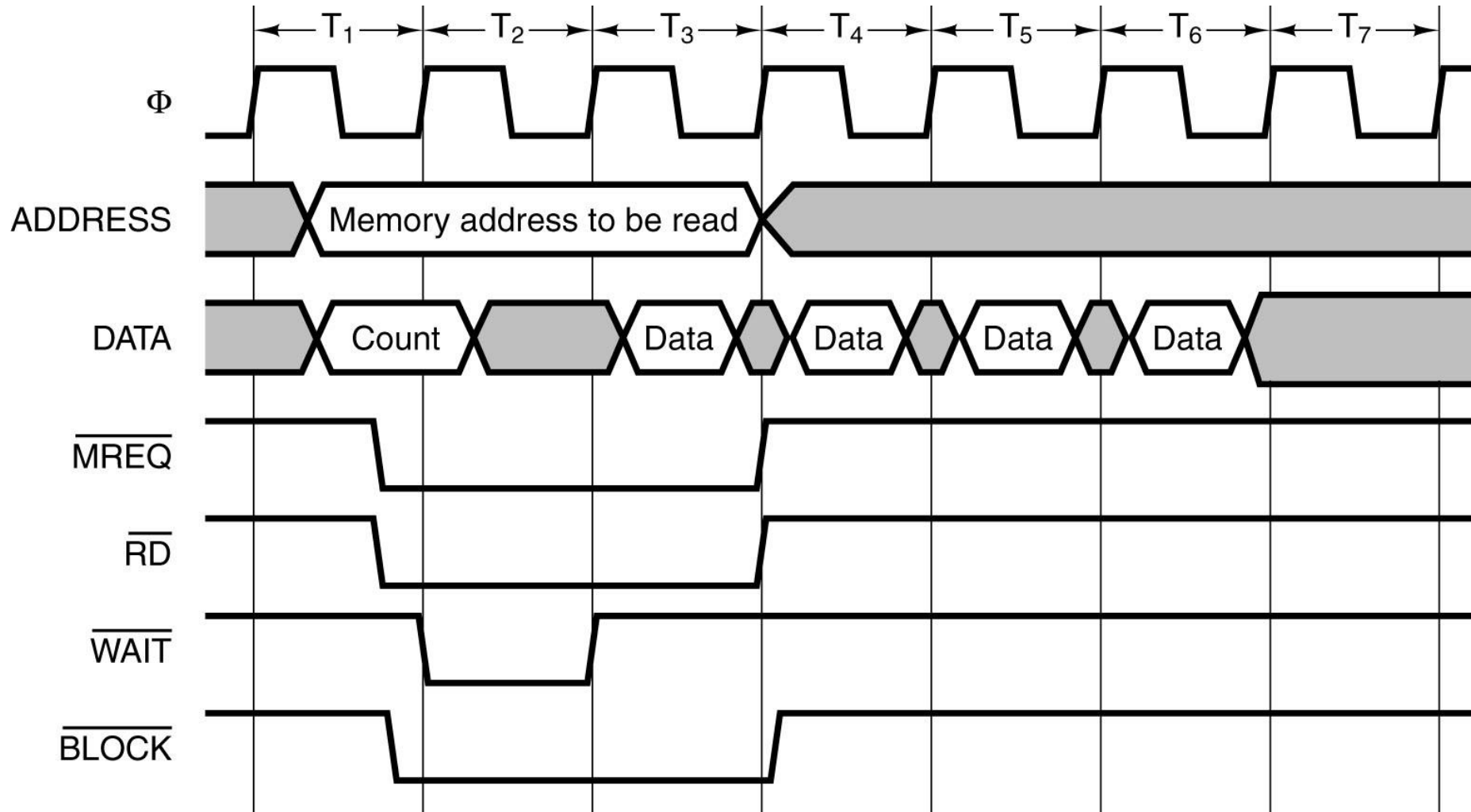


# Centralized Bus Arbitration (2 levels)

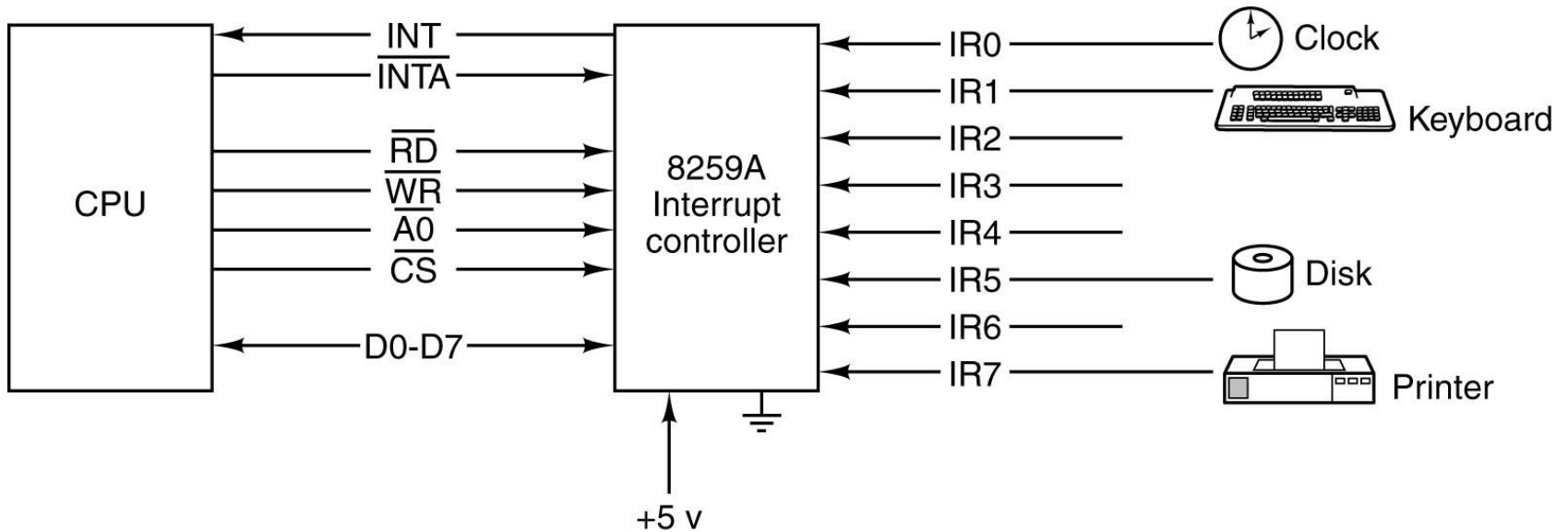


(b)

# Block Memory Access



# Typical Interrupt Controller



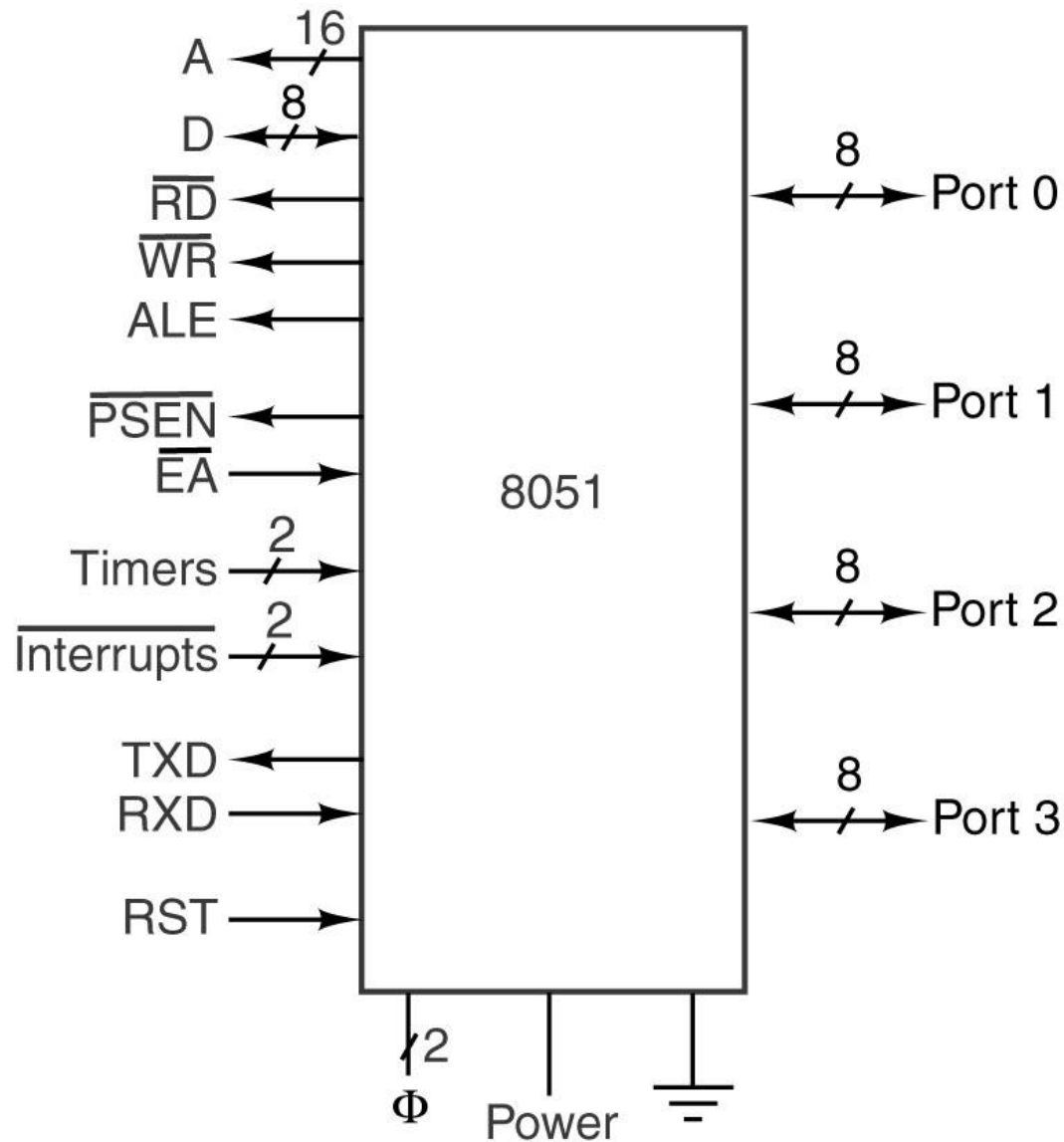
# Intel 8051 (Physical Pinout)

P1.0	1	40	VCC
P1.1	2	39	P0.0 / AD0
P1.2	3	38	P0.1 / AD1
P1.3	4	37	P0.2 / AD2
P1.4	5	36	P0.3 / AD3
P1.5	6	35	P0.4 / AD4
P1.6	7	34	P0.5 / AD5
P1.7	8	33	P0.6 / AD6
RST	9	32	P0.7 / AD7
RXD / P3.0	10	31	$\overline{EA}$ / VPP
TXD / P3.1	11	30	ALE
$\overline{INT0}$ / P3.2	12	29	$\overline{PSEN}$
$\overline{INT1}$ / P3.3	13	28	P2.7 / A15
TO / P3.4	14	27	P2.6 / A14
T1 / P3.5	15	26	P2.5 / A13
$\overline{WR}$ / P3.6	16	25	P2.4 / A12
$\overline{RD}$ / P3.7	17	24	P2.3 / A11
XTAL2	18	23	P2.2 / A10
XTAL1	19	22	P2.1 / A9
VSS	20	21	P2.0 / A8

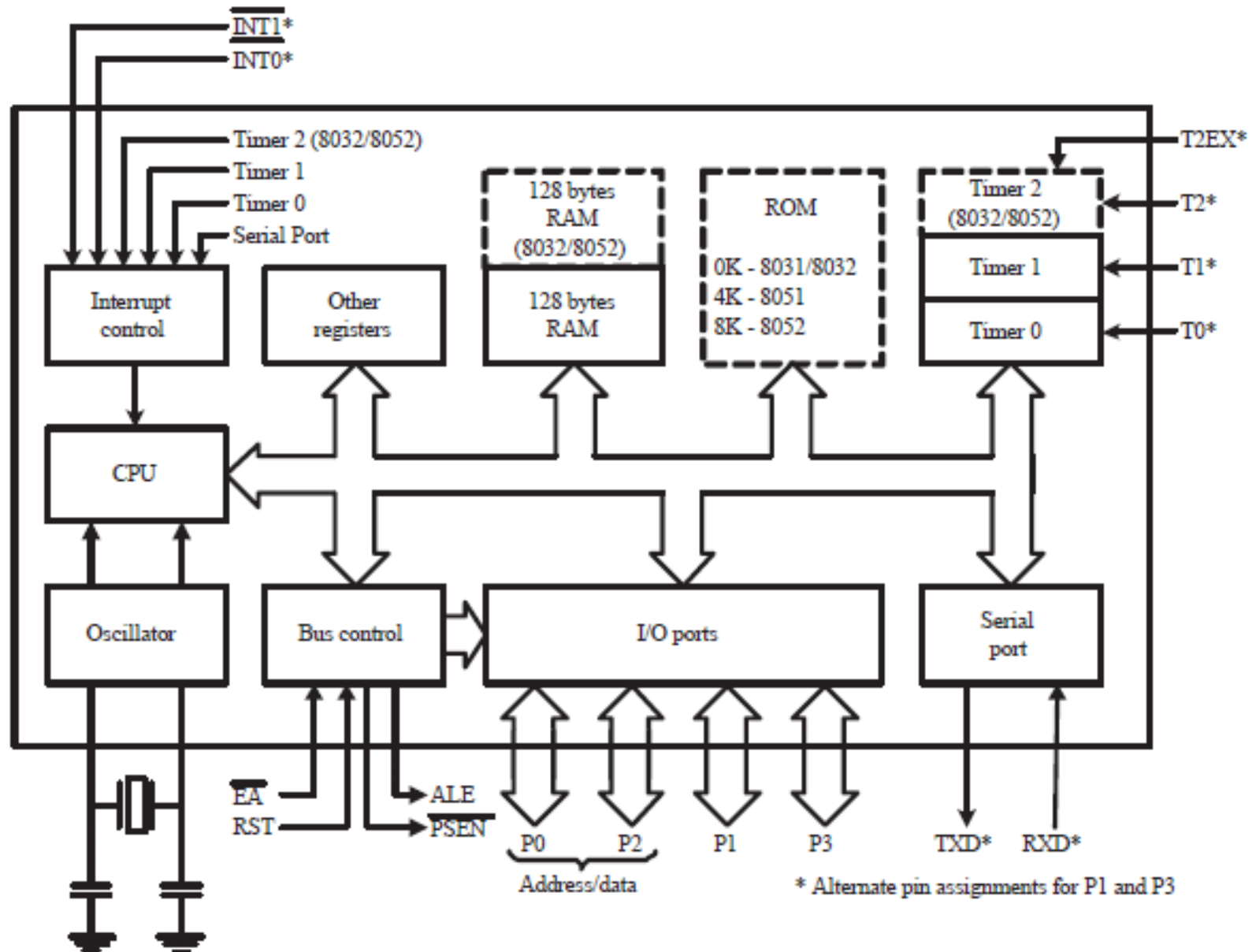




# Intel 8051 (Logical Pinout)



# Intel 8051 (Logical Block Diagram)



# Intel 8051 Memory Map

7F	General Purpose RAM (including the stack)							
...								
30								
2F	7F	7E	7D	7C	7B	7A	79	78
2E	77	76	75	74	73	72	71	70
2D	6F	6E	6D	6C	6B	6A	69	68
2C	67	66	65	64	63	62	61	60
2B	5F	5E	5D	5C	5B	5A	59	58
2A	57	56	55	54	53	52	51	50
29	4F	4E	4D	4C	4B	4A	49	48
28	47	46	45	44	43	42	41	40
27	3F	3E	3D	3C	3B	3A	39	38
26	37	36	35	34	33	32	31	30
25	2F	2E	2D	2C	2B	2A	29	28
24	27	26	25	24	23	22	21	20
23	1F	1E	1D	1C	1B	1A	19	18
22	17	16	15	14	13	12	11	10
21	0F	0E	0D	0C	0B	0A	09	08
20	07	06	05	04	03	02	01	00
1F	Register Bank 3							
...								
18								
17	Register Bank 2							
...								
10								
0F	Register Bank 1							
...								
08								
07	Register Bank 0							
...								
00								

128 Bytes (00 to 7F)

Byte Address

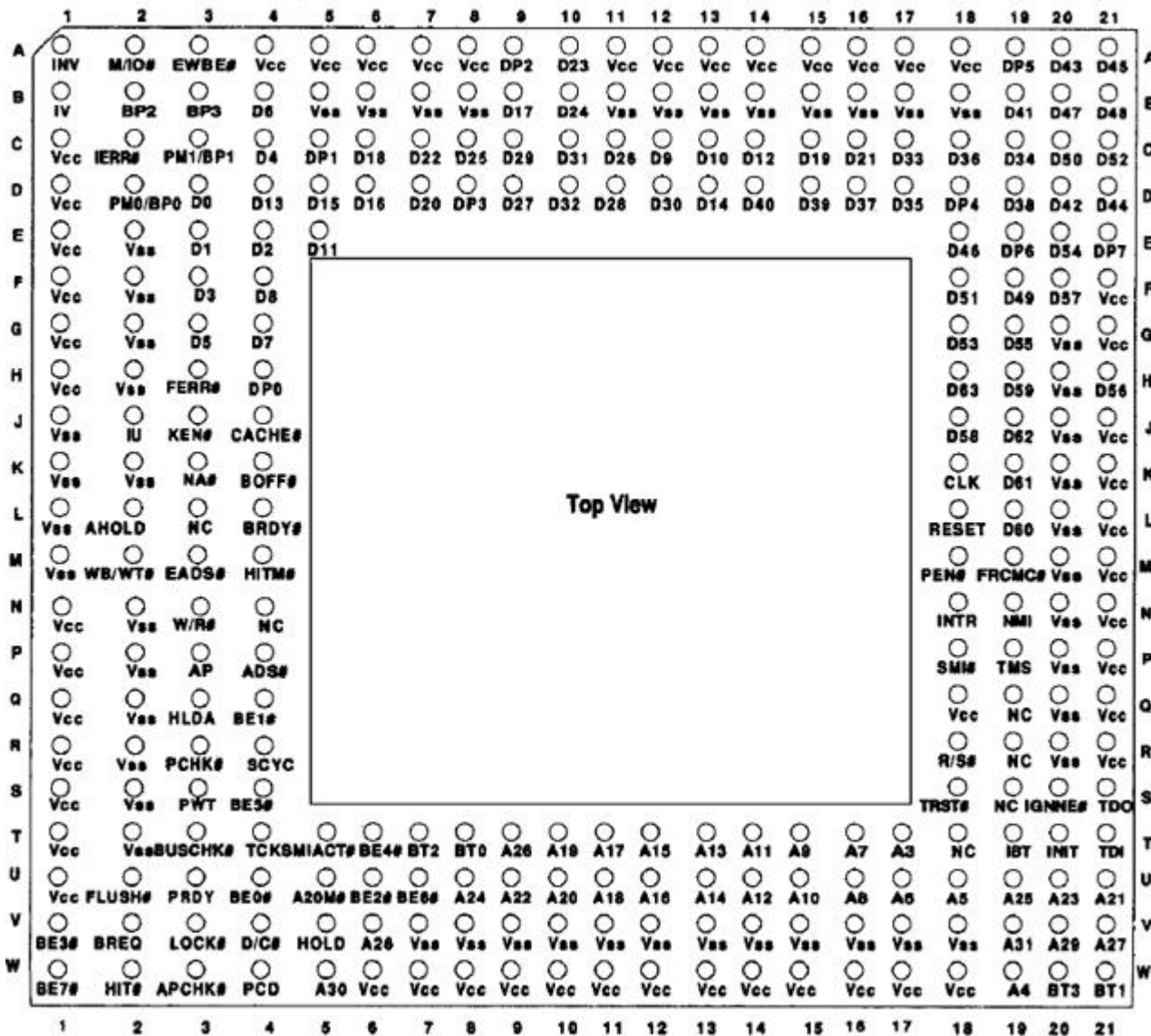
Bit Address

...										
F0	F7	F6	F5	F4	F3	F2	F1	F0	B	
...										
E0	E7	E6	E5	E4	E3	E2	E1	E0	ACC	
...										
D0	D7	D6	D5	D4	D3	D2	D1	D0	PSW	
...										
B8	BF	BE	BD	BC	BB	BA	B9	B8	IP	
...										
B0	B7	B6	B5	B4	B3	B2	B1	B0	P3	
...										
A8	AF	AE	AD	AC	AB	AA	A9	A8	IE	
...										
A0	A7	A6	A5	A4	A3	A2	A1	A0	P2	
...										
99										SBUF
98	9F	9E	9D	9C	9B	9A	99	98	SCON	
...										
90	97	96	95	94	93	92	91	90	P1	
...										
8D										TH1
8C										TH0
8B										TL1
8A										TL0
89										TMOD
88	8F	8E	8D	8C	8B	8A	89	88	TCON	
87										PCON
...										
83										DPH
82										DPL
81										SP
80	87	86	85	84	83	82	81	80	P0	

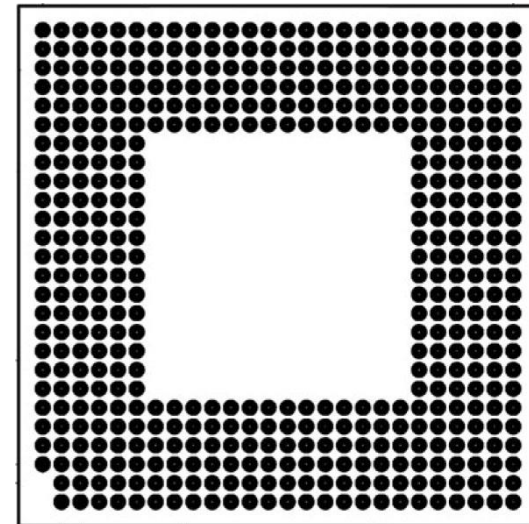
128 Bytes (80 to FF) - the SFRs

Unused in the 8051

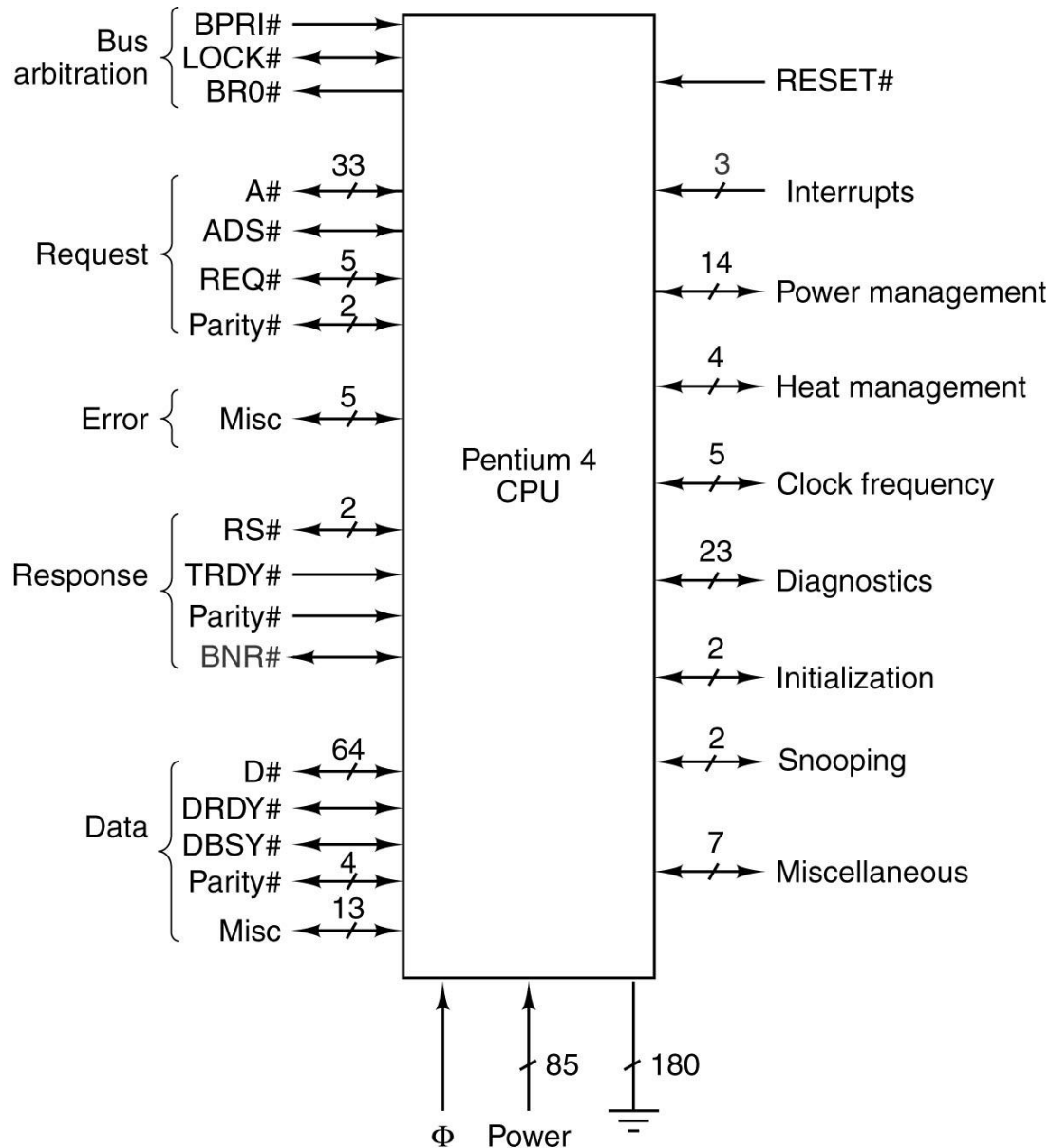
# Intel Pentium 4 (Physical Pinout)



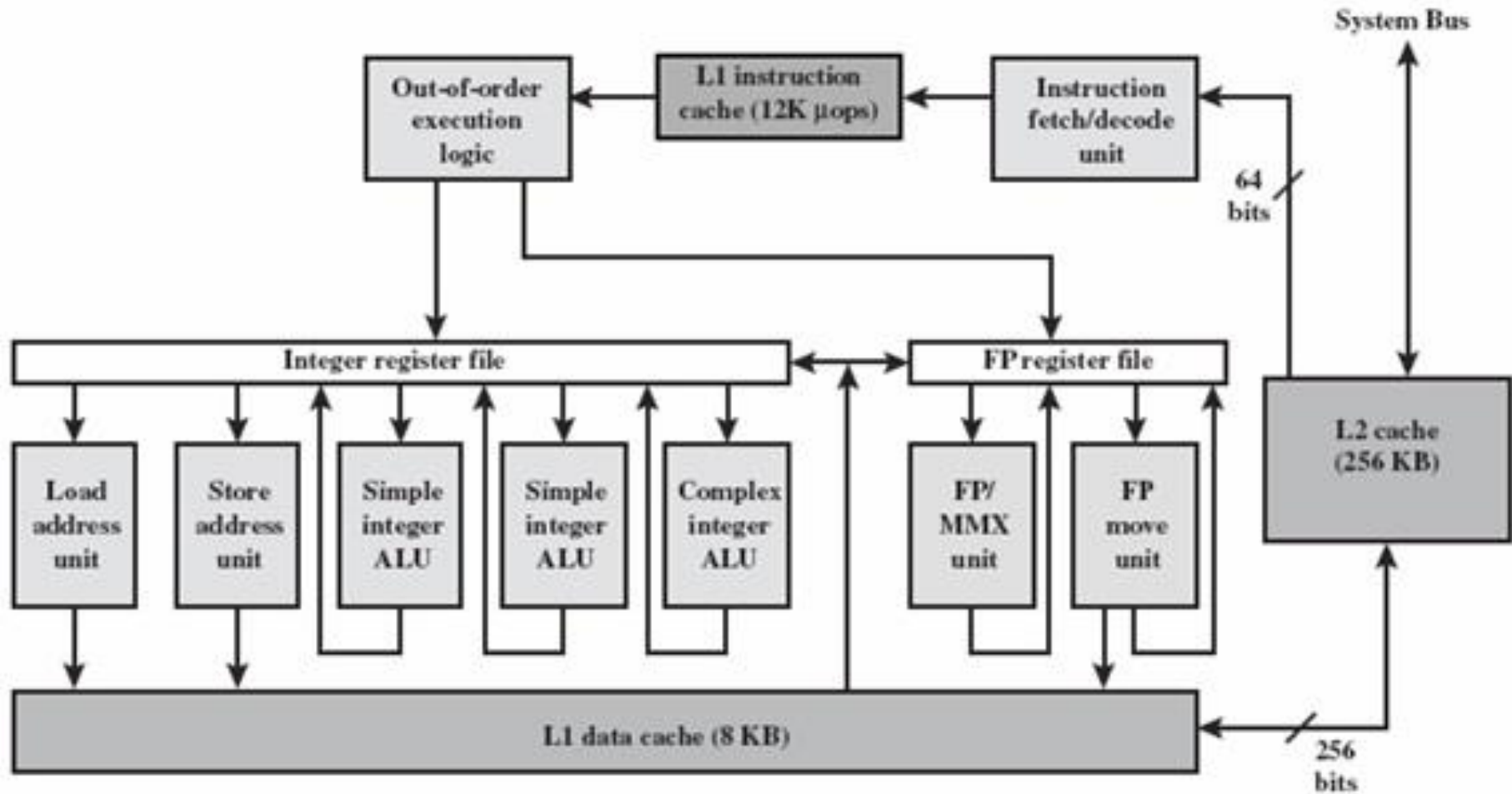
35 mm



# Intel Pentium 4 (Logical Pinout)

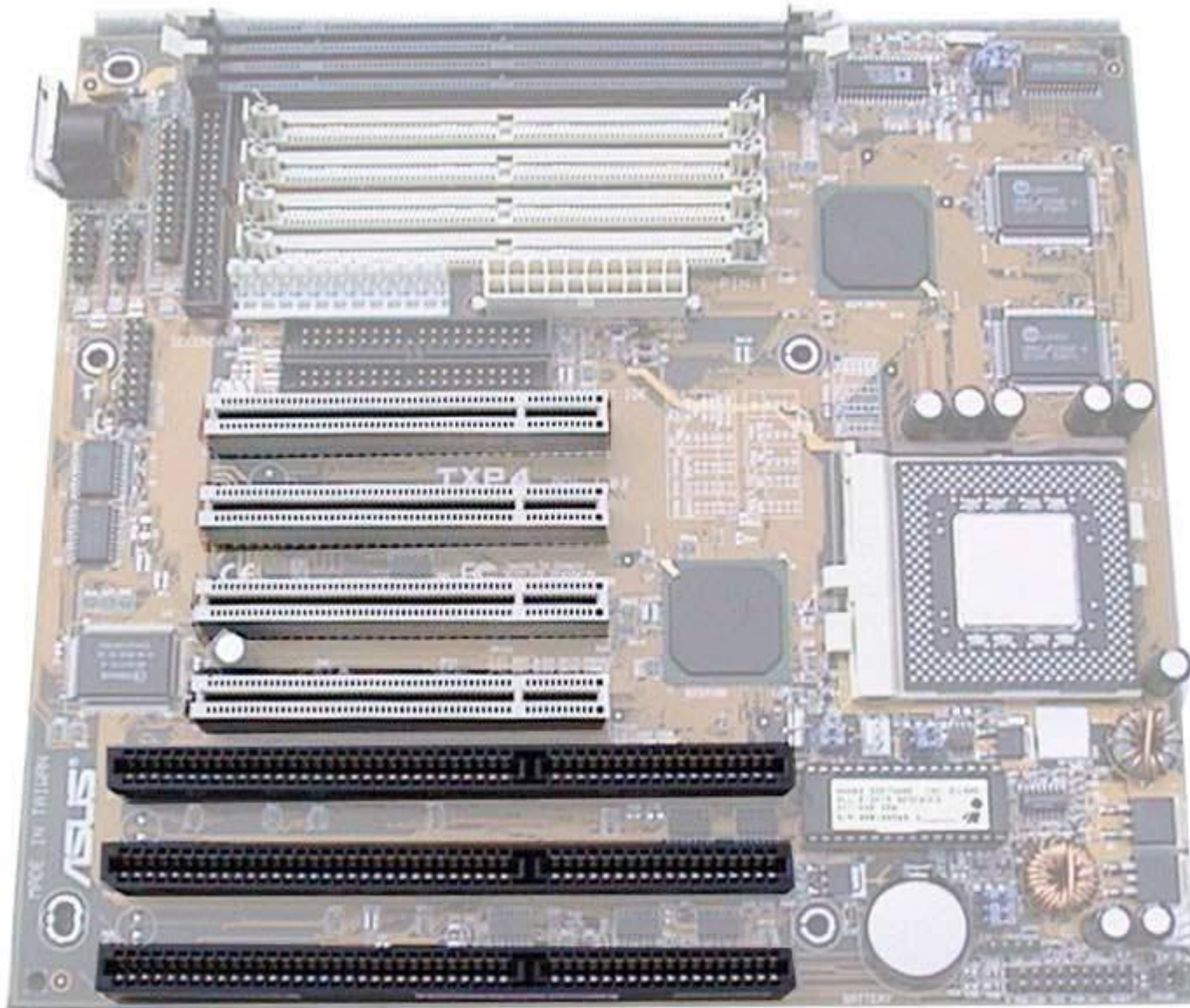


# Intel Pentium 4 (Logical Block Diagram)





# The PCI Bus – The ISA Bus

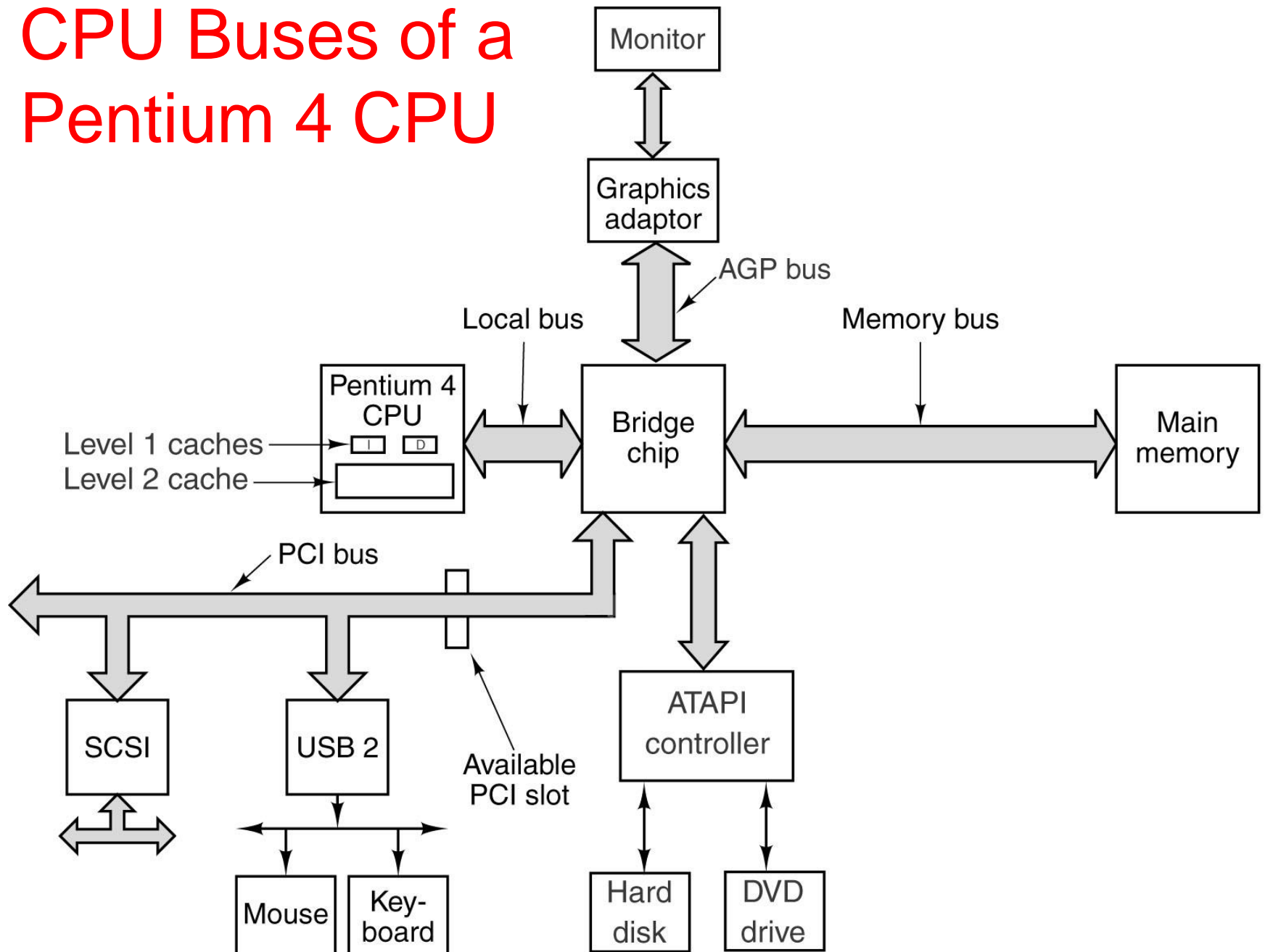


# A Typical PCI Bus External Peripheral

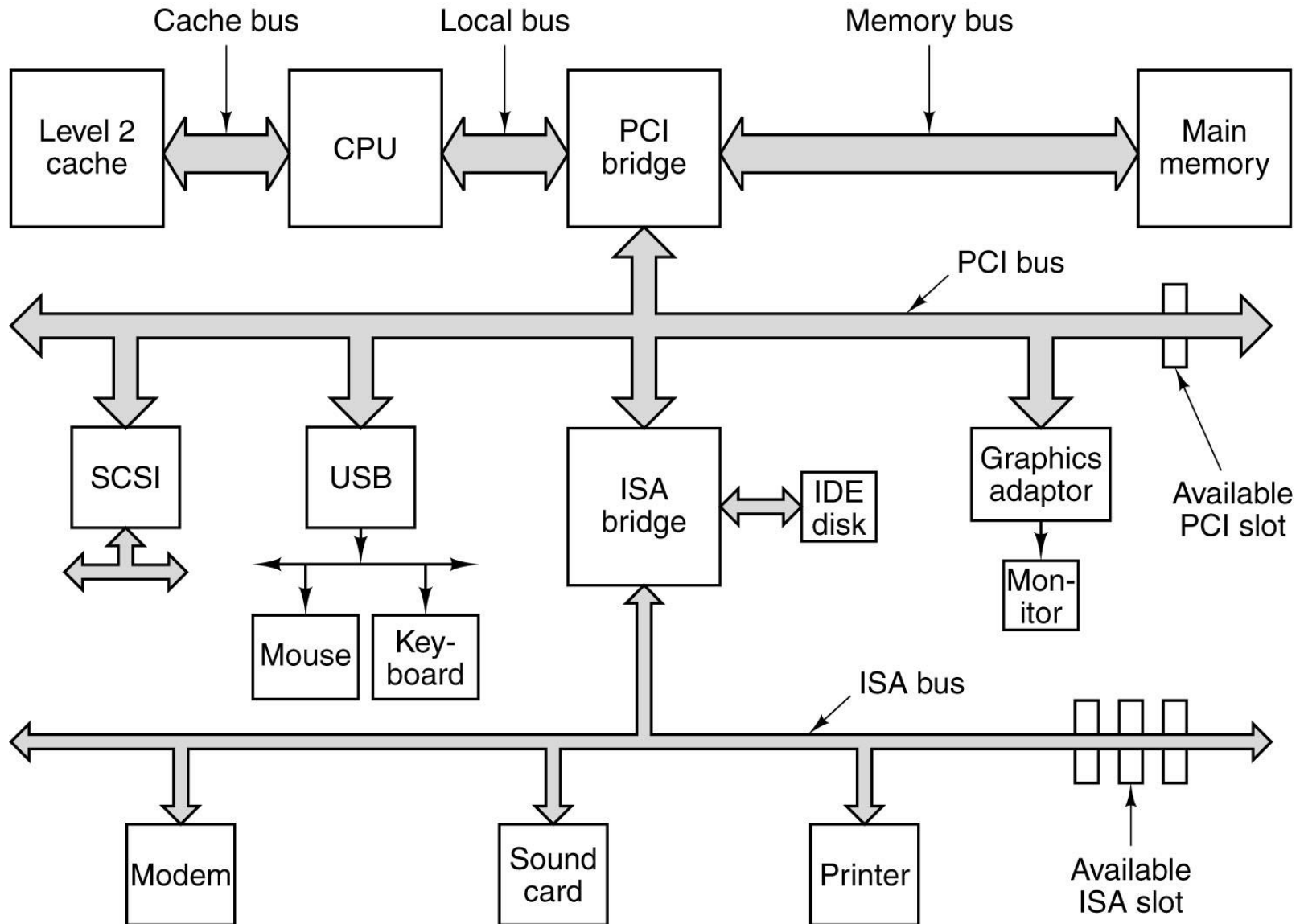




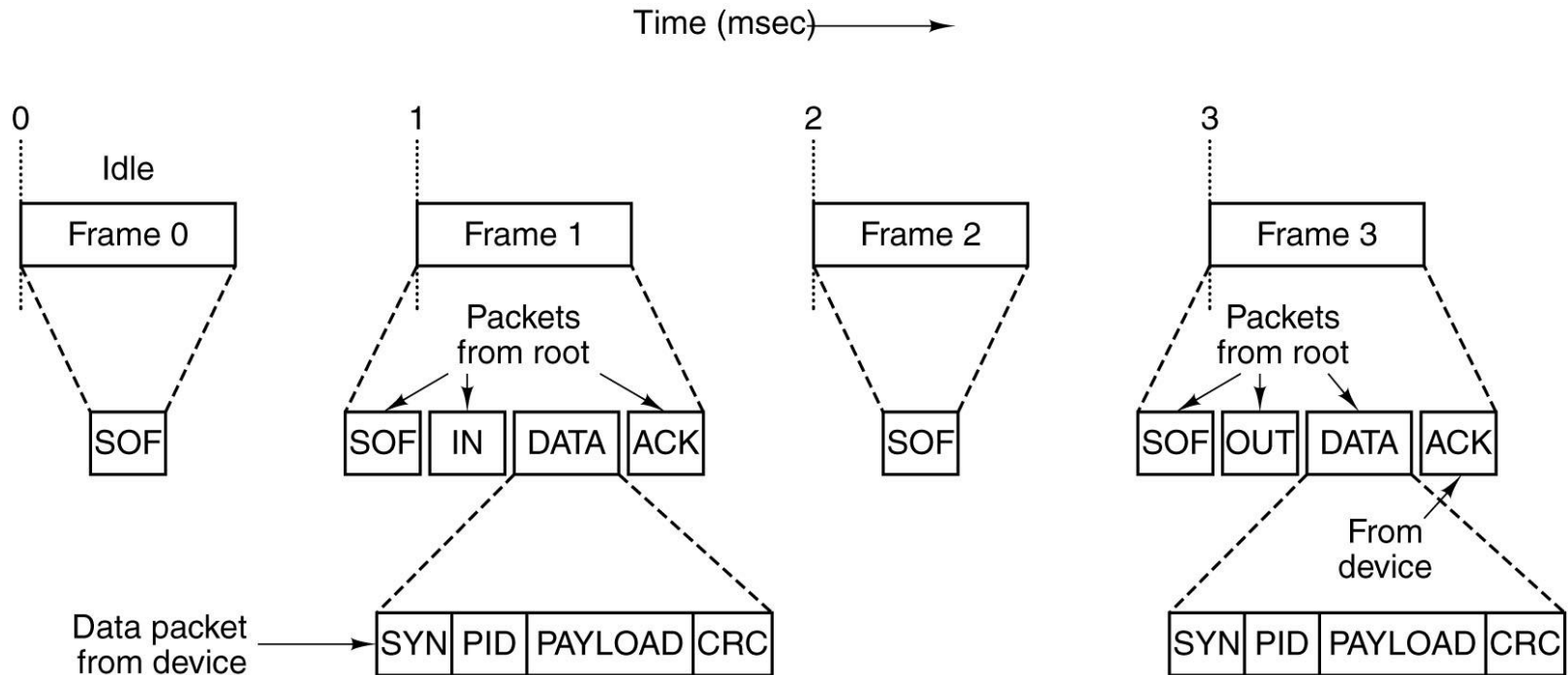
# CPU Buses of a Pentium 4 CPU



# The PCI Bus – The ISA Bus

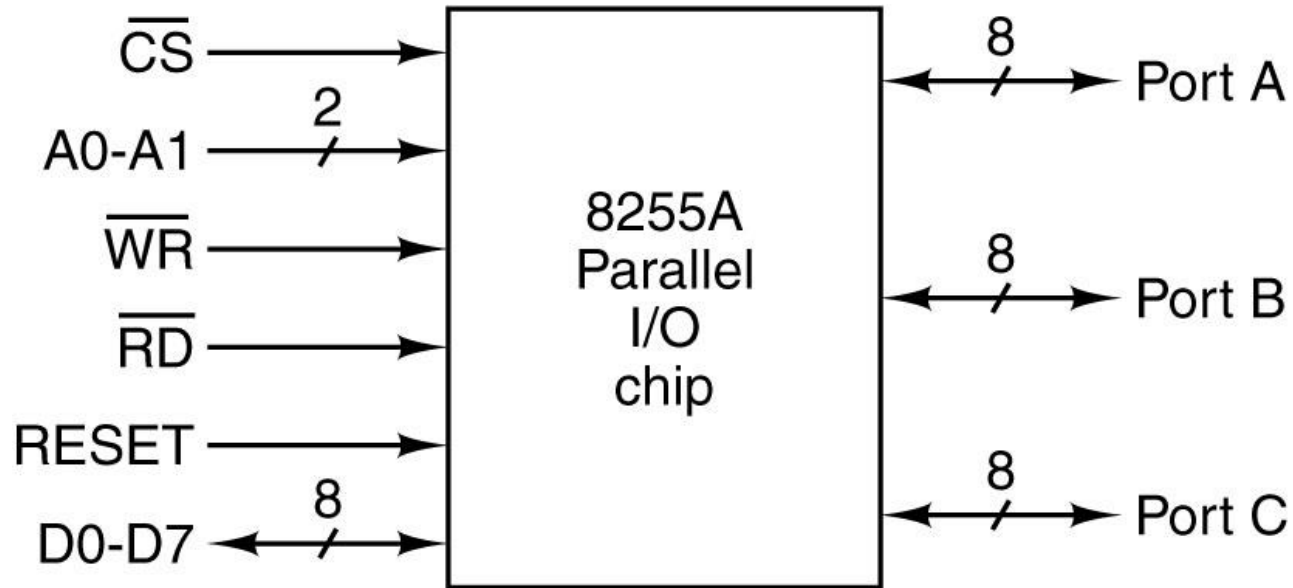


# The Universal Serial Bus



The USB root hub sends out frames every 1.00 ms.

# PIO Chips



An 8255A PIO chip.