CPE 186 Computer Hardware Design

Power Management

Dr. Pang

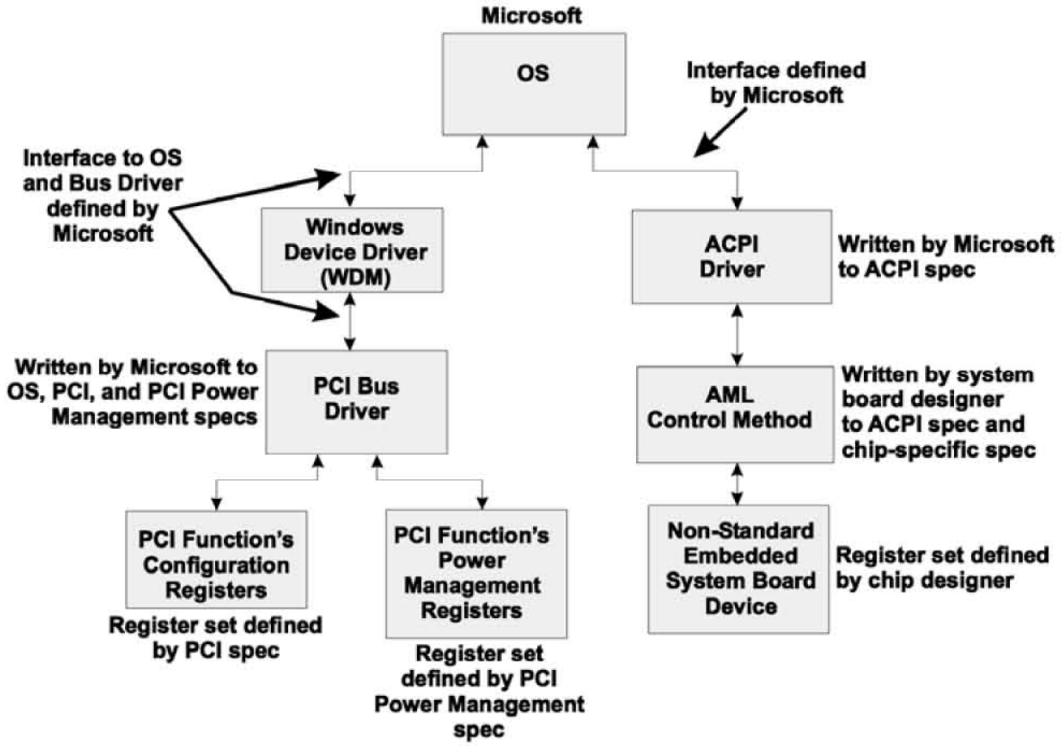
Device Support for PCI PM Optional

- It is optional whether or not a PCI device implements power management capability.

PCI Power Management

- The PCI Bus PM Interface Specification describes how to implement the optional PCI PM registers and signals. These registers and signals permit the OS to manage the power environment of PCI buses and the functions that reside on them.

Relationship of OS, Device Drivers, Bus Driver, PCI Registers, and ACPI (Advanced Configuration and Power Interface)



Power Management-PCI Bus vs. PCI Function

- OS can manage the PM state of a PCI function, it may also be able to manage the PM state of a PCI bus.
- In other words, hardware (specifically, the host/PCI bridge or PCI-to-PCI bridges) may permit the PM software to turn off the clock on a PCI bus. It may also allow power to be removed from the devices that reside on a PCI bus. A bridge design may permit one, the other, both or neither of these capabilities.

Bridge - Originating Device for a Secondary PCI Bus

- A system may include one or more PCI buses and each PCI bus is controlled by a bus bridge.
- For example, PCI bus zero is controlled by the Processor-to-PCI Bridge. This device is also referred to as the Host/PCI bridge, or the North bridge. From a PM standpoint, the bridge that controls a PCI bus is referred to as its originating device. The PCI-to-PCI bridge can be used as the originating device for PCI bus one. In this case, relative to the PCI-to-PCI bridge, PCI bus 0 is referred to as its primary bus, while PCI bus one is its secondary bus.

PCI Function Power States

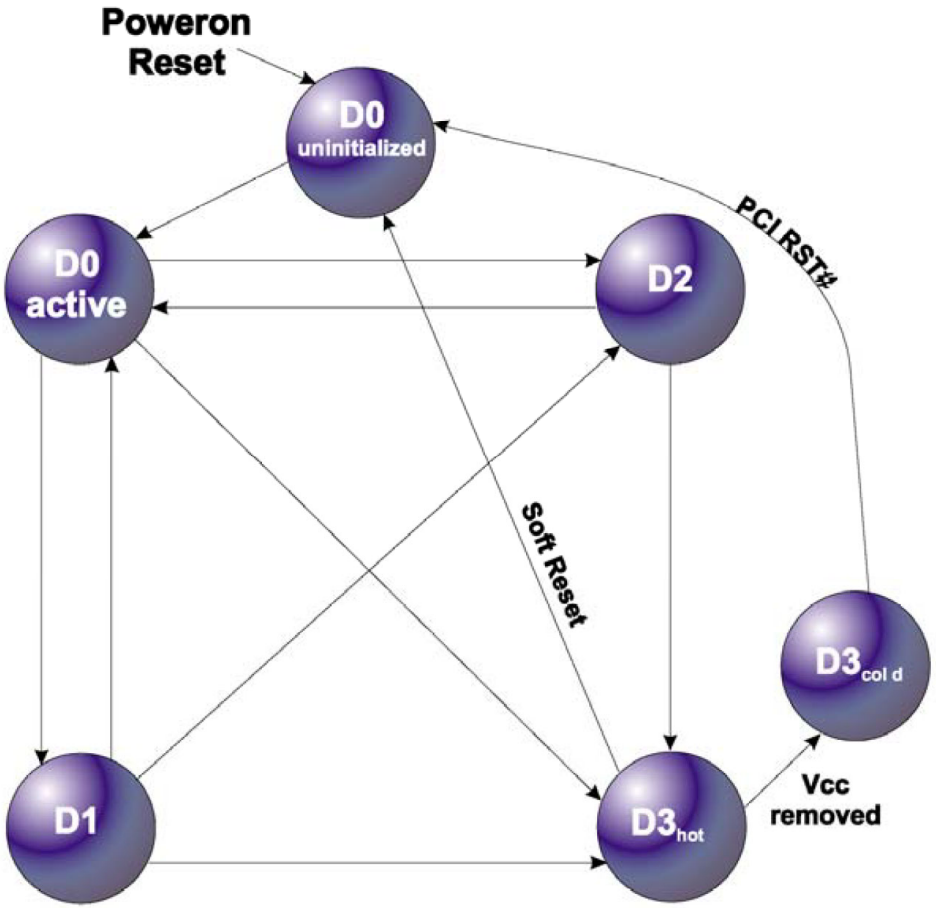
States:

- D0 (active): the maximum powered state
- D3 (full off): the minimum powered state.

  - Removal of power (Vcc) from the device. This is referred to as the **$D3_{cold}$** PM state. The function could transition into the $D3_{cold}$ state for one of two reasons: if the bus it resides on is placed in the B3 state; or the system is unplugged.
  - Vcc is still applied to the function and software commands the function to enter the D3 state. This is referred to as the **$D3_{hot}$** PM state.

- D1 (light sleep) and D2 (deep sleep) power management states enable intermediate power savings states between the D0 (on) and D3 (off) states.
- Each PCI function must support the full-on (D0) PM state and the full-off (D3) PM state. The D1 and D2 PM states are optional, as are the PM registers.

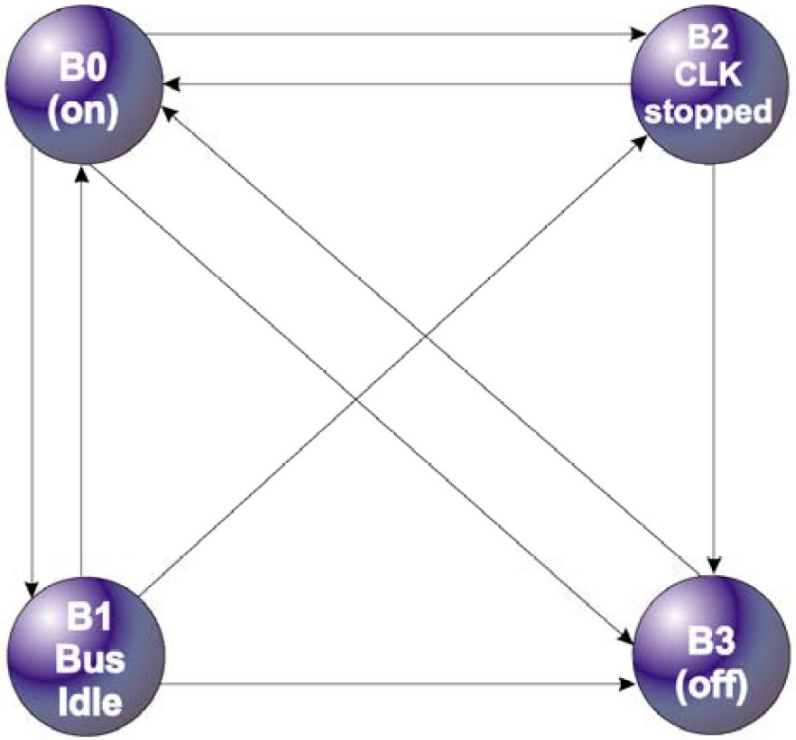
PCI Function Power Management State Transitions



PCI Bus PM States

Like any other PCI device, the bridge may have a set of PM registers that define the PM capabilities and current PM state of the bridge. The current PM state of the bridge also defines the current PM state of the bridge's secondary bus.

PCI Bus Power Management State Transitions



Baric Description of PCI Bus PM States

Bus PM State	State of Vcc	State of PCI CLK	Permissible PCI Activity on Secondary PCI Bus
B0 (full on)	on	free running	1. Any PCI bus transaction. 2. Function may generate interrupts. 3. Function may assert PME# (if enabled to do so by PME_En bit in PMCSR;).
B1	on	free running	Function may assert PME# (if enabled to do so by PME_En bit in PMCSR;).
B2	on	Stopped in low state. *Note*: If CLK normally 33.33MHz - 66MHz, RST# must be asserted when frequency changed.	
B3 (full off)	off	NA—no power	

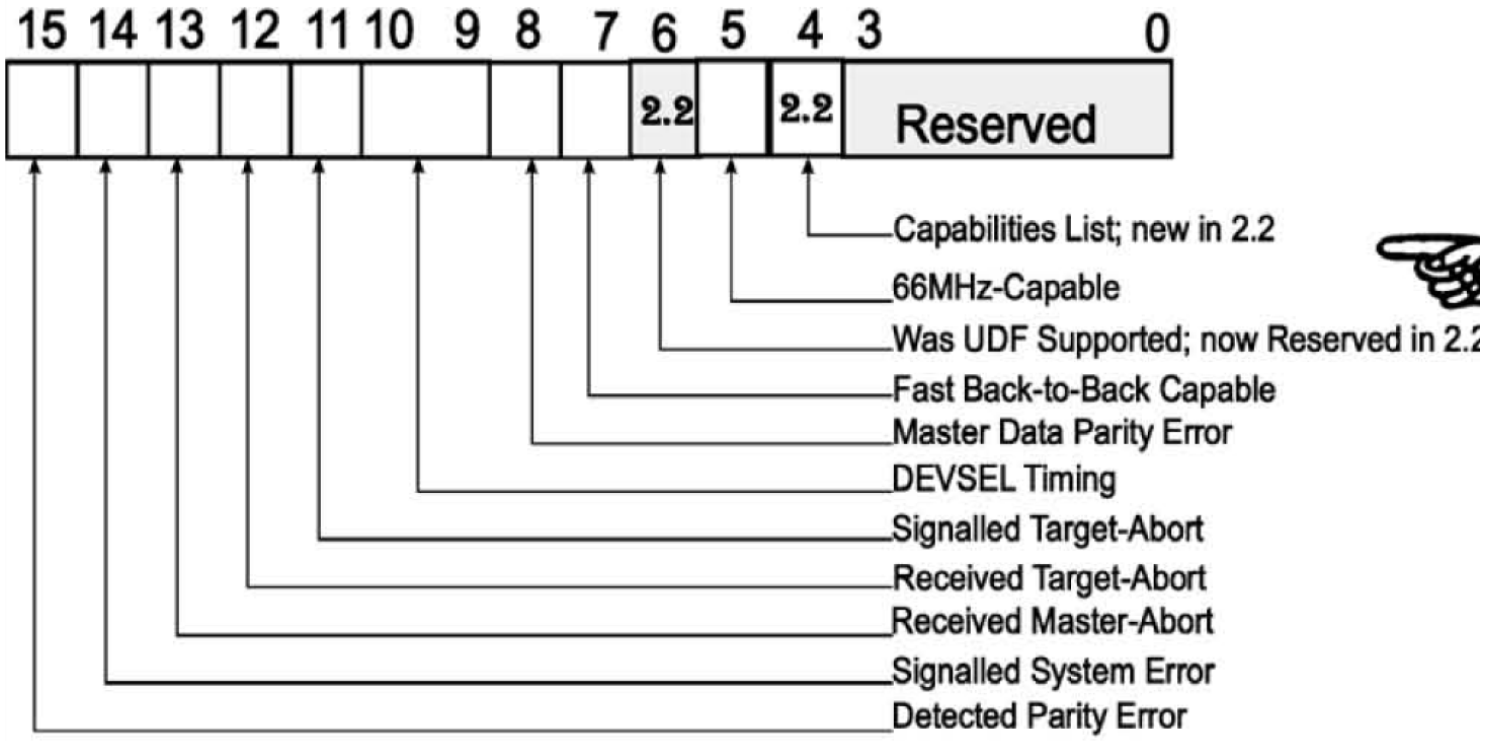
Bus PM States vs. PM State of the PCI Functions On the Bus

- Each PCI device may contain between one and eight PCI functions.
- Each function may implement its own set of PM registers that are used to report its PM capable and to control its current PM state.
- The bus PM state can not be in a numerically higher PM state than the numerically lowest PM state of any of the functions that reside on the bus.
- Functions are only aware of their own PM state.
- Bridge is only aware of its own PM state.

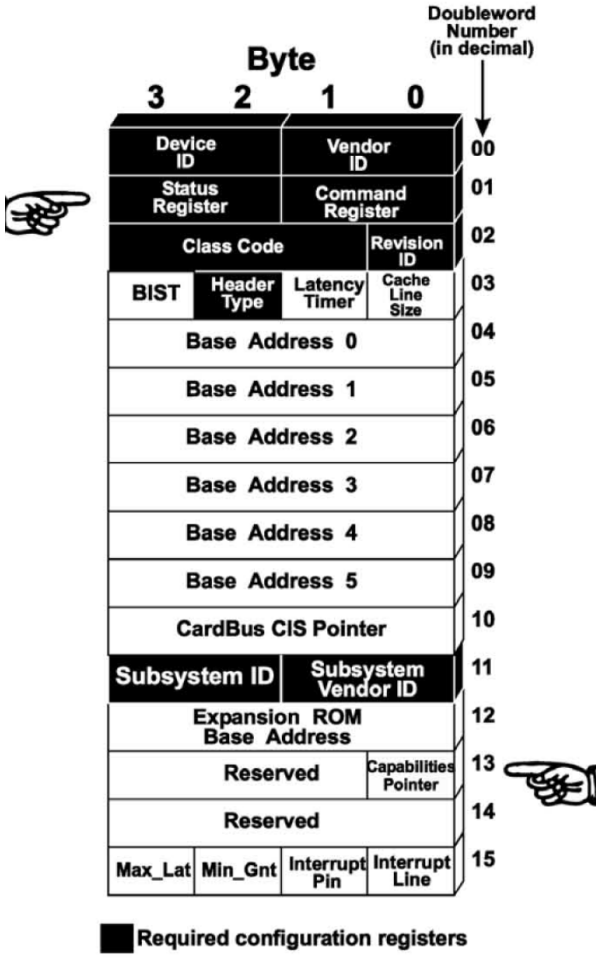
Relationship of Originating Bridge's PM State to Secondary Bus PM State

If Originating Bridge's PM State is	then Secondary Bus PM State is	Description
D0	B0	No power conservation in effect for bridge or bus.
D1	B1	Bridge is in light sleep. Transactions are not permitted on the secondary bus (because the bridge cannot deal with transactions while in the D1 mode). The PCI bus remains in the Idle state because all functions on the bus have been placed in a PM mode other than D0.
D2	B2	Bridge is in deep sleep and the PCI CLK is stopped on the secondary bus.
$D3_{hot}$ and B2_B3# bit = 1 (see Figure 23-15 on page 527)	B2	PCI **CLK stopped**, but **Vcc still applied** to all PCI devices on secondary bus. The bridge designer can choose to only turn off the CLK but not Vcc when the bridge is programmed to the $D3_{hot}$ state.
$D3_{hot}$ and B2_B3# bit = 0 (see Figure 23-15 on page 527)	B3	PCI **CLK stopped** and **Vcc turned off** to all PCI devices on secondary bus. The bridge designer can choose to turn off the CLK **and** Vcc when the bridge is programmed to the $D3_{hot}$ state.
$D3_{cold}$	B3	PCI CLK stopped and Vcc turned off to all PCI devices on secondary bus.

PCI Configuration Status Register



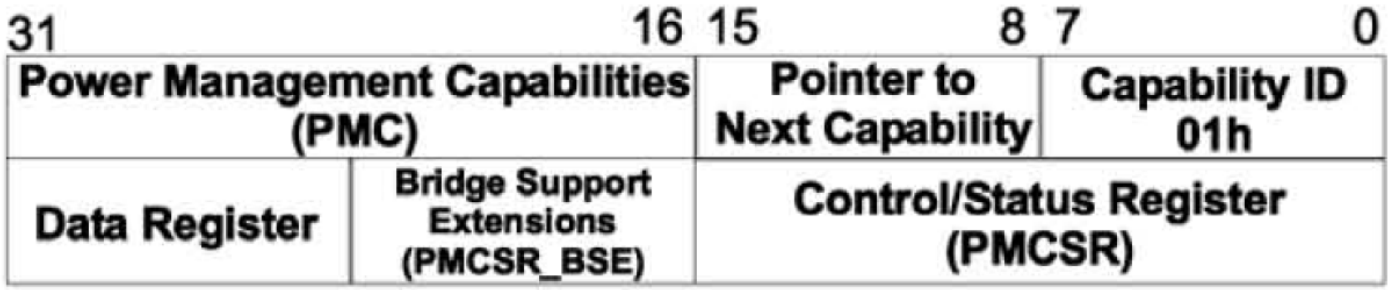
PCI Configuration Header Registers



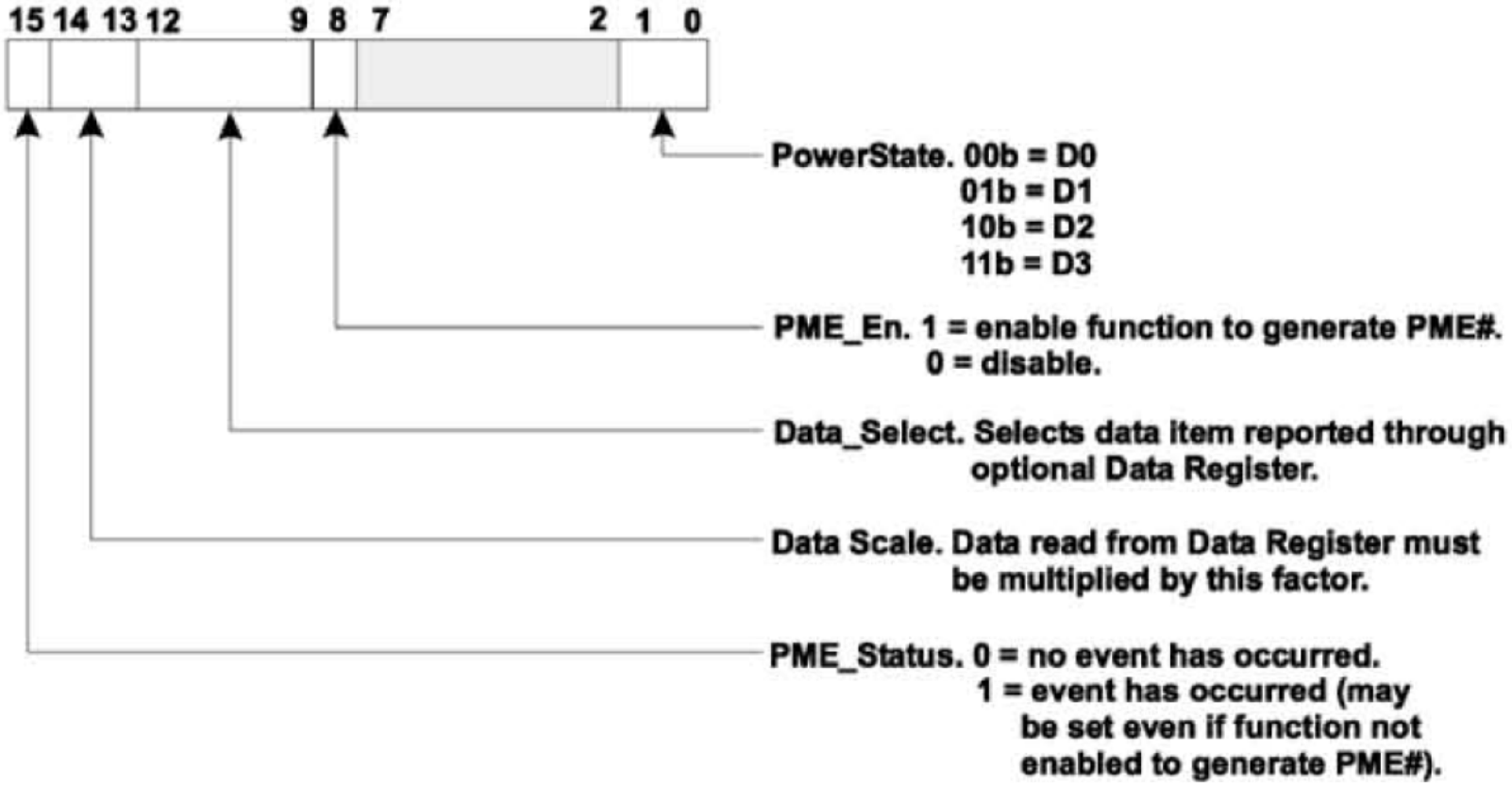
PCI Power Management

- Bit 4 (Capabities List bit) of the function's PCI configuration Status register: A one indicates that the Capabilities Pointer register is implemented in the first byte of dword 13d of the function's Configuration Header space.
- If the first (i.e.. least-significant) byte of the dword read contains Capability ID 01h, this identifies it as the PM register set used to control the function's power state.

PCI Power Management Capability Register Set



Power Management Control Registers (PMCSR)



OS Power Management Function Calls

- In order to support power management, the OS must implement the basic function call capabilities:
  - **Get Capabilities Function Call**
  - **Set Power State Function Call**
  - **Get Power Status Function Call**

BIOS/POST Responsibilities at Startup

- In an environment wherein the OS is responsible for managing power, the system BIOS isn't involved in PM but is responsible for basic system initialization before the OS loads and takes over.