CPE 186 Computer Hardware Design

PCI-to-PCI Bridge

Dr. Pang

Figure : Basic Bridge Terminology

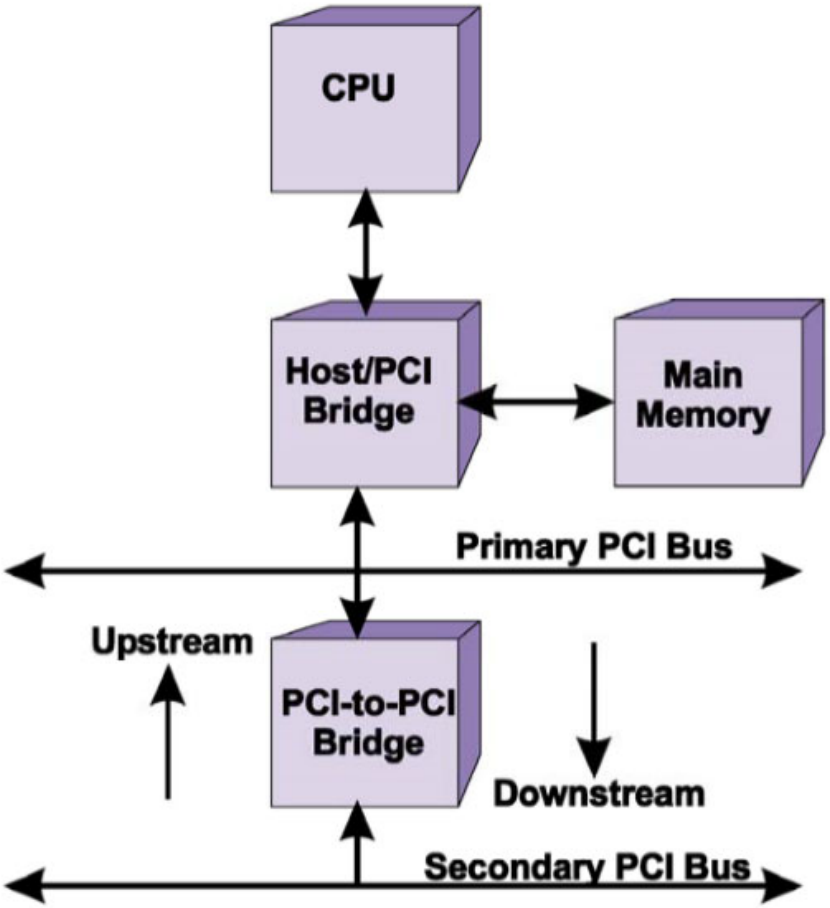
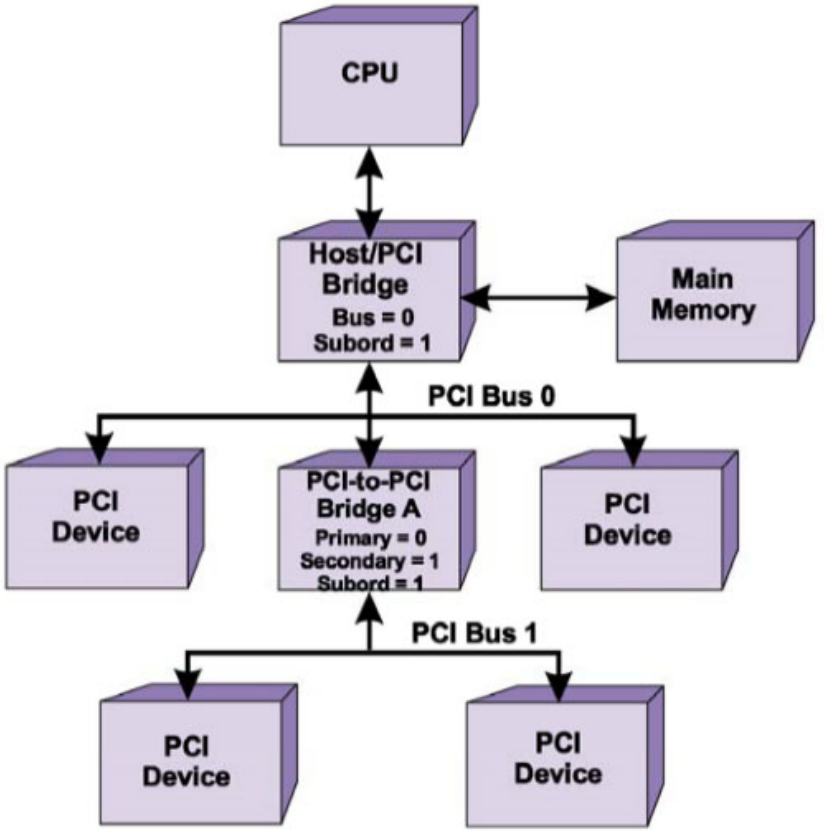
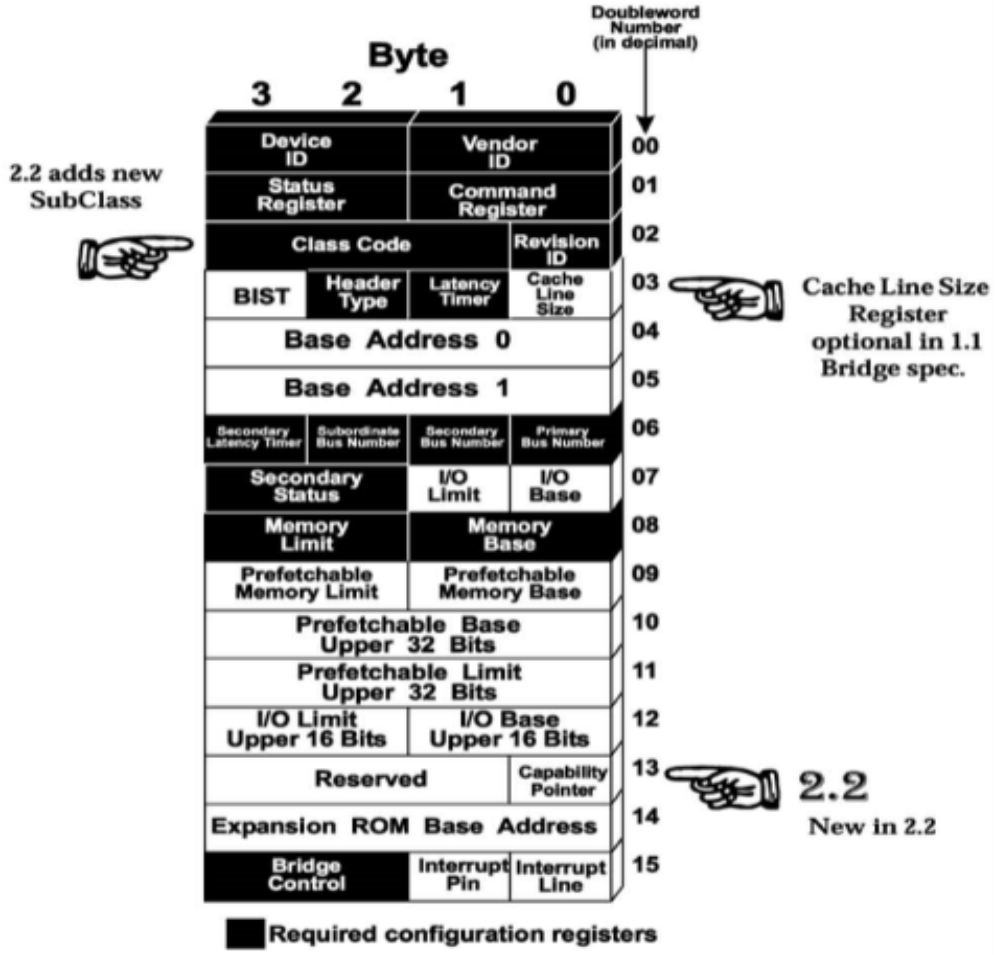


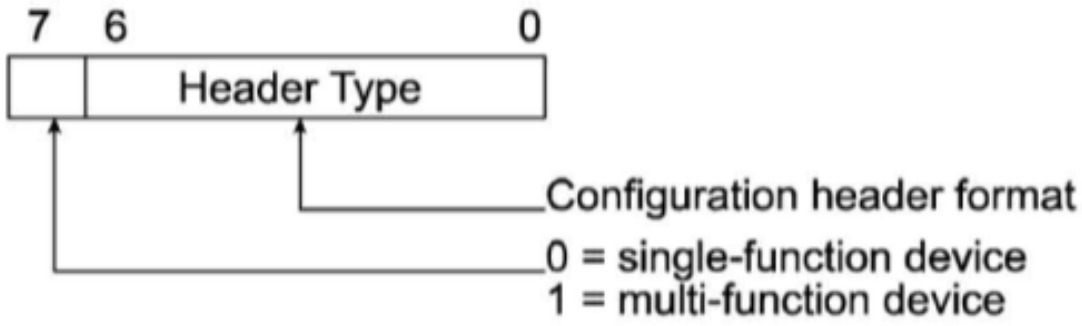
Figure : Example System One



PCI-to-PCI Bridge's Configuration Registers



Header Type Register



Bus Number Registers

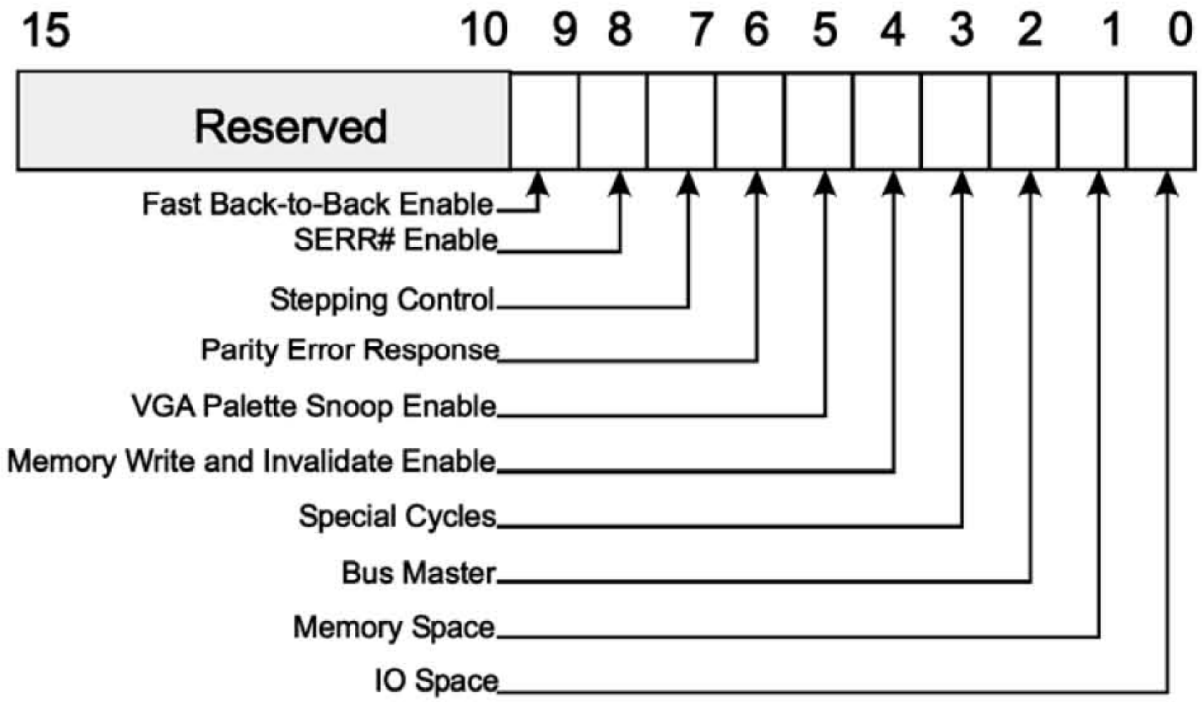
- Primary Bus Number register
- Secondary Bus Number register
- Subordinate Bus Number register.

Bus Number Registers

The information supplied by the three registers (Primary Bus Number register, Secondary Bus Number register, Subordinate Bus Number register) is used by the bridge to determine whether or not to pass through:

- Type 1 configuration reads and writes on the primary side that are to be passed through as a Type 0 configuration access (if the target is on the bridge's secondary bus) or as a Type 1 configuration access (if the target is on a bus subordinate to the bridge's secondary bus).
- Type 1 configuration writes received on either the primary or secondary side that are to be converted to Special Cycles on the specified target bus.

Command Register



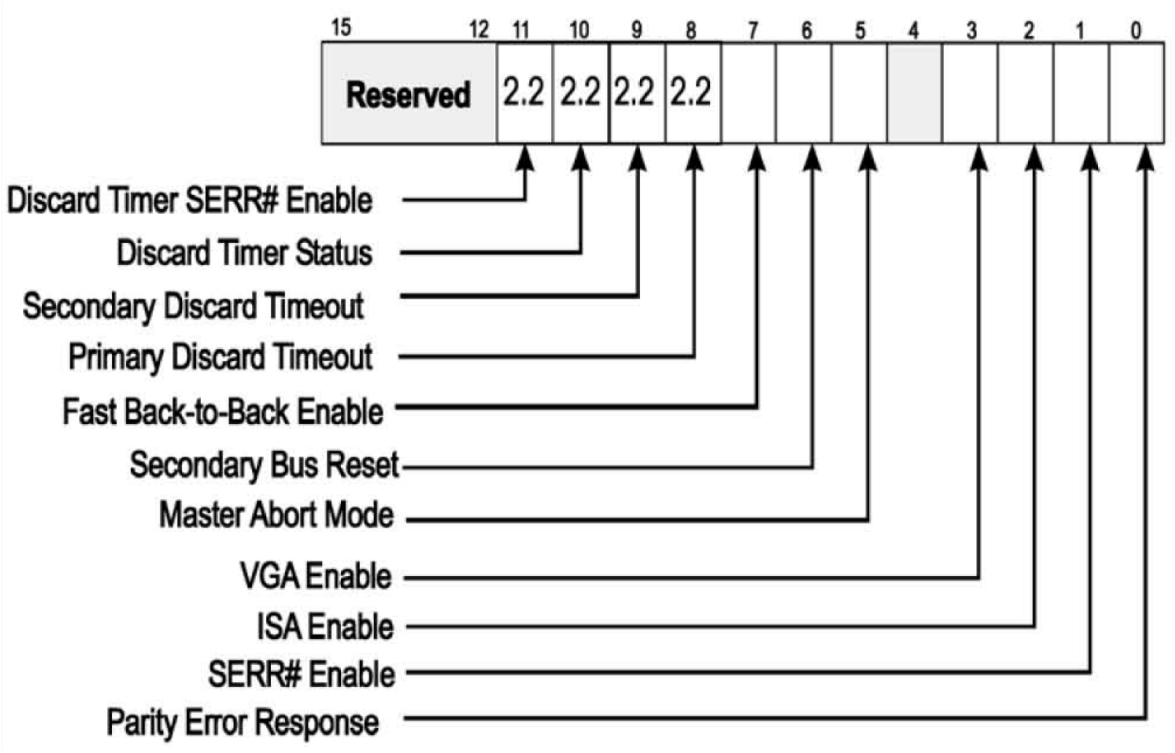
Command Register Bit Assignment

0	**IO Space**. When set, the bridge's IO address decoders on its primary side are enabled. When cleared, they are disabled. If cleared, any IO transactions detected on the secondary side are passed through to the primary side and all IO transactions detected on the primary side are ignored. Reset clears this bit.
1	**Memory Space**. When set, the bridge's memory and memory-mapped IO address decoders on its primary side are enabled. When cleared, they are disabled. If cleared, any memory transactions detected on the secondary side are passed through to the primary side and all memory transactions on the primary side are ignored. Reset clears this bit.
2	**Bus Master**. Control's the bridge's ability to act as a master on the primary side. However, the bridge is always enabled to forward and convert configuration transactions. When cleared, the bridge ignores all memory and IO transactions detected on the secondary side (because it cannot act as a master to pass the transactions through to the primary side). Reset clears this bit.
3	**Special Cycles**. Hardwired to zero (because PCI-to-PCI bridges don't monitor Special Cycles).

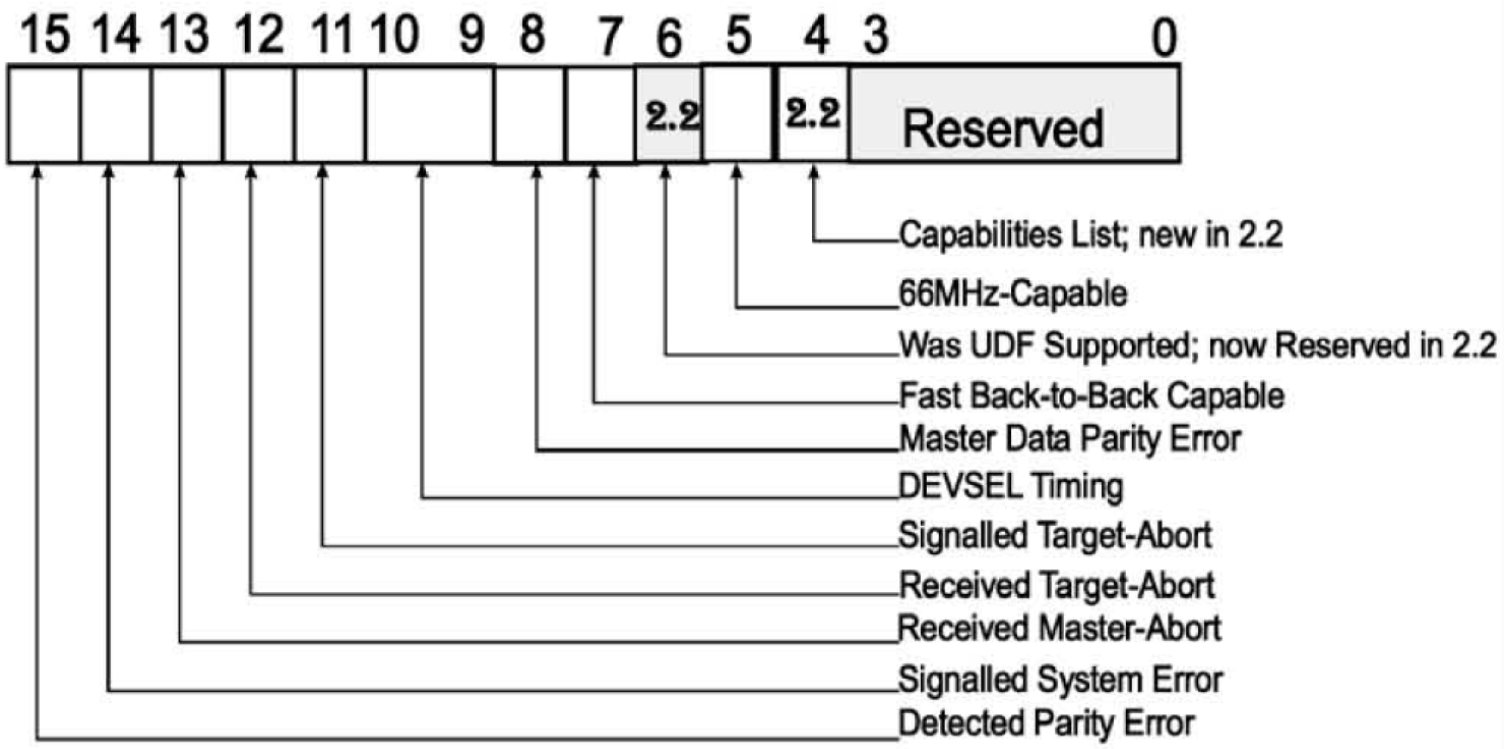
Command Register Bit Assignment

4	**Memory Write and Invalidate Enable** : optional
5	**VGA Palette Snoop** : optional.
6	Parity **Error** Response. When set, the bridge takes the normal actions defined by the specification when a parity error is detected on the primary side. When cleared, parity errors are ignored, but the bridge must generate proper parity. Reset clears this bit.
7	**Stepping Control.** 0(disable) or 1 (enable)
8	SERR#: primary bus 0(disable) or 1 (enable)
9	Fast Back-to-Back Enable: 0(disable) or 1 (enable)
15:10	Reserved. Read-only and must return zero when read.

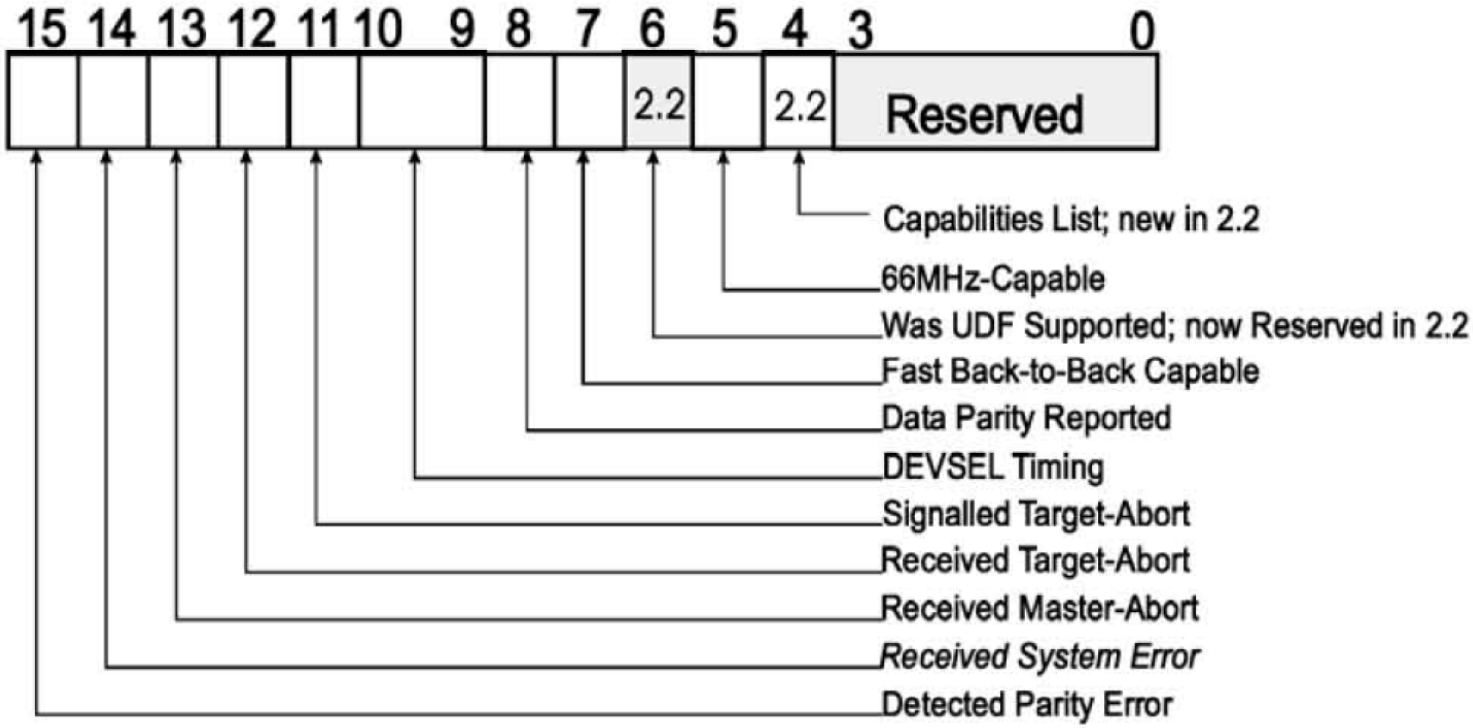
Bridge Control Register



Primary Interface Status Register



Secondary Status Register



Basic Transaction Filtering Mechanism

- The configuration program assigns all IO devices that reside behind a PCI-to-PCI bridge mutually-exclusive address ranges that are blocked together within a common overall range of IO locations.
- The PCI-to-PCI bridge passes any IO transactions detected on the primary side of the bridge to the secondary side if the target address is within the range associated with the community of IO devices that reside behind the bridge.

Basic Transaction Filtering Mechanism

- Any IO transactions detected on the secondary side of the bridge are passed to the primary side if the target address is outside the range associated with the community of IO devices that reside on the secondary side (because the target device doesn't reside on the secondary side, but may reside on the primary side).

Basic Transaction Filtering Mechanism

- All memory-mapped IO devices (i.e.. non-prefetchable memory) that reside behind a PCI-to-PCI bridge are assigned mutually-exclusive memory address ranges within a common block of memory locations.

Basic Transaction Filtering Mechanism

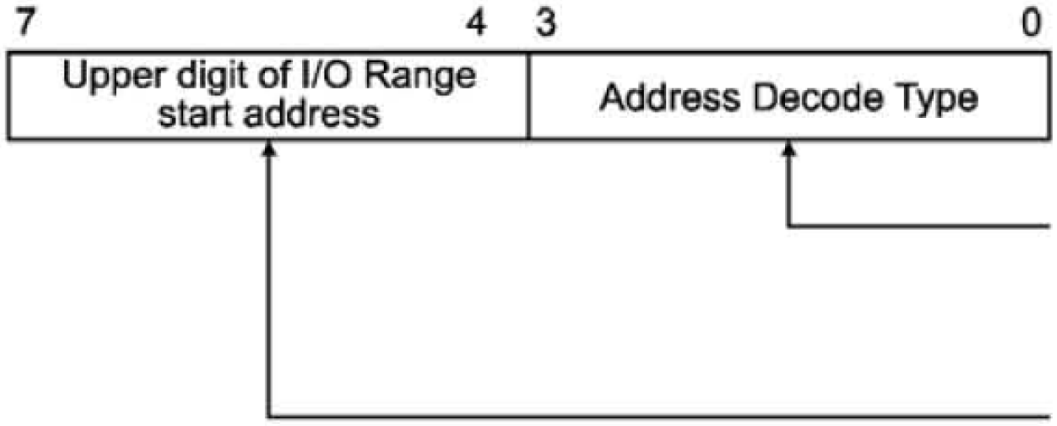
- All memory devices (i.e., regular memory, not memory-mapped IO) that reside behind a PCI-to-PCI bridge are assigned mutually-exclusive memory address ranges within a common overall range of memory locations. The PCI-to-PCI bridge is then programmed to pass any memory transactions detected on the primary side of the bridge to the secondary side if the target address is within the range associated with the community of memory devices that reside behind the bridge.
- Conversely, any memory transactions detected on the secondary side of the bridge are passed to the primary side if the target address is outside the range associated with the community of memory devices that reside on the secondary side (because the target device doesn't reside on the secondary side, but may reside on the primary side).

Bridge's IO Filter (Optional)

The optional configuration registers within the bridge that support this "filtering“ capability are:

- Base Address Registers.
- IO Base and IO Limit registers.
- IO Extension registers

IO Base Register

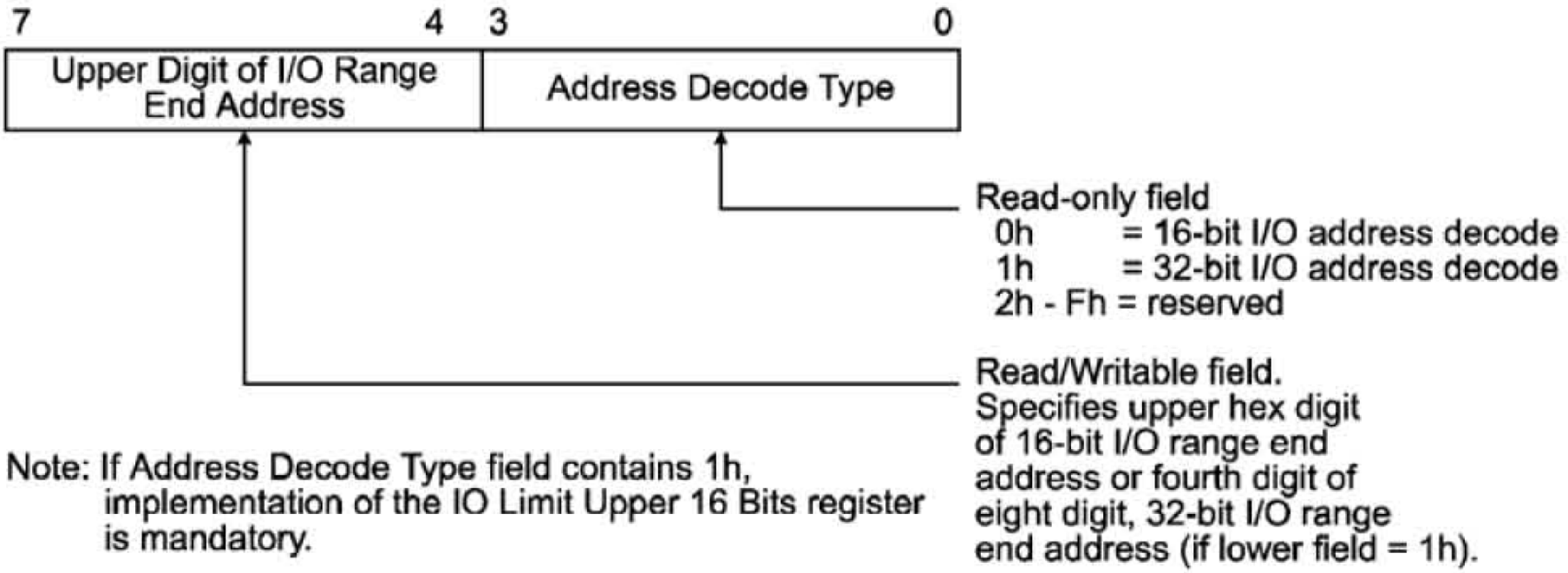


Read-only field
0h = 16-bit I/O address decode
1h = 32-bit I/O address decode
2h - Fh = reserved

Read/Writable field.
Specifies upper hex digit
of four digit, 16-bit I/O range start address
or fourth digit, [15:12], of eight digit
32-bit I/O range start address (if 3:0 = 1h).

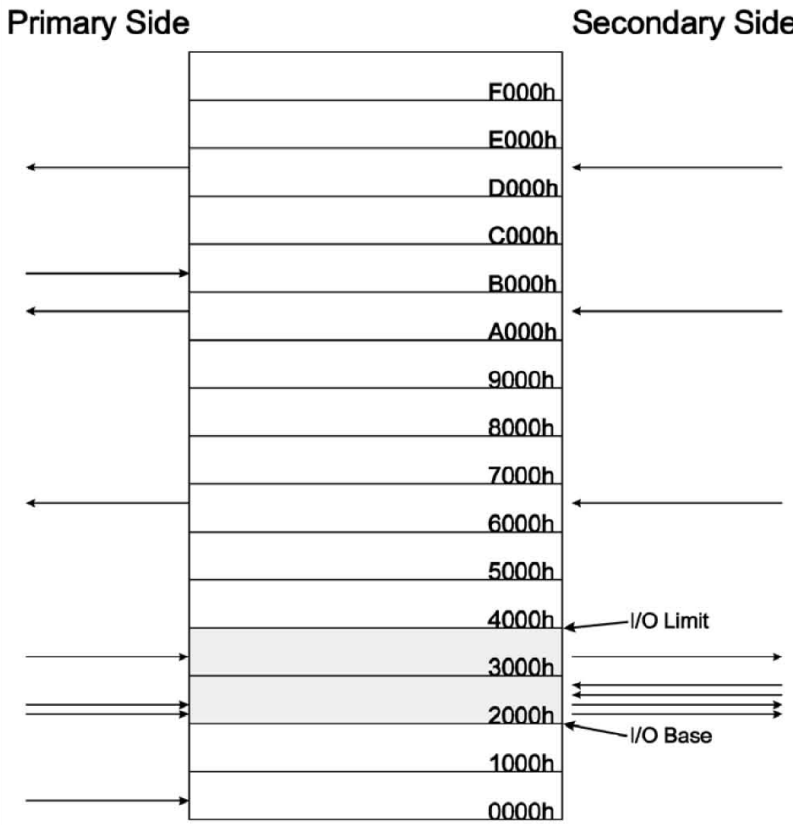
Note: If Address Decode Type field contains 1h, implementation of the IO Base Upper 16 Bits register is mandatory.

IO Limit Register



Note: If Address Decode Type field contains 1h, implementation of the IO Limit Upper 16 Bits register is mandatory.

Example of IO Filtering Actions



IO Base Register
IO Limit Register

Example of IO Filtering Actions

- Anytime that the bridge detects an I0 transaction on the primary bus with an address inside the 2000h through 3FFFh range, it claims the transaction and passes it through (because it's within the range defined by the IO Base and Limit registers and may therefore be for an IO device that resides behind the bridge).
- Anytime that the bridge detects an I0 transaction on the primary bus with an address outside the 2000h through 3FFFh range, it ignores the transaction (because the target IO address is outside the range of addresses assigned to IO devices that reside behind the bridge).
- Anytime that the bridge detects an IO transaction on the secondary bus with an address inside the 2000h through 3FFFh range, it ignores the transaction (because the target address falls within the range assigned to I0 devices that reside on the secondary side of the bridge).
- Anytime that the bridge detects an I0 transaction on the secondary bus with an address outside the 2000h through 3FFFh range, it claims the transaction and passes it through to the primary side (because the target address falls outside the range assigned to I0 devices that reside on the secondary side of the bridge, but it may be for an I0 device on the primary side).