Sc/CpE 142 – Exam 2

Name.....

1) Fill in the blanks /Short answer (30 points, 3 points each)

a) List two primary methods for enhancing instruction-level parallelism.
   I. ...deeper pipeline
   II. ...multiple issue

b) ...miss rate... is the unit of information transferred between the cache and main memory o
miss.

c) ...write through.... is a scheme (policy) in which writes always update both cache and t
next lower level of memory hierarchy, ensuring that the data is always consistent between th
two.

d) ...Temporal locality... is the principle stating that if a data location is referenced, then it will
to be referenced again soon.

e) ...Branch Prediction... is a method of resolving a branch hazard that assumes a given outc
for the branch and proceeds based on that assumption rather than waiting for the actual out

f) Increasing ...hits... can improve hit ratio due to temporal locality.

g) In a direct-mapped cache each block has only one word. True or False.

h) The five stages in a pipeline implementation require 4, 5, 4, 2, and , 8 nanoseconds. Wha
fastest clock rate at which this datapath can operate?.....

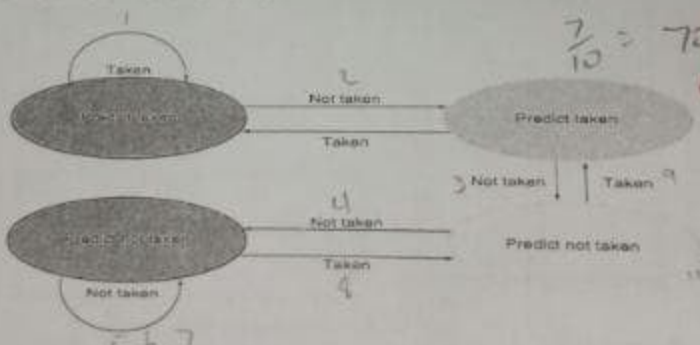
Clock rate = Cycles / Time = 1 / (8 ns) = 2.1[illegible] x 10^8 Hz

i) Consider a 2-bit branch prediction scheme illustrated by the following figure. What is the
accuracy of this ***2-bit predictor*** for the following repeating pattern of branch outcomes as
the predictor starts in the top left state? .....

T, NT, NT, NT, NT, NT, NT, T, T, NT

3/10 = 30.00 %

7/10 = 70.00 %



List three types of hazards that can degrade the performance of a pipelined datapath.

i) data hazard
ii) structural hazard
iii) control hazard

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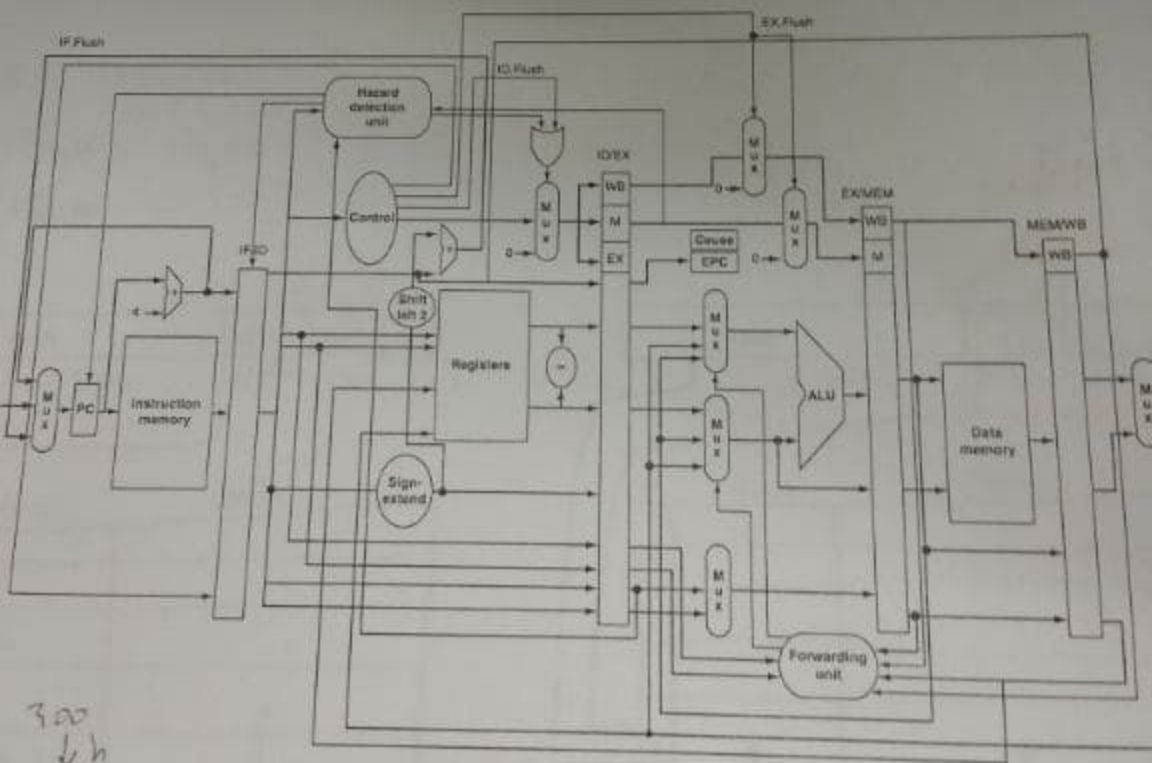
2) Consider the pipelined system shown below. Find the number of cycles required to execute the following MIPS code assuming that branch is taken. Justify your result. (15 points)

			1	2	3	4	5	6	7	8	9	10	11	12	13
300		SLT $6, $8, $7	IF	ID	EX	M	WB								
304		LW $5, 100($6)		IF	ID	EX	M	WB							
308		LW $7, 100($15)			IF	ID	EX	M	WB						
30C		BEQ $8, $15, L1				IF	ID	EX	M	WB					
310		SUB $9, $7, $4													
314		SUB $20, $9, $7													
318	L1:	LW $8, 100($9)							IF	ID	EX	M	WB		
31C		ADD $11, $8, $12								IF	ID	EX	M	WB	
320		SW $8, 104($9)									IF	ID	EX	M	WB

5+7-1 + [delays]

5+7-1 + [+1 (branch taken) +1 (Lw hazard)] = 13 clock cy



300
304
308
30C
310
314
318
320

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3) A computer uses 16-bit addresses, with byte addressable locations. Assume this system has a cache containing 32 **(thirty two) 8-word** blocks. Each word is 16 bits long. Show the implementation of the cache assuming **2-way set associativity**. You need to show how a given 16-bit address is divided into different parts to perform a cache reference. Show all necessary components of the cache. Provide the size of each component and the widths of its inputs and outputs, if applicable. **(15 points)**

2-way set associative

32 blocks

2 blocks per set

1 block = 8 words

1 word = 16 bits = 2 bytes

size = 32 · (8 · 16) = 4096 bits = 512 bytes

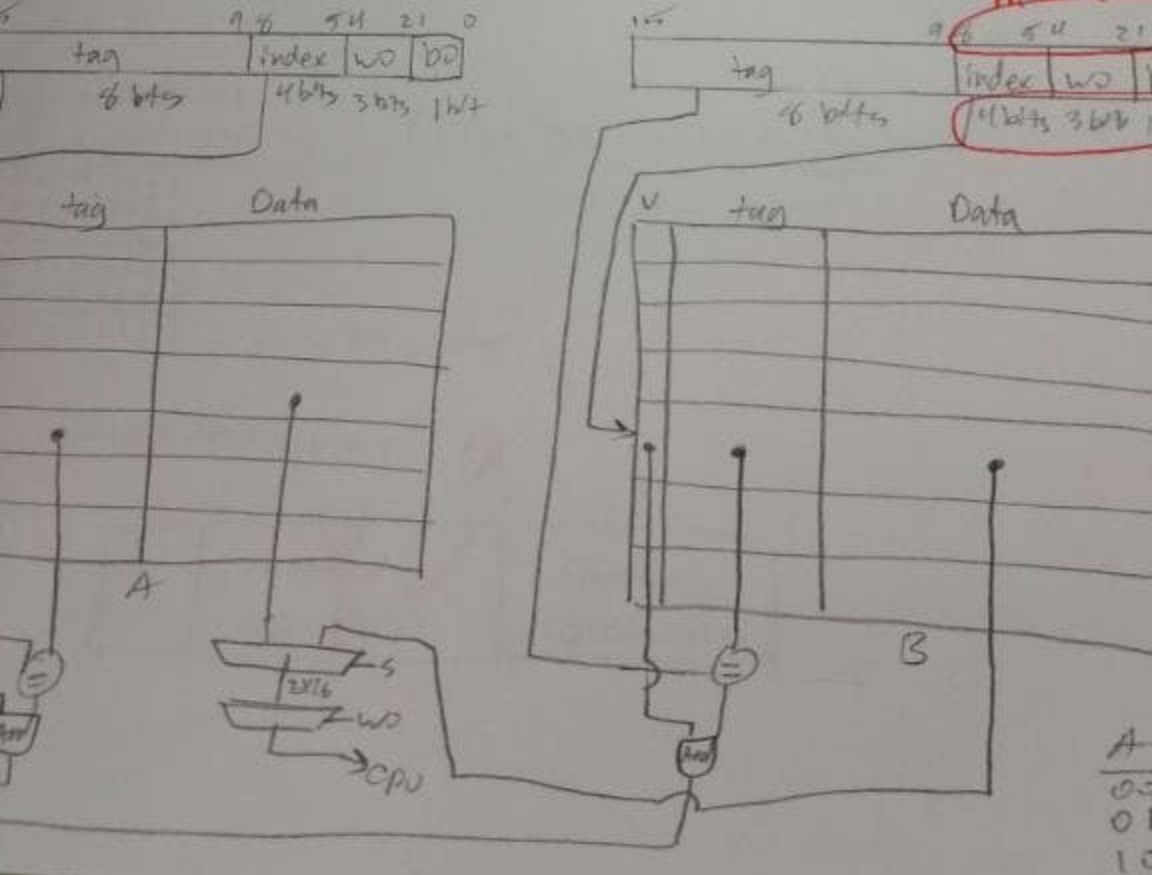
$$\frac{512 \text{ bytes}}{\text{cache}} \cdot \frac{1 \text{ word}}{2 \text{ bytes}} \cdot \frac{1 \text{ block}}{8 \text{ words}} \cdot \frac{1 \text{ set}}{2 \text{ blocks}} = 16 \text{ sets/cach}$$

index = $\log_2(16) = 4$

word offset = $\log_2(8) = 3$

byte offset = $\log(2) = 1$

indicies match



4. Convert the following decimal numbers into IEEE 754 floating-point format. Then, product using floating-point multiplication. Express the product using the 754 forn 745 uses a 1-bit sign, an 8-bit biased exponent, a 23-bit normalized fraction, ar exponent bias. Show all the work (**15 points**)

A = - 33.75
B = 25

(A) -33.75 $0.75 \cdot 2 = 1$

-100001.11 $.5 \cdot 2 = 1$

-1.0000111×2^5

$E_b = E + 127 = 5 + 127 = 132 = 100$

S	exponent	fraction
1	1000_0100	00001110 0 ...
1bit	8 bits	23 bits

(B) 25

11001.0

1.1001×2^4

$Eb = E + 127 = 4 + 127 = 131 = 1$

S	exponent	fraction
X	1000_0011	10010...
1bit	8 bits	23 bits

-1

1.0000111
1.1001000

Eb E

$(131 + 132) - 127 = 136 = 9$

0 0111
0 000x
0 00xx
1 1xxx
1 xxxx
01111

$= -843.75$

$= -1.101001011111 \times 10^9$

S	Exponent	Fraction
1	1000_1000	10100101111...

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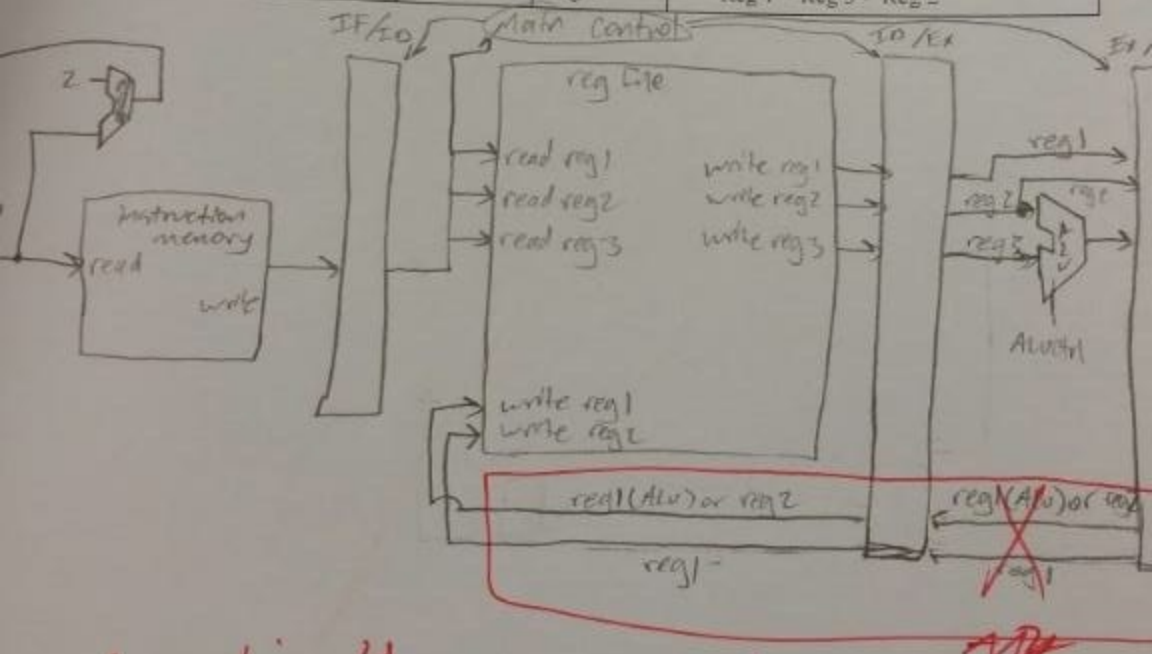
5) Consider a hypothetical 16-bit assembly language with only three instructions. The format for these instructions is given below. Design a pipelined CPU which can fetch and execute any of these instructions. Show all necessary components. Label each component (including its ports). Assume that the memory is byte-addressable. The internal design of the control logic is not required. You must use minimum number of components possible. (25 points)

	Bits (15 - 12)	bits (11 - 8)	bits (7 - 4)	bits (3 - 0)	
Instruction	opcode	operand 1	operand 2	Operand 3	operation
SWAP	0000	Reg 1	Reg 2	not used	Swaps the contents of operand 1 and operan2; Reg 1 <= Reg 2 Reg 2 <= Reg1
ADD	0010	Reg 1	Reg 2	Reg 3	Reg 1 = Reg 3 + Reg 2
SUB	1000	Reg 1	Reg 2	Reg 3	Reg 1 = Reg 3 - Reg 2



-forwarding -4

allocate another buffer -1