CSc/CPE 142
Advanced Computer Organization
Spring 2011 Exam 2
Dr. Arad

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Time: 75 minutes

Exam Rules:

- *This is a closed book/notes exam. You must show all the work for problems 2-4.*
- *Use only the paper provided by the instructor.*
- *Do not take the exam apart.*
- *Any incident of cheating can lead to score zero on the test.*
- *All cell phone, pagers, and other electronic devices must be turned off.*

Problem 1	30 /30
Problem 2	15 /15
Problem 3	10 /10
Problem 4	21 /25
Problem 5	14 /20
Total	90 /100

95

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1) Fill in the blanks / True False **(2 points each; no partial credit)**

a) List two primary methods for enhancing instruction-level parallelism.
   I. deeper pipeline
   II. multi issue pipeline

b) block is the unit of information transferred between the cache and main memory on a miss.

c) Write through policy is a reasonable choice for handling a page faults. True or False

d) temporal locality is the principle stating that if a data location is referenced, then it will tend to be referenced again soon.

e) A TLB miss will always lead to a page fault. True or False.

f) Increasing block size can improve hit ratio due to spatial locality.

g) A page table maps each page in a virtual memory to either a page in main memory or a page stored on a disk, which is the next level in the hierarchy.

h) In a direct-mapped cache each block has only one word. True or False.

i) "4" in 4-way set associative cache refers to number of blocks per set

j) speculation is an approach whereby the compiler or processor guesses the outcome of an instruction to remove it as dependence in executing other instructions.

k) very wide instruction set architecture (VLIW) is a style of instruction set architecture that launches many operations that are defined to be independent in a single wide instruction, typically with many separate opcode fields.

l) List three categories of cache misses known as "the three Cs".
   I. cold miss
   II. miss due to cache size
   III. collision miss

m) By doubling the clock rate we can always reduce miss penalty by 50%. True or False

n) In virtual memory context, TLB is a cache that keeps track of recently used address mappings to try to avoid an access to the page table.

o) List the possible negative performance effect of increasing set associativity

more comparison, more hardware, slower

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2) Consider a 2-level memory organization consisting of cache and main memory. Assume a system that uses the memory organization has an overall average CPI of 3 without any memory stalls. Consider an instruction miss rate of 4% and a data miss rate of 6%. Also, assume that only 25% of instructions access memory data. Determine the number of clock cycles required to execute a program with 100 instructions on this machine if miss penalty is 50 cycles. (15 points)

3 CPI × 100 inst = 300 cycles

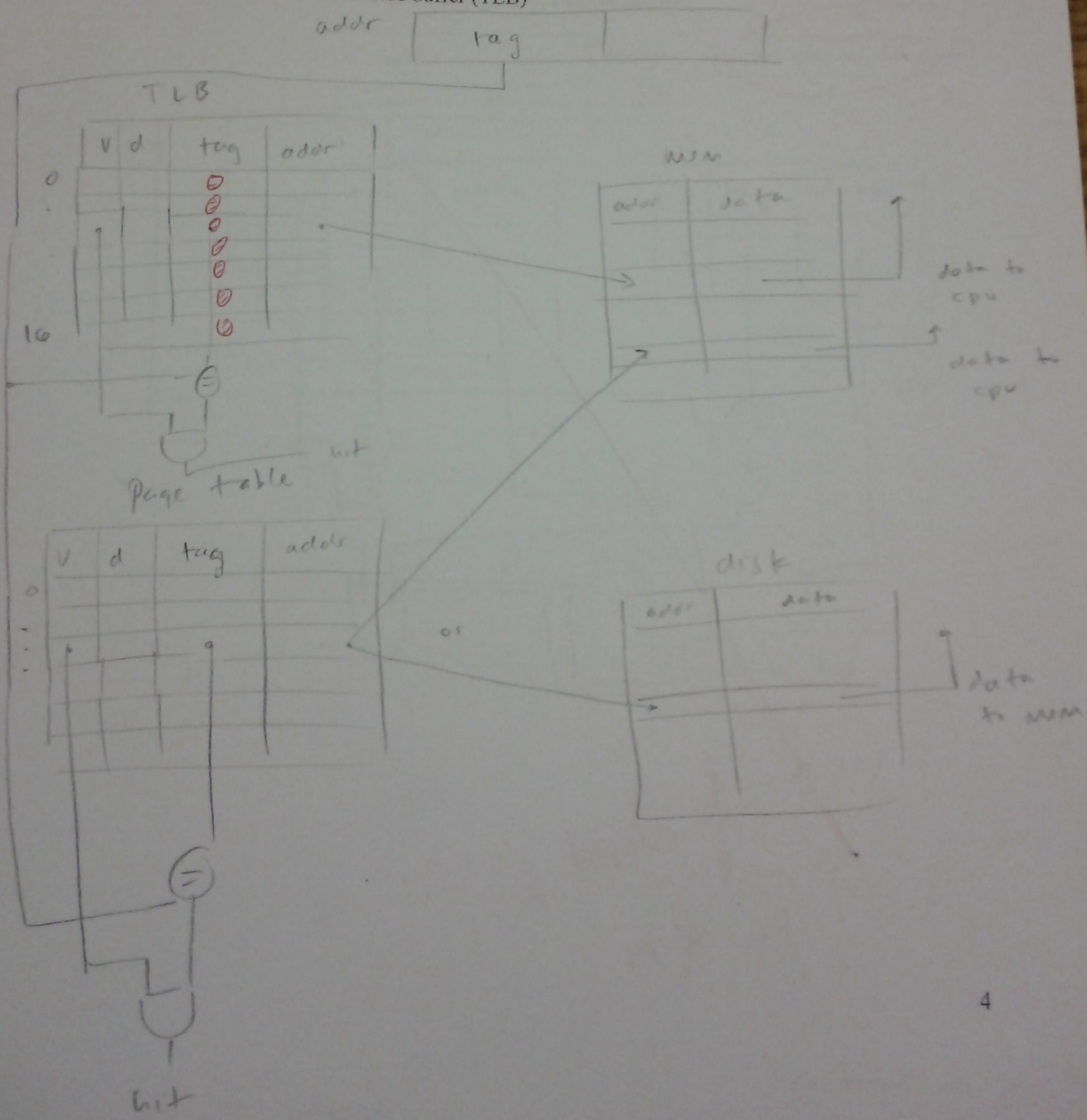
100 inst × 0.04 × 50 = 200 cycles

100 inst × 0.25 × 0.06 × 50 = 75 cycles

Total cycles = 300 + 200 + 75 = 575 cycles

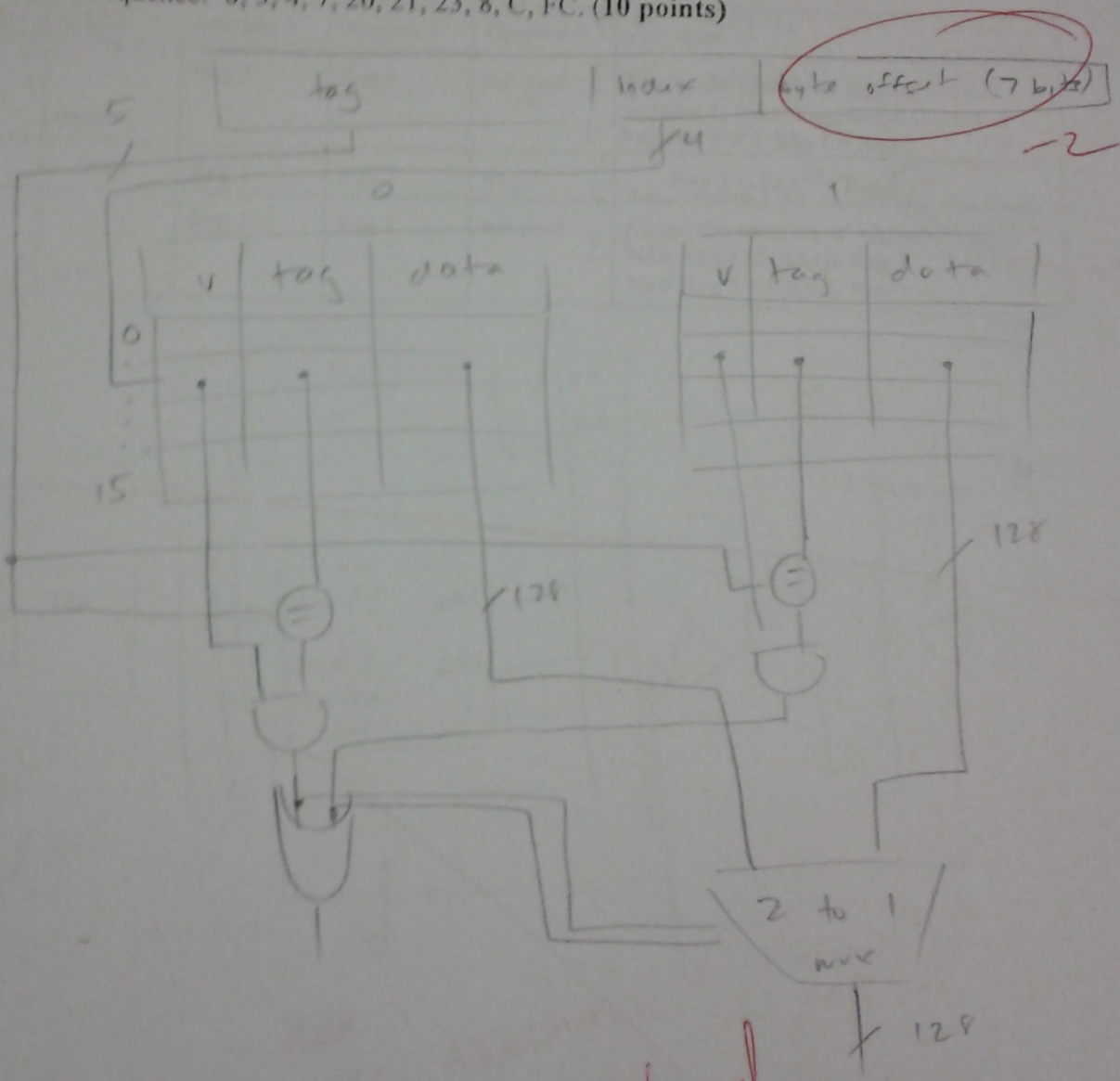
3) Using a detailed figure clearly illustrate how the search for the data associated with a virtual address takes place in a virtual memory configuration with the following assumptions: (10 points)

- 32-bit virtual address
- 26-bit physical address
- 8KB page size
- 16-entry translation-lookaside buffer (TLB)



4) A computer uses 16-bit addresses, with byte addressable locations. Assume this system has a cache containing 32 **(thirty two) 8-word** blocks. Each word is 16 **bits** long. Show the implementation of the cache assuming **2-way set associativity**.

- You need to show how a given 16-bit address is divided into **different** parts to perform a cache reference. Show all necessary components of the cache. Provide the size of each component and the widths of its inputs and outputs, if applic**able**. **(15 points)**
- Assume the cache is empty. Find the number of misses for **the** following hexadecimal address sequence: 0, 5, 4, 7, 20, 21, 23, 8, C, FC. **(10 points)**



	block 0	block 1	block 2	block 3
	00 ... 0F	10 ... 1F	20 ... 2F	30 ... 3F

ador	hit/miss	block 0	block 1
0	miss	M[00-0F]	
5	hit	M[00-0F]	
4	hit	M[00-0F]	
7	hit	M[00-0F]	
20	miss	M[20-2F]	
21	hit	M[20-2F]	
22	hit	M[20-2F]	
C	miss	M[00-0F]	
C	hit	M[00-0F]	—
FC	miss		

4 misses

5) Consider a hypothetical 16-bit assembly language with only three register-type instructions. The format for these instructions is given below. Design a pipelined which can fetch and execute any of these instructions. Show all necessary components. Label each component (including its ports). Assume that the memory is byte-addressable. The internal design of the control logic is not required. You must use minimum number of components possible. (20 points)

	bits (15 - 12)	bits (11 - 8)	bits (7 - 4)	bits (3 - 0)	
Instruction	opcode	operand 1	operand 2	Operand 3	operation
MOV	0000	Reg 1	Reg 2	not used	Moves the content of register 2 into register 1; No change to the content of register 2. Reg 1 = Reg 2
ADD	0011	Reg 1	Reg 2	Reg 3	Reg 1 = Reg 3 + Reg 2
SWAP	1100	Reg 1	Reg 2	not used	Swaps the contents of registers 1 and 2 New Reg 1 = Current Reg 2 New Reg 2 = Current Reg 1