Computer Systems & Introduction to PCI

CPE 186 Computer Hardware

Handout

Professor Pang

Processors

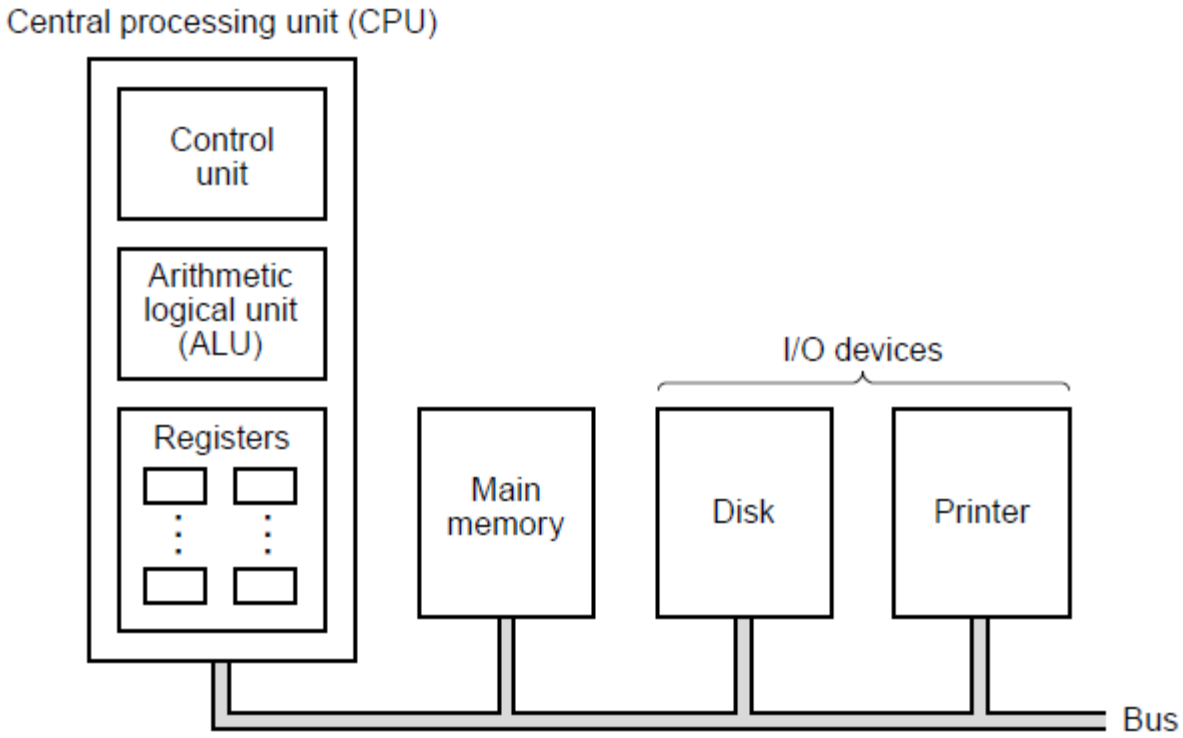


Figure 1. The organization of a simple computer with one CPU and two I/O devices.

CPU Organization

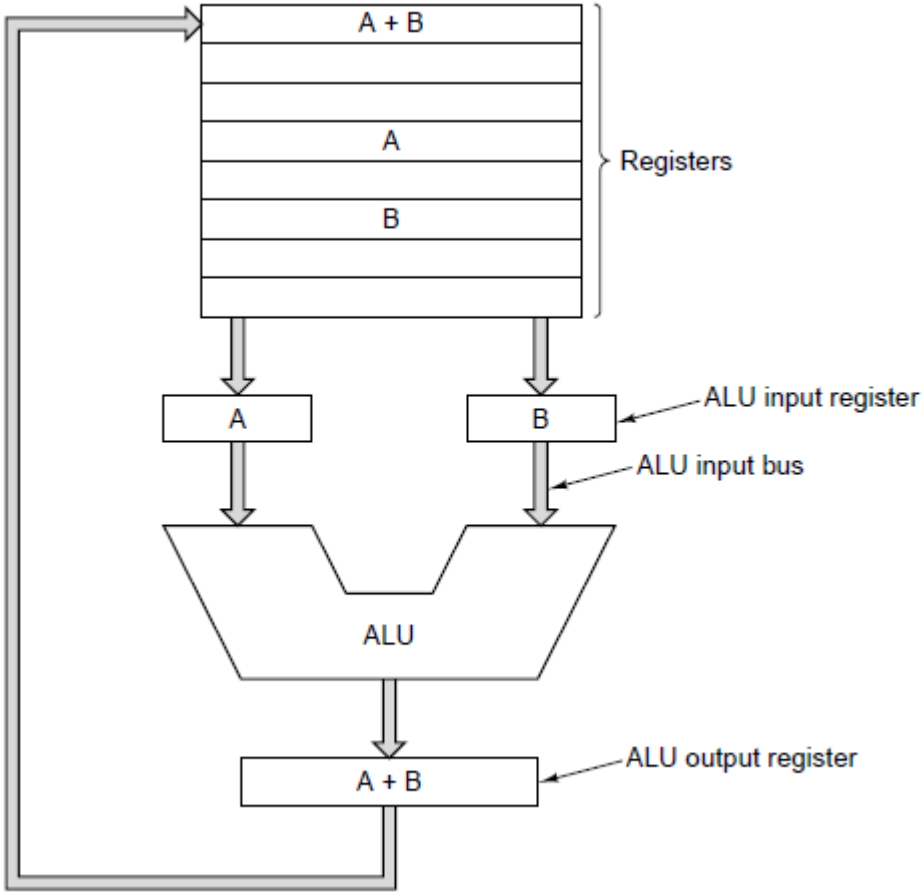


Figure 2. The data path of a typical von Neumann machine.

Design Principles for Modern Computers

- All instructions directly executed by hardware
- Maximize rate at which instructions are issued
- Instructions should be easy to decode
- Only loads and stores should reference memory
- Provide plenty of registers

Pipelining

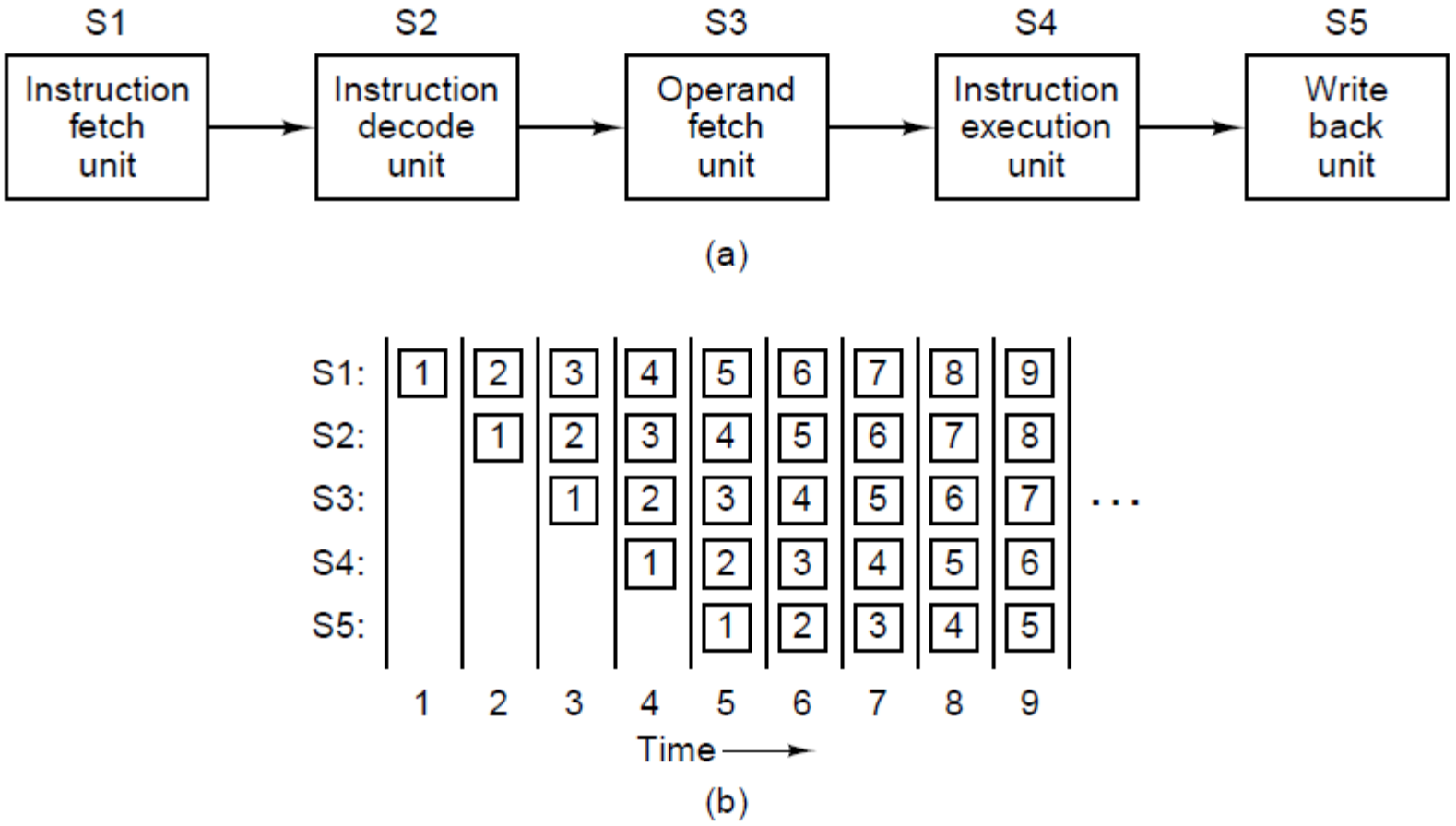


Figure 3. (a) A five-stage pipeline. (b) The state of each stage as a function of time. Nine clock cycles are illustrated

Superscalar Architectures (1)

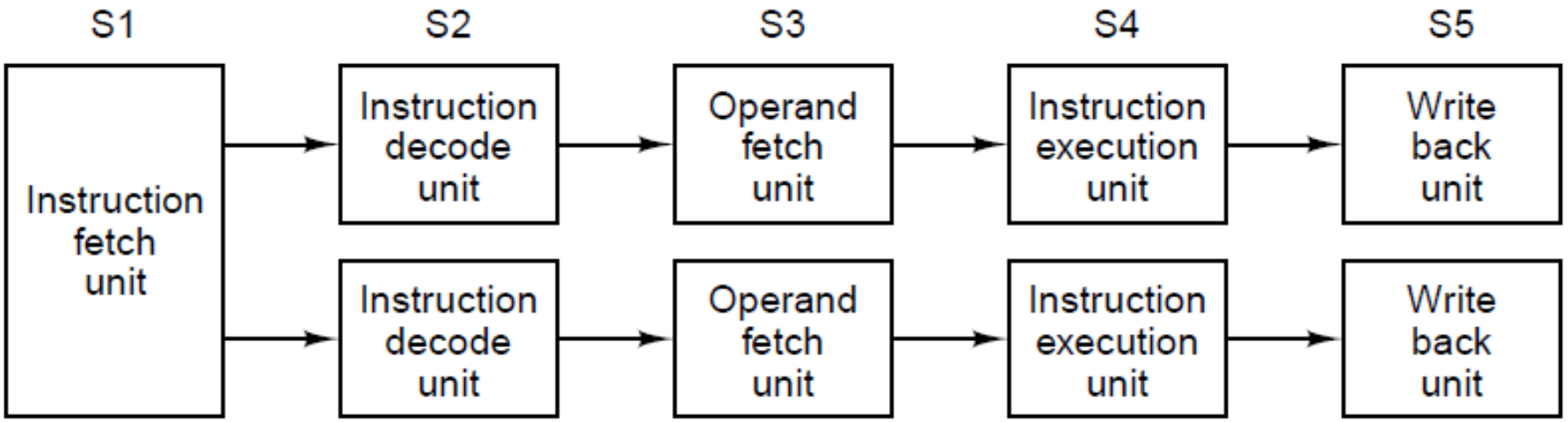


Figure 4. Dual five-stage pipelines
with a common instruction fetch unit.

Superscalar Architectures (2)

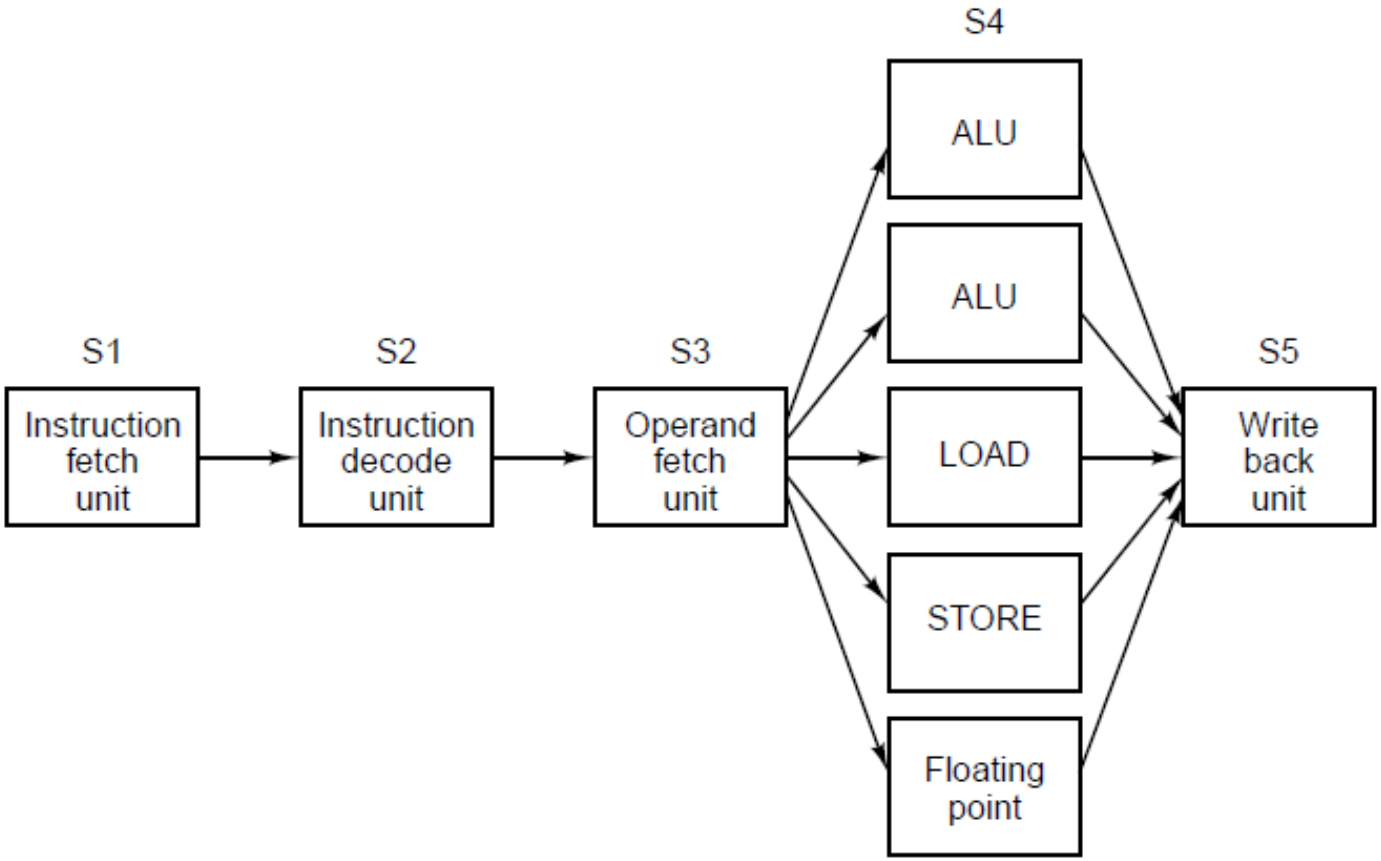


Figure 5. A superscalar processor with five functional units.

Data Parallel Computers

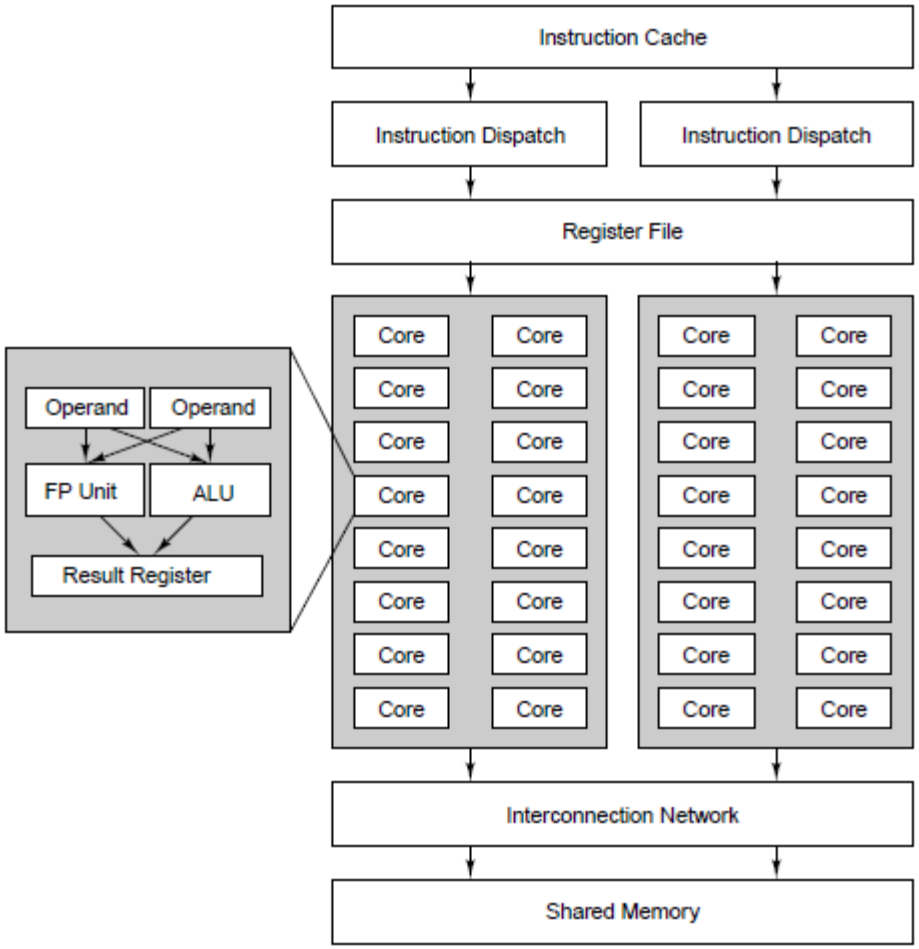


Figure 6. The SIMD core of the graphics processing unit.

Multiprocessors (1)

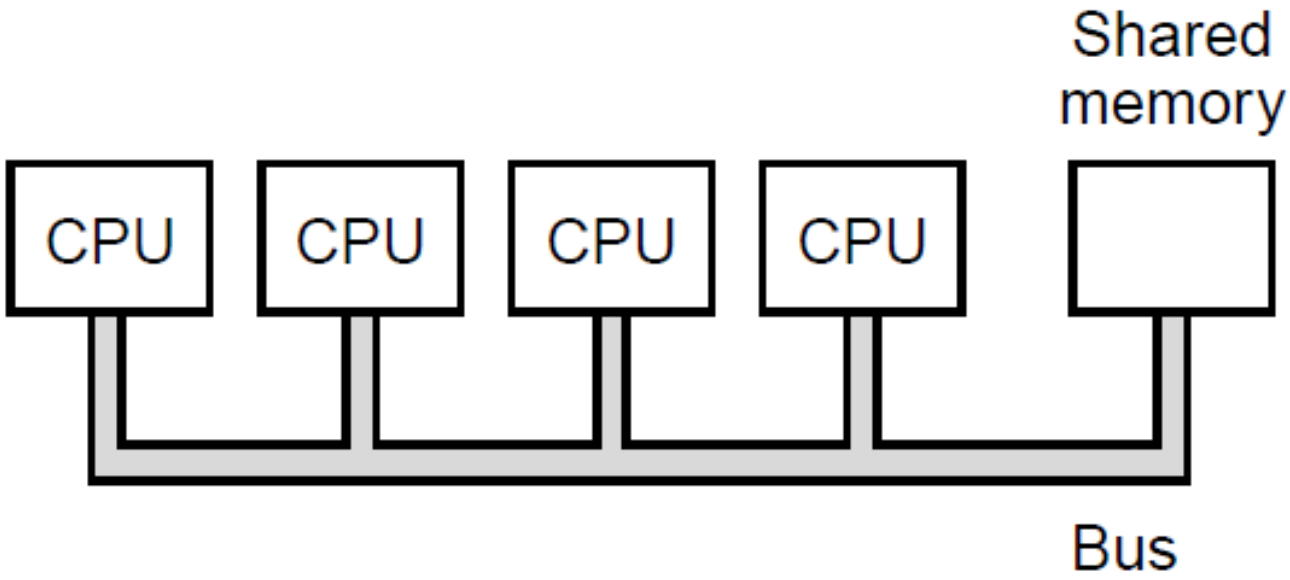


Figure 7. (a) A single-bus multiprocessor.

Multiprocessors (1)

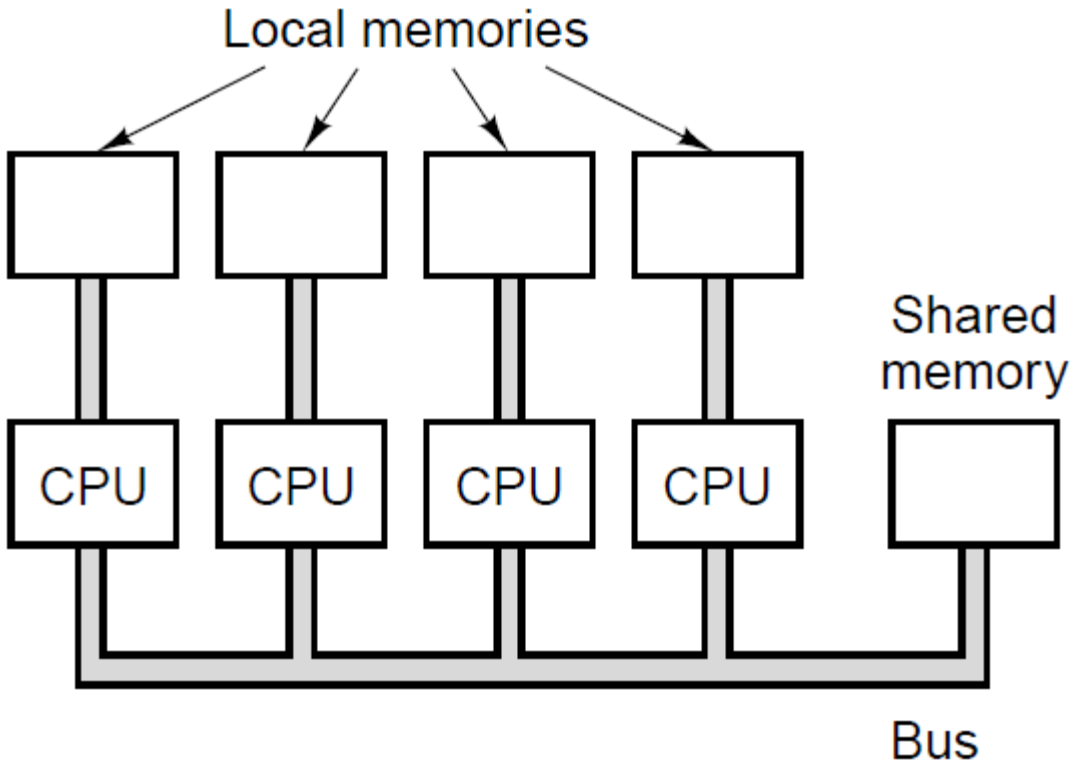


Figure 7(b). A multicomputer with local memories.

Buses

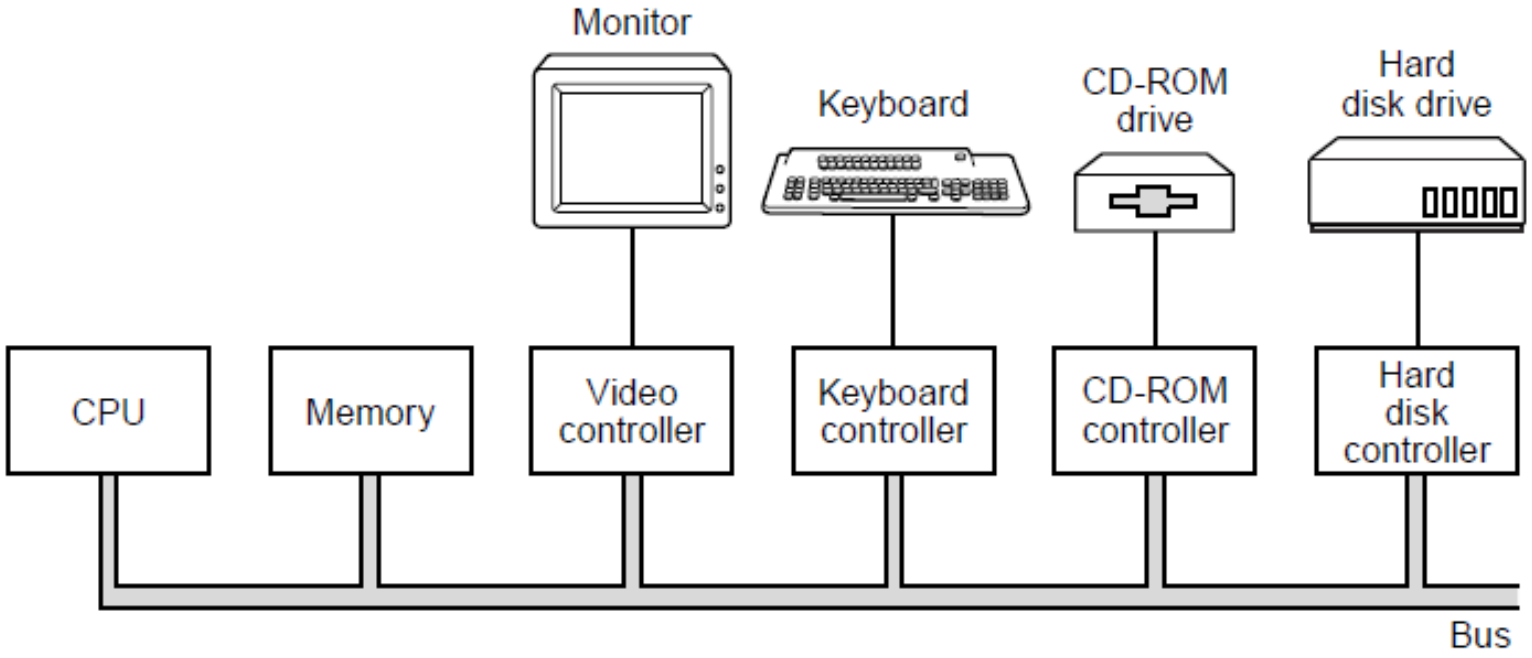


Figure 8. Logical structure of a simple personal computer.

PCI Bus

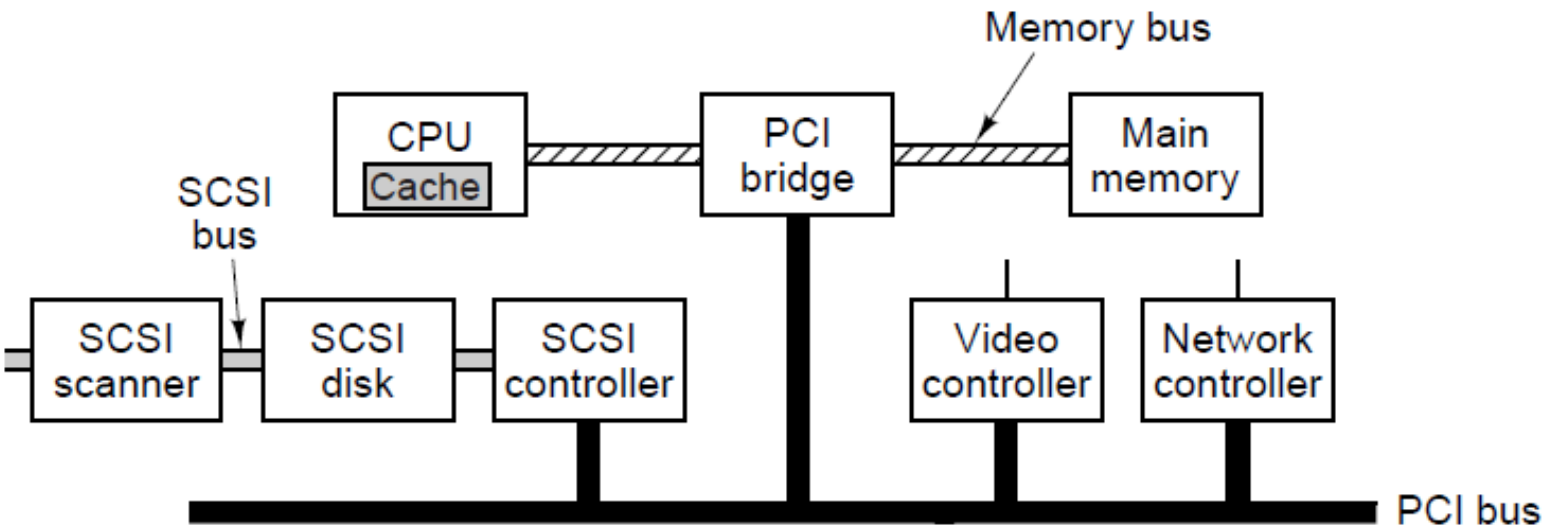
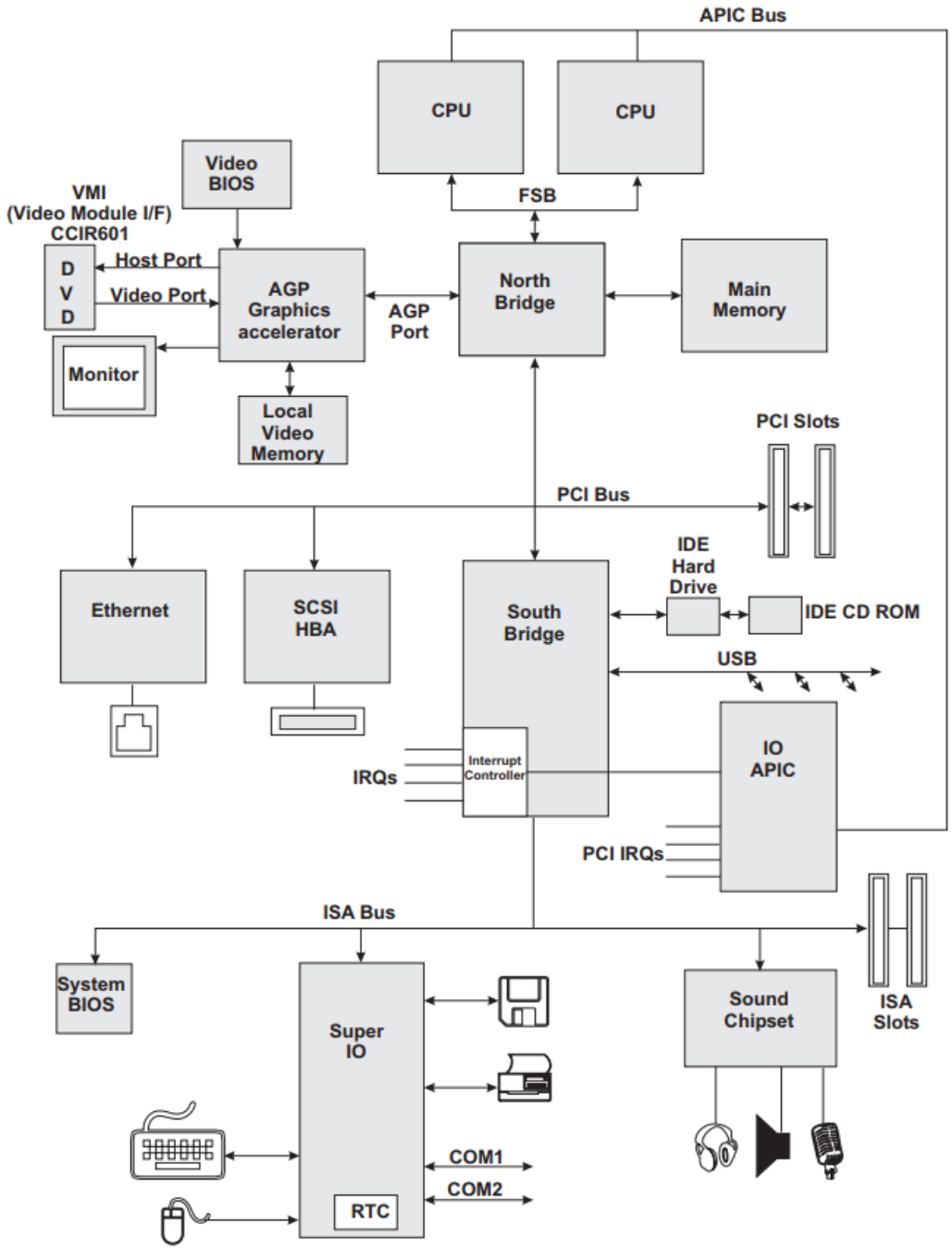


Figure 9. A typical PC built around the PCI bus


APIC Bus
CPU
CPU
FSB
Video BIOS
VMI (Video Module I/F) CCIR601
D V D
Host Port
Video Port
AGP Graphics accelerator
AGP Port
North Bridge
Main Memory
Monitor
Local Video Memory
PCI Slots
PCI Bus
Ethernet
SCSI HBA
South Bridge
IDE Hard Drive
IDE CD ROM
USB
Interrupt Controller
IRQs
IO APIC
PCI IRQs
ISA Bus
System BIOS
Super IO
Sound Chipset
ISA Slots
COM1
COM2
RTC

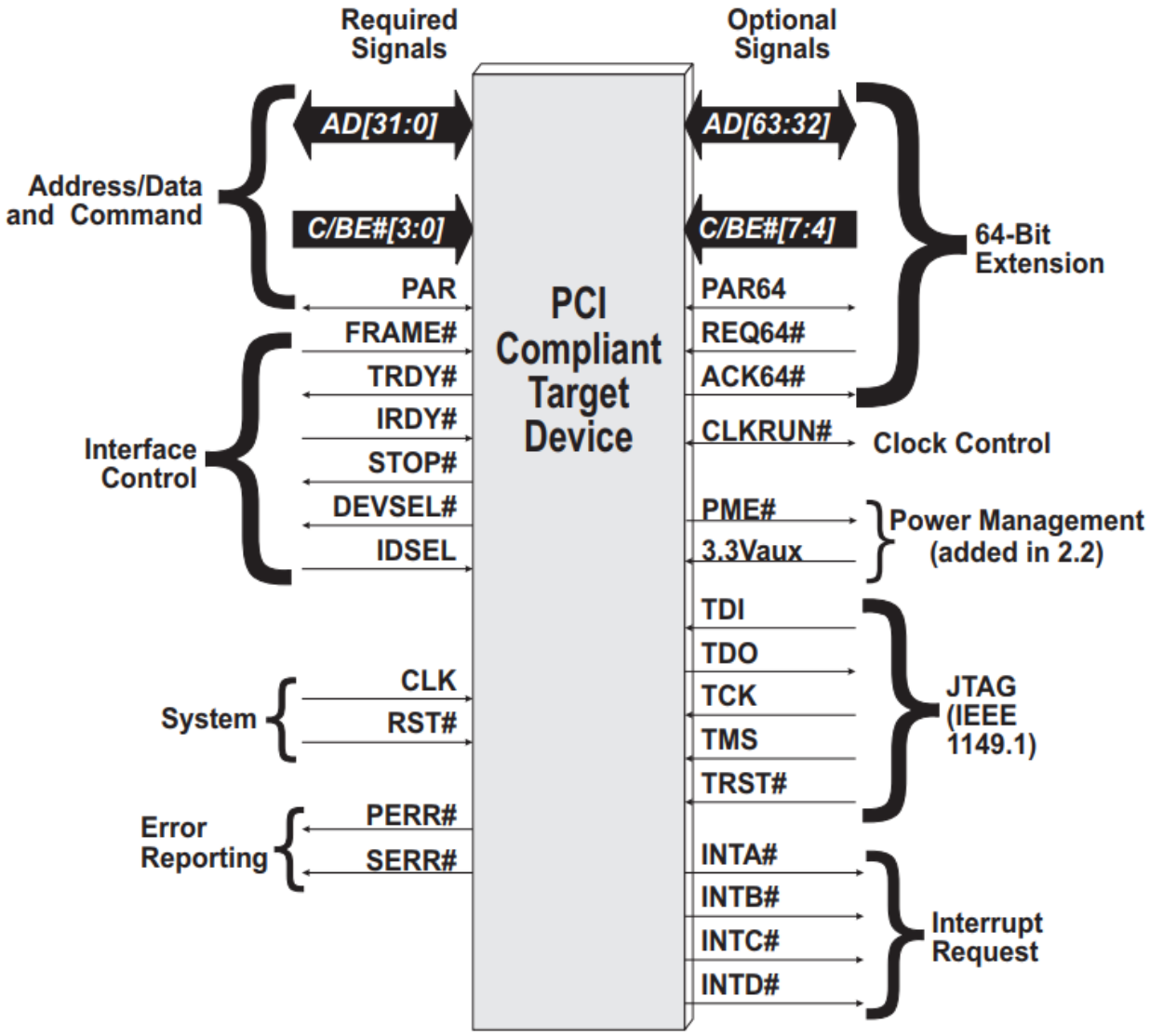
PCI

- PCI (Peripheral Component Interconnect)
- Developed by Intel(1993)
- Used for interfacing processor with its chipset
  - Synchronous Bus Architecture.
  - PCI operates at 66MHz and at 33MHz.
  - Plug-and-Play(PnP).

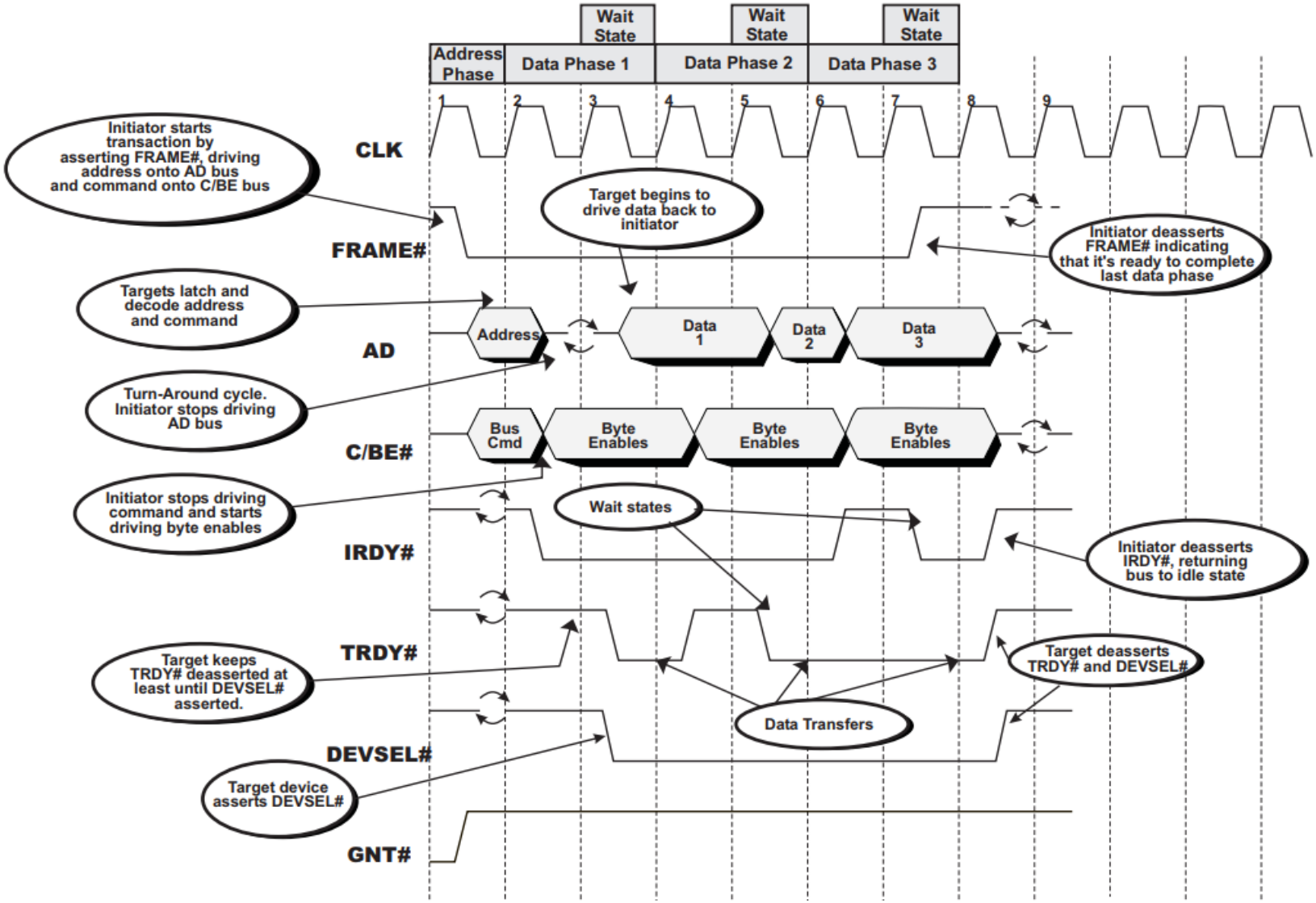
PCI

Bus Type	Bus Width	Bus Speed	MB/sec
PCI	32 bits	33 MHz	132 MBps
PCI	64 bits	33 MHz	264 MBps
PCI	64 bits	66 MHz	512 MBps
PCI	64 bits	133 MHz	1 GBps

PCI Signal Groups



Typical PCI Transaction



PCI Signals

Clock and Reset

- **CLK**
  - *— PCI input clock*
  - *— All signals sampled on rising edge*
  - *— 33MHz is really 33.33333MHz (30ns clk. period)*
  - *— The clock is allowed to vary from 0 to 33 MHz*
- **RST#**
  - *— Asynchronous reset*
  - *— PCI device must tri-state all I/Os during reset*

The revision 2.1 specification: support clk frequency up to 66 MHz.

PCI Signals

- **TRDY# – I/O**
  - — *"T-Ready"*
  - — *When the target asserts this signal, it tells the initiator that it is ready to send or receive data*
- **STOP# – I/O**
  - — *Used by target to indicate that it needs to terminate the*
  - *transaction*

PCI Signals

- **DEVSEL# – I/O**
  - — *Device select*
  - — *Part of PCI's distributed address decoding*
    - – Each target is responsible for decoding the address associated with each transaction
    - – When a target recognizes its address, it asserts DEVSEL# to claim the corresponding transaction

PCI Signals

- **FRAME# – I/O**
  - — *Signals the start and end of a transaction*
- **IRDY# – I/O**
  - — *"I-Ready"*
  - — *Assertion by initiator indicates that it is ready to send receive data*
- **IDSEL**
  - — *Individual device select for configuration – one unique IDSEL line per agent*

PCI Signals

- **AD[31:0] – I/O**
  - *— 32-bit address/data bus*
  - *— PCI is little endian (lowest numeric index is LSB)*
- **C/BE#[3:0] – I/O**
  - *— 4-bit command/byte enable bus*
  - *— Defines the PCI command during address phase*
  - *— Indicates byte enable during data phases*
    - – Each bit corresponds to a "byte-lane" in AD[31:0] – for example,C/BE#[0] is the byte enable for AD[7:0]

PCI Signals

- **PAR – I/O**
  - *— Parity bit*
  - *— Used to verify correct transmittal of address/data and command/byte-enable*
  - *— The XOR of AD[31:0], C/BE#[3:0], and PAR should return zero (even parity)*
    - – In other words, the number of 1's across these 37 signals should be even

PCI Signals

- **REQ# – O**
  - — *Asserted by initiator to* **request** *bus ownership*
  - — *Point-to-point connection to arbiter – each initiator has its own REQ# line*
- **GNT# – I**
  - — *Asserted by system arbiter to* **grant** *bus ownership to the initiator*
  - — *Point-to-point connection from arbiter – each initiator has its own GNT# line*
- **PERR# – I/O**
  - — *Indicates that a data* **parity error** *has occurred*
  - — *An agent that can report parity errors can have its PERR# turned off during PCI configuration*
- **SERR# – I/O**
  - — *Indicates a serious* **system error** *has occurred*

Intro to PCI Bus Operation

Example Burst Data Transfer

Intro to PCI Bus Operation

- **Initiator**
- — *Or Master*
- — *Owns the bus and initiates the data transfer*
- — *Every Initiator must also be a Target*
- **Target**
- — *Or Slave*
- — *Target of the data transfer (read or write)*
- **Agent**
- — *Any initiator/target or target on the PCI bus*

Single vs. Multi-Function PCI Devices

- A package containing one function is referred to as a **single-function** PCI **device**,
- while a package containing two or more PCI functions is referred to as a **multi-function PCI device**.