CPE 186 Computer Hardware Design

Early Transaction End – Part 1

Master-Initiated Termination

The initiator terminates a transaction for one of four reasons:

- 1. The transaction has completed normally.

- 2. The initiator has already used up its the slice and has been living on borrowed time and is then preempted by the arbiter (because one or more other bus masters are requesting the bus) before it completes its burst transfer.
  - The initiator's Latency Timer expired some time ago and the arbiter has now removed the initiator's bus grant signal (GNT#).

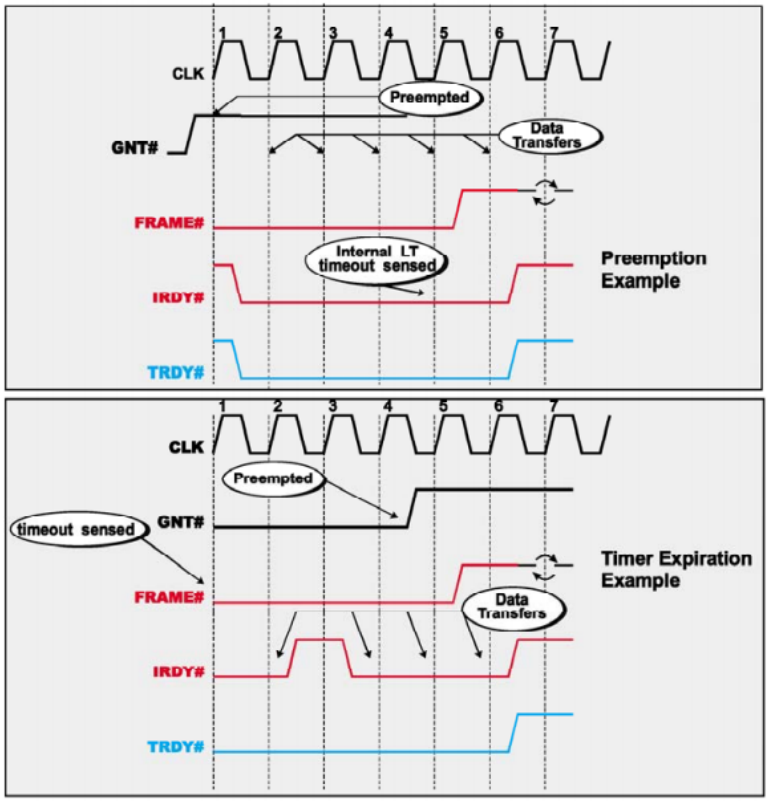
Master-Initiated Termination

The initiator terminates a transaction for one of four reasons:

- 3. The Initiator is preempted during its time slice and then uses up its allotted time slice before completing its overall transfer.

- 4. The initiator has aborted the transaction because no target has responded to the address. This is referred to as a Master Abort.

Master-Initiated Termination Due to Preemption and Master Latency Timer Expiration



Master Abort: Target Doesn't Claim Transaction

Generally speaking, a Master Abort occurs when the transaction is not claimed by a target (DEVSEL# is not sampled asserted).

This could occur for a number of reasons:

- Addressing Non-Existent Device
- Normal Response To Special Cycle Transaction (message broadcasting)
- Configuration Transaction Unclaimed
- No Target Will Claim Transaction Using Reserved Command

Master Abort On Single vs. Multiple-Data Phase Transaction

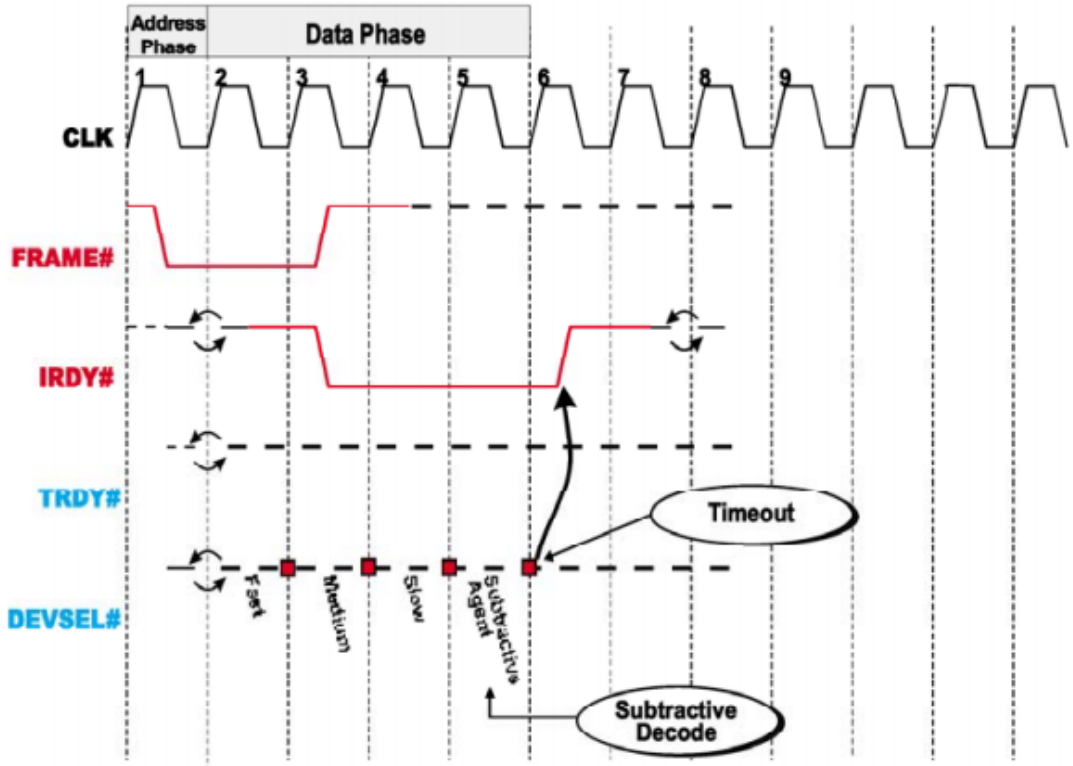
Two possible cases:

- CASE 1. The initiator starts a single data phase transaction and aborts it due to DEVSEL# not detected.

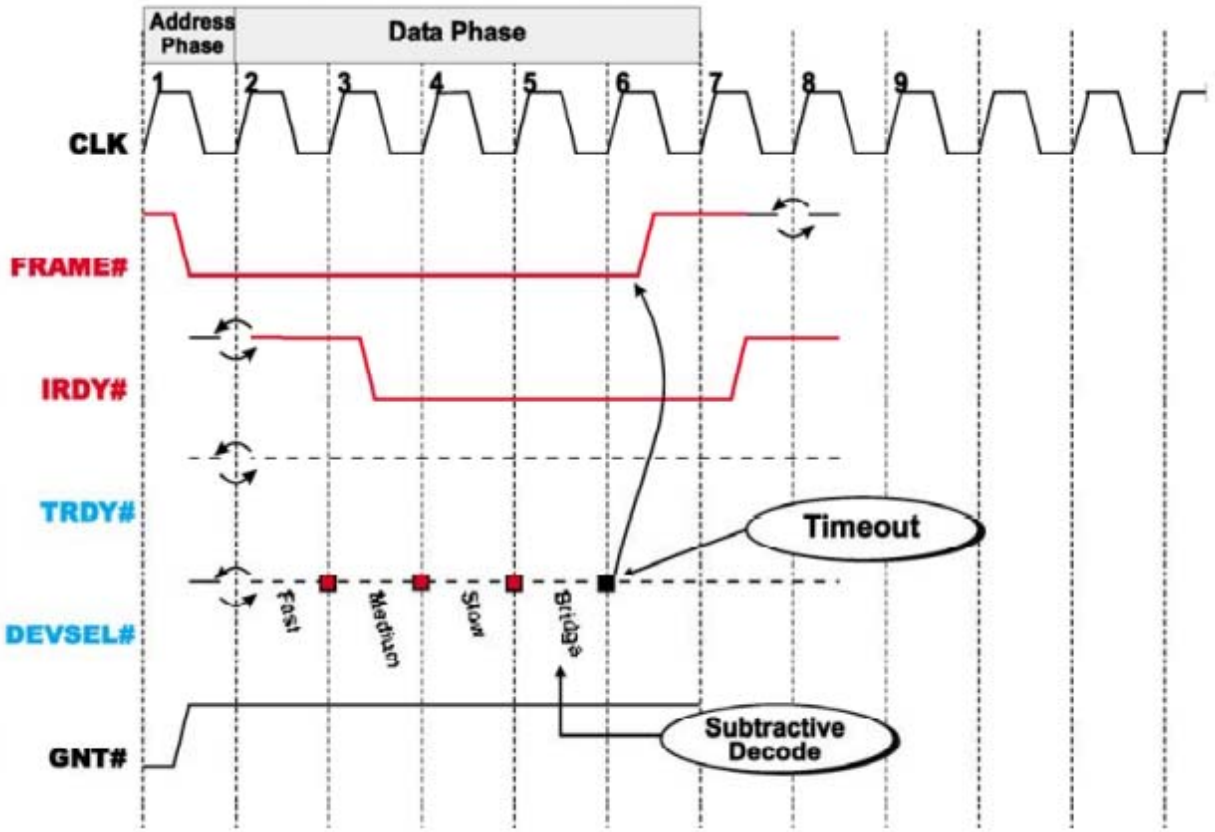
- CASE 2. The initiator starts a multi-data phase transaction and aborts it due to DEVSEL# not detected.

Master Abort on Single Data Phase Transaction

Figure : Example of Master Abort on Single-Data Phase Transaction
(note: this is not a special cycle)



Master Abort on Multi-Data Phase Transaction



Action Taken by Master In Response to Master Abort

General

- Set the Received Master Abort bit in its configuration Status register
- Report the error back to the device driver (typically, via an interrupt request).

Master Abort On Special Cycle Transaction

- The Received Master Abort status bit should not be set.
- No target is expected to assert DEVSEL# during a Special Cycle and it would be a protocol violation if one did.

Master Abort On Configuration Access

- When a Master Abort occurs on a configuration read, the host/PCI bridge must return all ones to the processor.
- On a configuration write, the processor write is permitted to terminate normally (i.e.. as if the data were successfully written).
- This is considered to be an error and the master must set the Received Master Abort bit in its Status register.