PCI Commands & Read Transfers

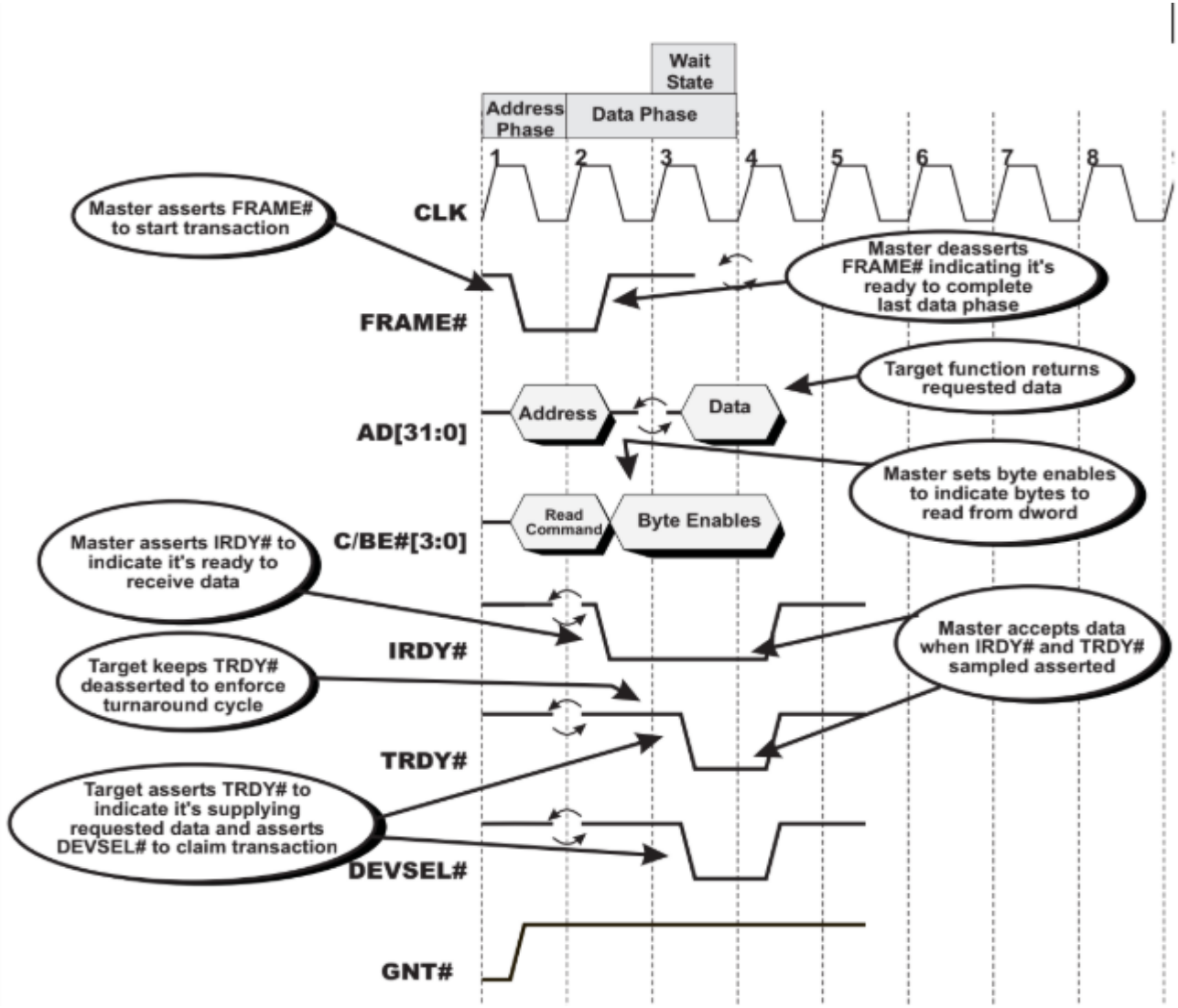
CPE186 Computer Hardware Design

Handout

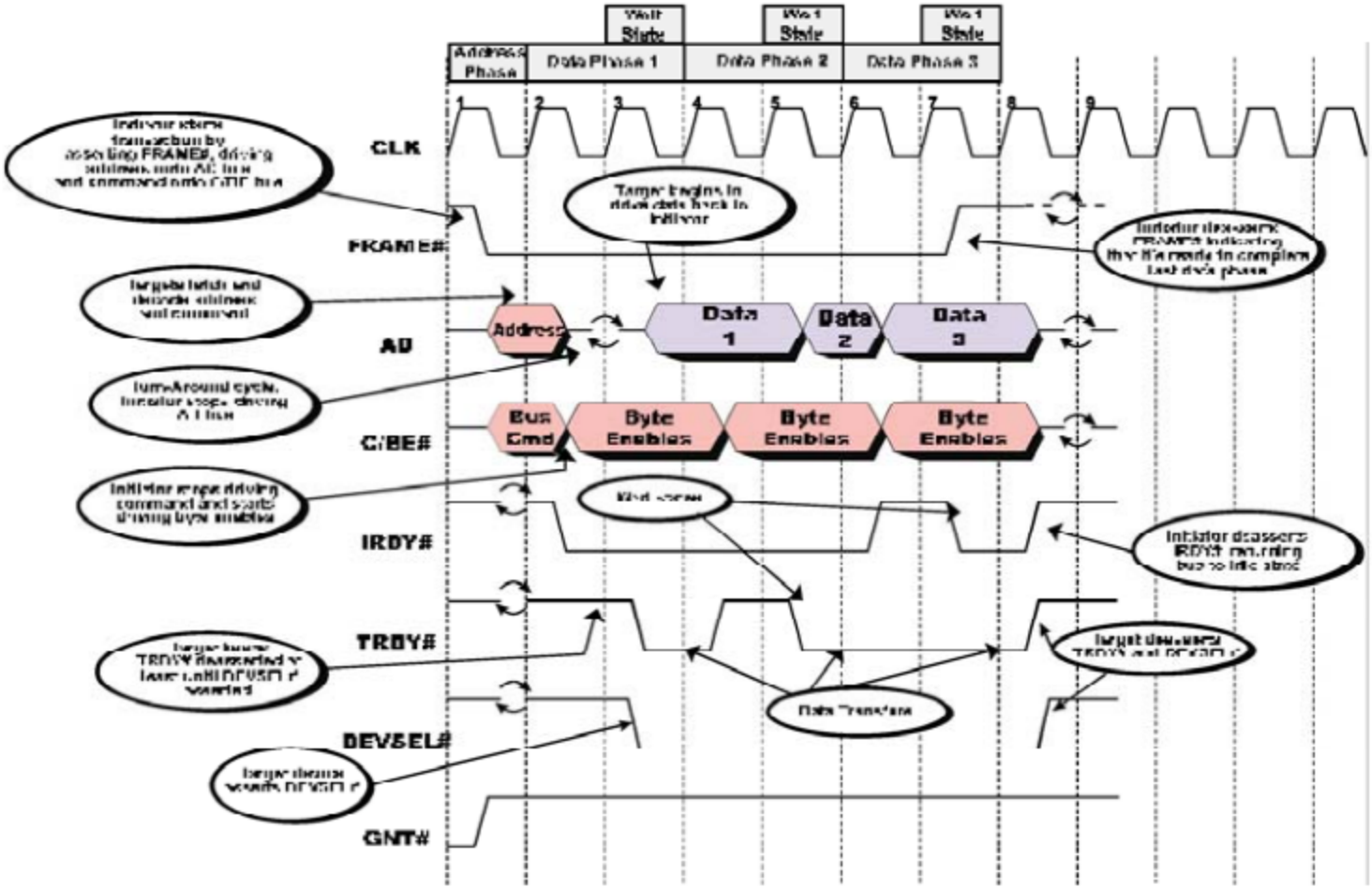
PCI Command Types

C/BE[3:0]# (binary)	Command Type
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write-and-Invalidate

Single Data Phase Read



Burst Read Transaction



Byte Enables

Byte Enables May Change In Each Data Phase

- PCI permits burst transactions where the byte enables change from one data phase to the next.

- The initiator may use any byte enable setting, consisting of contiguous or noncontiguous byte enables.

- During a read transaction, the initiator will typically assert all of the byte enables during each data phase (because burst reads are typically reading a stream of dwords or quadwords), but it may use any combination.

- During a burst transfer, If all byte enables are deasserted during the data phase, then a dword will be “skipped”.

Byte Enables

Target with Limited Byte Enable Support

- IO and memory targets may support restricted byte enable settings and may respond with Target Abort for any other pattern.
- All devices must support any byte enable combination during configuration transactions.

Performance During Read Transactions

A turn-around cycle must be included in the first data transfer of a read transaction.

A single data phase read from a target always consists of at least three clock cycles (one dock cycle for the address phase and two clock cycles for the data phase).

At a clock rate of 33MHz, a read transaction consisting of a single data transfer would take 90ns to complete. An idle cycle (30 ns in duration at 33MHz) must be included between transactions, resulting in 120 ns per transaction.

Using back-to-back single data phase read transfers, the data throughput would be 8.33 million transfers per second. If each transfer involved four bytes, the resultant transfer rate would be 33.33 Mbytes per second.

Performance During Read Transactions

- In actual practice, most read transactions Involve a burst transfer of multiple objects (dwords or quadwords) between the initiator and the currently-addressed target.
- The read transaction involving multiple data phases only requires the turnaround cycle during the first data phase.
- The second through the last data phases can each be accomplished in a single clock cycle (if both the initiator and the currently-addressed target are capable of zero wait state transfers).
- The achievable transfer rate during the second through the last data phases is thus one transfer every 30ns (at a PCI bus speed of 33MHz) or 33 million transfers per second. If each data phase involves the transfer of four bytes, the resultant data transfer rate is 132Mbytes per second.

Optimized Read Transaction (no wait states)