Part 1: Synthesizable Source Code

```
//32-bit ALU

module ALU(Ctrl, a, b, r);

        //32-bit input for a and b
        input [31:0] a, b;
        //1-bit input for CTRL
        input Ctrl;

        //32-bit ouput for r
        output [31:0] r;

        reg [31:0] r;

        always@(*)
        begin
                case(Ctrl)
                        1'b0: r = a + b;
                        1'b1: r = a - b;
                endcase
        end
endmodule
```

Part 2: Test File

```
//32-bit ALU Testbench

`include "ALU.v"

module ALU_fixture;

         reg [31:0] a, b;
         reg Ctrl;

         wire [31:0] r;

         ALU uut(.a(a), .b(b), .Ctrl(Ctrl), .r(r));

         initial
         begin

                  #0 $display("Addition:");
                  #0 a = 32'hFFFFFF00;   b = 32'hFFFFFFFF; Ctrl = 1'b0;
                 #20 a = 32'hFFFFFFFF;   b = 32'h000F00FF;
                 #20 a = 32'h98998998;   b = 32'h51416270;
                 #20 a = 32'hAAAAAAAA;   b = 32'hEFABCD12;
                 #20 a = 32'hFFFFFFFF;   b = 32'h00000001;
                 #20 a = 32'hFFFFFFFF;   b = 32'hFFFFFFFF;
                 #20 a = 32'h80000000;   b = 32'hFFFFFFFF;
                  #20 $display("Subtraction:");

                  #20 a = 32'hFFFFFF00;   b = 32'hFFFFFFFF; Ctrl =
1'b1;
                 #20 a = 32'hFFFFFFFF;   b = 32'h000F00FF;
                 #20 a = 32'h98998998;   b = 32'h51416270;
                 #20 a = 32'hAAAAAAAA;   b = 32'hEFABCD12;
                 #20 a = 32'hFFFFFFFF;   b = 32'h00000001;
                 #20 a = 32'hFFFFFFFF;   b = 32'hFFFFFFFF;
                 #20 a = 32'h80000000;   b = 32'hFFFFFFFF;
                  #20 $finish;
         end
         initial
         begin
                  $monitor($time, "   %h   %h   %h     %b", a, b, r,
Ctrl);
                  $display("               Time:   A          B
Results      Ctrl");
         end

endmodule
```

Part 3: Simulation Results

```
Chronologic VCS simulator copyright 1991-2014
Contains Synopsys proprietary information.
Compiler version J-2014.12-SP3_Full64; Runtime version J-2014.12-
SP3_Full64;  Sep 27 16:52 2017
               Time:   A          B          Results      Ctrl
Addition:
                   0   ffffff00   ffffffff   ffffffeff    0
                  20   ffffffff   000f00ff   000f00fe     0
                  40   98998998   51416270   e9daec08     0
                  60   aaaaaaaa   efabcd12   9a5677bc     0
                  80   ffffffff   00000001   00000000     0
                 100   ffffffff   ffffffff   fffffffe     0
                 120   80000000   ffffffff   7fffffff     0
Subtraction:
                 160   ffffff00   ffffffff   ffffff01     1
                 180   ffffffff   000f00ff   fff0ff00     1
                 200   98998998   51416270   47582728     1
                 220   aaaaaaaa   efabcd12   bafedd98     1
                 240   ffffffff   00000001   fffffffe     1
                 260   ffffffff   ffffffff   00000000     1
                 280   80000000   ffffffff   80000001     1
$finish called from file "ALU_fixture.v", line 36.
$finish at simulation time                  300
           V C S   S i m u l a t i o n   R e p o r t
Time: 300
CPU Time:      0.250 seconds;       Data structure size:   0.0Mb
Wed Sep 27 16:52:36 2017
```