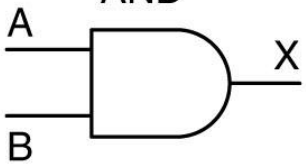
The Digital Logic Level

Chapter 3

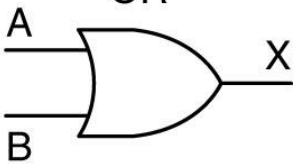
Gates and Boolean Algebra

AND



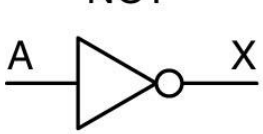
A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

OR



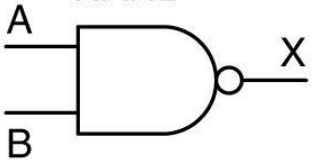
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

NOT



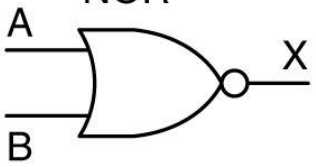
A	X
0	1
1	0

NAND



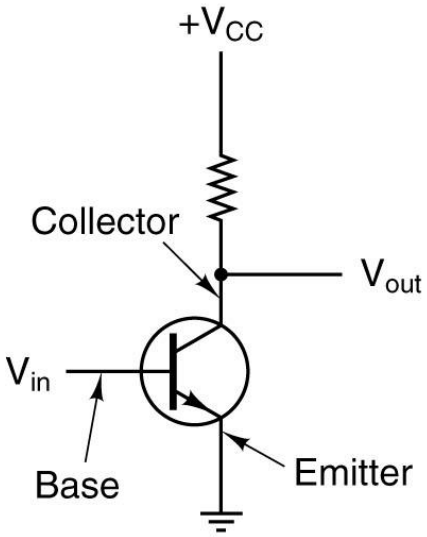
A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

NOR

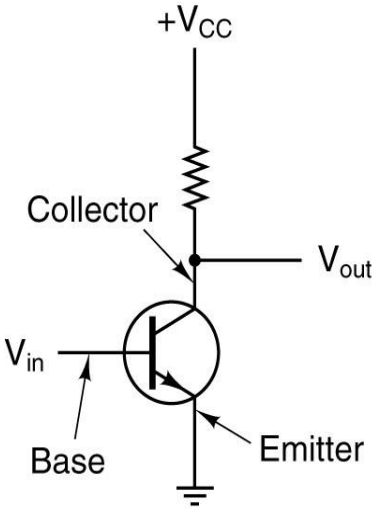


A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

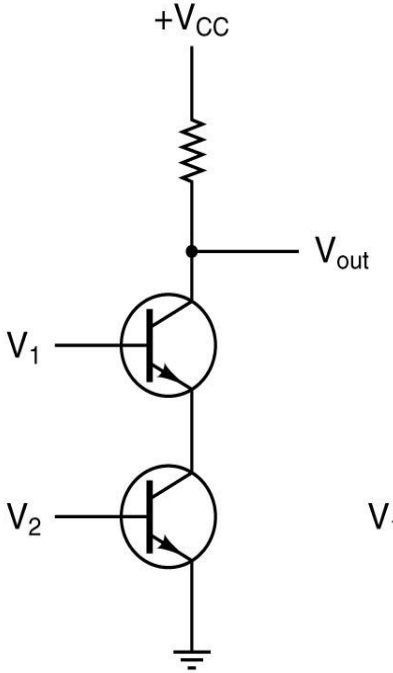
Transistor



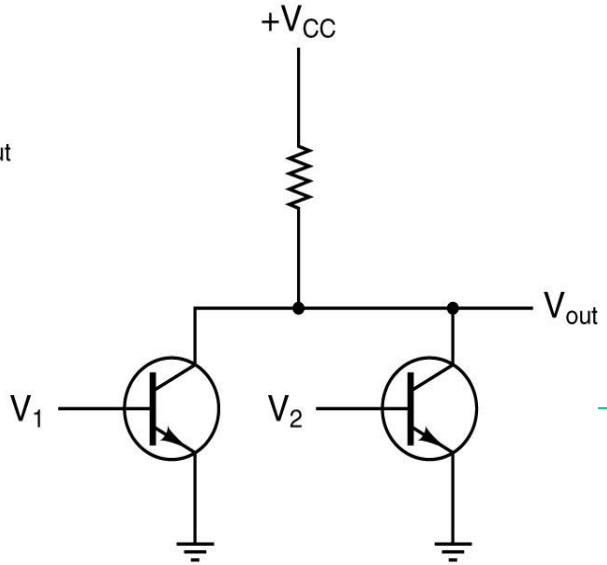
Gates and Boolean Algebra (1)



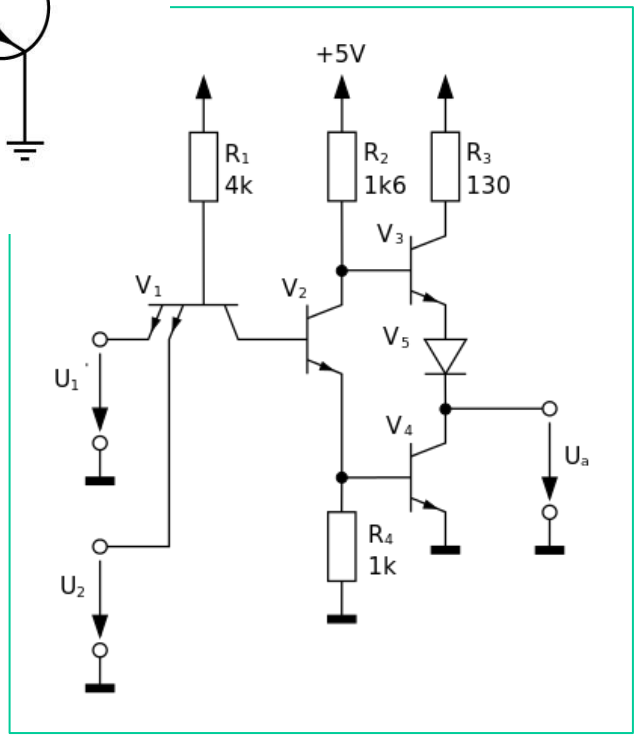
(a)



(b)



(c)

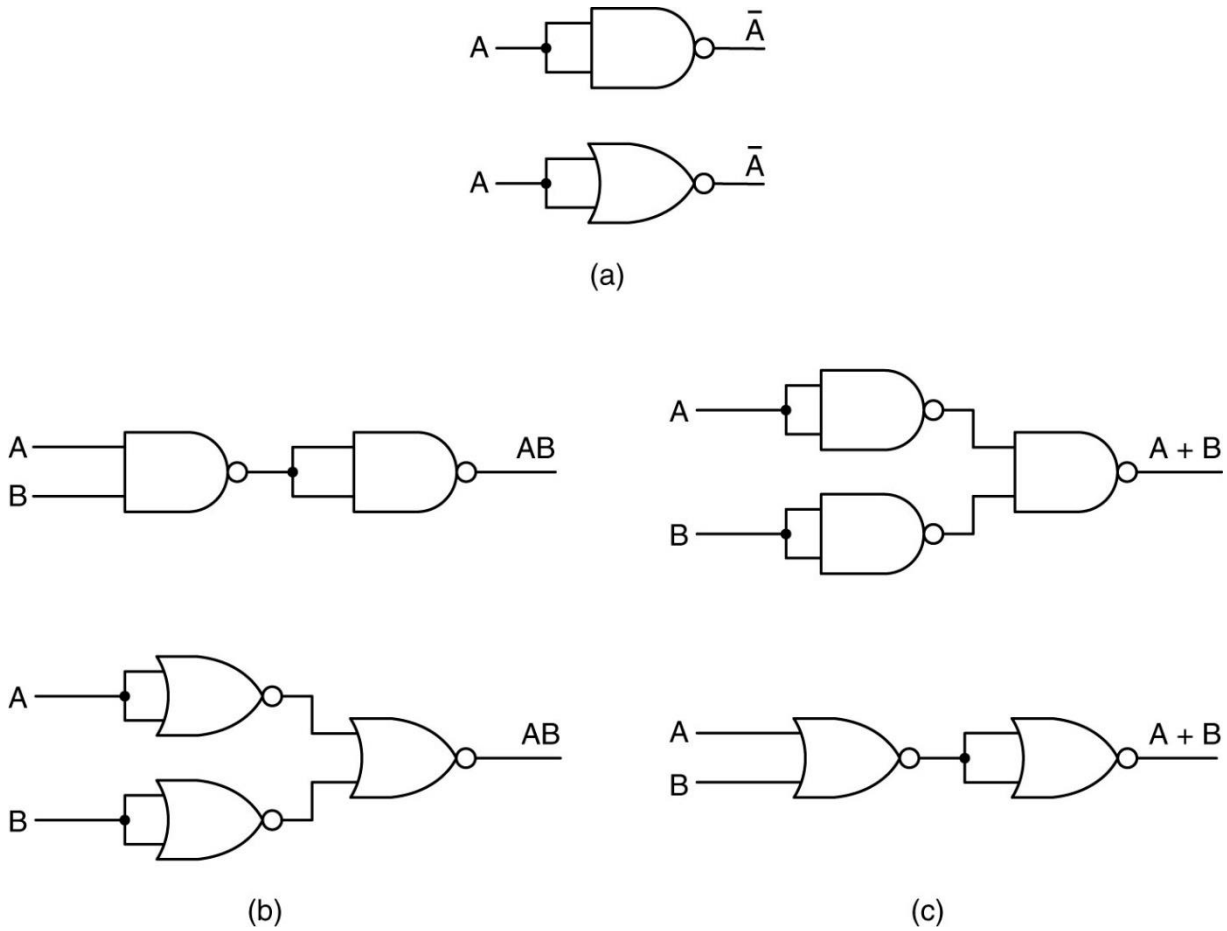


(a) A NOT gate (inverter)

(b) A NAND gate

(c) A NOR gate

Circuit Equivalence



Construction of (a) NOT, (b) AND, and (c) OR gates using only NAND gates or only NOR gates.

Positive & Negative Logic

A	B	F
0^V	0^V	0^V
0^V	5^V	0^V
5^V	0^V	0^V
5^V	5^V	5^V

(a)

A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

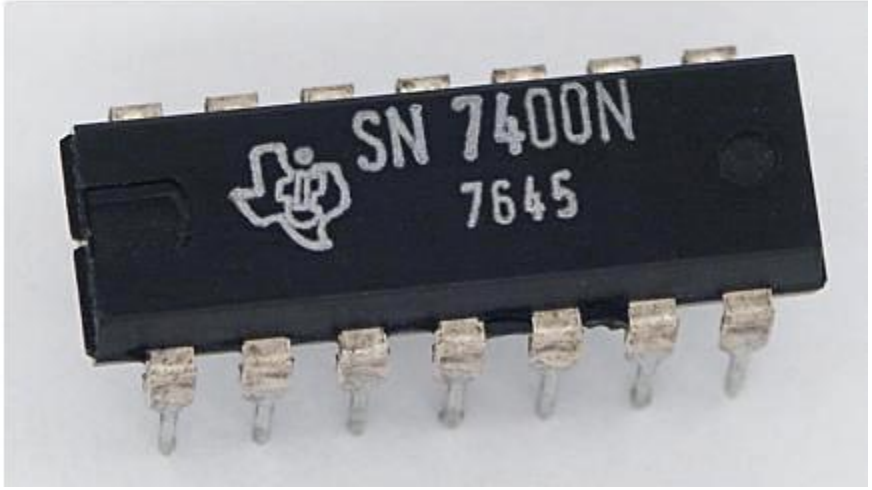
(b)

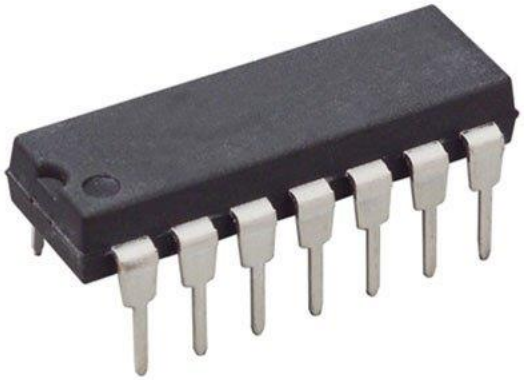
A	B	F
1	1	1
1	0	1
0	1	1
0	0	0

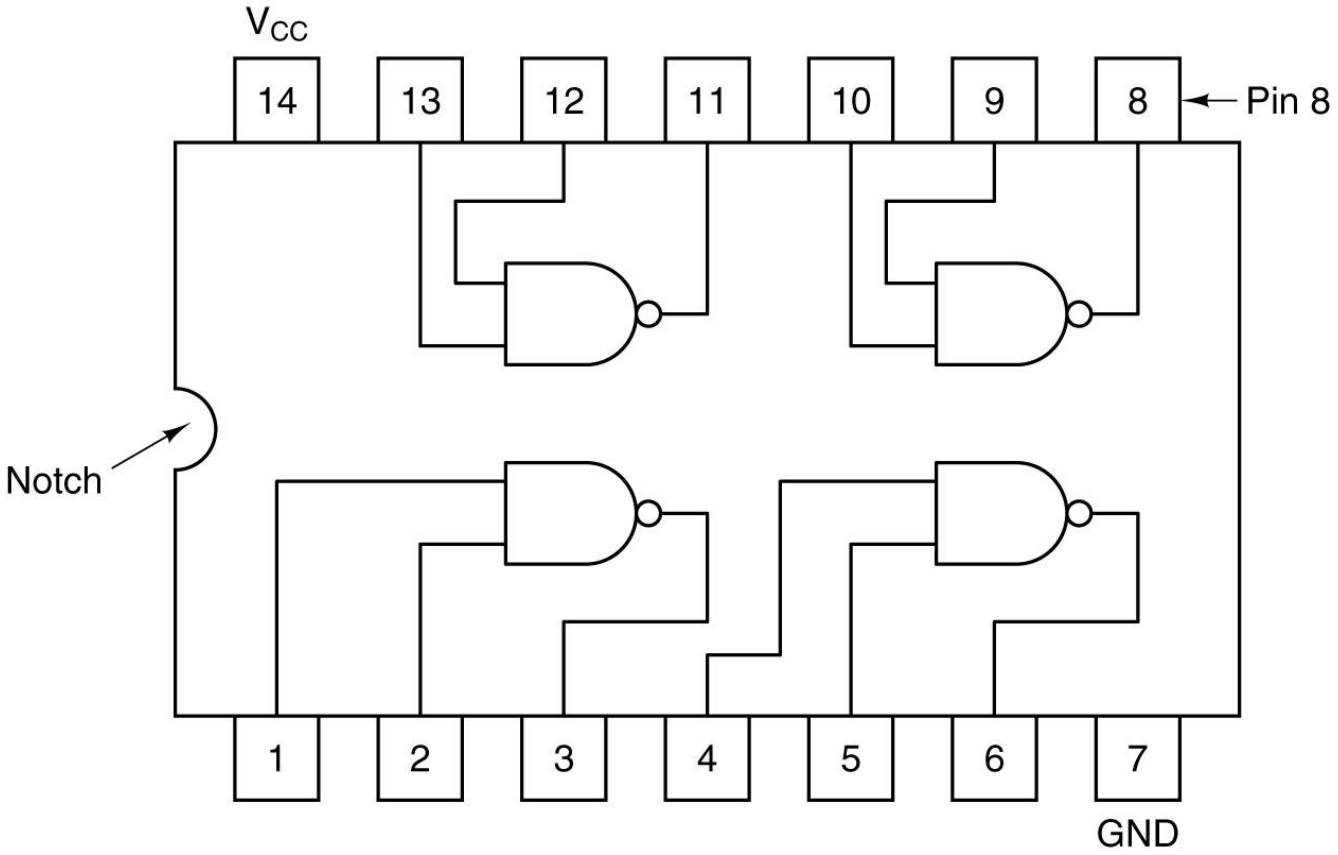
(c)

(a) Electrical characteristics of a device.
(b) Positive logic.
(c) Negative logic.

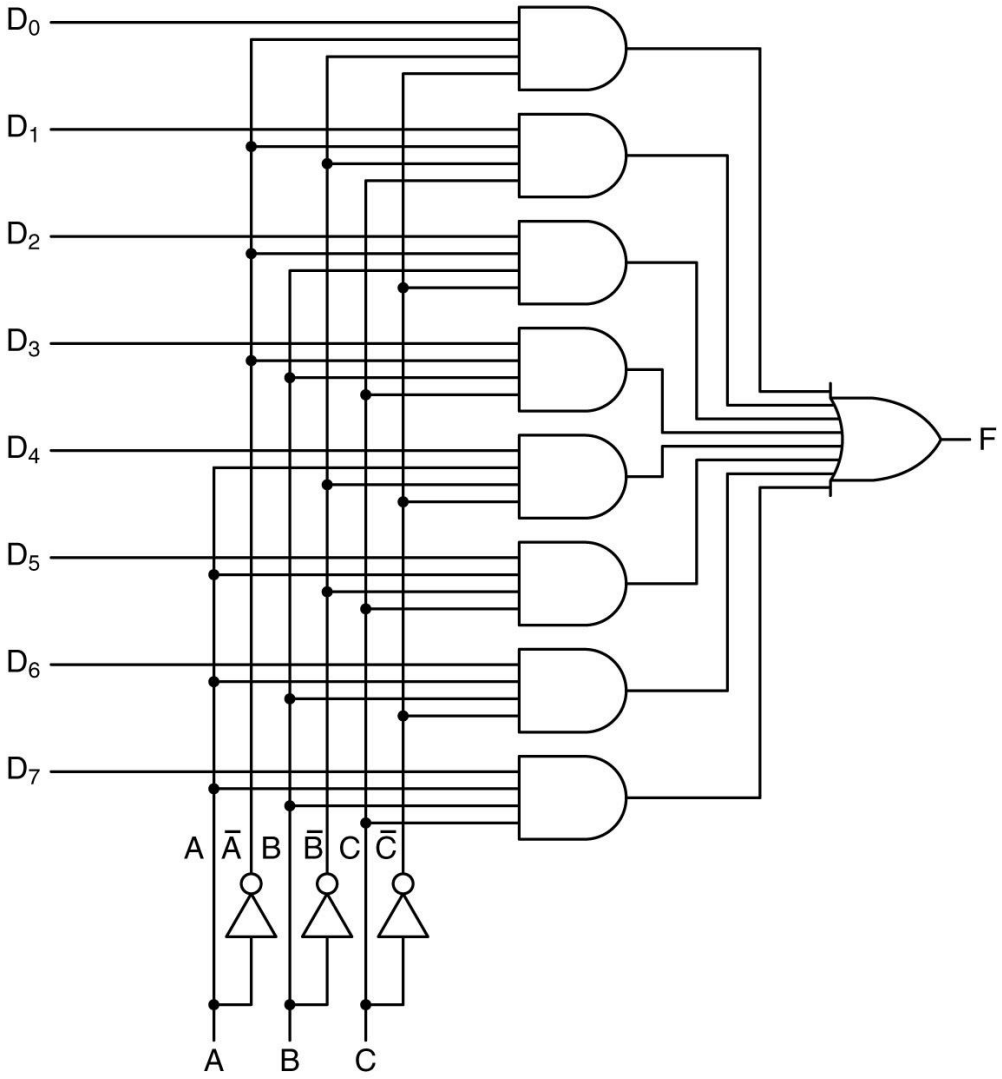
Integrated Circuits



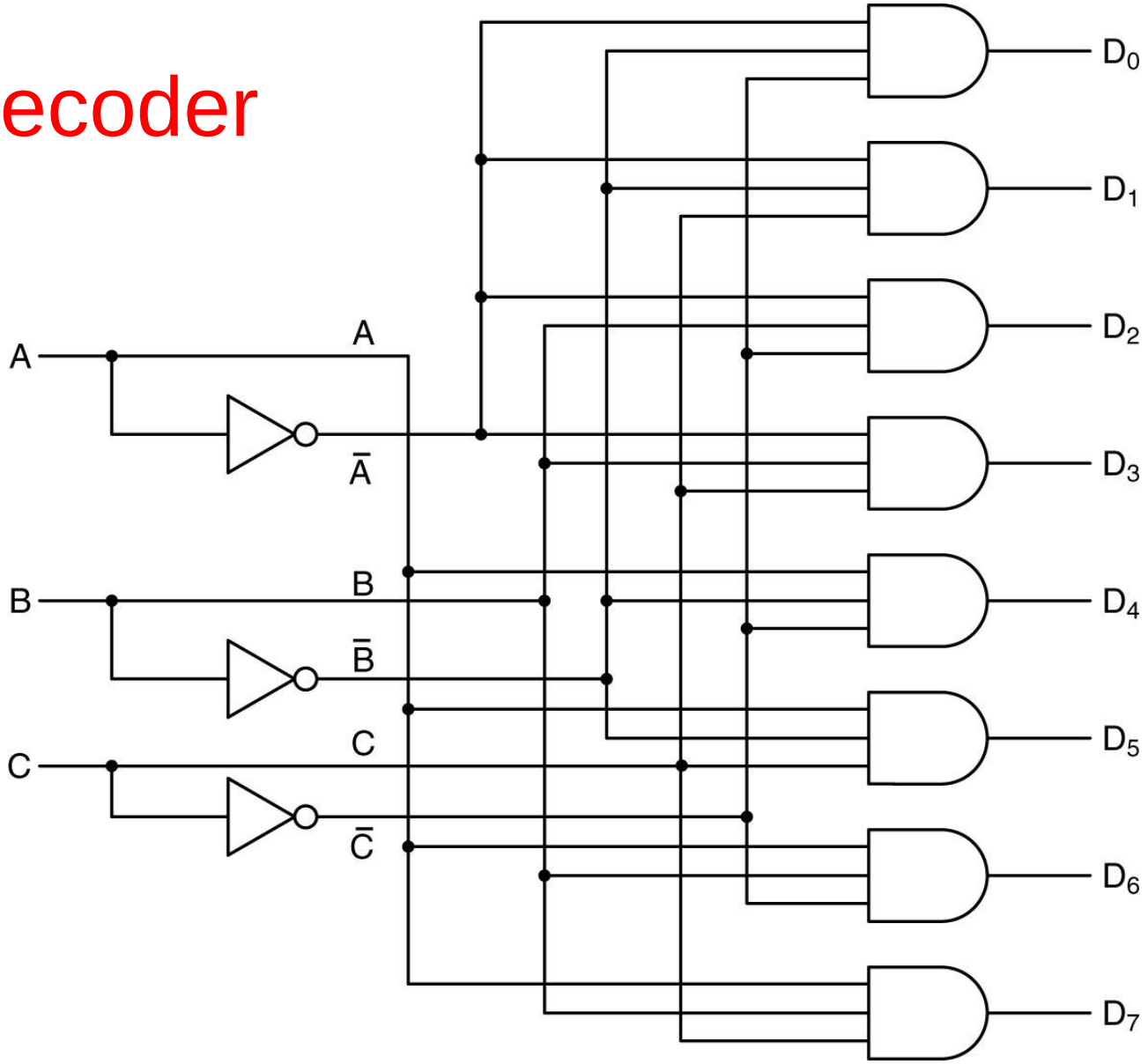




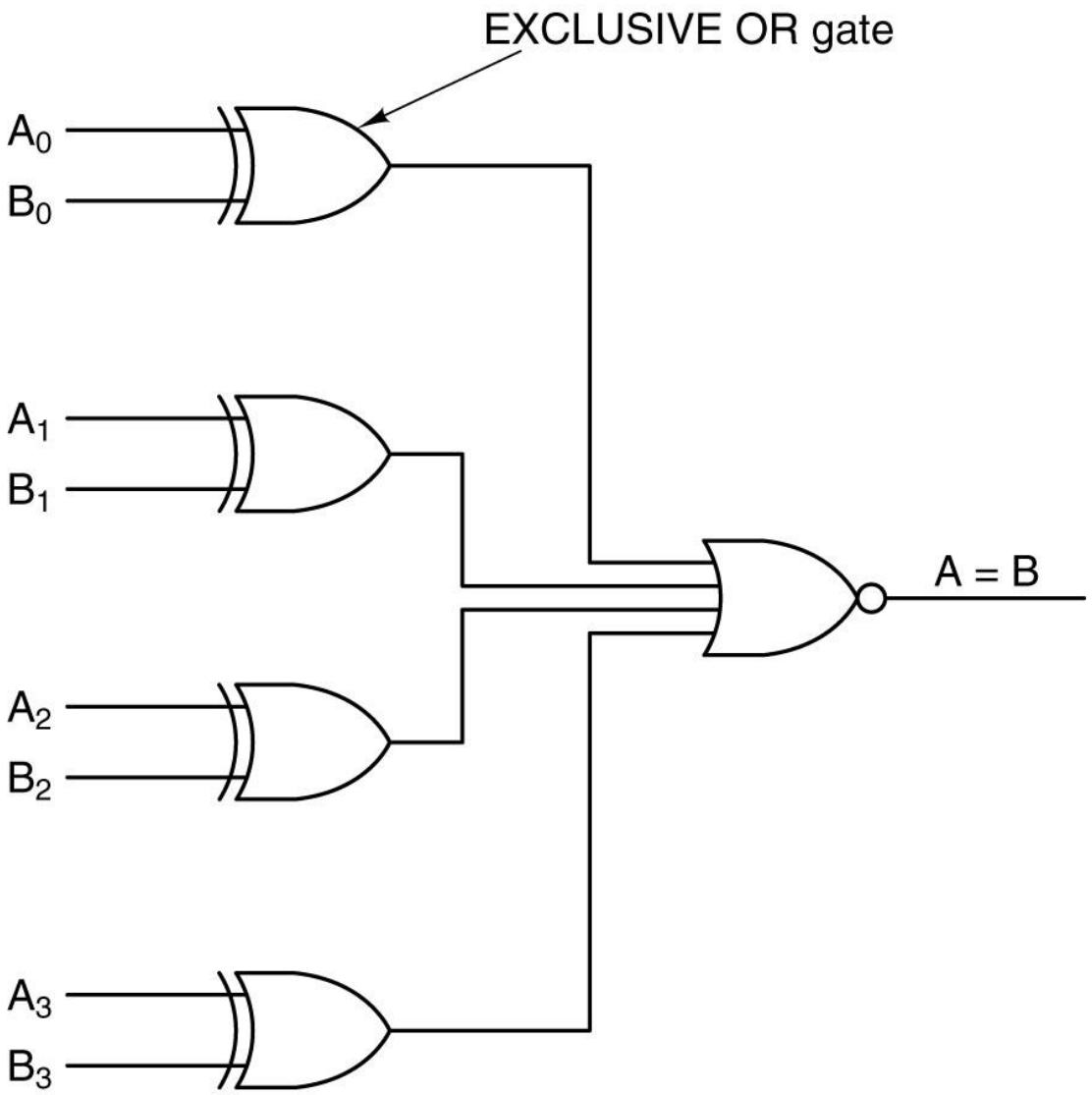
8-to-1 Multiplexer



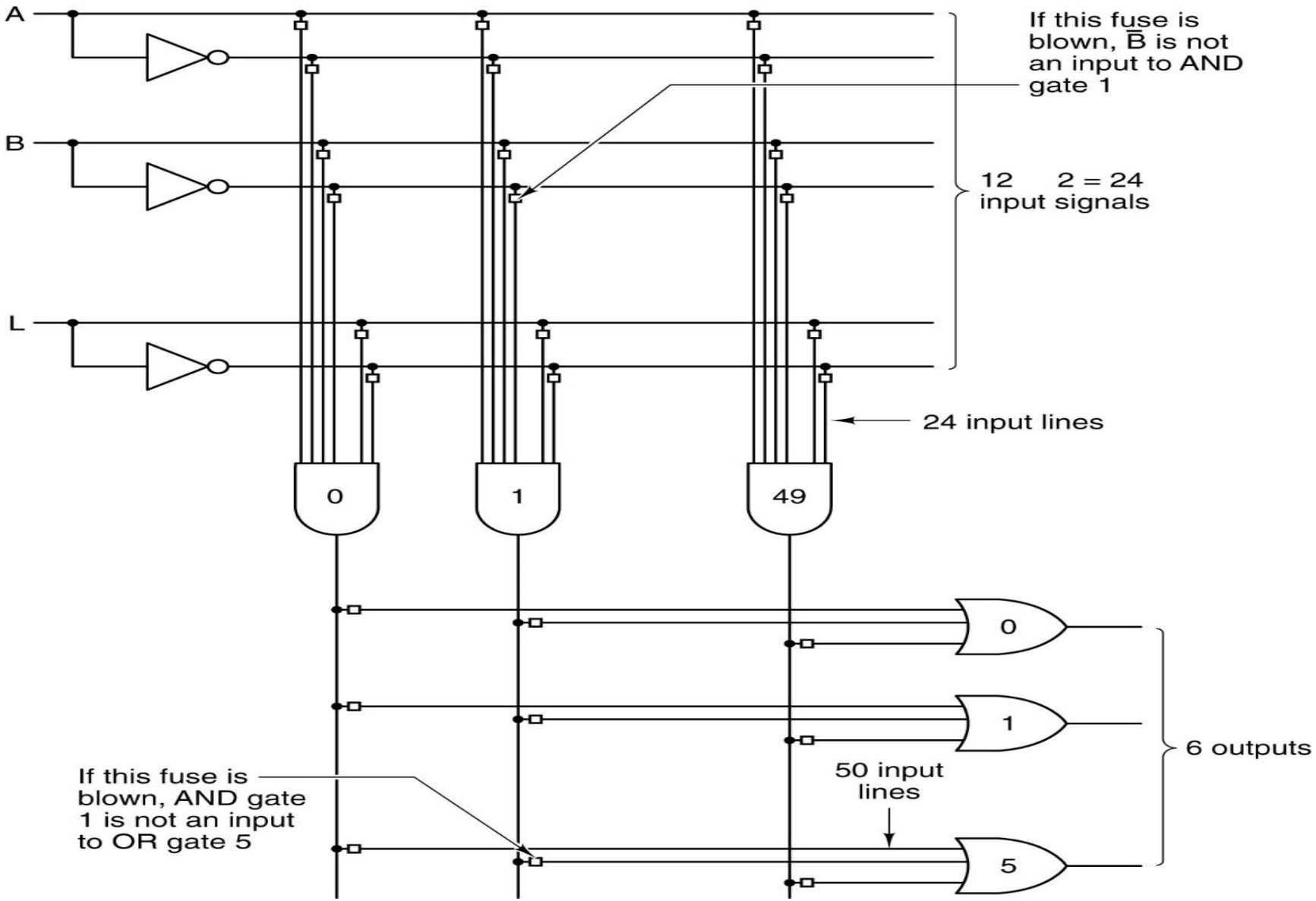
3-to-8 Decoder



4-bit Comparator



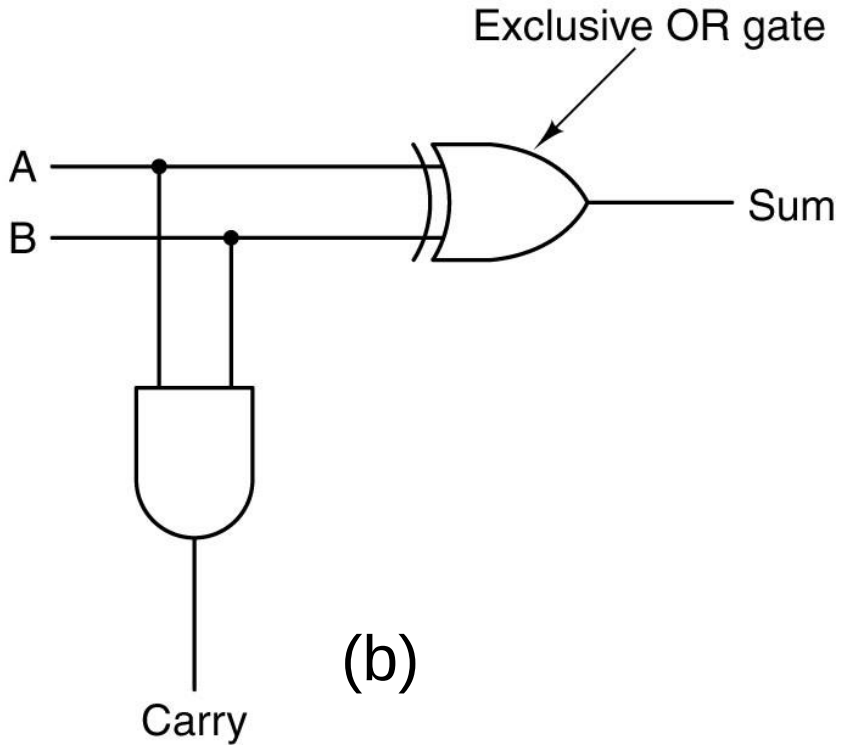
12-to-6 Programmable Logic Array (PLA)



1-bit Adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(a)

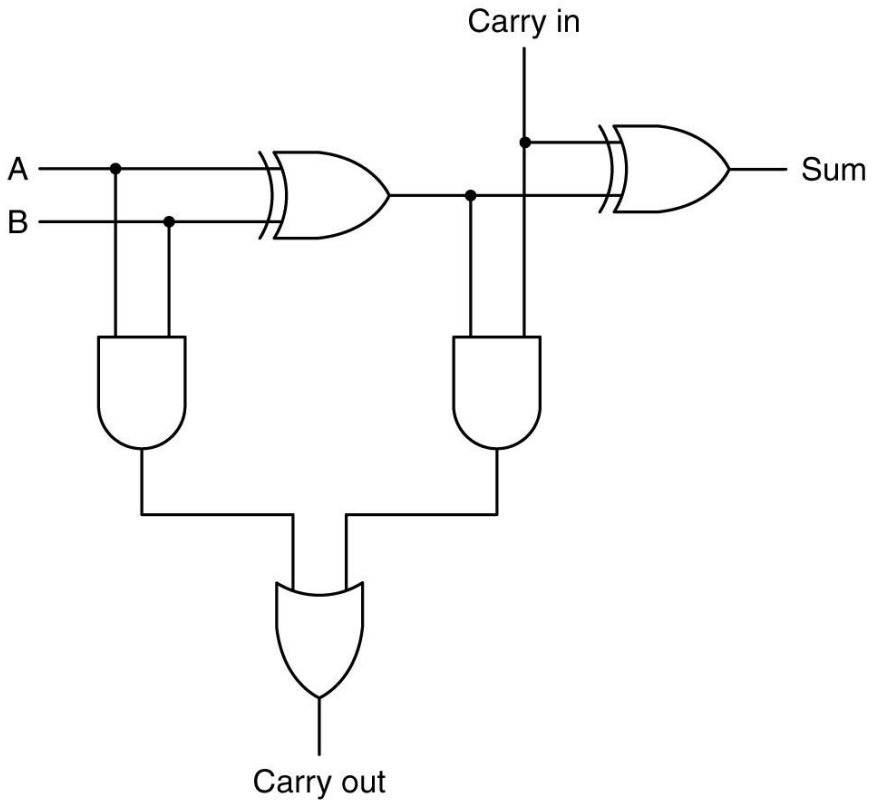


(b)

1-bit Full Adder

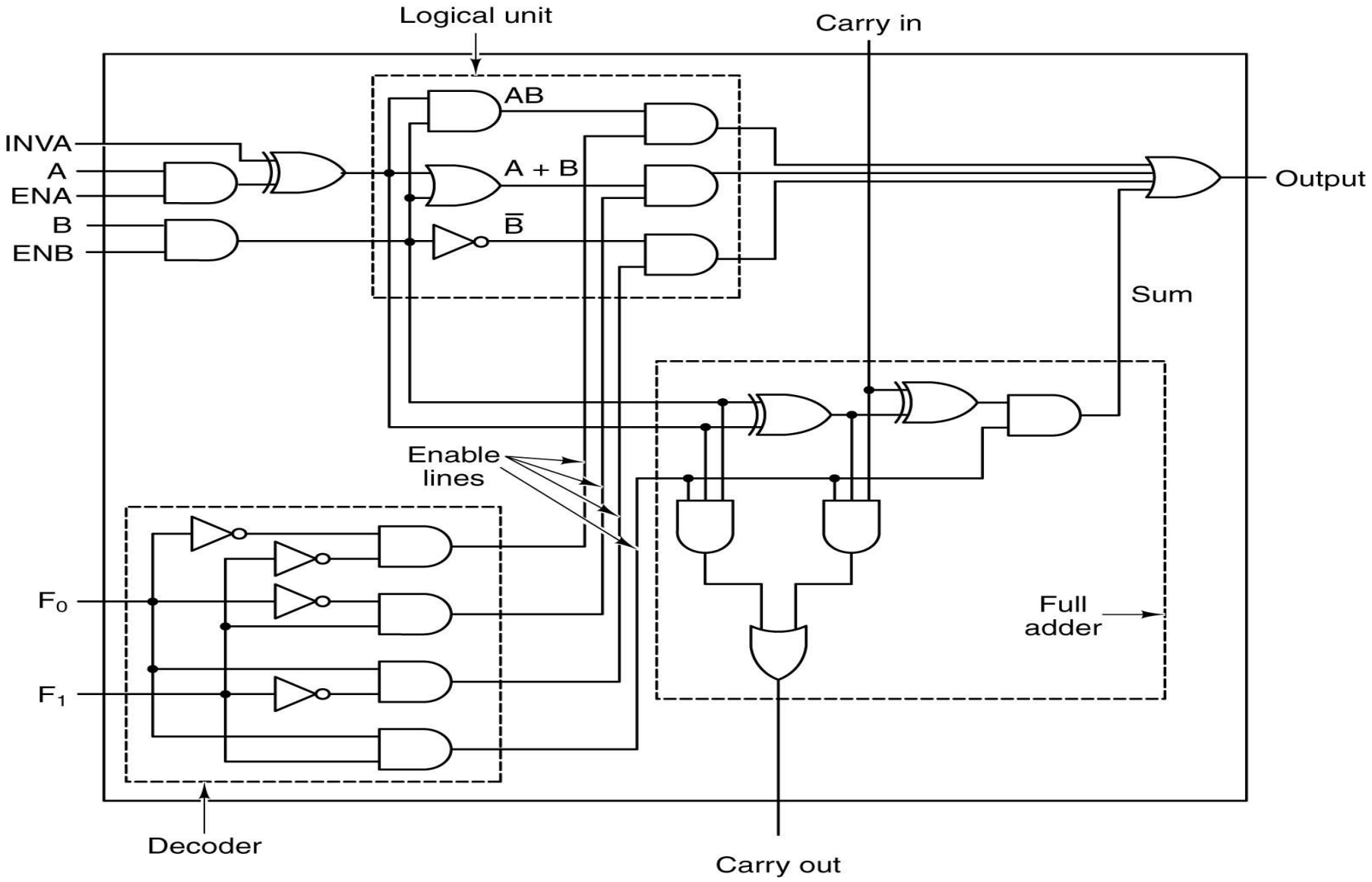
A	B	Carry in	Sum	Carry out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(a)

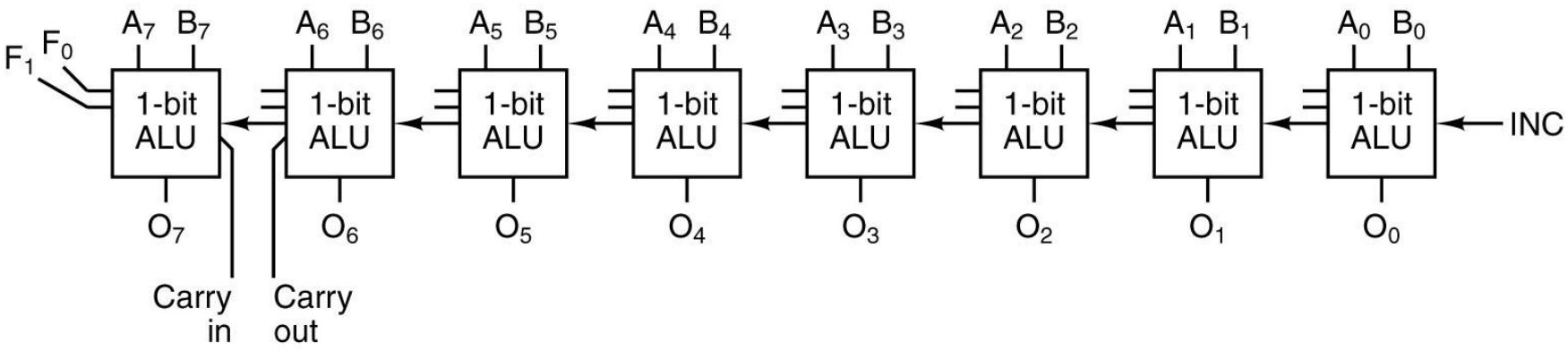


(b)

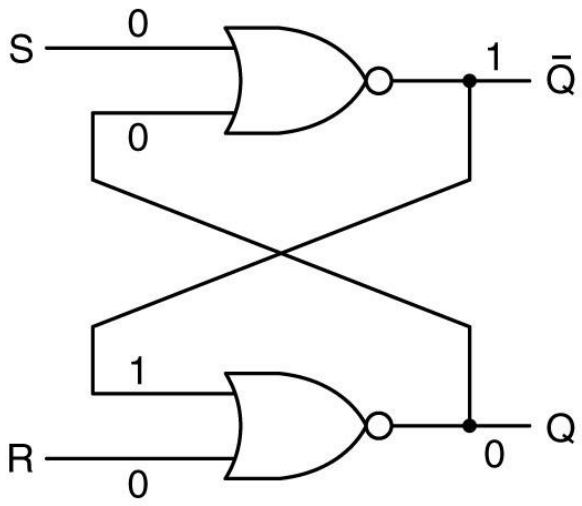
1-bit Arithmetic Logic Units (ALU)



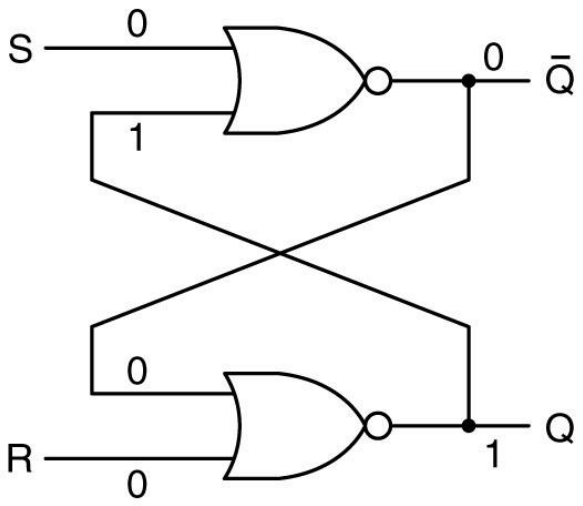
Arithmetic Logic Unit (ALU)



Latch



(a)



(b)

A	B	NOR
0	0	1
0	1	0
1	0	0
1	1	0

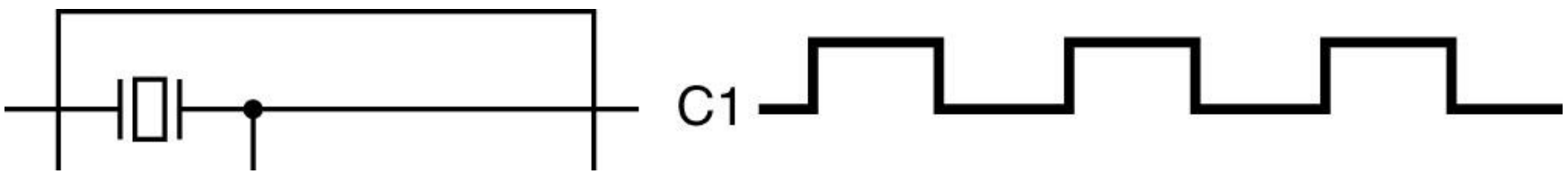
(c)

(a) NOR latch in state 0

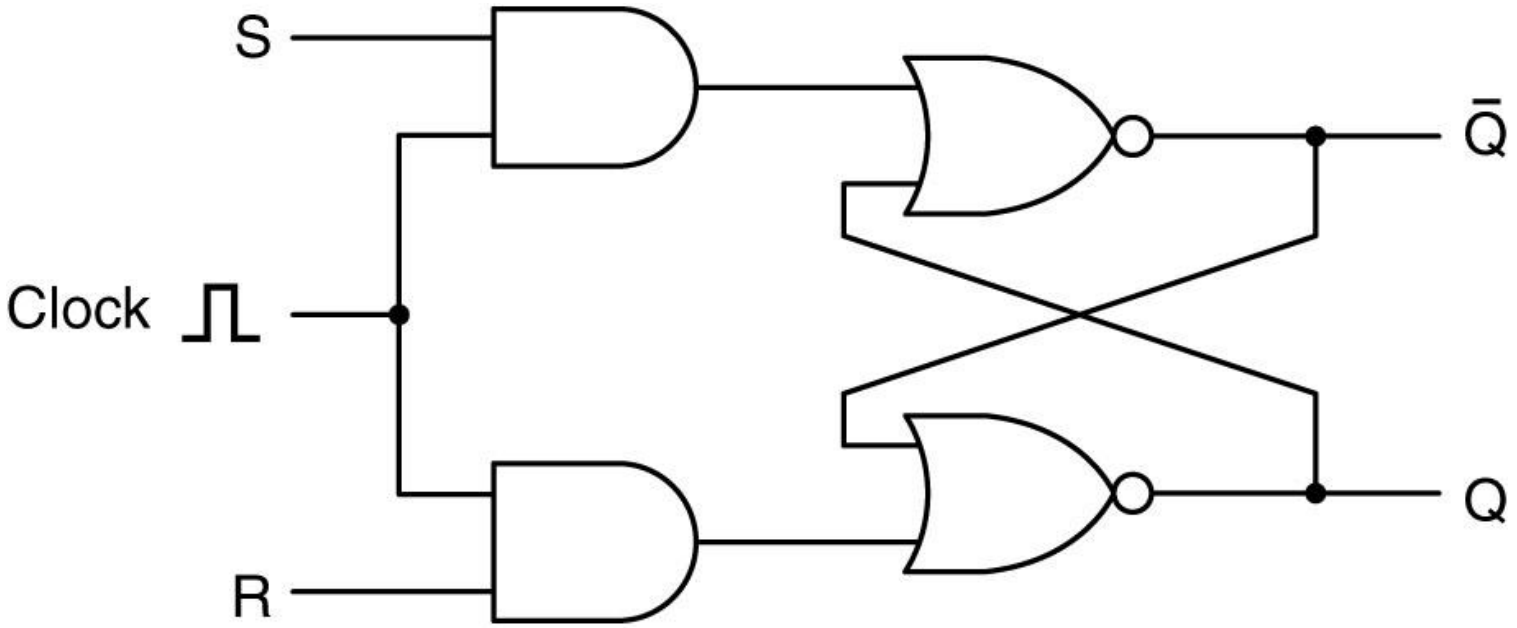
(b) NOR latch in state 1

(c) Truth table for NOR latch

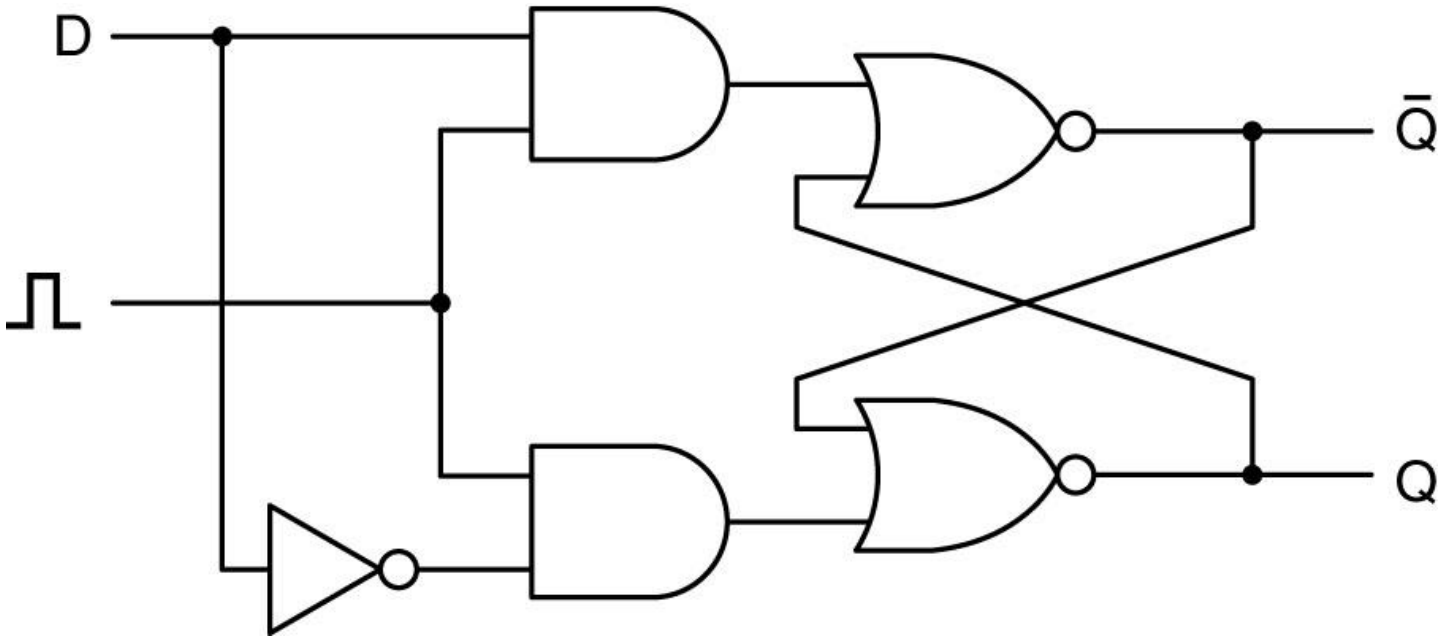
Clock



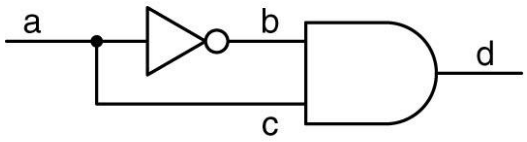
Clocked SR Latch



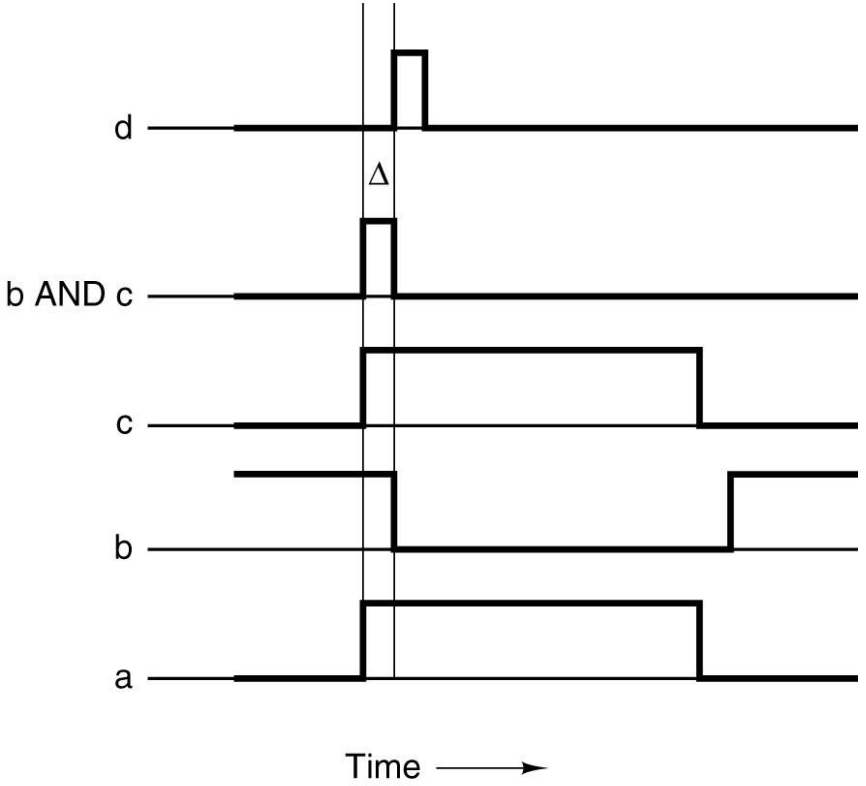
D Latch



Pulse Generator

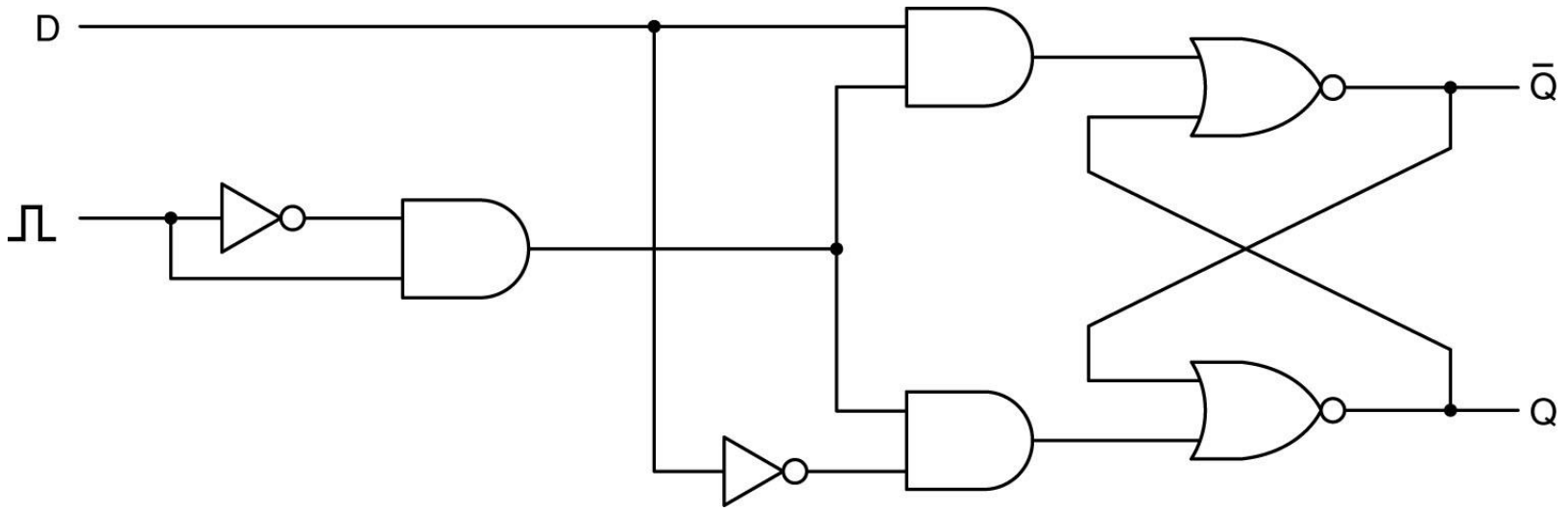


(a)

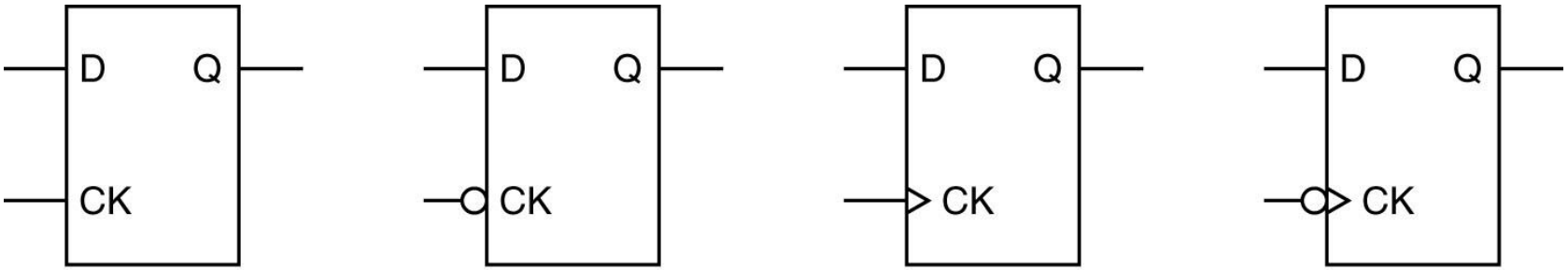


(b)

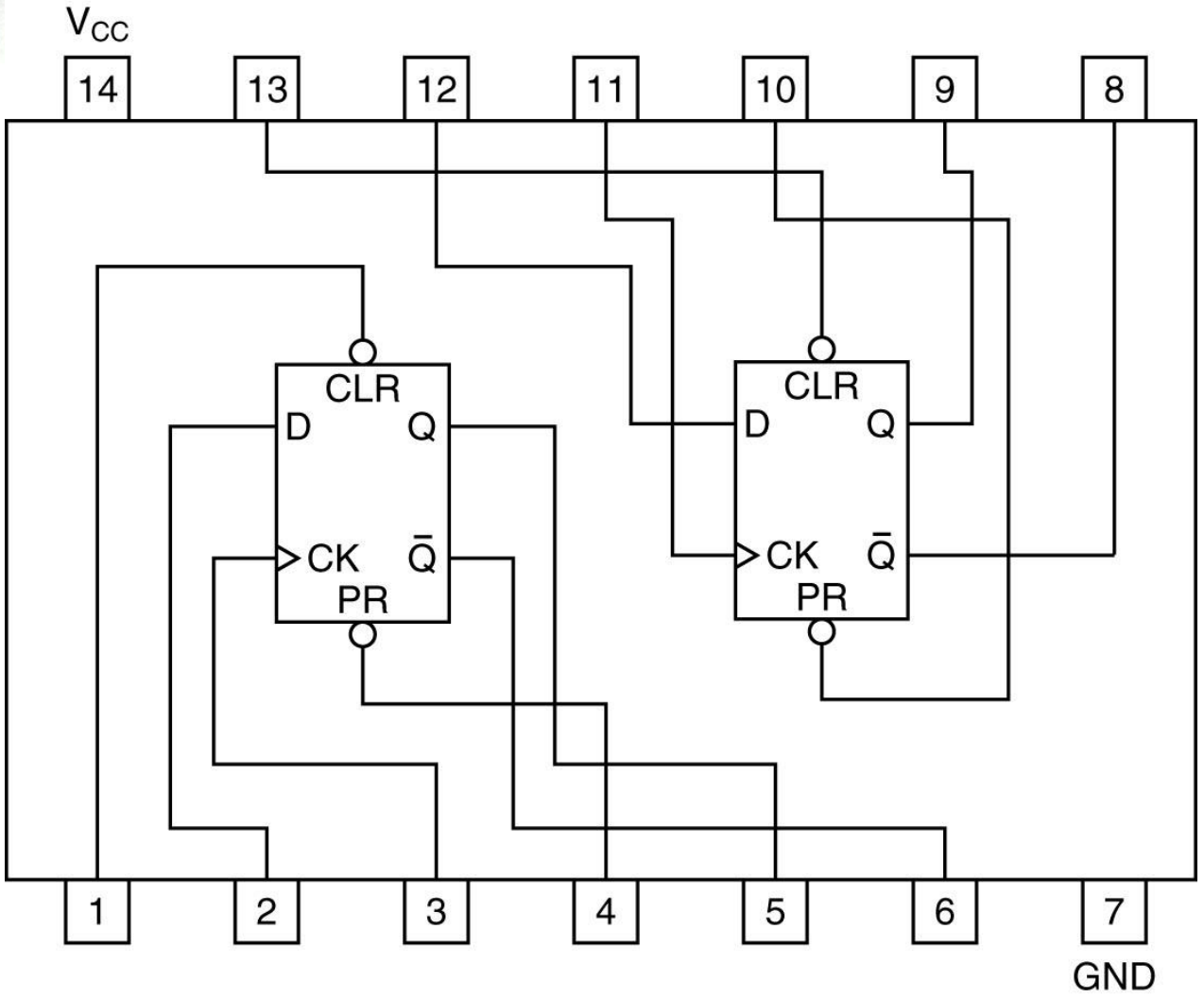
D Flip-Flop



Logic Notations for D Latch & D Flip-Flop

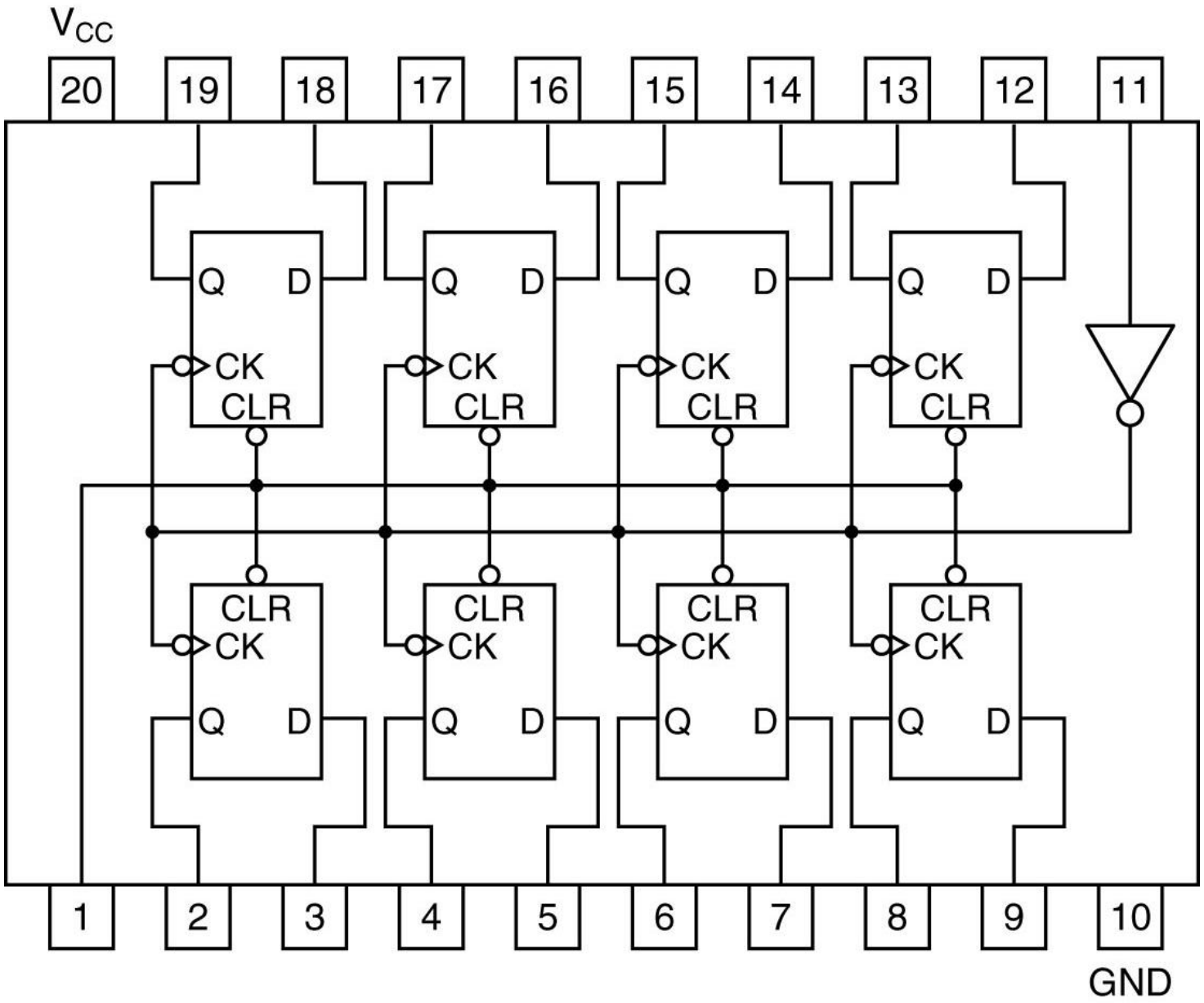


Dual D Flip-Flop Chip with Preset/Clear

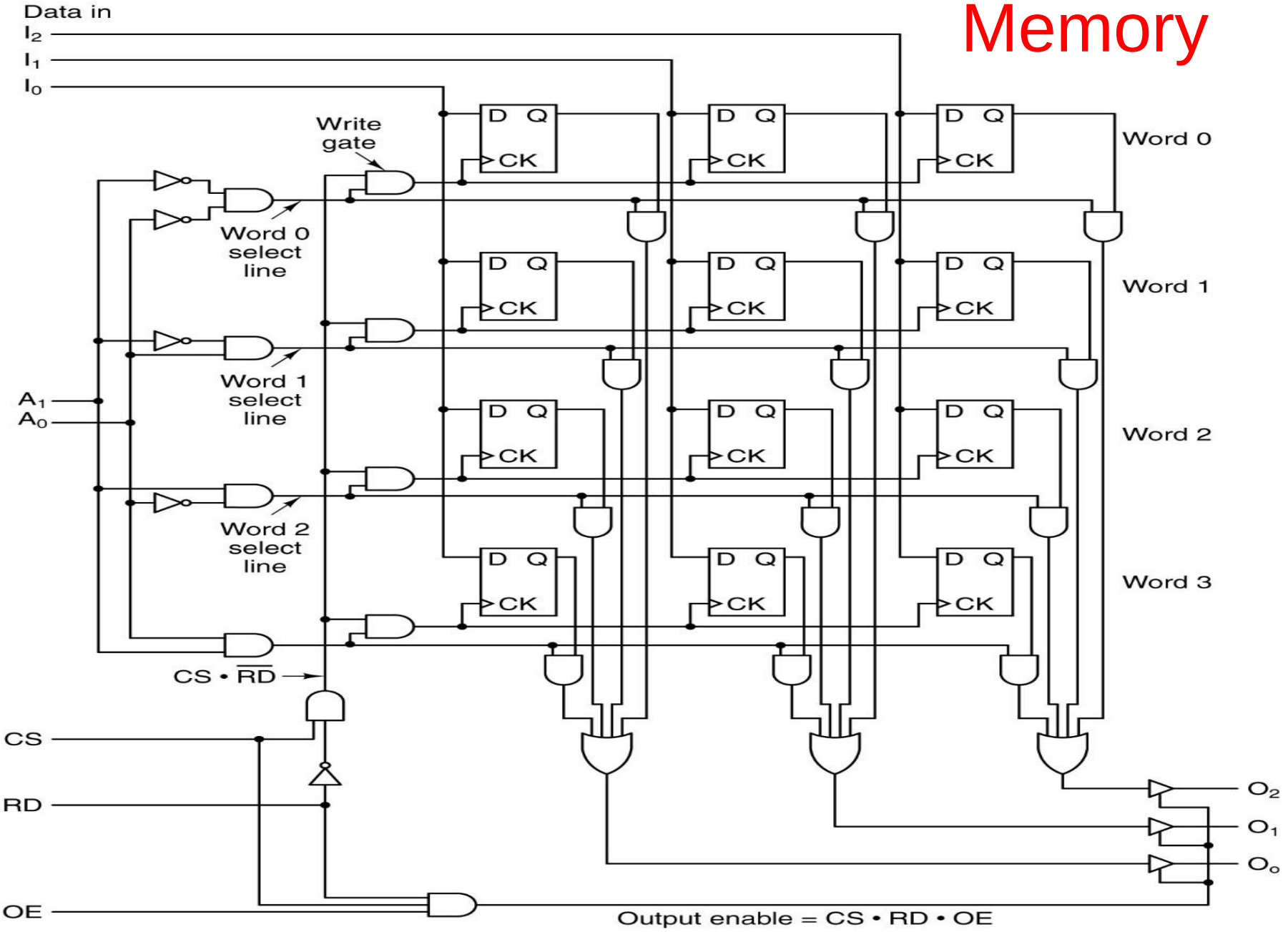


(a)

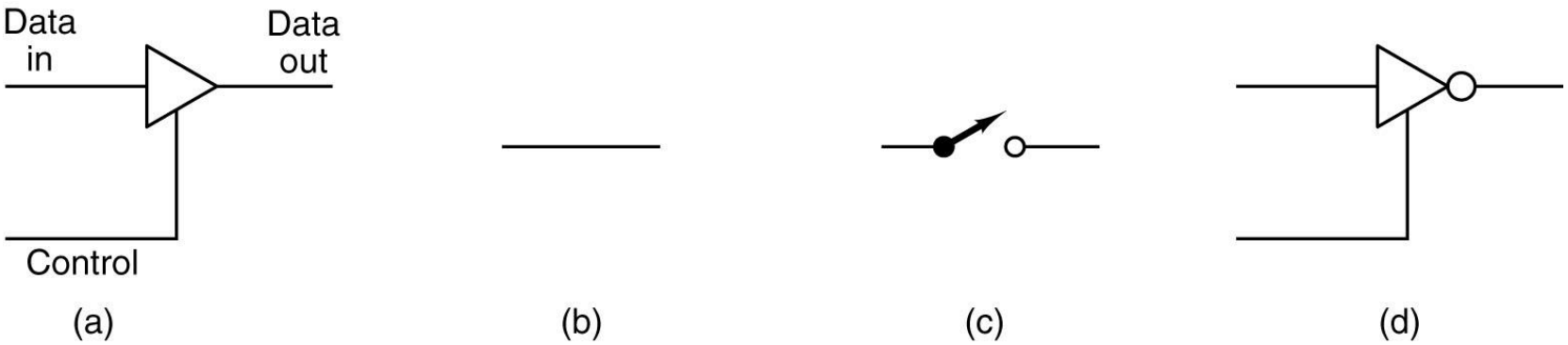
Octal D Flip-Flops with Clear



Memory


Data in
I_2
I_1
I_0
Write gate
Word 0 select line
Word 1 select line
Word 2 select line
A_1
A_0
D Q
CK
Word 0
Word 1
Word 2
Word 3
CS • $\overline{RD}$
CS
RD
OE
O_2
O_1
O_0
Output enable = CS • RD • OE

Buffer



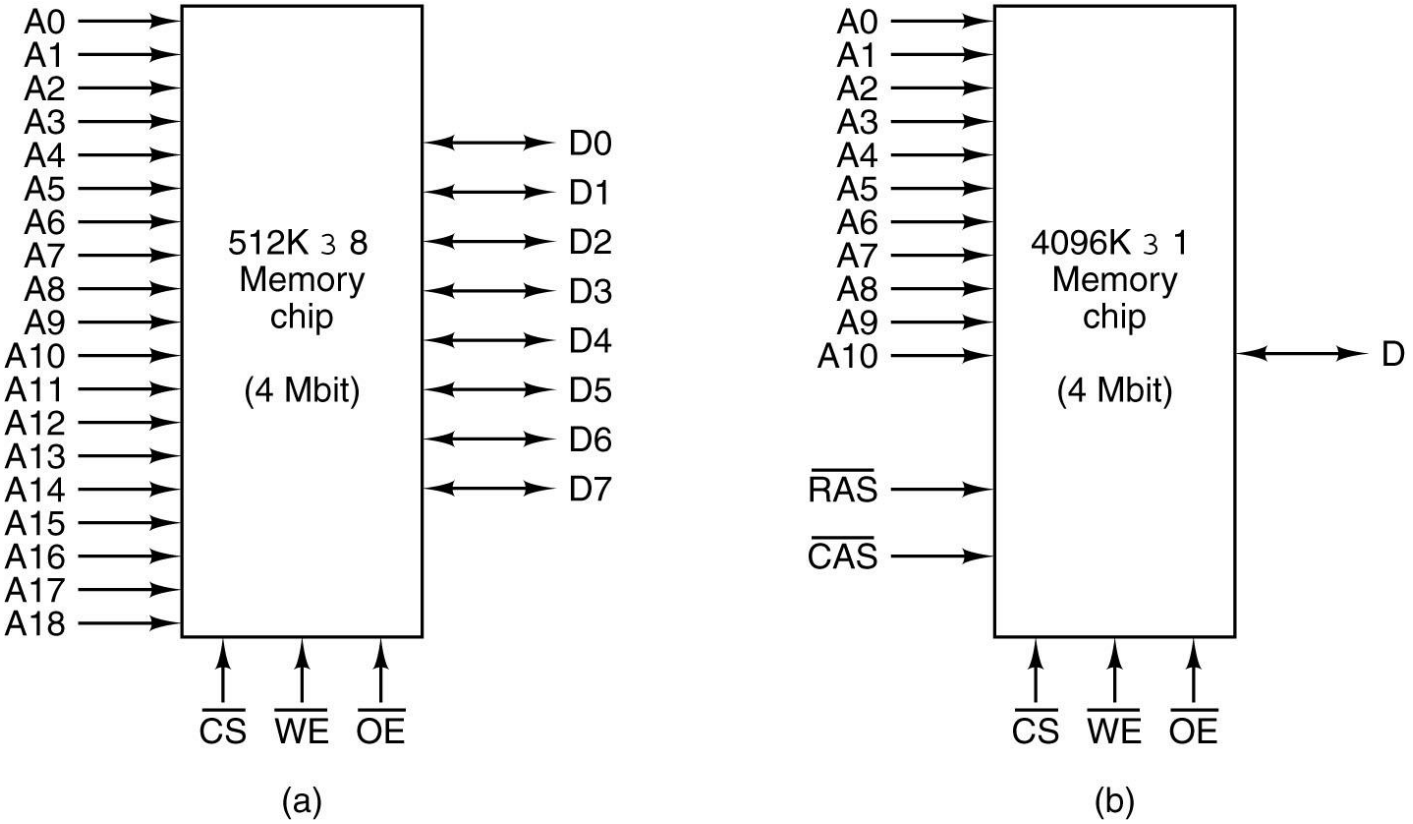
(a) A noninverting buffer.

(b) Effect of (a) when control is high.

(c) Effect of (a) when control is low.

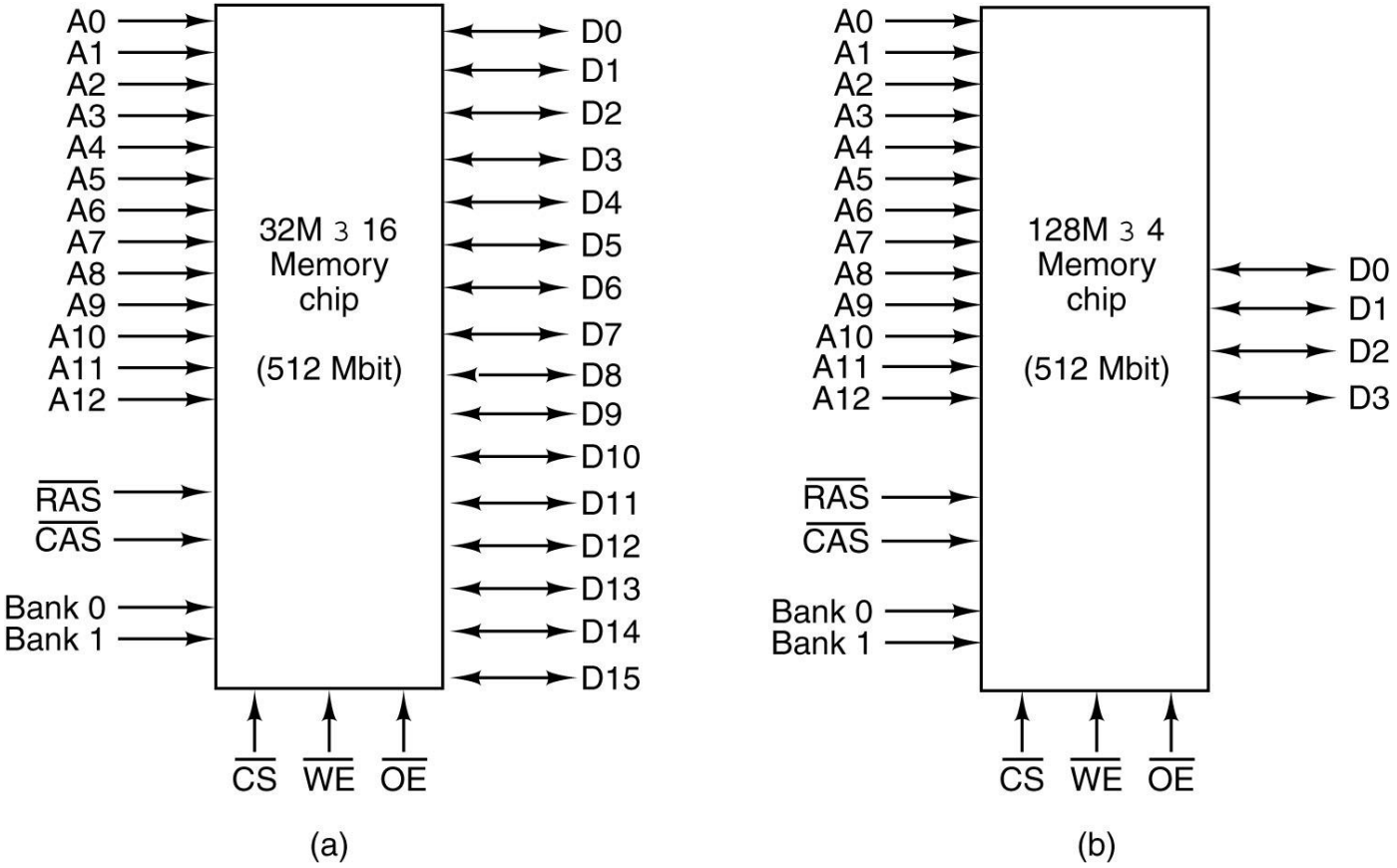
(d) An inverting buffer.

Memory Chips (1)



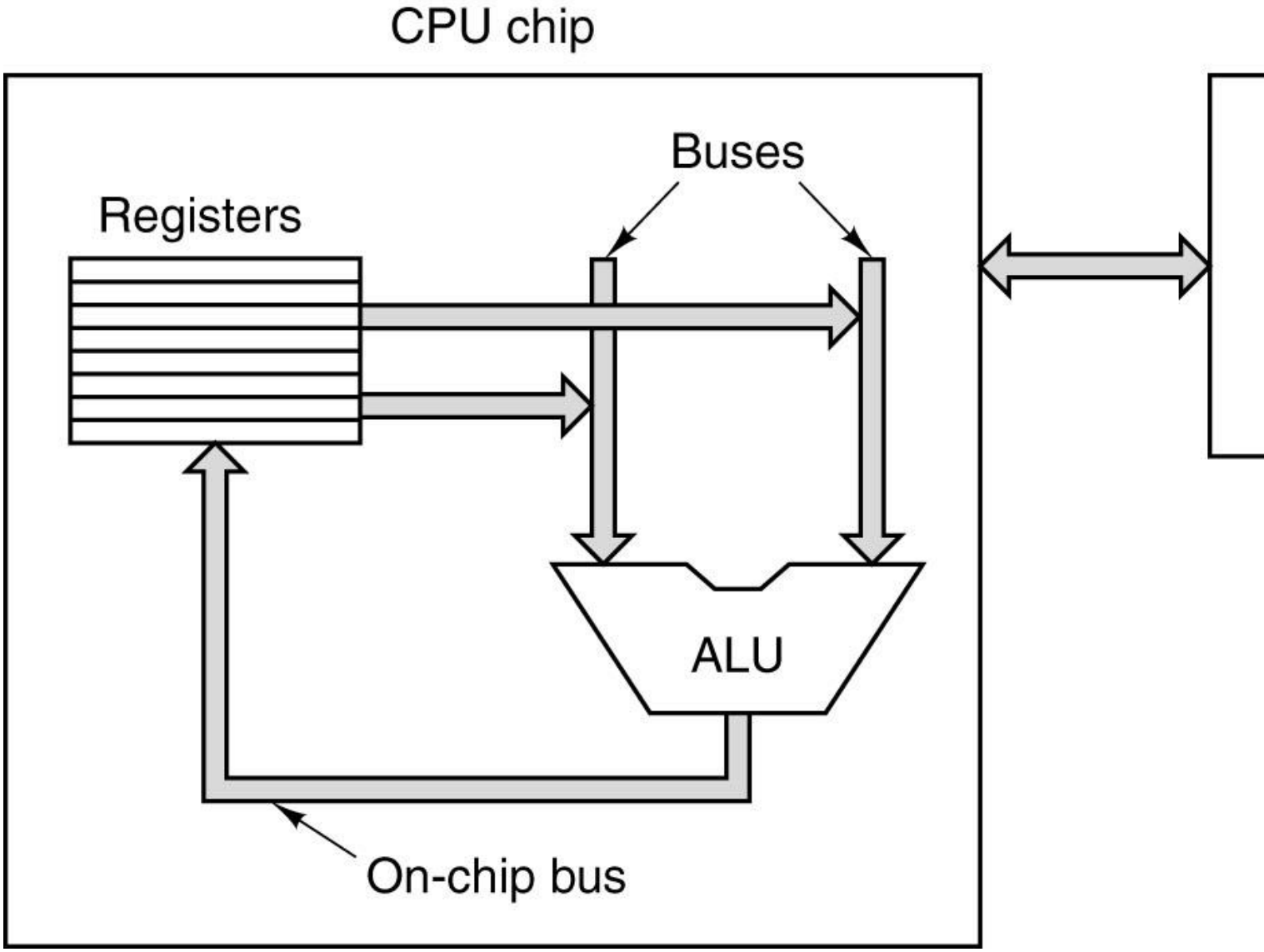
Two ways of organizing a 4-Mbit memory chip.

Memory Chips (2)

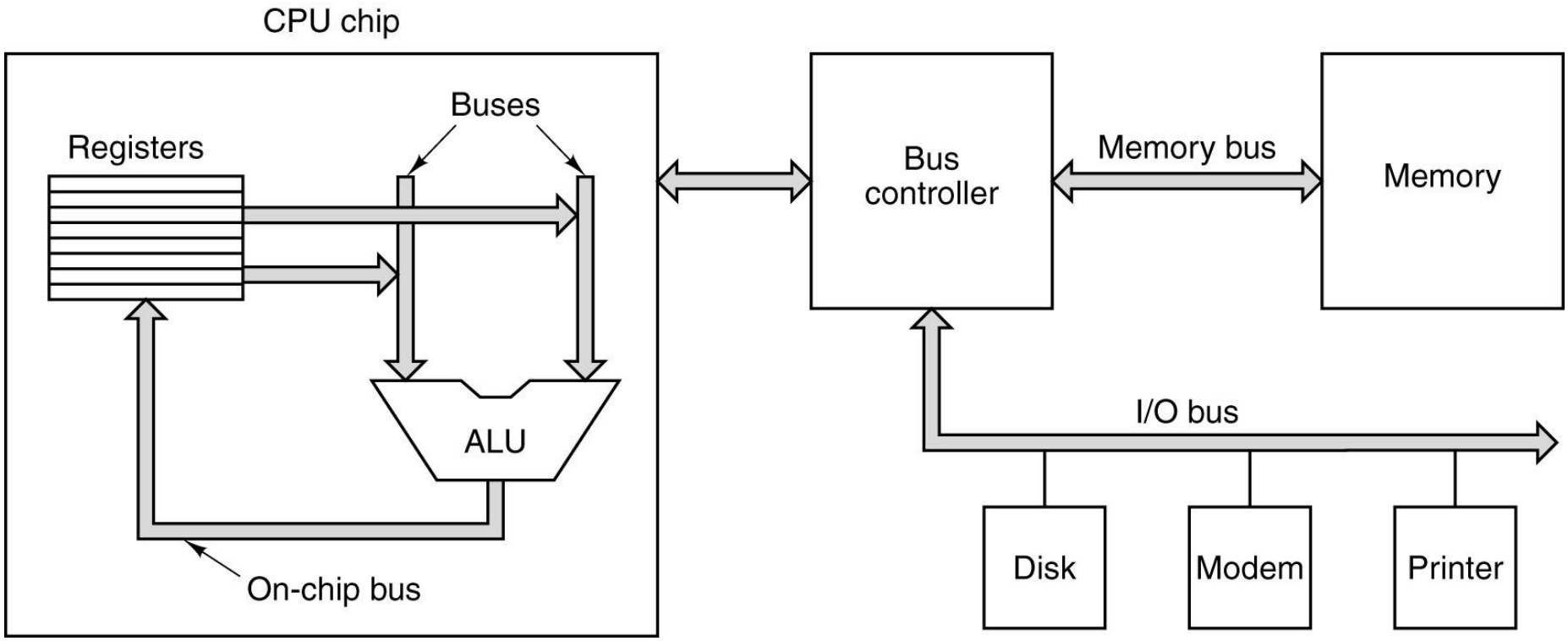


Two ways of organizing a 512 Mbit memory chip.

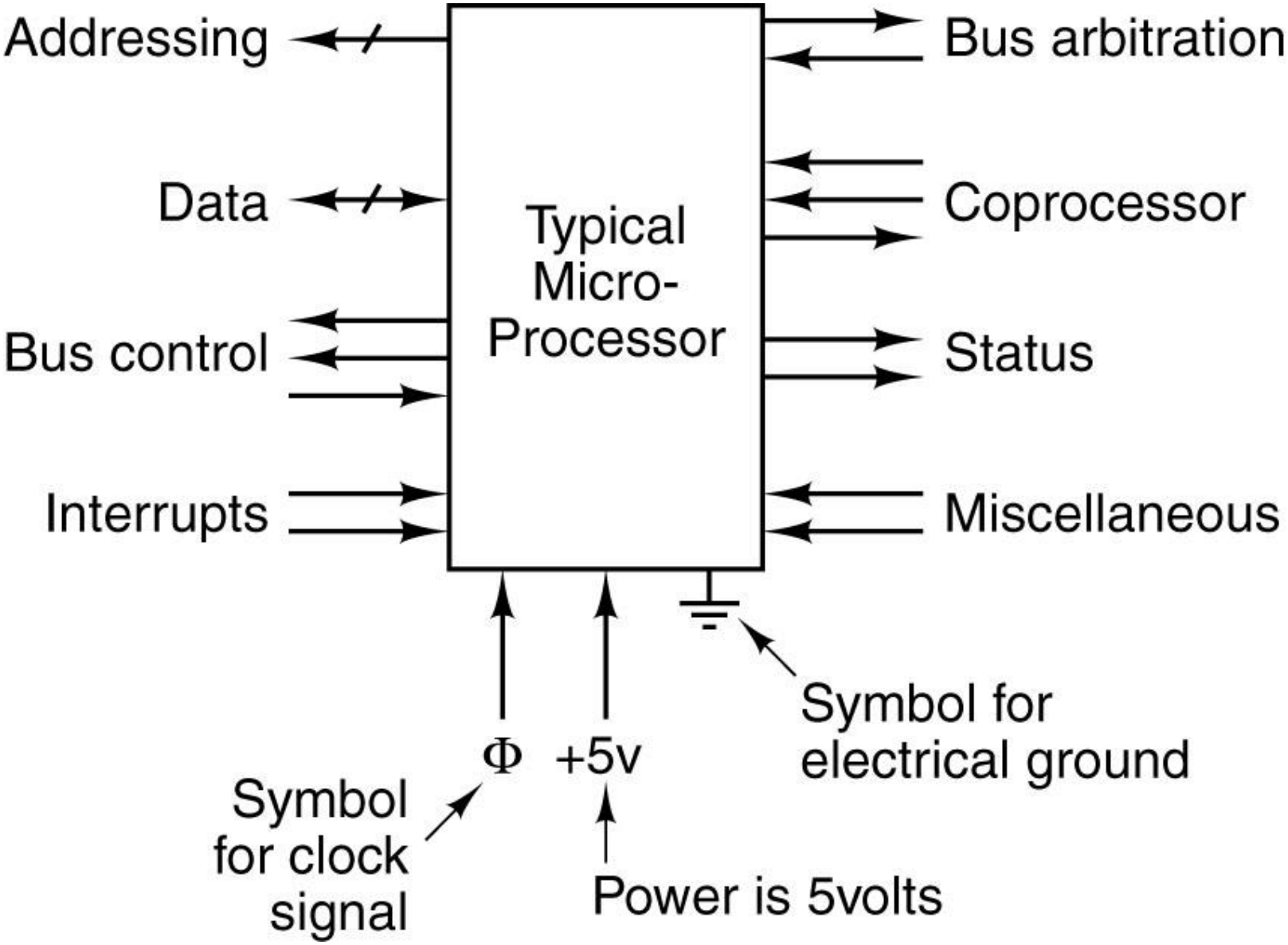
Typical CPU



Typical Computer System



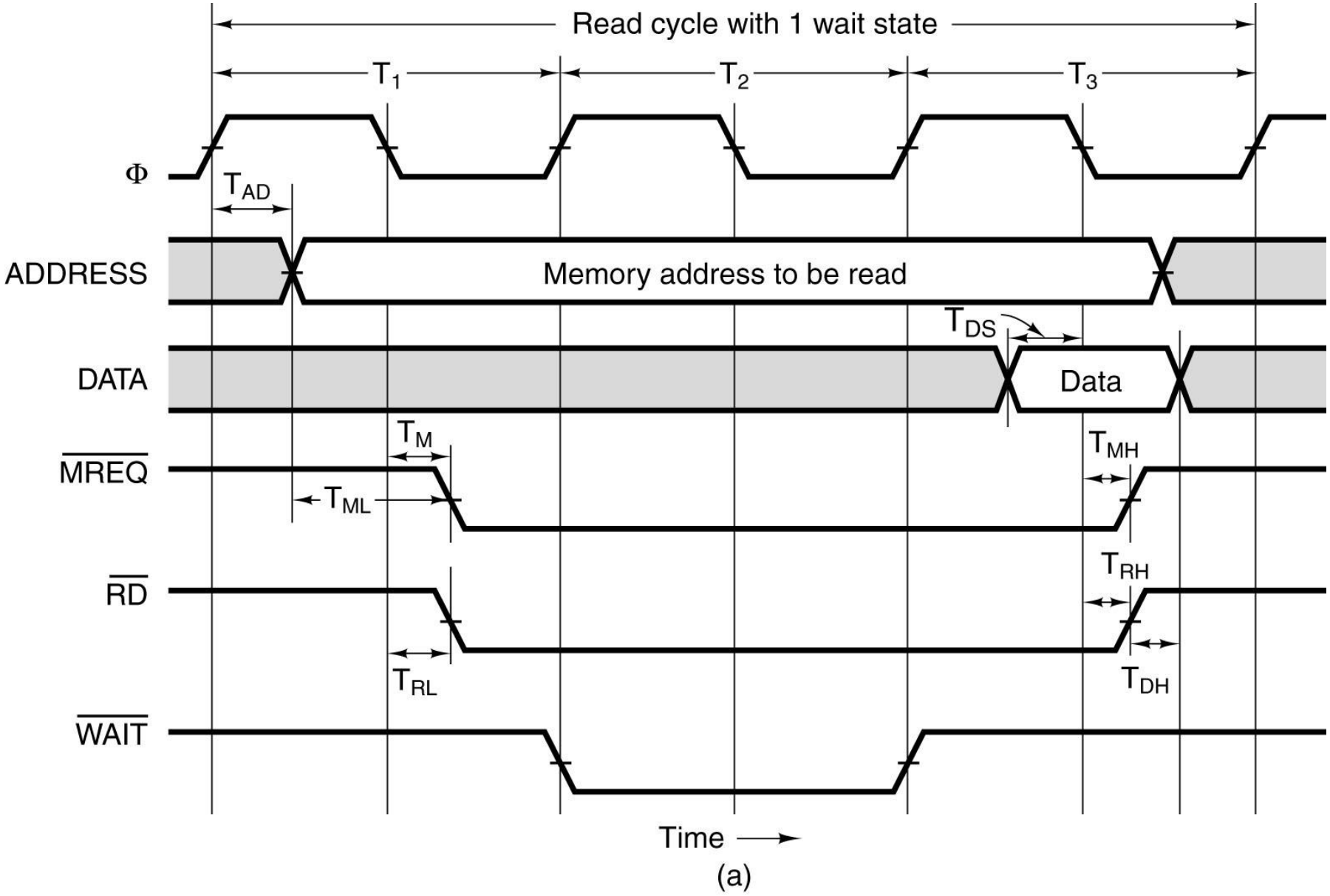
Microprocessor Chips



Bus

Master	Slave	Example
CPU	Memory	Fetching instructions and data
CPU	I/O device	Initiating data transfer
CPU	Coprocessor	CPU handing instruction off to coprocessor
I/O	Memory	DMA (Direct Memory Access)
Coprocessor	CPU	Coprocessor fetching operands from CPU

Synchronous Bus Timing

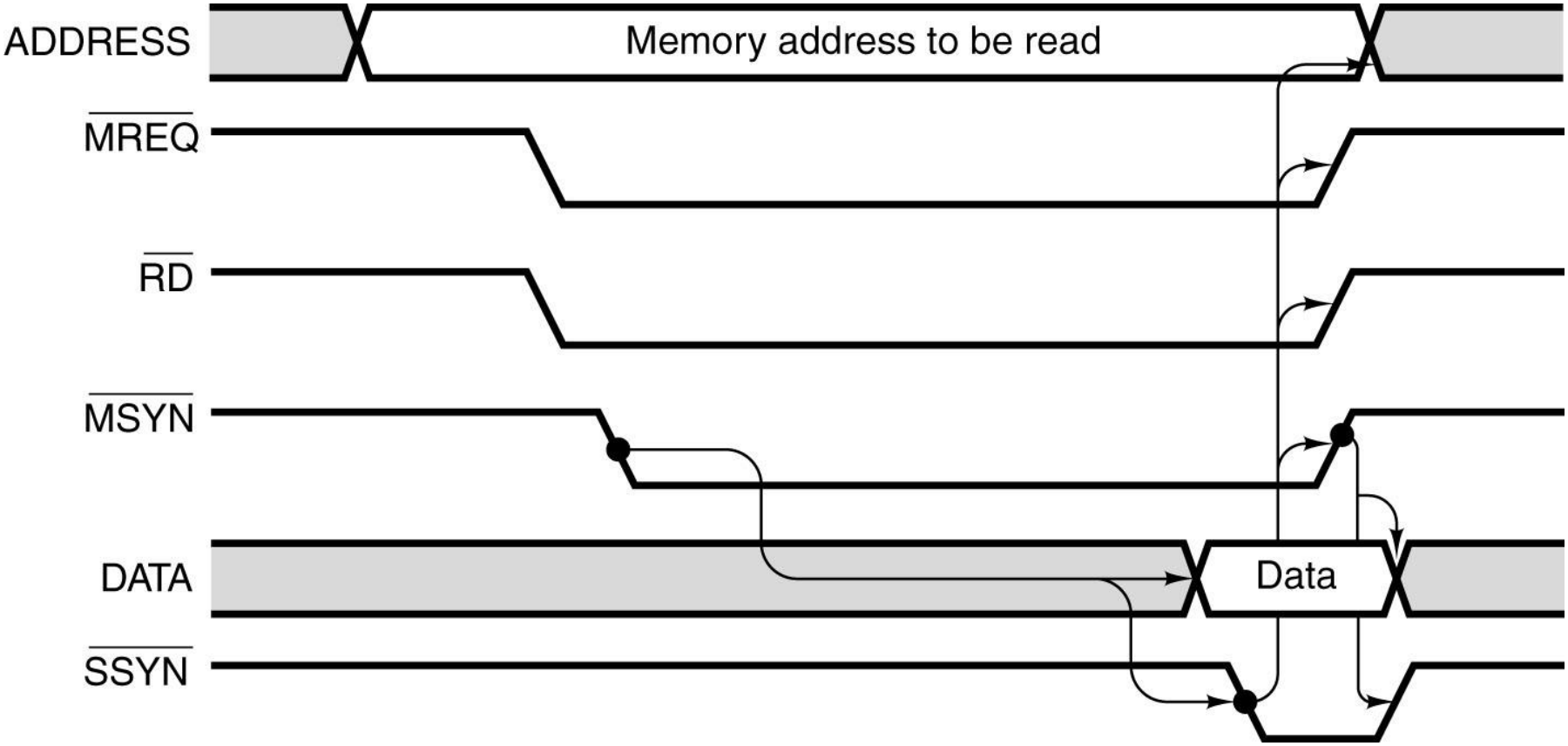


Critical Times

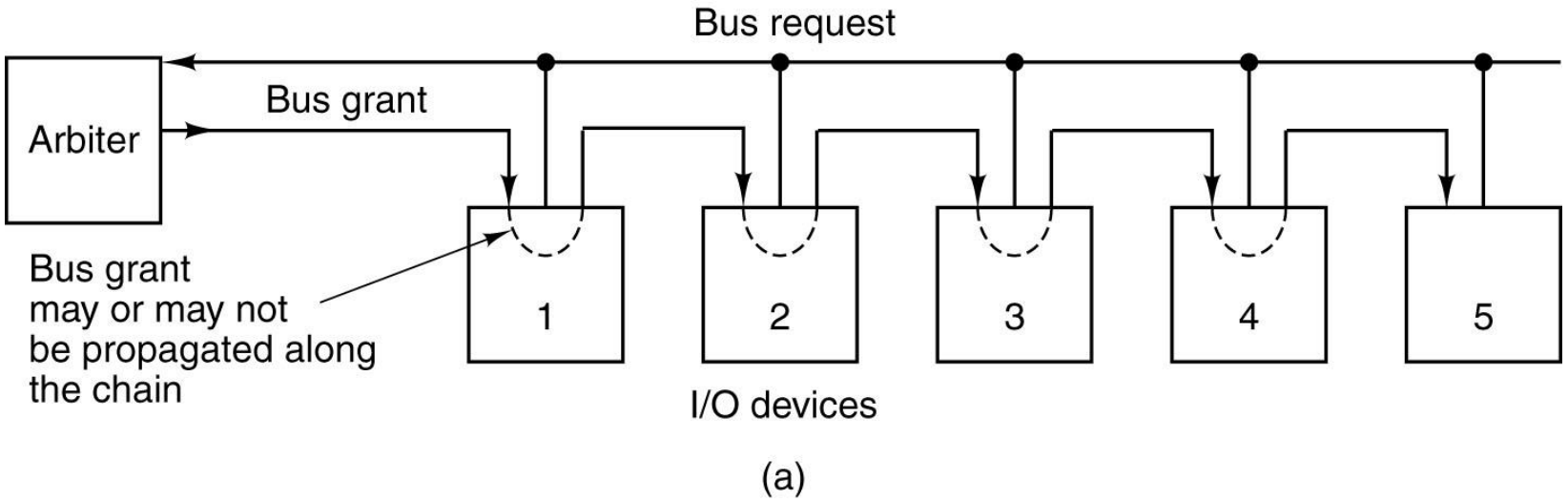
Symbol	Parameter	Min	Max	Unit
T_{AD}	Address output delay		4	nsec
T_{ML}	Address stable prior to $\overline{MREQ}$	2		nsec
T_M	$\overline{MREQ}$ delay from falling edge of Φ in T_1		3	nsec
T_{RL}	RD delay from falling edge of Φ in T_1		3	nsec
T_{DS}	Data setup time prior to falling edge of Φ	2		nsec
T_{MH}	$\overline{MREQ}$ delay from falling edge of Φ in T_3		3	nsec
T_{RH}	$\overline{RD}$ delay from falling edge of Φ in T_3		3	nsec
T_{DH}	Data hold time from negation of $\overline{RD}$	0		nsec

(b)

Asynchronous Bus Timing

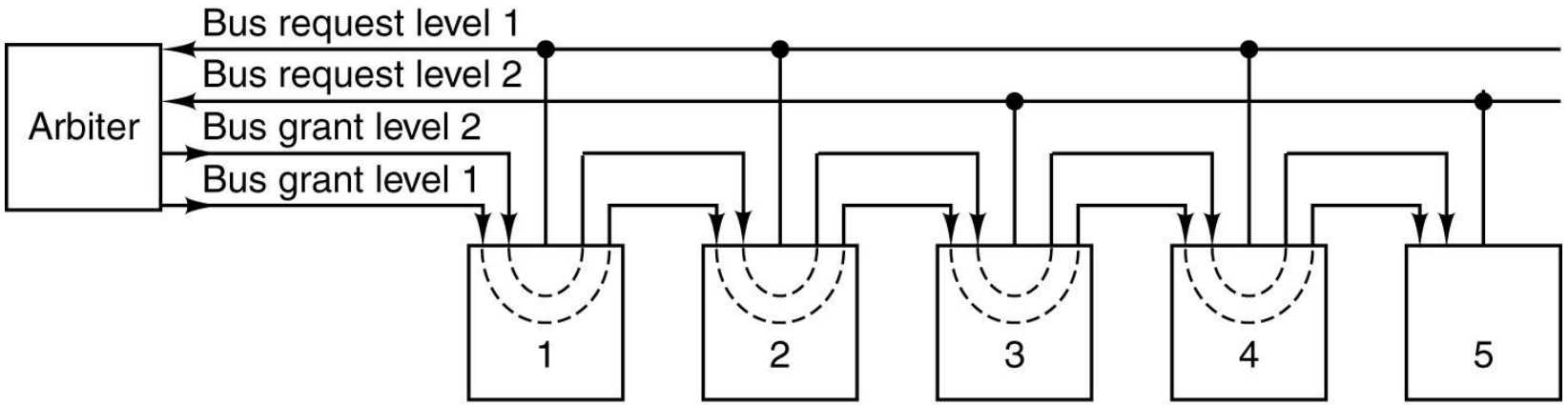


Centralized Bus Arbitration (1 level)



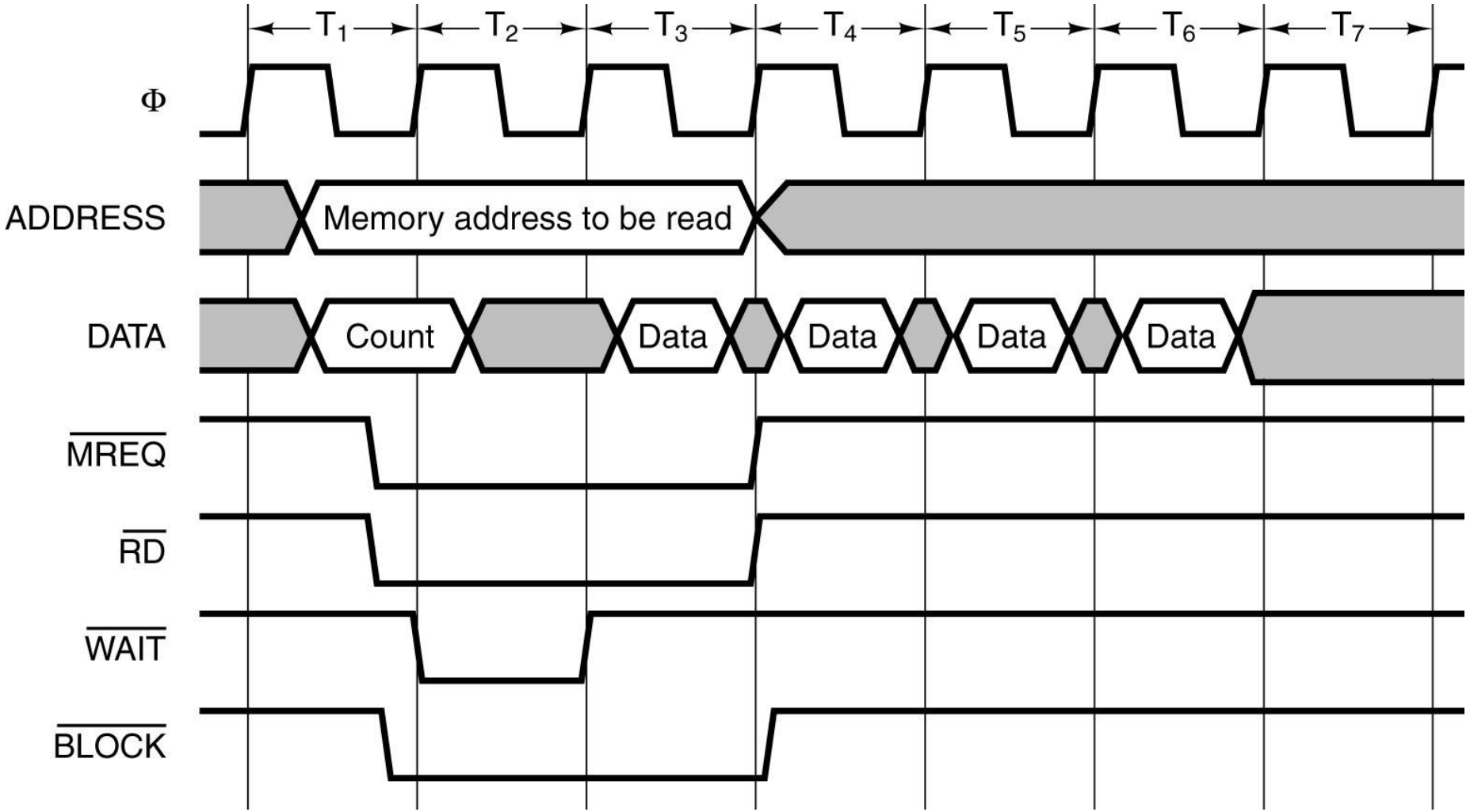
(a)

Centralized Bus Arbitration (2 levels)

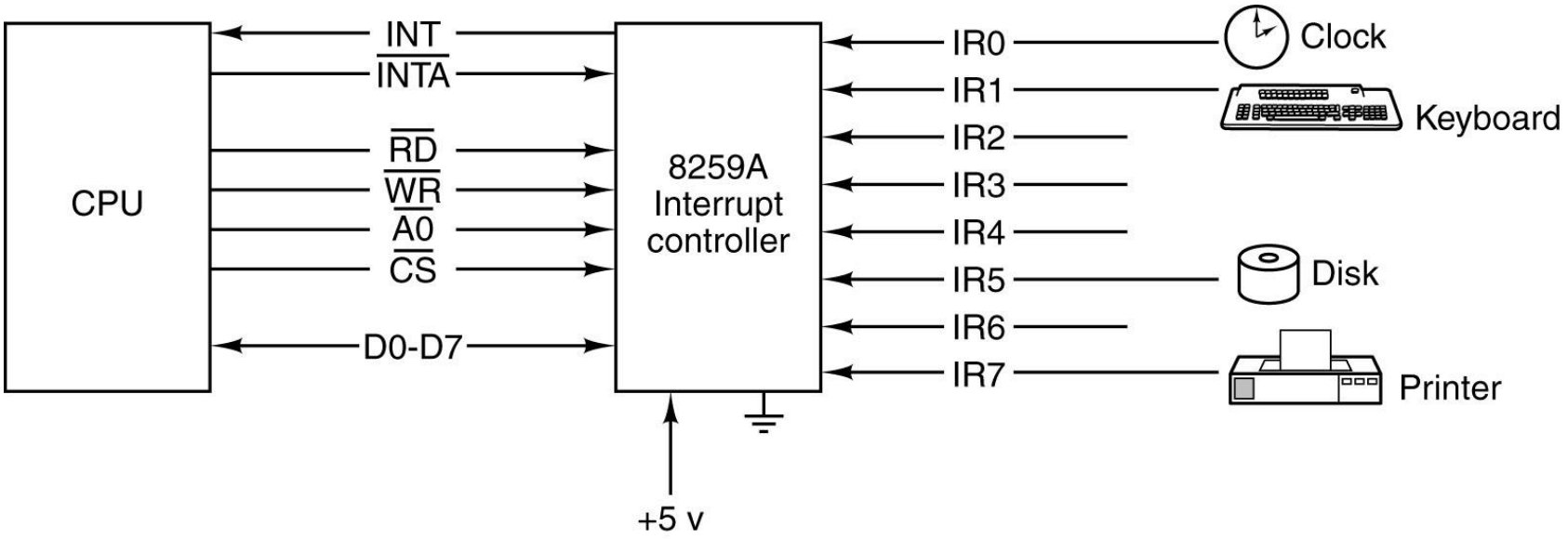


(b)

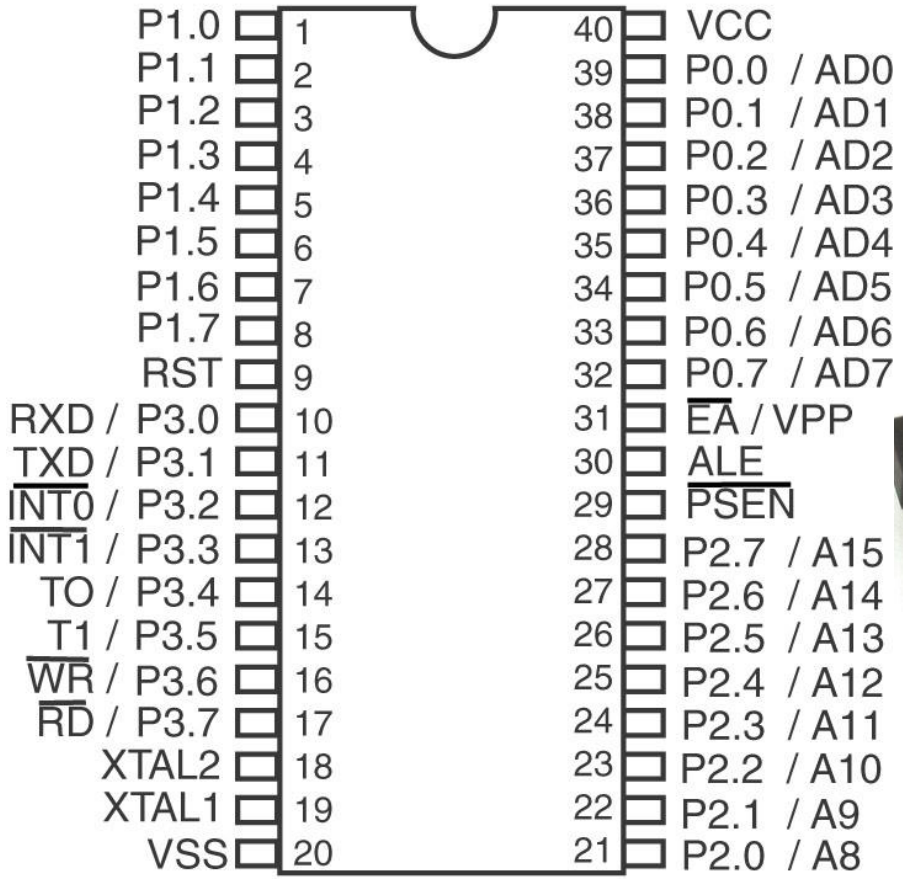
Block Memory Access

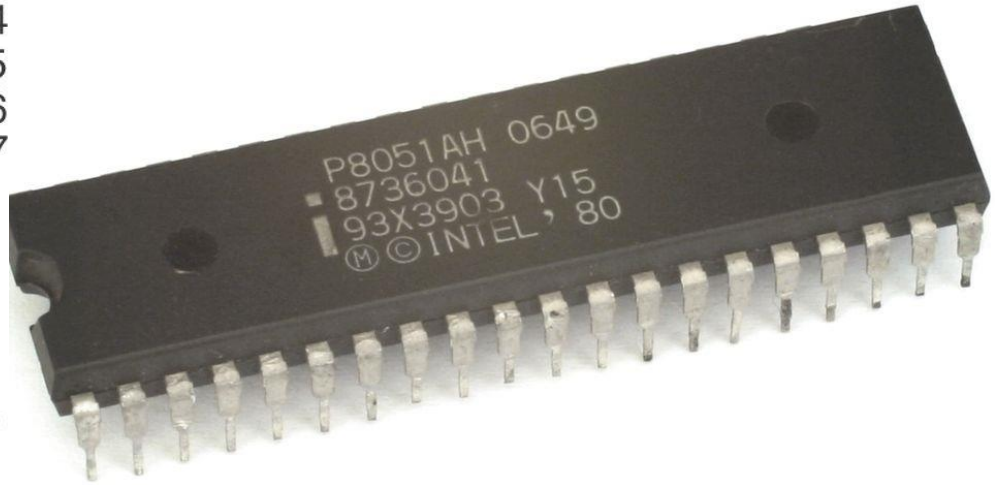


Typical Interrupt Controller

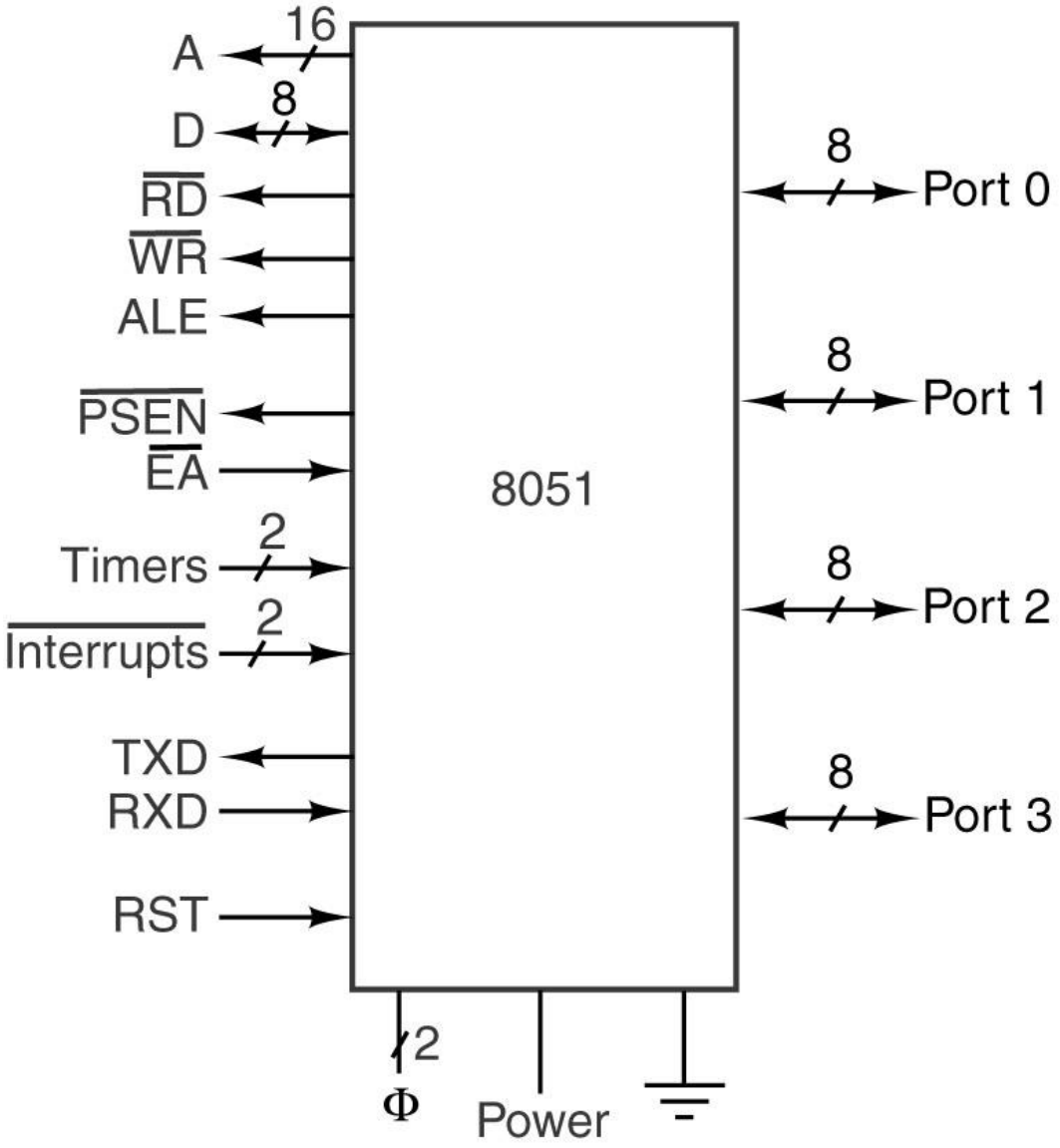


Intel 8051 (Physical Pinout)

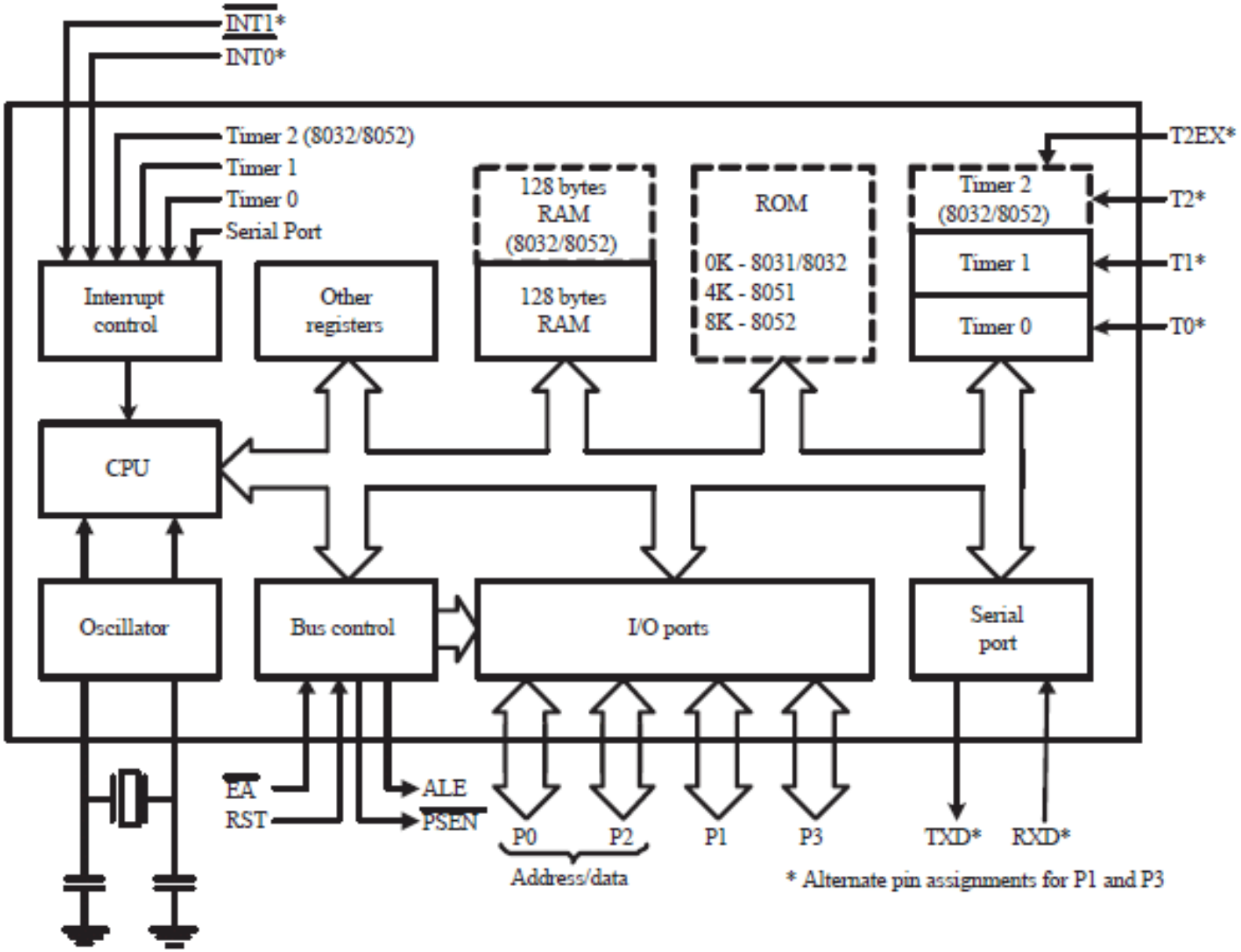




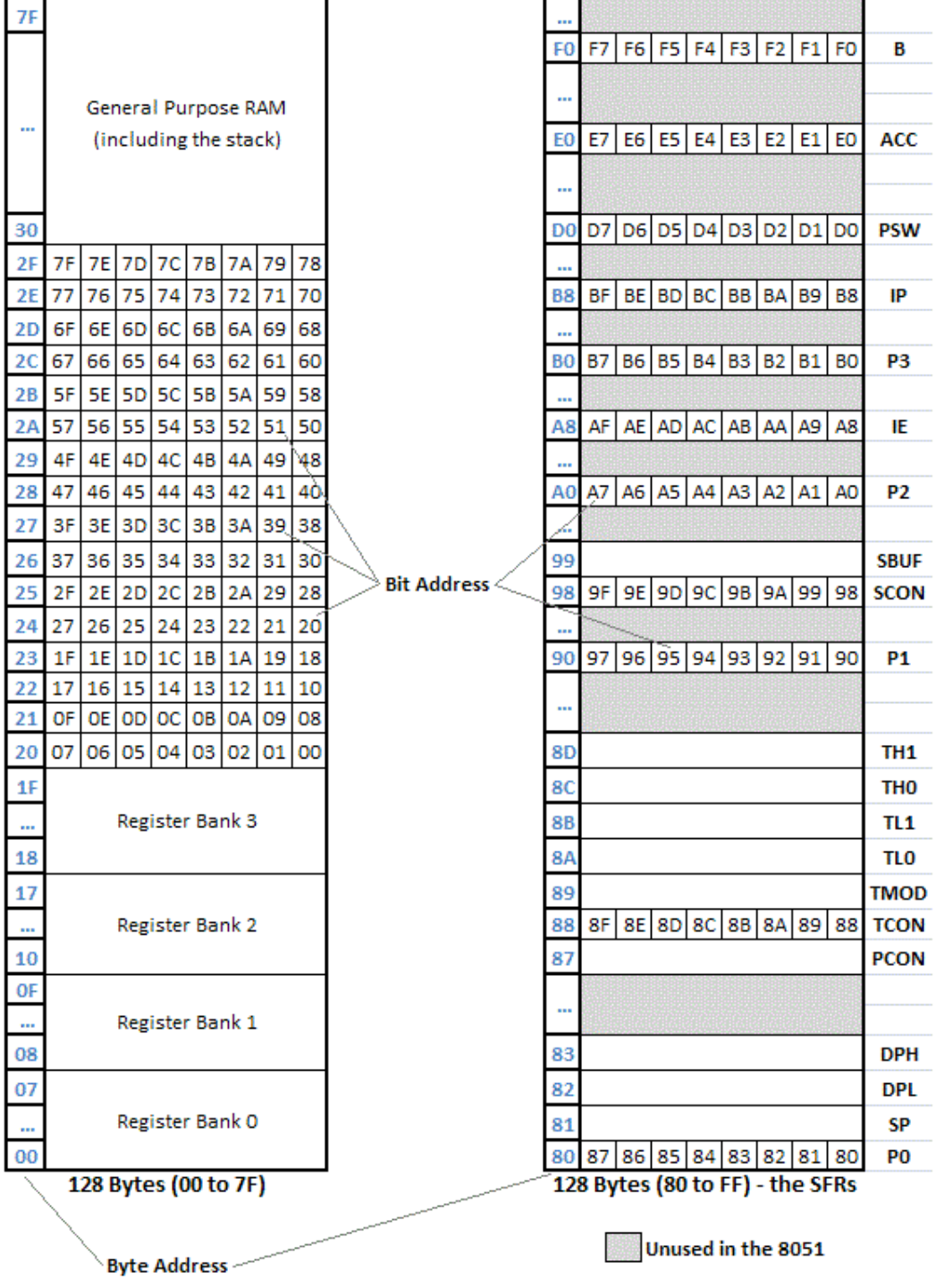
Intel 8051 (Logical Pinout)



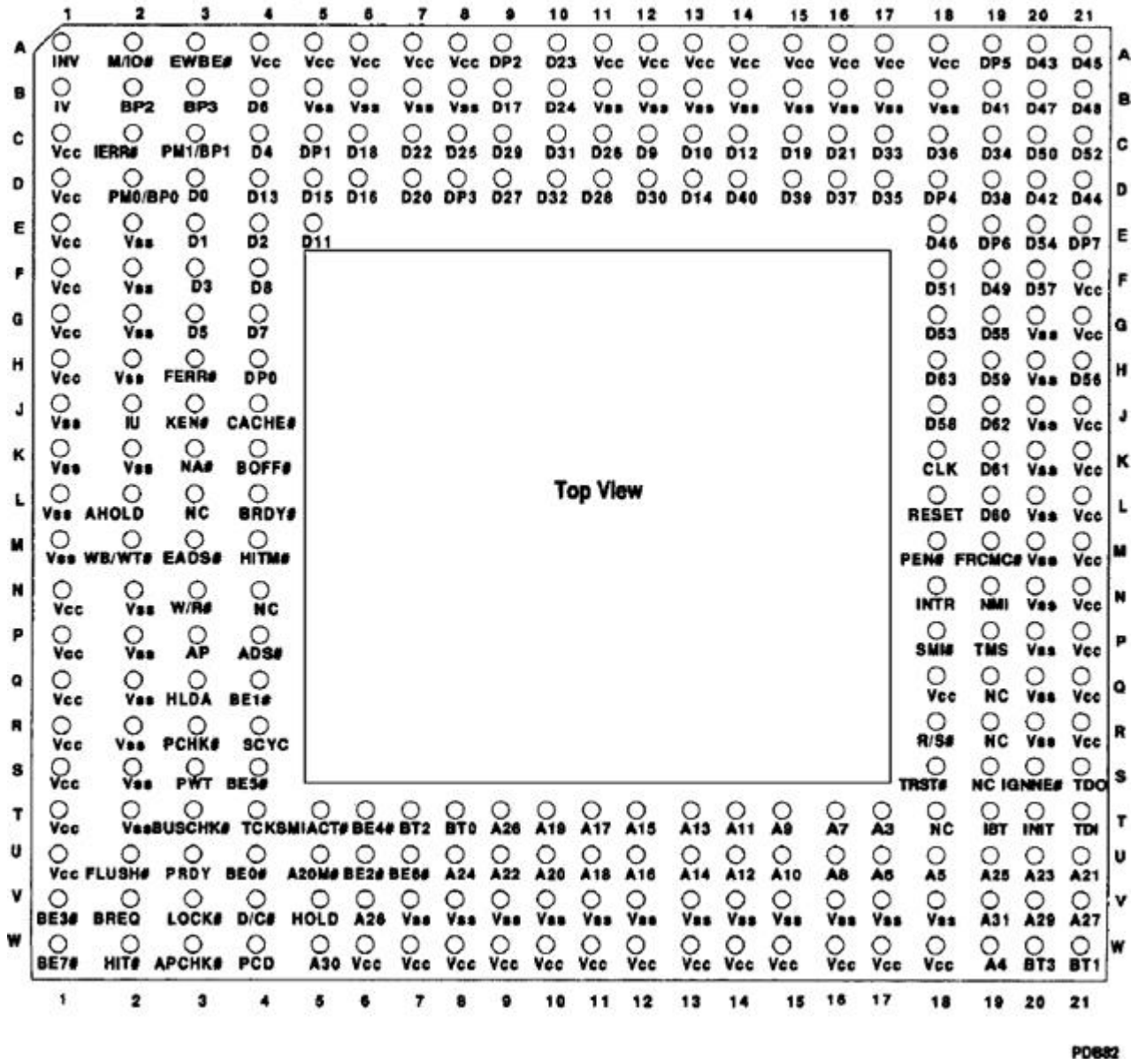
Intel 8051 (Logical Block Diagram)



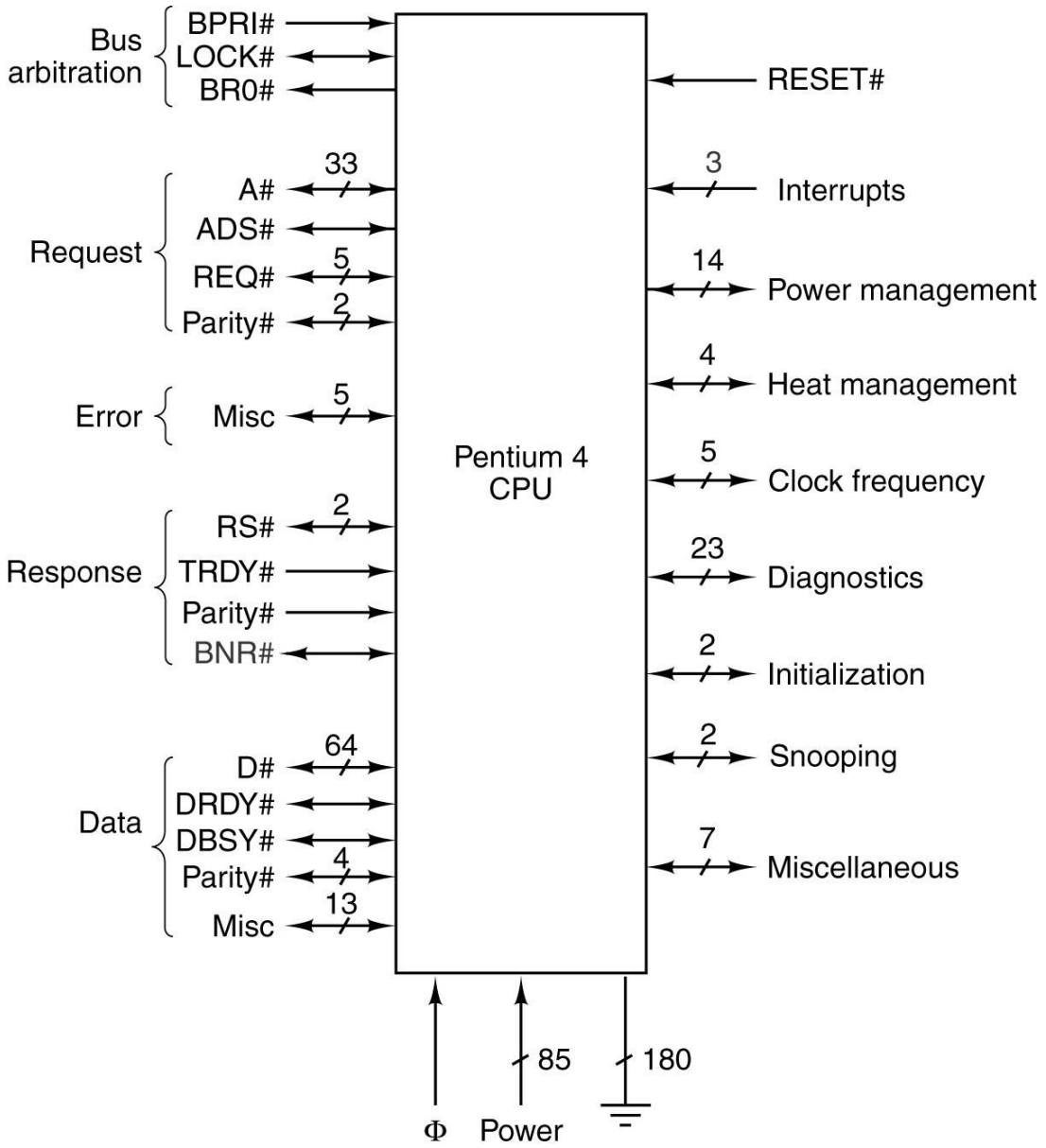
Intel 8051 Memory Map



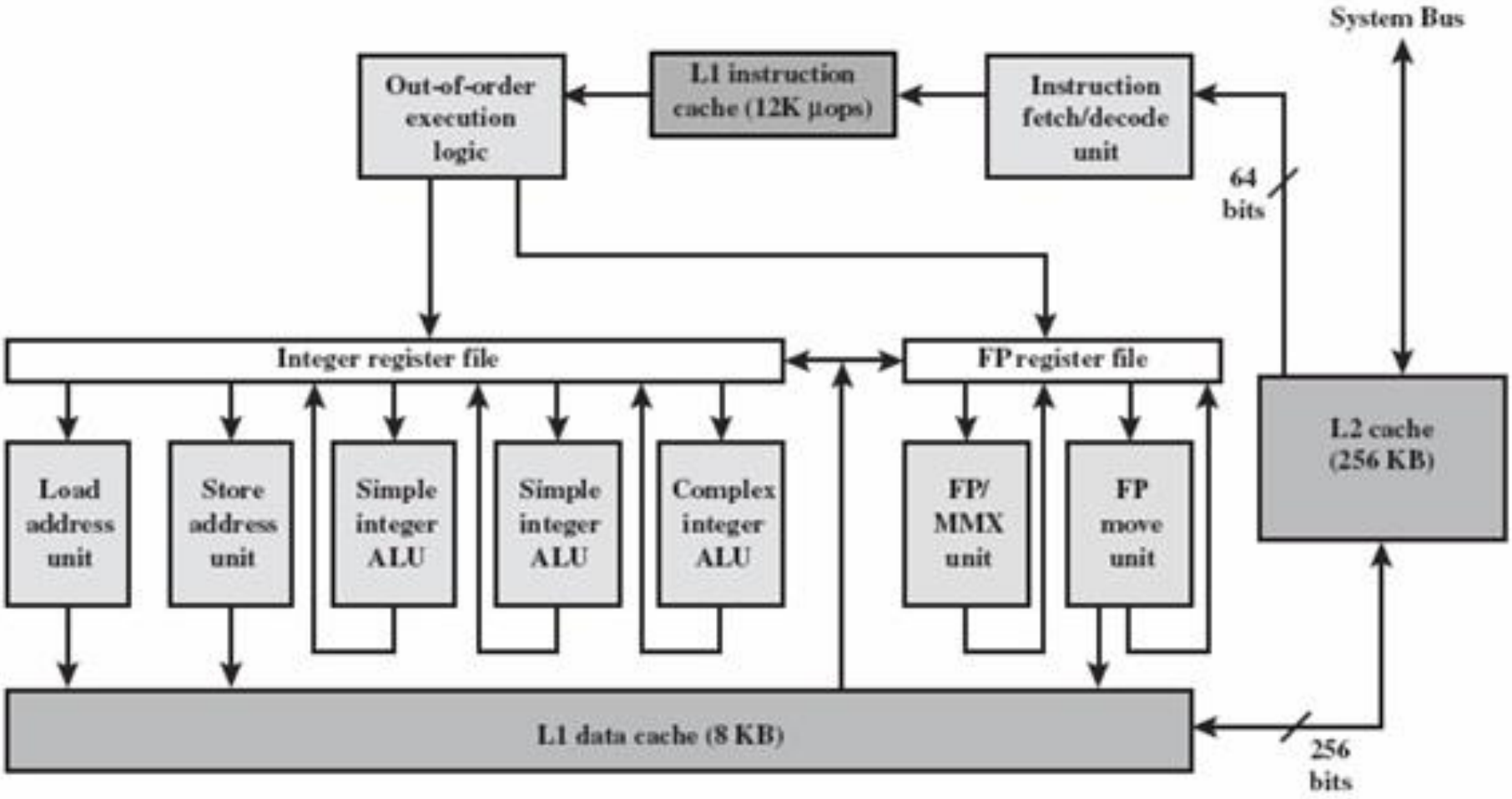
Intel Pentium 4 (Physical Pinout)



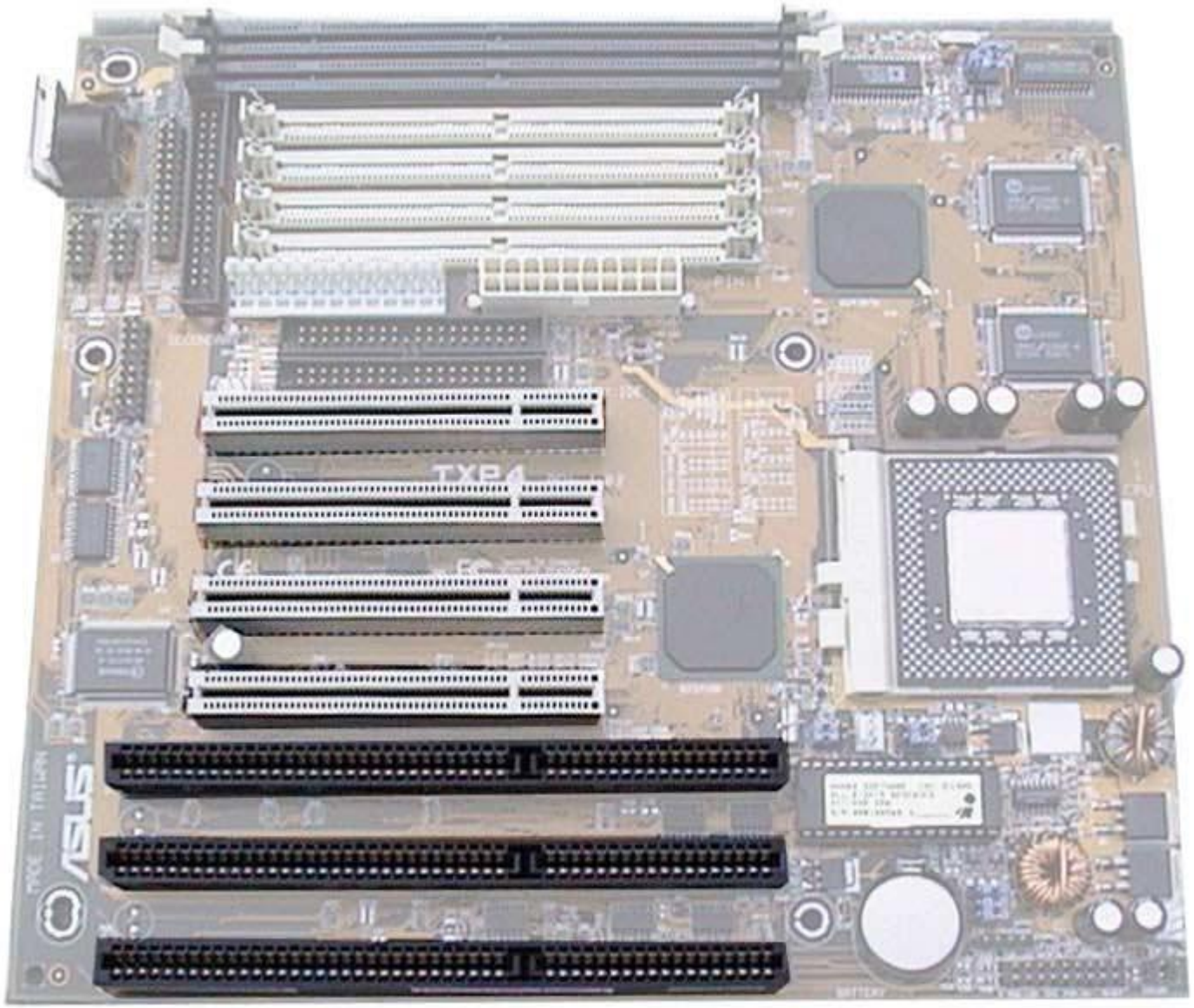
Intel Pentium 4 (Logical Pinout)



Intel Pentium 4 (Logical Block Diagram)

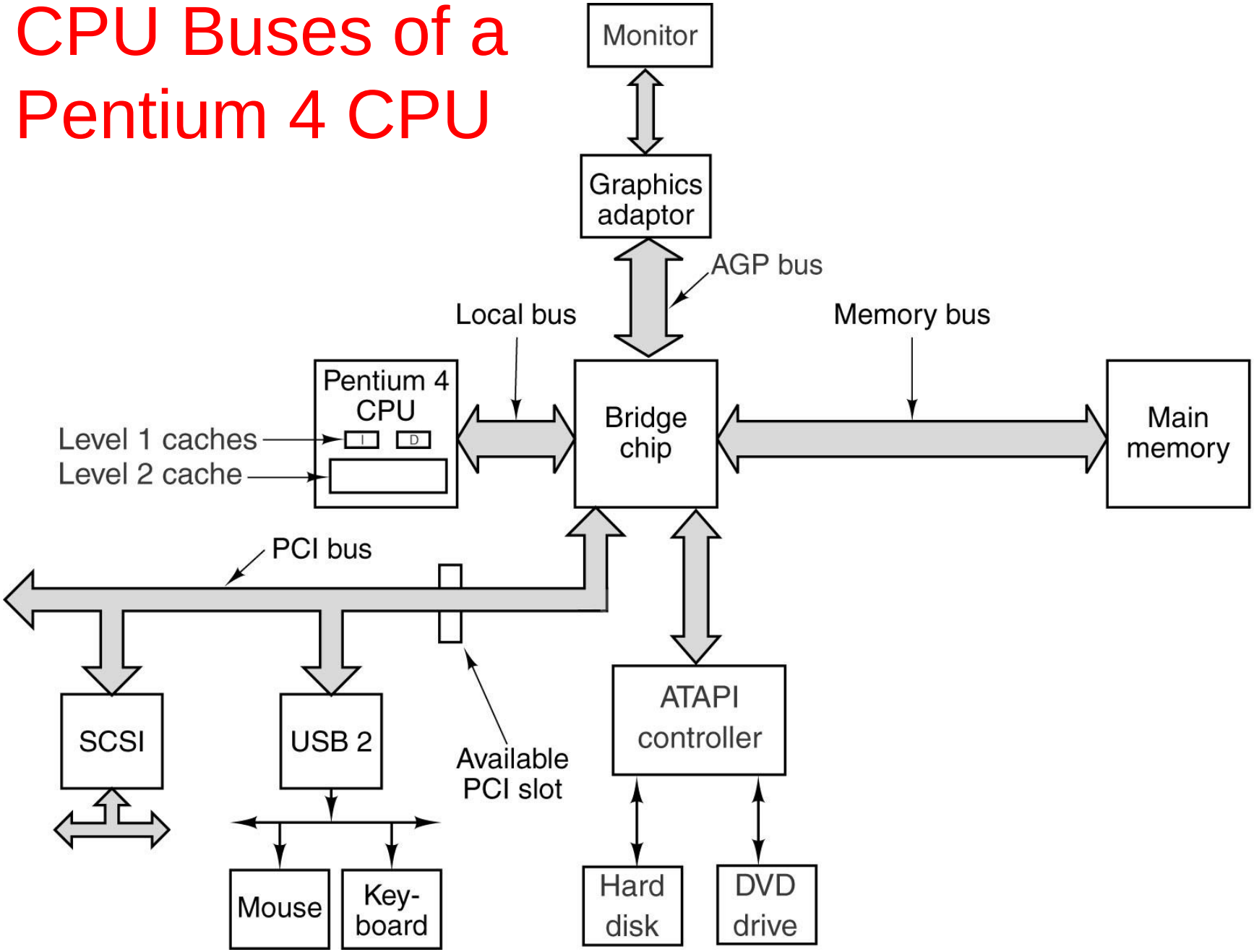


The PCI Bus – The ISA Bus

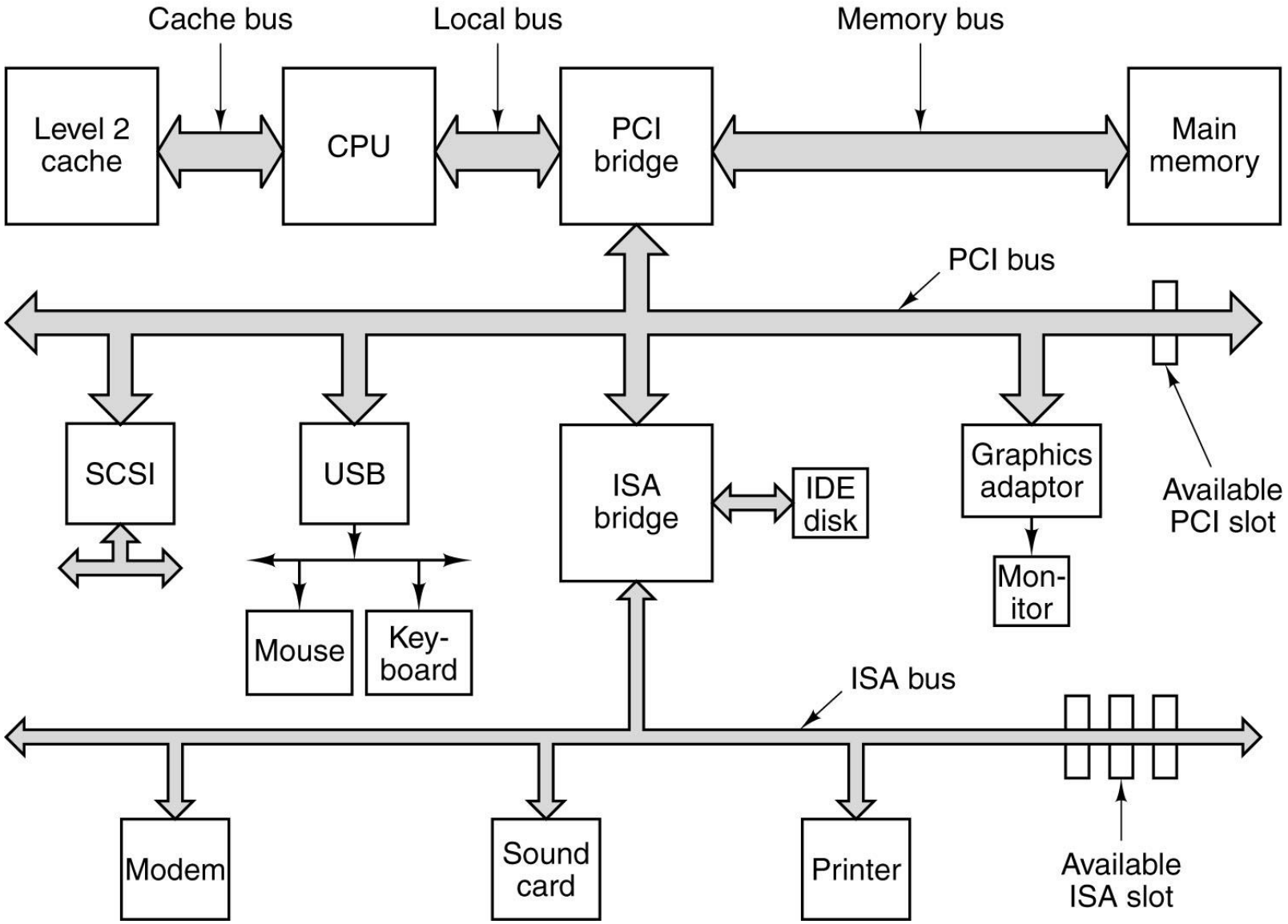


A Typical PCI Bus External Peripheral

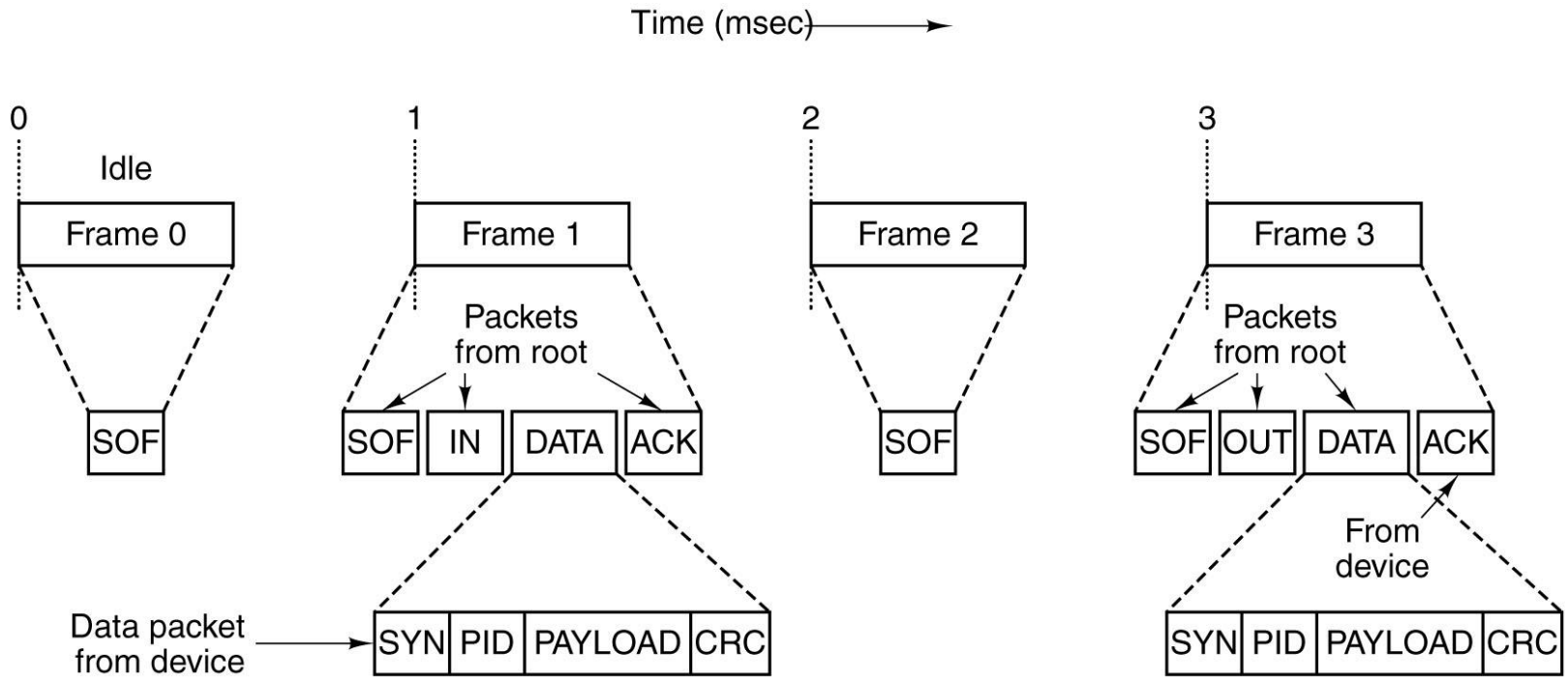
CPU Buses of a Pentium 4 CPU



The PCI Bus – The ISA Bus

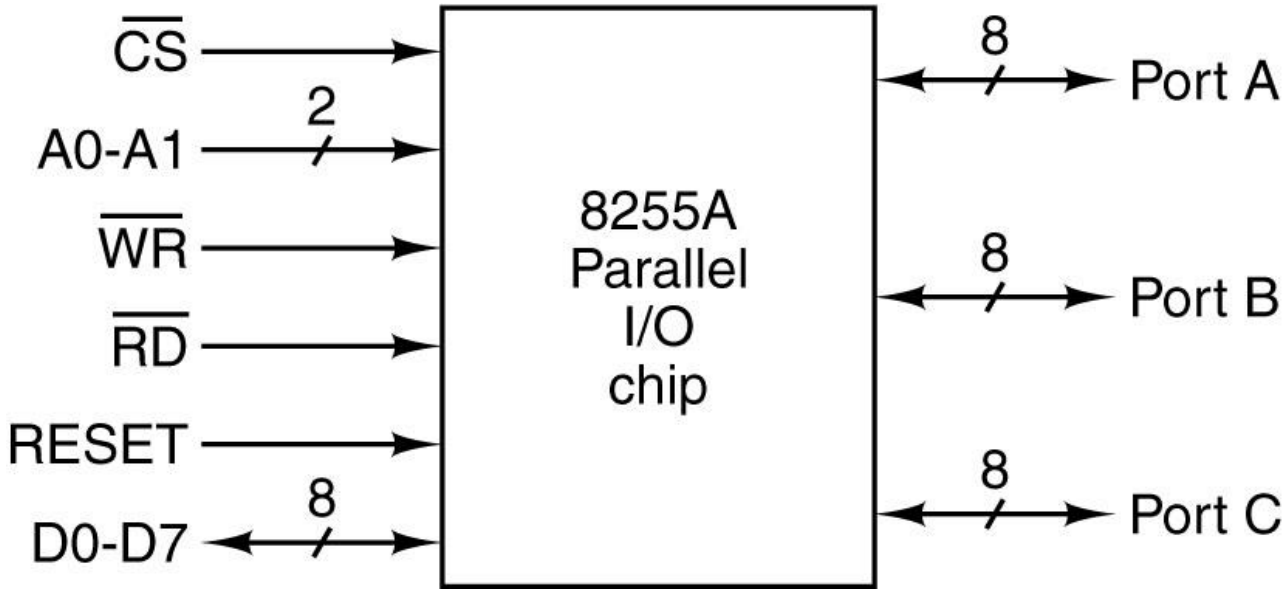


The Universal Serial Bus



The USB root hub sends out frames every 1.00 ms.

PIO Chips



An 8255A PIO chip.