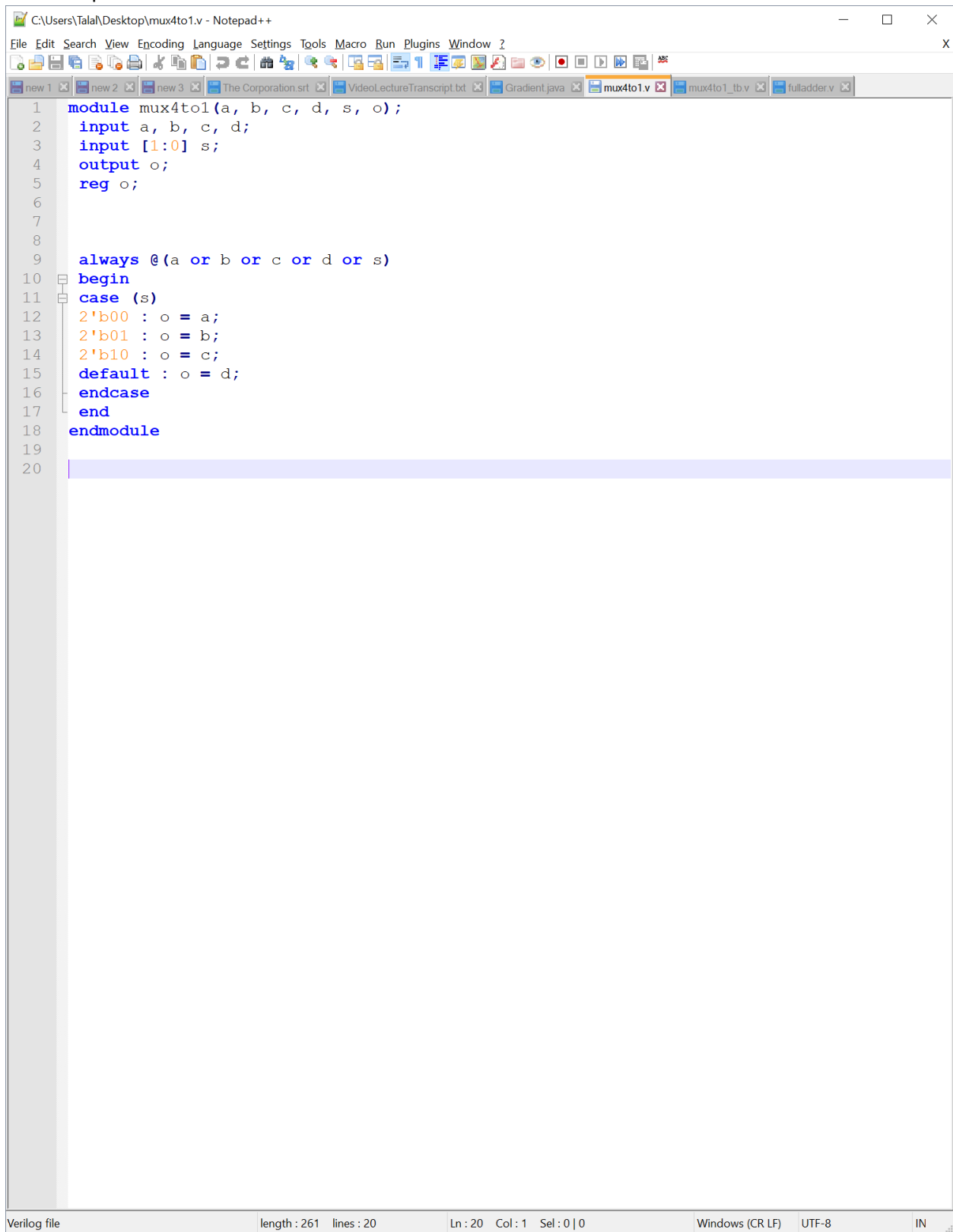


4x1 Multiplexer



```
1 module mux4to1(a, b, c, d, s, o);
2   input a, b, c, d;
3   input [1:0] s;
4   output o;
5   reg o;
6
7
8
9   always @(a or b or c or d or s)
10  begin
11    case (s)
12      2'b00 : o = a;
13      2'b01 : o = b;
14      2'b10 : o = c;
15      default : o = d;
16    endcase
17  end
18 endmodule
19
20
```

Verilog file length : 261 lines : 20 Ln : 20 Col : 1 Sel : 0 | 0 Windows (CR LF) UTF-8 IN

Attempting to compile

```
[jawaiddt@titan:19]> vcs +v2k mux4tol.v
Chronologic VCS (TM)
Version I-2014.03-2 -- Tue Oct 9 01:38:54 2018
Copyright (c) 1991-2014 by Synopsys Inc.
ALL RIGHTS RESERVED

This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.

Warning : License for product VCSCompiler_Net(723) will expire within 24 days, on: 01-nov-2018.

If you would like to temporarily disable this message, set
the VCS_LIC_EXPIRE_WARNING environment variable to the number of days
before expiration that you want this message to start (the minimum is 0).
Parsing design file 'mux4tol.v'
Top Level Modules:
    mux4tol
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module mux4tol
Warning : License for product VCSCompiler_Net(723) will expire within 24 days, on: 01-nov-2018.

If you would like to temporarily disable this message, set
the VCS_LIC_EXPIRE_WARNING environment variable to the number of days
before expiration that you want this message to start (the minimum is 0).
rm -f _csrc*.so linux_scvhdl_*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -m elf_i386 -shared -o ../../simv.daidir//_csrc1.so --whole-archive _vcsobj_1
ld -m elf_i386 -shared -o ../../simv.daidir//_csrc0.so 5NrI_d.o 5NrIB_d.o SIM_1.
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -m32 -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl
tubs.so /titan/software/synopsys14/vcs/linux/lib/libvirsim.so /titan/software/sy
are/synopsys14/vcs/linux/lib/libuclinaive.so -Wl,-whole-archive /titan/softwa
/linux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .219 seconds to compile + .166 seconds to elab + .395 seconds to link
[jawaiddt@titan:20]>
```

```
titan.ecs.csus.edu - PuTTY
Parsing design file 'mux4tol.v'
Top Level Modules:
    mux4tol
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module mux4tol
Warning : License for product VCSCompiler_Net(723) will expire within 24 days, on: 01-nov-2018.

If you would like to temporarily disable this message, set
the VCS_LIC_EXPIRE_WARNING environment variable to the number of days
before expiration that you want this message to start (the minimum is 0).
rm -f _csrc*.so linux_scvhdl_*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -m elf_i386 -shared -o ../../simv.daidir/_csrc1.so --whole-archive _vcsobj_1
ld -m elf_i386 -shared -o ../../simv.daidir/_csrc0.so 5NrI_d.o 5NrIB_d.o SIM_1.
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -m32 -Wl,-rpath-link=./ -Wl,-rpath=$ORIGIN/../../simv.daidir/ -Wl
tubs.so /titan/software/synopsys14/vcs/linux/lib/libvirsim.so /titan/software/sy
are/synopsys14/vcs/linux/lib/libuclnactive.so -Wl,-whole-archive /titan/softwa
/linux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .219 seconds to compile + .166 seconds to elab + .395 seconds to link
[jawaidt@titan:20]> simv
simv
simv.daidir/
[jawaidt@titan:20]> simv
Warning : License for product VCSRuntime_Net(725) will expire within 24 days, on: 01-nov-2018.

If you would like to temporarily disable this message, set
the VCS_LIC_EXPIRE_WARNING environment variable to the number of days
before expiration that you want this message to start (the minimum is 0).
Chronologic VCS simulator copyright 1991-2014
Contains Synopsys proprietary information.
Compiler version I-2014.03-2; Runtime version I-2014.03-2; Oct 9 01:40 2018
V C S   S i m u l a t i o n   R e p o r t
Time: 0
CPU Time:      0.530 seconds;      Data structure size:  0.0Mb
Tue Oct 9 01:40:01 2018
[jawaidt@titan:21]>
```

Attempting to run via simv

```
titan.ecs.csus.edu - PuTTY
Top Level Modules:
    mux4to1_tb
No TimeScale specified

Error-[URMI] Unresolved modules
mux4to1_tb.v, 6
"mux4to1 mux1( .a (a), .b (b), .c (c), .d (d), .s (s), .o (o));"
    Module definition of above instance is not found in the design.

1 error
CPU time: .128 seconds to compile
[jawaidt@titan:24]> vcs +v2k mux4to1_tb.v
                    Chronologic VCS (TM)
                    Version I-2014.03-2 -- Tue Oct  9 01:43:41 2018
                    Copyright (c) 1991-2014 by Synopsys Inc.
                    ALL RIGHTS RESERVED

This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.

Warning : License for product VCSCompiler_Net(723) will expire within 24 days, on: 01-nov-2018.

If you would like to temporarily disable this message, set
the VCS_LIC_EXPIRE_WARNING environment variable to the number of days
before expiration that you want this message to start (the minimum is 0).
Parsing design file 'mux4to1_tb.v'
Top Level Modules:
    mux4to1_tb
No TimeScale specified

Error-[URMI] Unresolved modules
mux4to1_tb.v, 6
"mux4to1 mux1( .a (a), .b (b), .c (c), .d (d), .s (s), .o (o));"
    Module definition of above instance is not found in the design.

1 error
CPU time: .126 seconds to compile
[jawaidt@titan:25]> █
```

Attempting to compile mux4to1_tb

4x1 Multiplexer test bench

```
C:\Users\Tala\Desktop\mux4to1_tb.v - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
new 1 new 2 new 3 The Corporation.srt VideoLectureTranscript.txt Gradient.java mux4to1.v mux4to1_tb.v fulladder.v
1 module mux4to1_tb;
2   reg a,b,c,d;
3   reg [1:0] s;
4   wire o;
5
6   mux4to1_mux mux1(.a(a),.b(b),.c(c),.d(d),s.(s),.o(o));
7
8   initial begin
9     $display("Talal Jawaaid");
10    $display("Time s d o");
11    $display("-----");
12    $monitor("%04d %b %b %b", $time, s, d, o);
13  end
14
15  initial begin
16
17      s = 2'b00; a=0; b=0; c=0; d=0; #10;
18      s = 2'b01; a=0; b=0; c=0; d=1; #10;
19      s = 2'b10; a=0; b=0; c=1; d=0; #10;
20      s = 2'b11; a=0; b=0; c=1; d=1; #10;
21      s = 2'b00; a=0; b=1; c=0; d=0; #10;
22      s = 2'b10; a=0; b=1; c=0; d=1; #10;
23  end
24 endmodule
```

Verilog file length : 604 lines : 24 Ln : 24 Col : 11 Sel : 0 | 0 Windows (CR LF) UTF-8 IN

Full Adder, 8 bit ripple carry adder, test bench

```
C:\Users\Tala\School\CSC 137\Project1\fulladder.v - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
new 1 new 2 new 3 The Corporation.srt VideoLectureTranscript.txt Gradient.java mux4to1.v mux4to1_tb.v fulladder.v
1 `timescale 1ns/1ps
2
3 module fullAdder(a,b,cin,sum,cout)
4     input a,b,cin;
5
6     output sum,cout;
7     assign sum = a^b^cin;
8     assign cout = (a&b) | (b&cin) | (c&a);
9 endmodule
10
11 module rippleAdder(a,b,cin,s,cout)
12
13     input [7:0] a,b;
14     input cin;
15     output [7:0] s;
16     output cout;
17     wire [7:1] c;
18
19     fullAdder f1(a[0],b[0],cin,s[0],c[1]);
20     fullAdder f2(a[1],b[1],cin,s[1],c[2]);
21     fullAdder f3(a[2],b[2],cin,s[2],c[3]);
22     fullAdder f4(a[3],b[3],cin,s[3],c[4]);
23     fullAdder f5(a[4],b[4],cin,s[4],c[5]);
24     fullAdder f6(a[5],b[5],cin,s[5],c[6]);
25     fullAdder f7(a[6],b[6],cin,s[6],c[7]);
26     fullAdder f8(a[7],b[7],cin,s[7],cout);
27
28 endmodule
29
30 module rippleAdder_tb;
31     reg [7:0] a,b;
32     reg cin;
33
34     wire [7:0] s;
35     wire cout;
36
37     fullAdder uut(.a(a),.b(b),.cin(cin),.sum(sum),.cout(cout));
38
39     initial begin
40         $display("Talal Jawaaid");
41     end
42
43     initial begin
44         a = 7'b0;
45
46         b = 7'b0;
47
48         cin = 7'b0;
49
50         #10;
51
52         a = 7'b0;
53
54         b = 7'b0;
55
56         cin = 7'b0;
57
58         #10;
59
Verilog file length: 1,690 lines: 139 Ln: 29 Col: 1 Sel: 0 | 0 Windows (CR LF) UTF-8 IN
```

C:\Users\Tala\School\CSC 137\Project1\fulladder.v - Notepad++

File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?

new 1 new 2 new 3 The Corporation srl VideoLectureTranscript.txt Gradient.java mux4to1.v mux4to1_tb.v fulladder.v

```
57
58     #10;
59
60     a = 7'b100010;
61
62     b = 7'b0;
63
64     cin = 7'b0;
65     #10;
66
67     a = 7'b110;
68
69     b = 7'b0;
70
71     cin = 7'b0;
72     #10;
73
74     a = 7'b101111;
75
76     b = 7'b0;
77
78     cin = 7'b0;
79     #10;
80
81     a = 7'b110;
82
83     b = 7'b0;
84
85     cin = 7'b0;
86     #10;
87
88     a = 7'b0;
89
90     b = 7'b0;
91
92     cin = 7'b11011;
93     #10;
94
95     a = 7'b1101;
96
97     b = 7'b0;
98
99     cin = 7'b0;
100    #10;
101
102    a = 7'b0;
103
104    b = 7'b0;
105
106    cin = 7'b0;
107    #10;
108
109    a = 7'b11110;
110
111    b = 7'b0;
112
113    cin = 7'b0;
114    #10;
```

Verilog file length : 1,690 lines : 139 Ln : 29 Col : 1 Sel : 0 | 0 Windows (CR LF) UTF-8 IN

```
C:\Users\Tala\School\CSC 137\Project1\fulladder.v - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
new 1 new 2 new 3 The Corporation srl VideoLectureTranscript.txt Gradient.java mux4to1.v mux4to1_tb.v fulladder.v
82
83     b = 7'b0;
84
85     cin = 7'b0;
86         #10;
87
88     a = 7'b0;
89
90     b = 7'b0;
91
92     cin = 7'b11011;
93         #10;
94
95     a = 7'b1101;
96
97     b = 7'b0;
98
99     cin = 7'b0;
100         #10;
101
102     a = 7'b0;
103
104     b = 7'b0;
105
106     cin = 7'b0;
107         #10;
108
109     a = 7'b11110;
110
111     b = 7'b0;
112
113     cin = 7'b0;
114         #10;
115
116     a = 7'b110;
117
118     b = 7'b0;
119
120     cin = 7'b0;
121         #10;
122
123     a = 7'b101;
124
125     b = 7'b1111;
126
127     cin = 7'b0;
128         #10;
129
130     a = 7'b101;
131
132     b = 7'b10;
133
134     cin = 7'b0;
135         #10;
136
137     end
138 endmodule
139
Verilog file length : 1,690 lines : 139 Ln : 29 Col : 1 Sel : 0 | 0 Windows (CR LF) UTF-8 IN
```



```
titan.ecs.csus.edu - PuTTY
Warning-[PCWM-W] Port connection width mismatch
fulladder.v, 37
"fulladder uut( .a (a), .b (b), .cin (cin), .sum (sum), .cout (cout));"
  The following 8-bit expression is connected to 1-bit port "b" of module
  "fulladder", instance "uut".
  Expression: b
    use +lint=PCWM for more details

Starting vcs inline pass...
2 modules and 0 UDP read.
recompiling module rippleAdder because:
  Generated file (15f6_1) not found, or not incremental.
recompiling module rippleAdder_tb because:
  Generated file (Zyh8_1) not found, or not incremental.
Both modules done.
Warning : License for product VCSCompiler_Net(723) will expire within 24 days, on: 01-nov-2018.

If you would like to temporarily disable this message, set
the VCS_LIC_EXPIRE_WARNING environment variable to the number of days
before expiration that you want this message to start (the minimum is 0).
rm -f _csrc*.so linux_scvhdl *.so pre_vcsobj *.so share_vcsobj *.so
ld -m elf_i386 -shared -o ../simv.daidir/_csrc1.so --whole-archive _vcsobj_1
1.a --no-whole-archive
ld -m elf_i386 -shared -o ../simv.daidir/_csrc0.so 5NrI_d.o 5NrIB_d.o SIM_1.
o
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -m32 -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl
,-rpath='$ORIGIN'/simv.daidir/scsim.db.dir _csrc1.so _csrc0.so rmapats_mop
.o rmapats.o rmar.o /titan/software/synopsys14/vcs/linux/lib/libzeroso
ft_rt_stubs.so /titan/software/synopsys14/vcs/linux/lib/libvirsim.so /titan/soft
ware/synopsys14/vcs/linux/lib/librterrorinf.so /titan/software/synopsys14/vcs/li
nux/lib/libsnpsmalloc.so /titan/software/synopsys14/vcs/linux/lib/libvcsnew.s
o /titan/software/synopsys14/vcs/linux/lib/libuclinative.so -Wl,-whole-archive
/titan/software/synopsys14/vcs/linux/lib/libvcsucli.so -Wl,-no-whole-archive
/titan/software/synopsys14/vcs/linux/lib/vcs_save_restore_new.o /titan/so
ftware/synopsys14/vcs/linux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .241 seconds to compile + .176 seconds to elab + .403 seconds to link
[jawaidt@titan:37]>
```

Compiling fulladder.v

```
titan.ecs.csus.edu - PuTTY
Warning : License for product VCSCompiler_Net(723) will expire within 24 days, on
n: 01-nov-2018.

If you would like to temporarily disable this message, set
the VCS_LIC_EXPIRE_WARNING environment variable to the number of days
before expiration that you want this message to start (the minimum is 0).
rm -f _csrc*.so linux_scvhdl_*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -m elf_i386 -shared -o ../simv.daidir/_csrc1.so --whole-archive _vcsobj_1
1.a --no-whole-archive
ld -m elf_i386 -shared -o ../simv.daidir/_csrc0.so 5NrI_d.o 5NrIB_d.o SIM_1.
o
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -m32 -Wl,-rpath-link=../ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl
,-rpath='$ORIGIN'/simv.daidir/scsim.db.dir _csrc1.so _csrc0.so rmapats_mop
.o rmapats.o rmar.o /titan/software/synopsys14/vcs/linux/lib/libzeroso
ft_rt_stubs.so /titan/software/synopsys14/vcs/linux/lib/libvirsim.so /titan/soft
ware/synopsys14/vcs/linux/lib/librterrorinf.so /titan/software/synopsys14/vcs/li
nux/lib/libsnpsmalloc.so /titan/software/synopsys14/vcs/linux/lib/libvcsnew.s
o /titan/software/synopsys14/vcs/linux/lib/libuclinative.so -Wl,-whole-archive
/titan/software/synopsys14/vcs/linux/lib/libvcsucli.so -Wl,-no-whole-archive
/titan/software/synopsys14/vcs/linux/lib/vcs_save_restore_new.o /titan/so
ftware/synopsys14/vcs/linux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .241 seconds to compile + .176 seconds to elab + .403 seconds to link
[jawaidt@titan:37]> simv
Warning : License for product VCSRuntime_Net(725) will expire within 24 days, on
: 01-nov-2018.

If you would like to temporarily disable this message, set
the VCS_LIC_EXPIRE_WARNING environment variable to the number of days
before expiration that you want this message to start (the minimum is 0).
Chronologic VCS simulator copyright 1991-2014
Contains Synopsys proprietary information.
Compiler version I-2014.03-2; Runtime version I-2014.03-2; Oct 9 01:49 2018
Talal Jawaidd

V C S   S i m u l a t i o n   R e p o r t
Time: 120000 ps
CPU Time:      0.550 seconds;      Data structure size:  0.0Mb
Tue Oct 9 01:49:29 2018
[jawaidt@titan:38]>
```

Attempting to run via simv

All files compiled, synthesized, and ran through Quartus and Vivado. Not sure why VCS and SIMV weren't working. Test benches did not correctly work in Quartus or Vivado.