SACRAMENTO STATE

CPE 151/EEE 234
Digital IC Design

Project No. 1

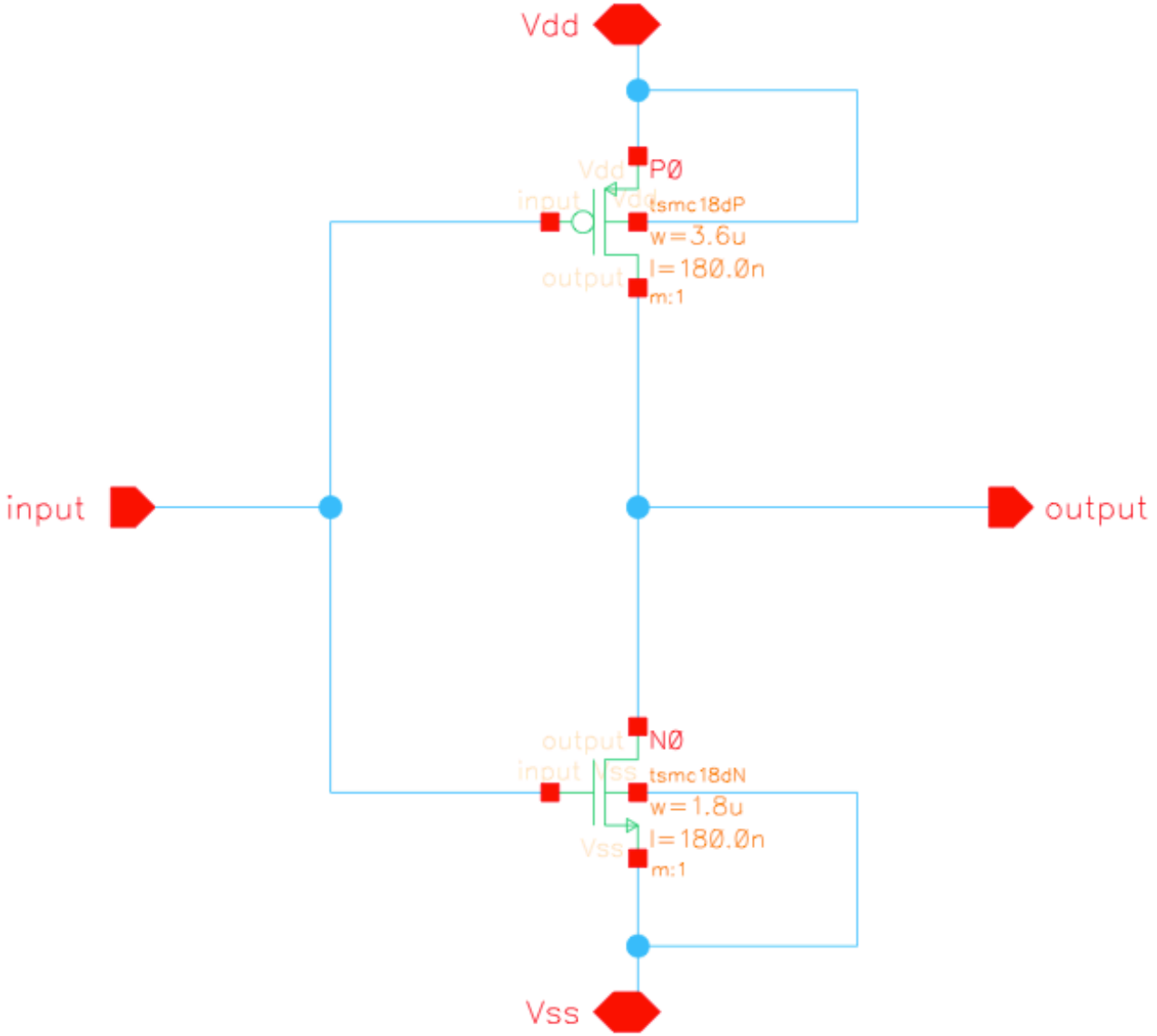
Student Name:
Email ID:
Date of Submission:

Table of Contents

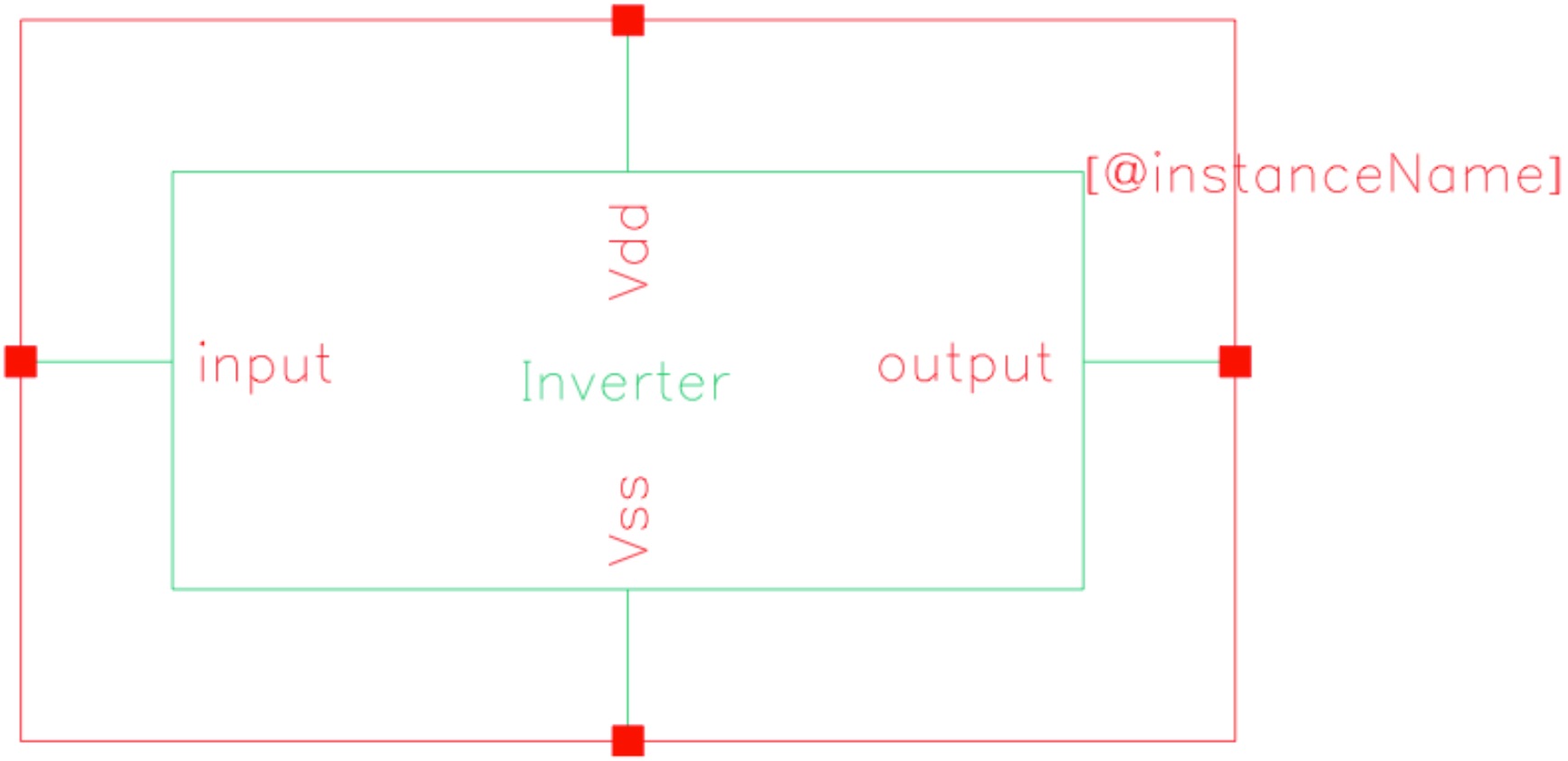
Inverter

$(W/L)_n = 1.8/0.18$
$(W/L)_p = 3.6/0.18$

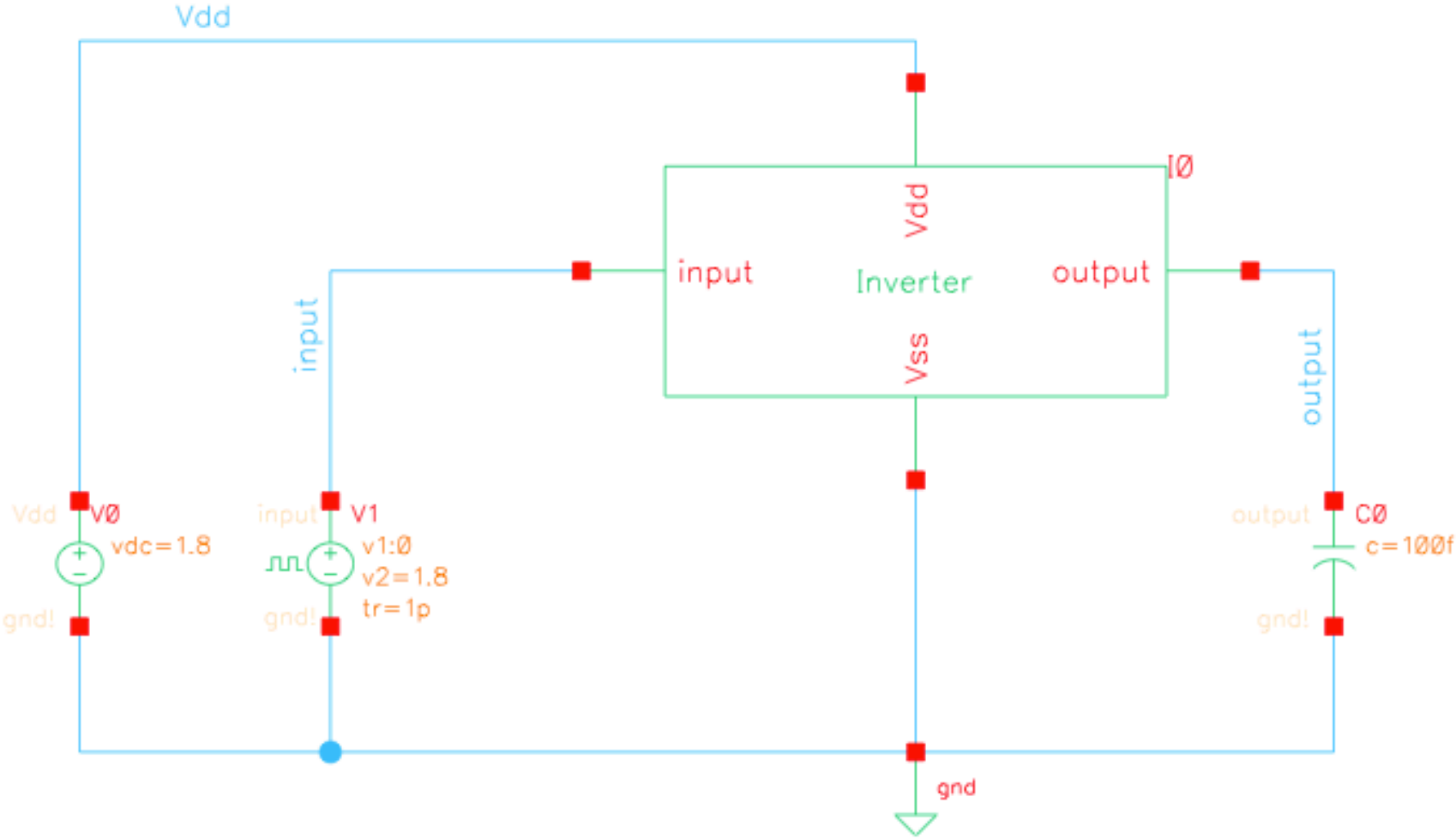
Inverter Schematic



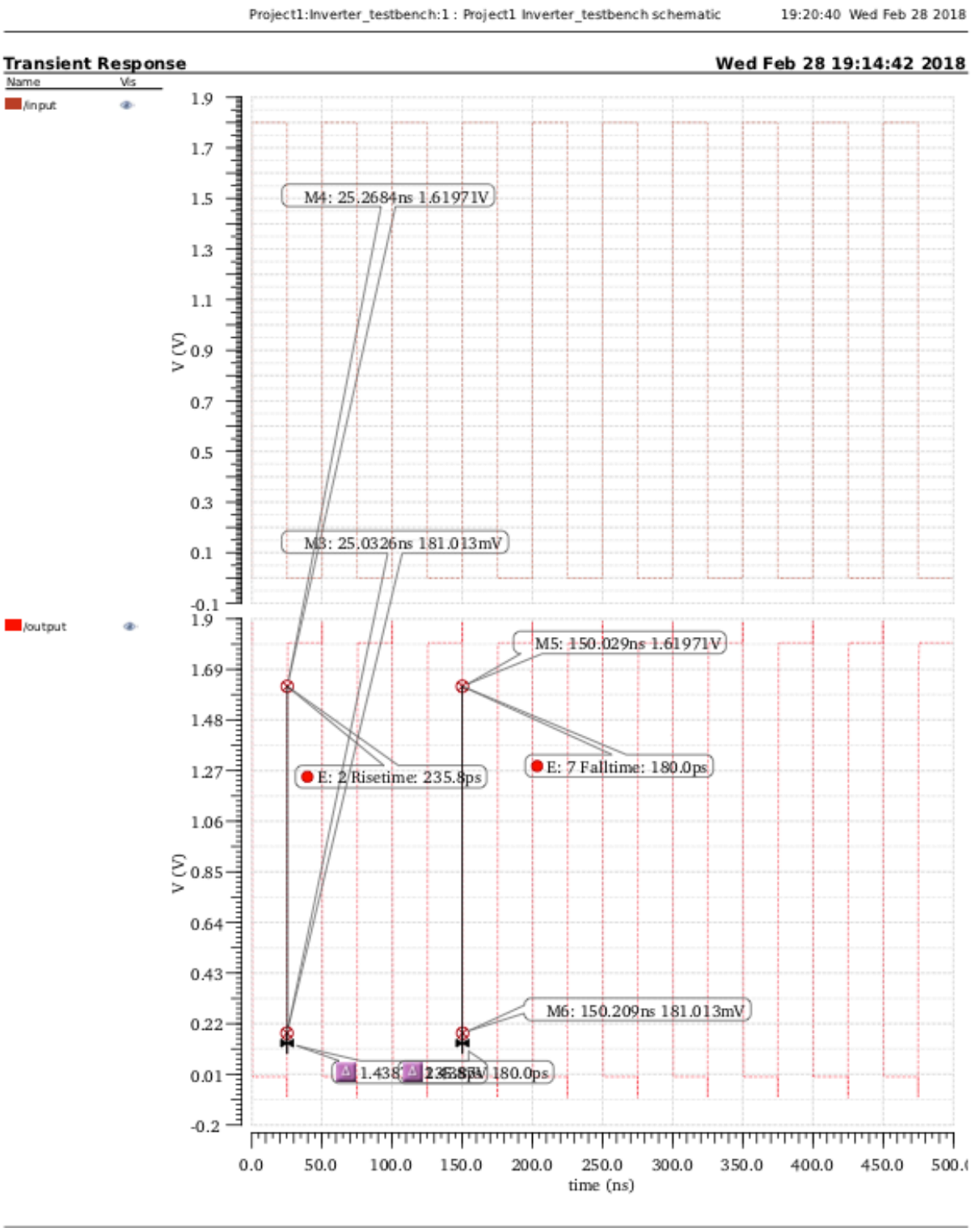
Inverter Symbol



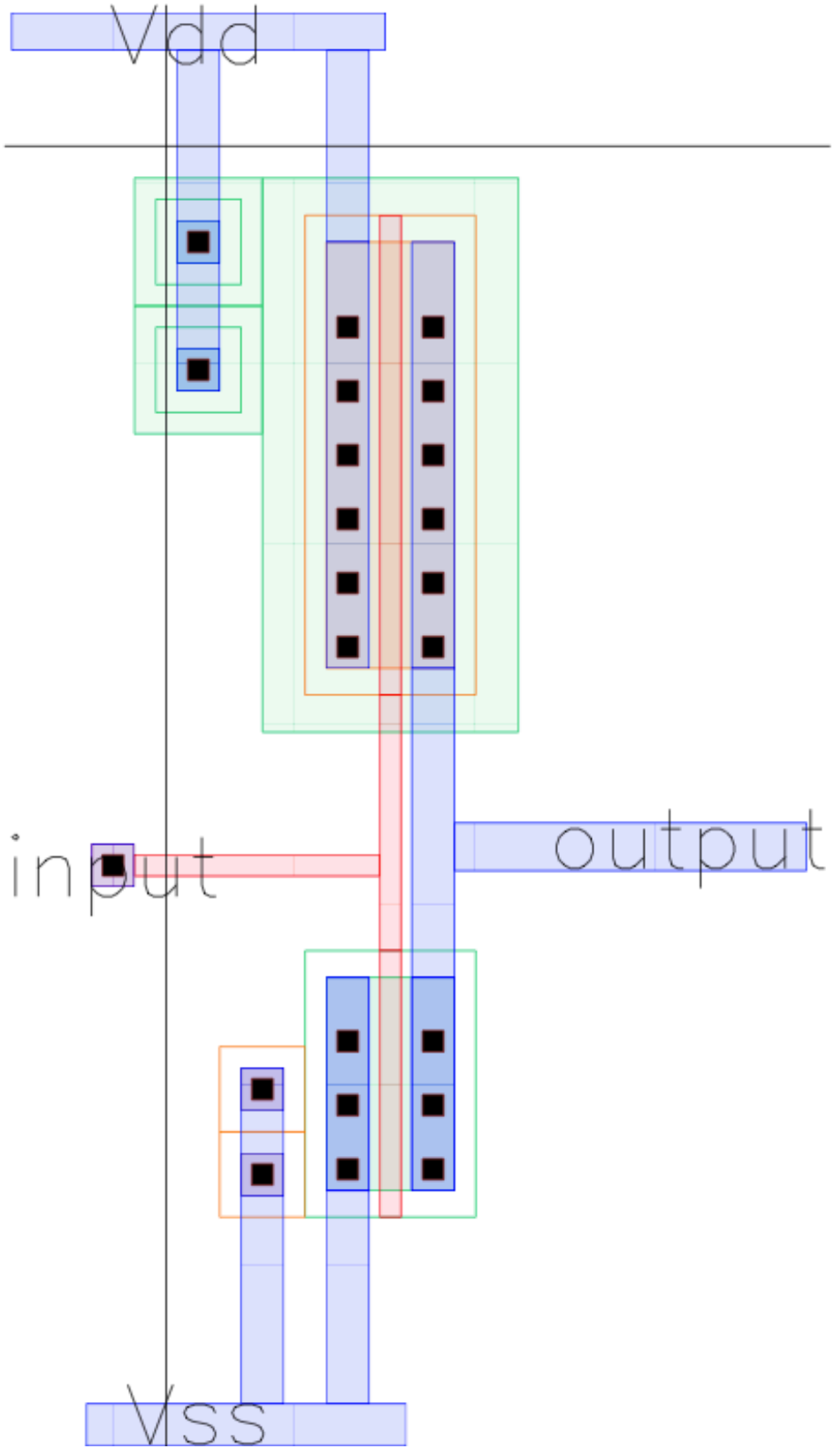
Inverter Testbench



Inverter Testbench Waveform



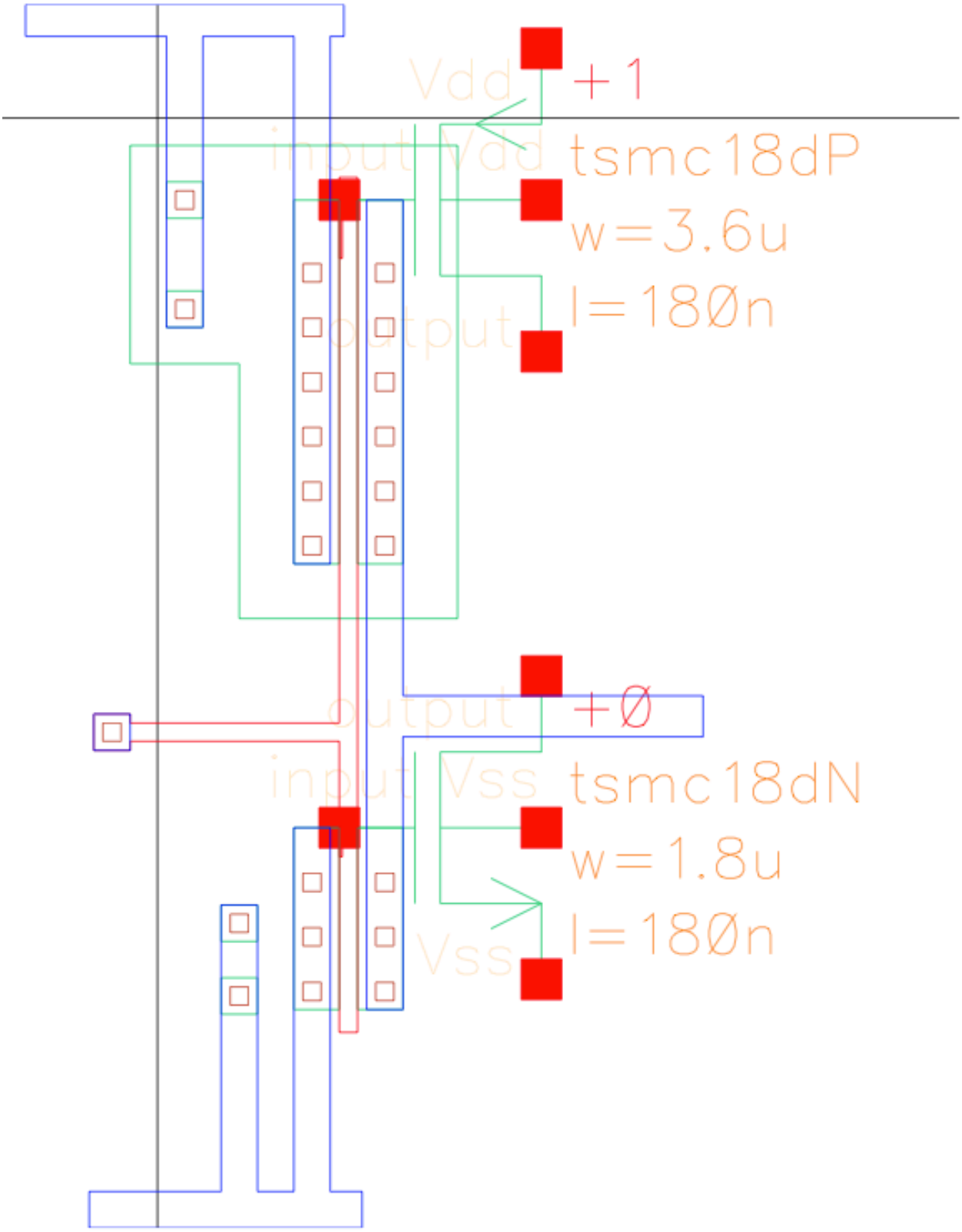
Inverter Layout



Inverter DRC

```
Getting layout propert bag
DRC started at Thu Mar  1 22:07:09 2018

Validating hierarchy instantiation for:
library: Project1
cell:    Inverter_Layout
view:    layout
Rules come from library NCSU_TechLib_tsmc02d.
Rules path is divaDRC.rul.
Inclusion limit is set to 1000.
Running layout DRC analysis
Flat mode
Full checking.
DRC started.......Thu Mar  1 22:07:09 2018
    completed ....Thu Mar  1 22:07:09 2018
    CPU TIME = 00:00:00  TOTAL TIME = 00:00:00
*********   Summary of rule violations for cell "Inverter_Layout layout"   *********
   Total errors found: 0
```

Inverter Extract



Inverter LVS

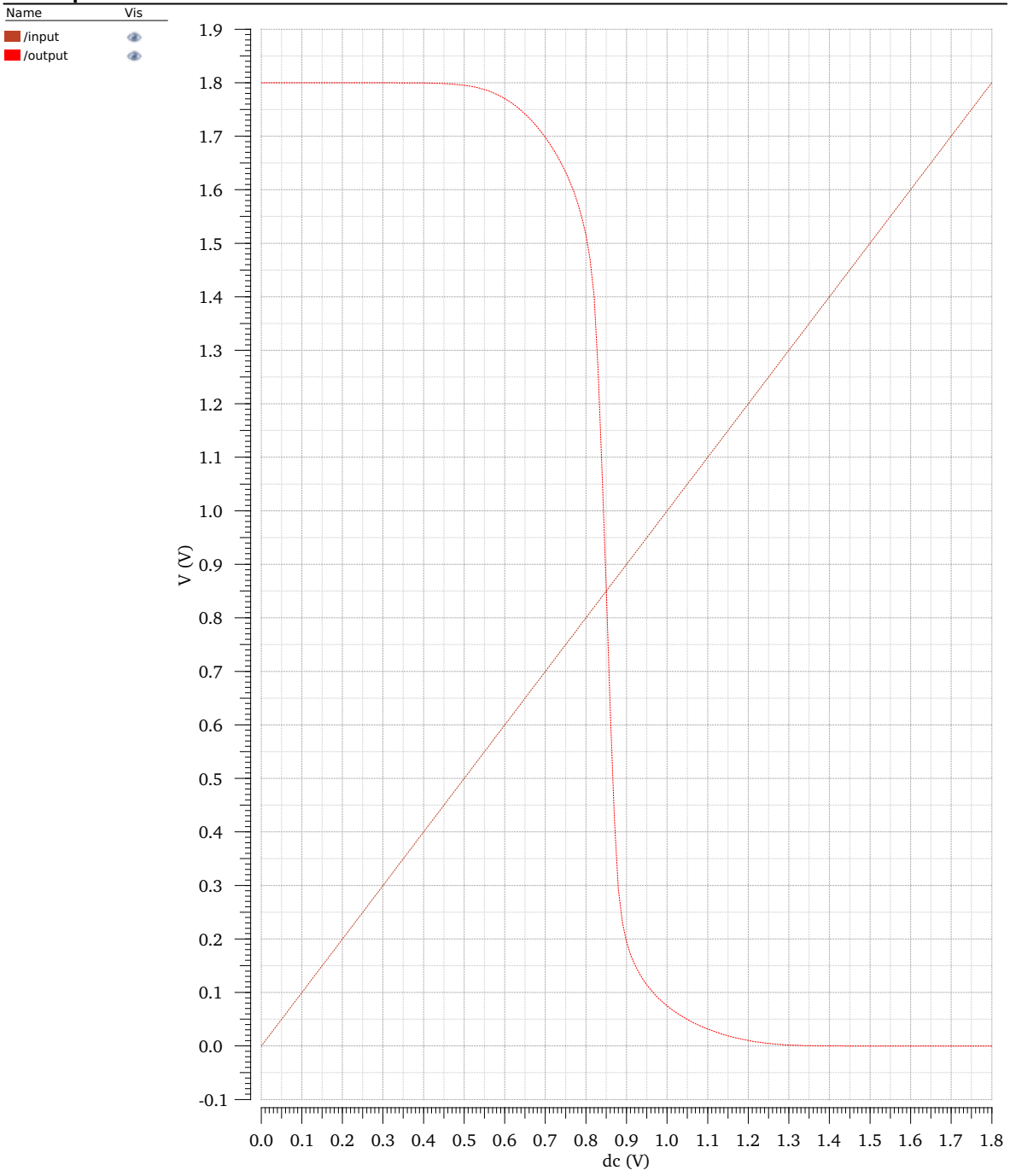
```
@(#)$CDS: LVS version 6.1.7-64b 09/27/2016 19:41 (sjfhw305) $

Command line: /software/cadence/installs/IC617/tools.lnx86/dfII/bin/
64bit/LVS -dir /gaia/class/studen[redacted]/CPE151/LVS -l -s -t /gaia/
class/student/[redacted]CPE151/LVS/layout /gaia/class/student/[redacted]
CPE151/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

    Net-list summary for /gaia/class/student/[redacted]CPE151/LVS/layout/
netlist
       count
        4               nets
        0               terminals
        1               pmos
        1               nmos

    Net-list summary for /gaia/class/student[redacted]CPE151/LVS/
schematic/netlist
       count
        4               nets
        4               terminals
        1               pmos
        1               nmos

Devices in the rules but not in the netlist:
        cap nfet pfet nmos4 pmos4

The net-lists match.

                            layout  schematic
                               instances
        un-matched              0       0
        rewired                 0       0
        size errors             0       0
        pruned                  0       0
        active                  2       2
        total                   2       2

                                 nets
        un-matched              0       0
        merged                  0       0
        pruned                  0       0
        active                  4       4
        total                   4       4

                               terminals
        un-matched              0       0
```

```
        matched but
        different type          0       0
        total                   0       4

Probe files from /gaia/class/student[redacted]CPE151/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /gaia/class/student[redacted]CPE151/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:
```

Inverter Post Layout Simulation

Project1:Inverter_testbench:1 : Project1 Inverter_testbench schematic 22:09:15 Thu Mar 1 2018

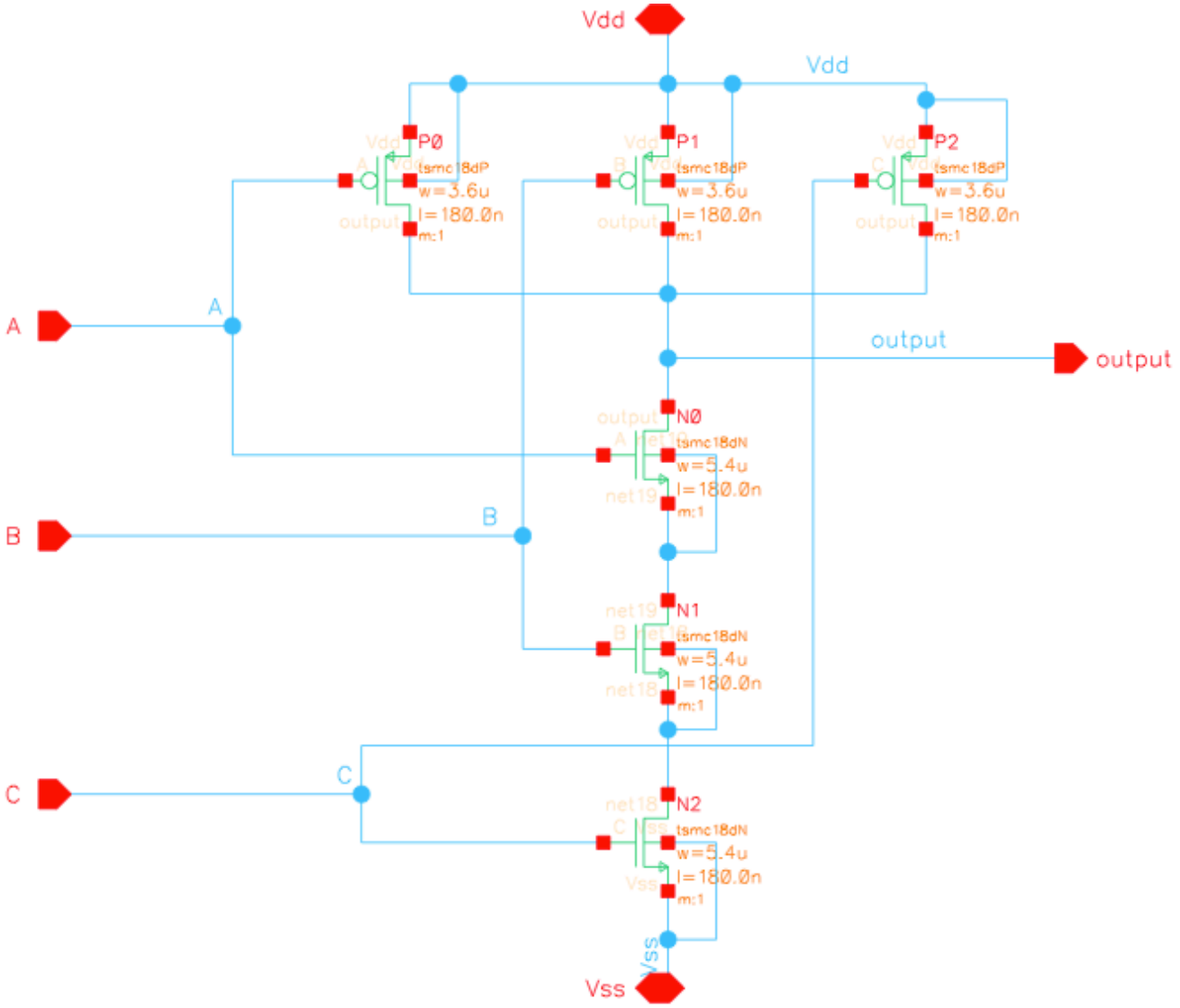
DC Response **Thu Mar 1 22:05:08 2018**



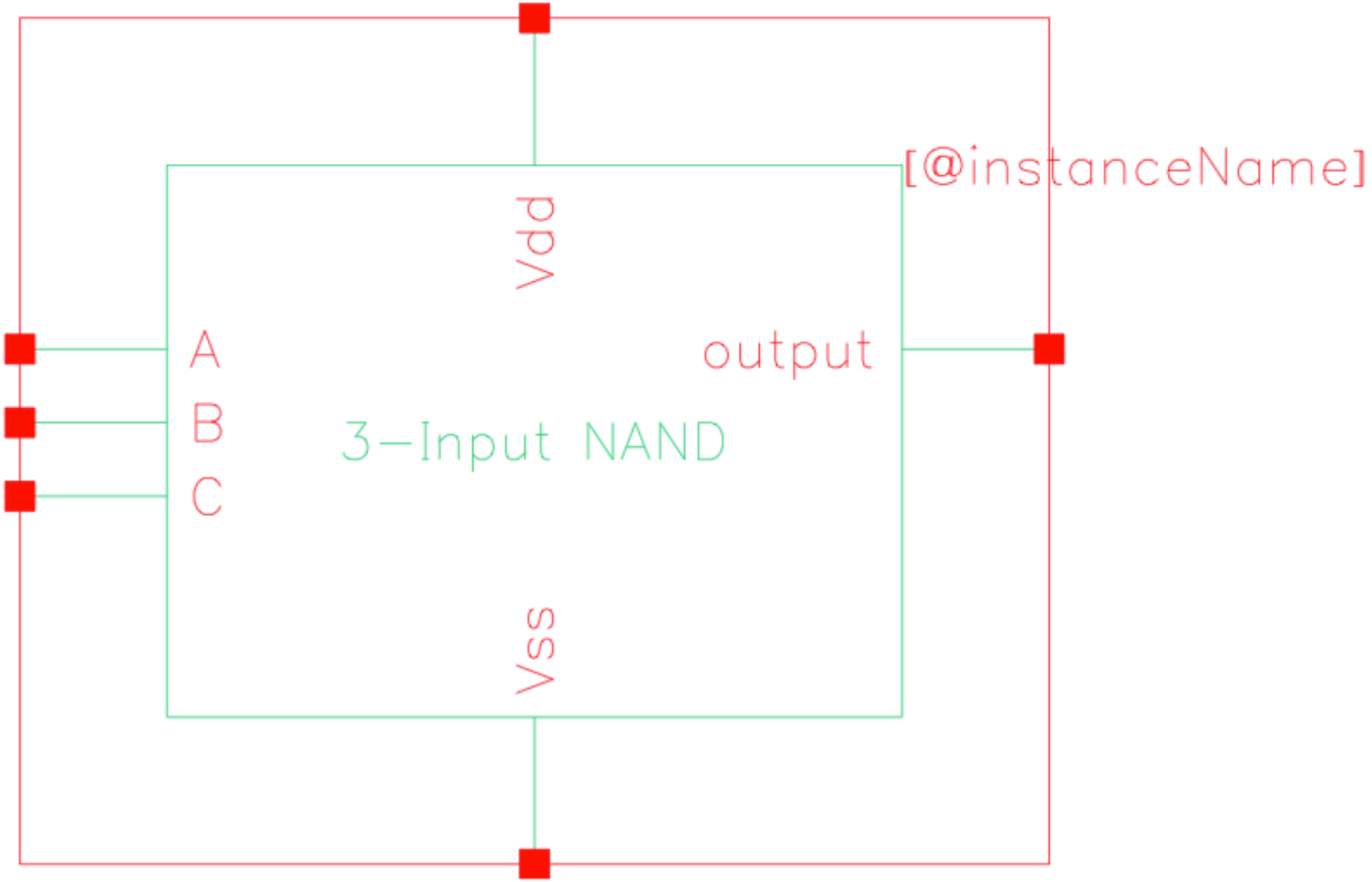
3-Input NAND Gate

$(W/L)_n = 5.4/0.18$
$(W/L)_p = 3.6/0.18$

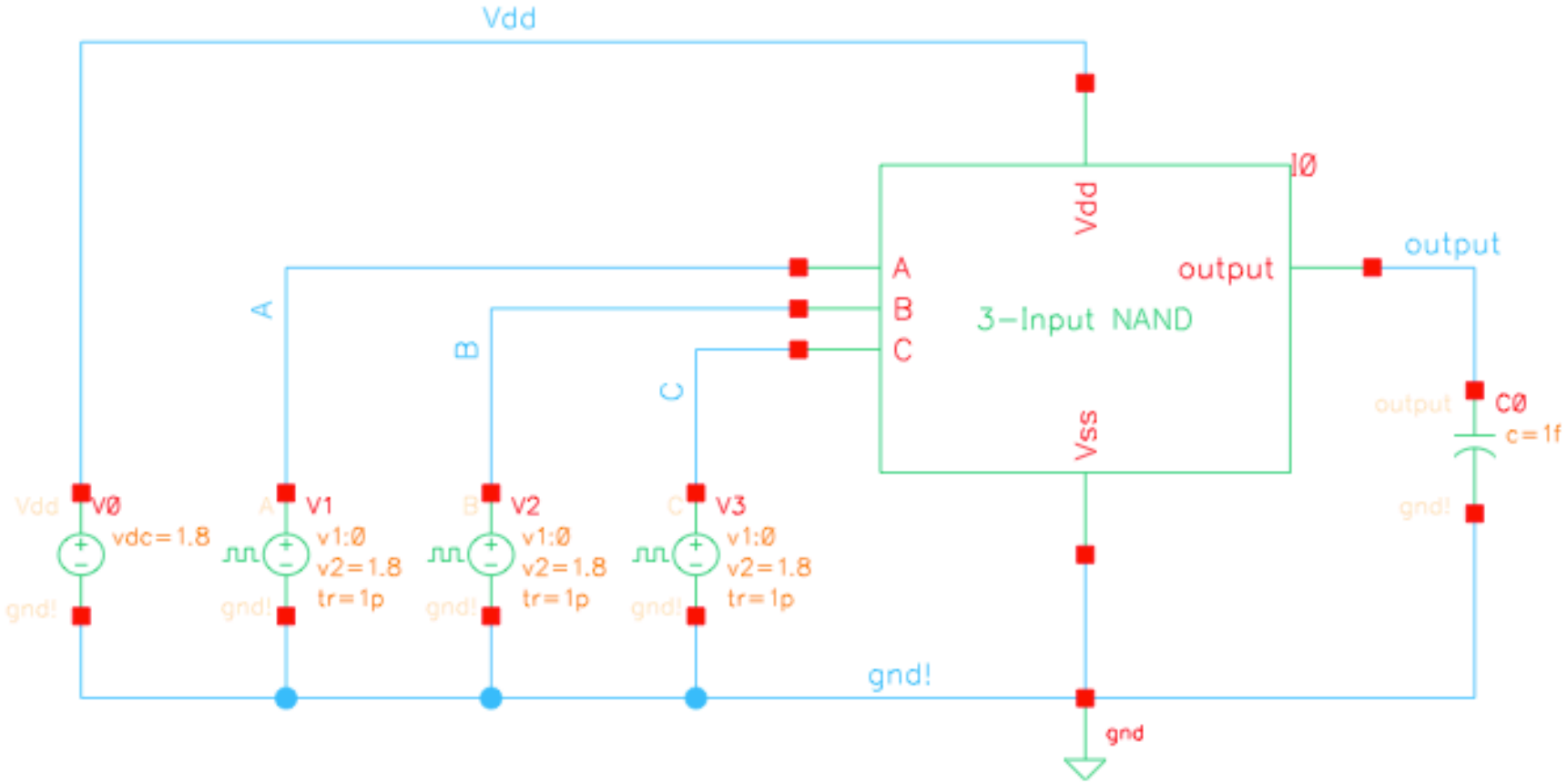
3-Input NAND Gate Schematic



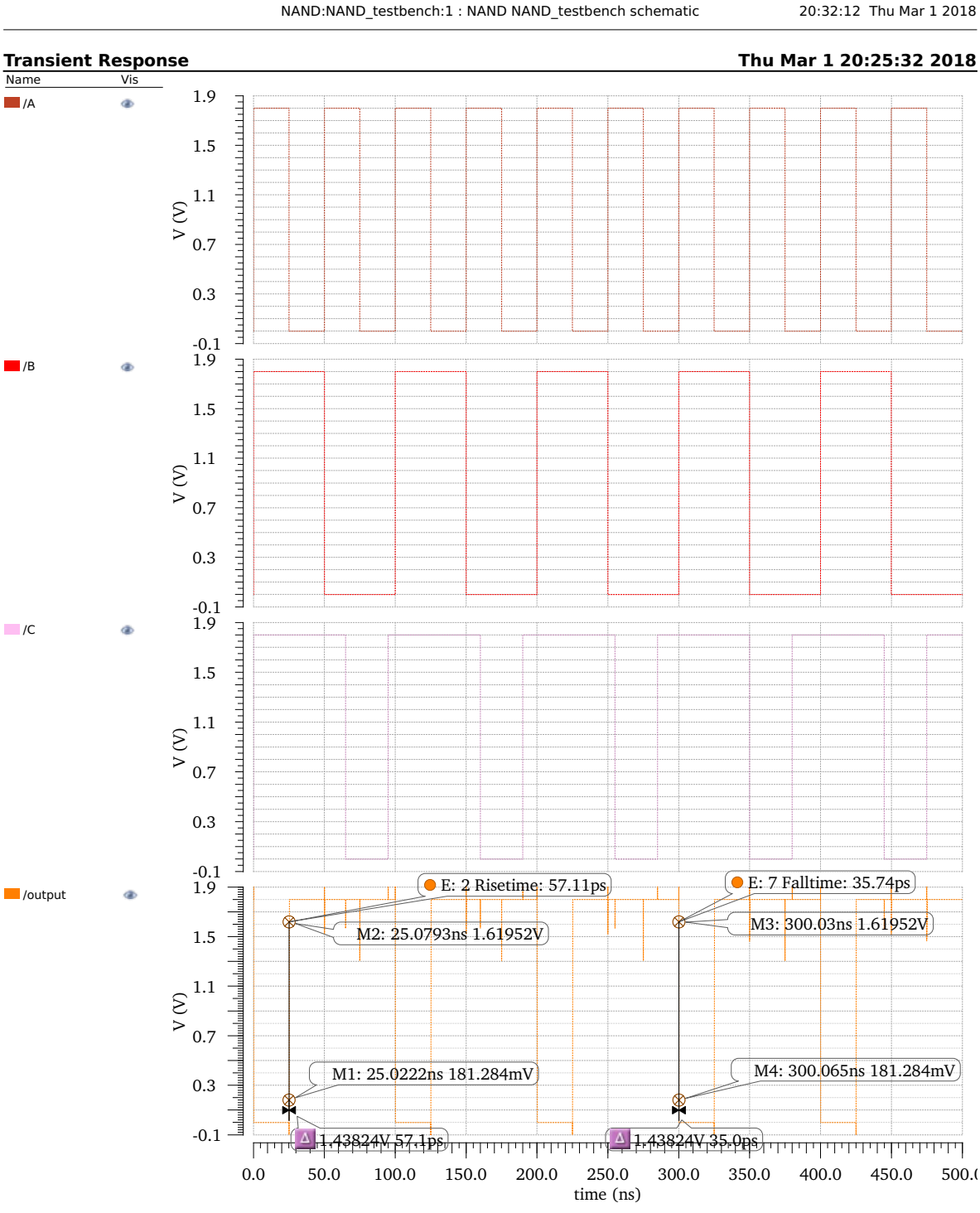
3-Input NAND Gate Symbol



3-Input NAND Gate Testbench



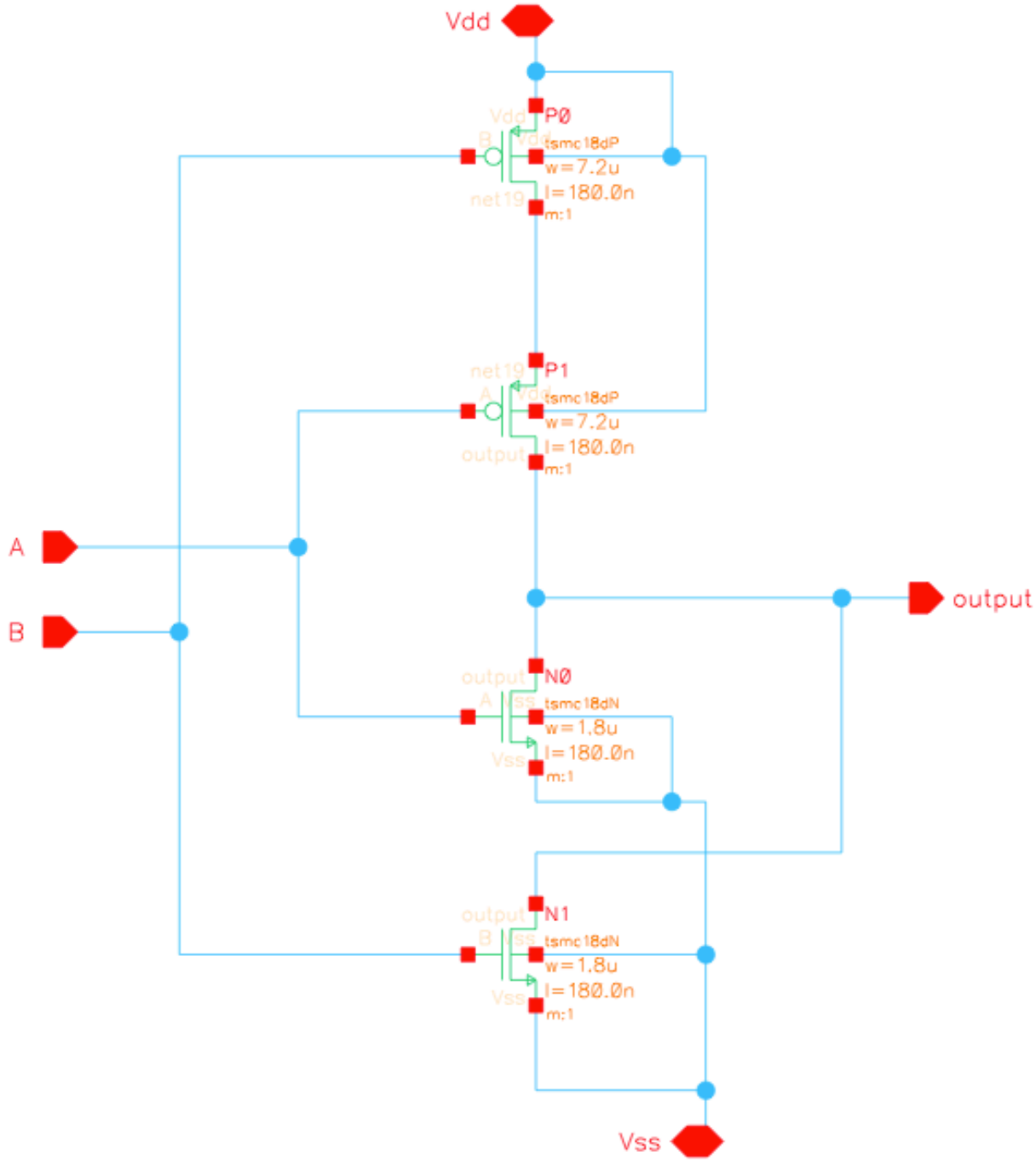
3-Input NAND Gate Testbench Waveform



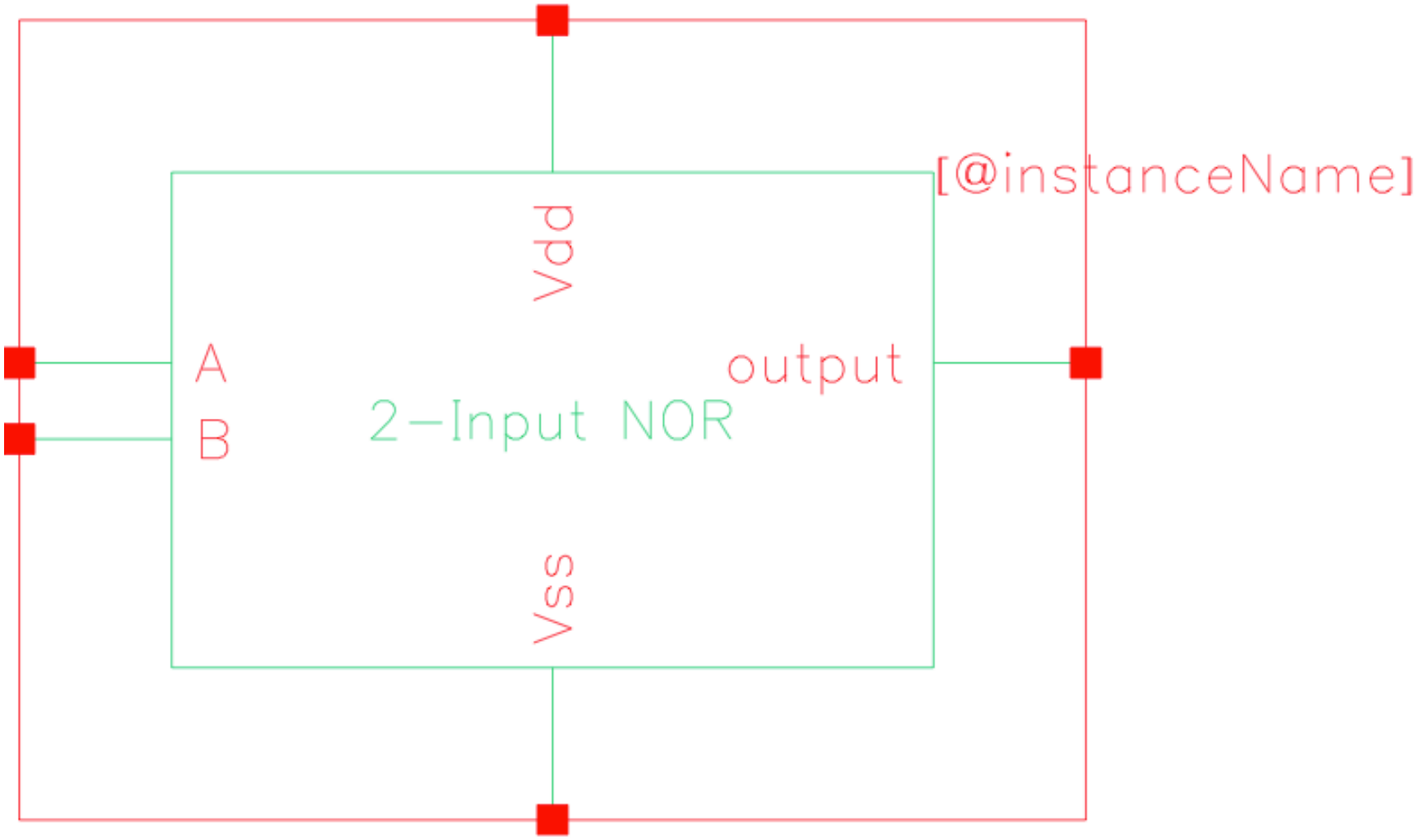
2-Input NOR Gate

$(W/L)_n = 1.8/0.18$
$(W/L)_p = 7.2/0.18$

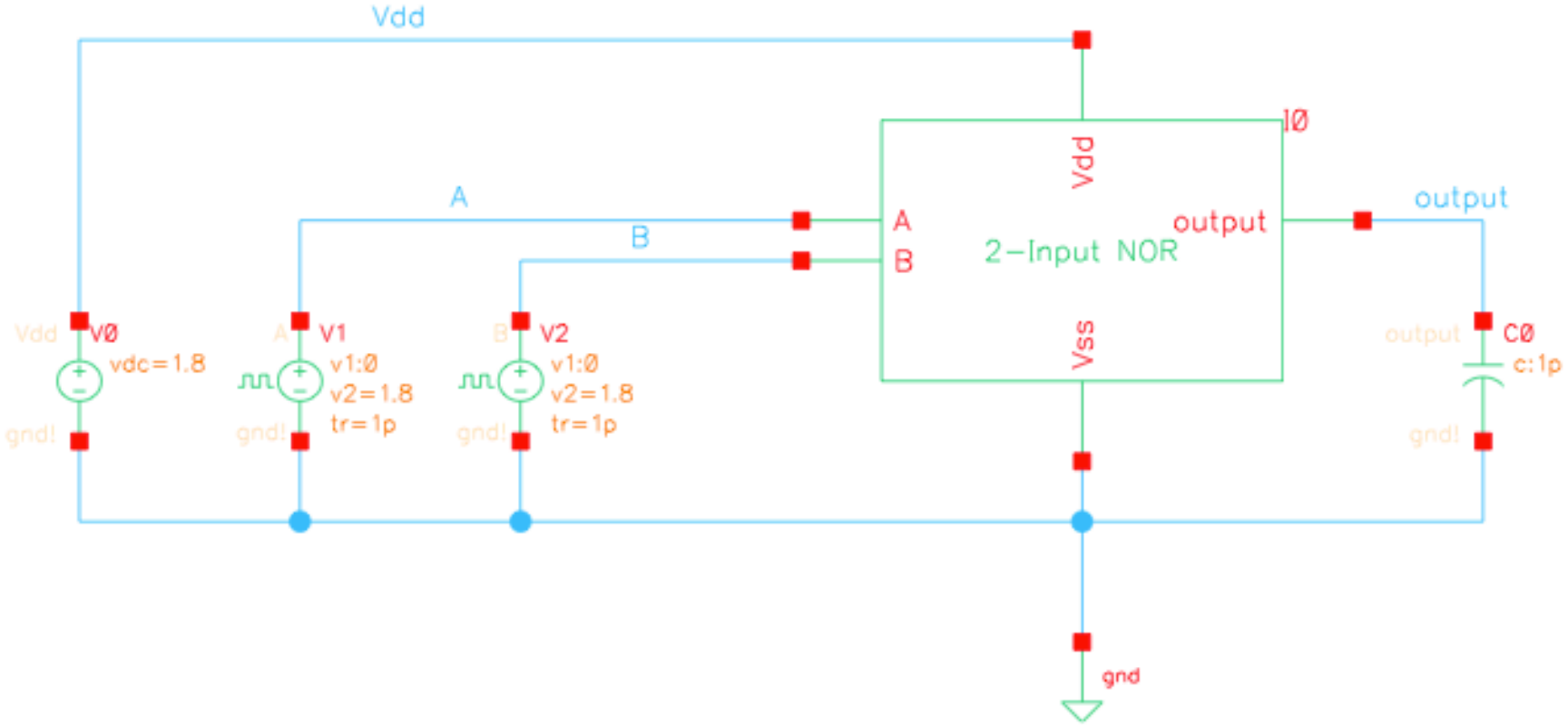
2-Input NOR Gate Schematic



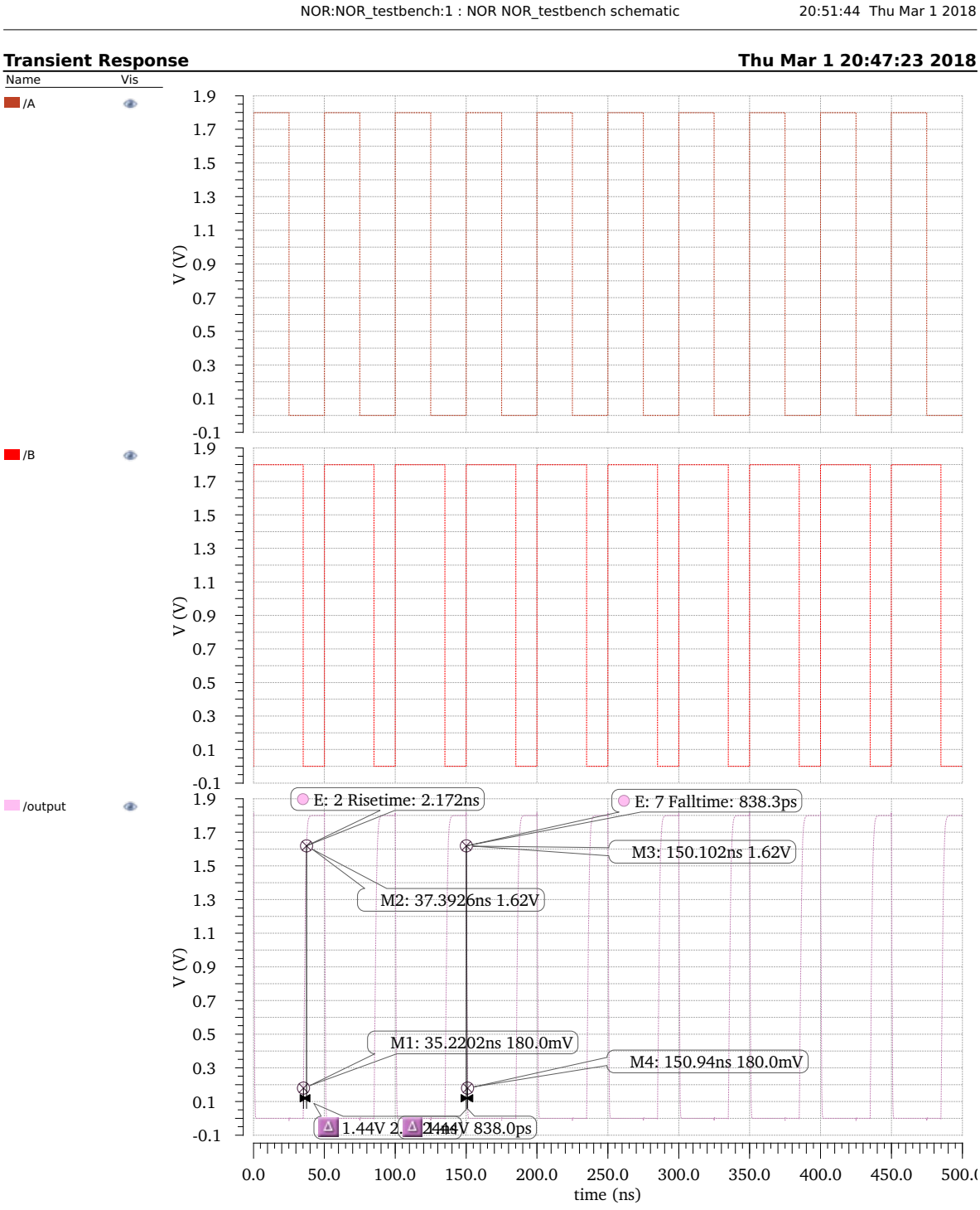
2-Input NOR Gate Symbol



2-Input NOR Gate Testbench



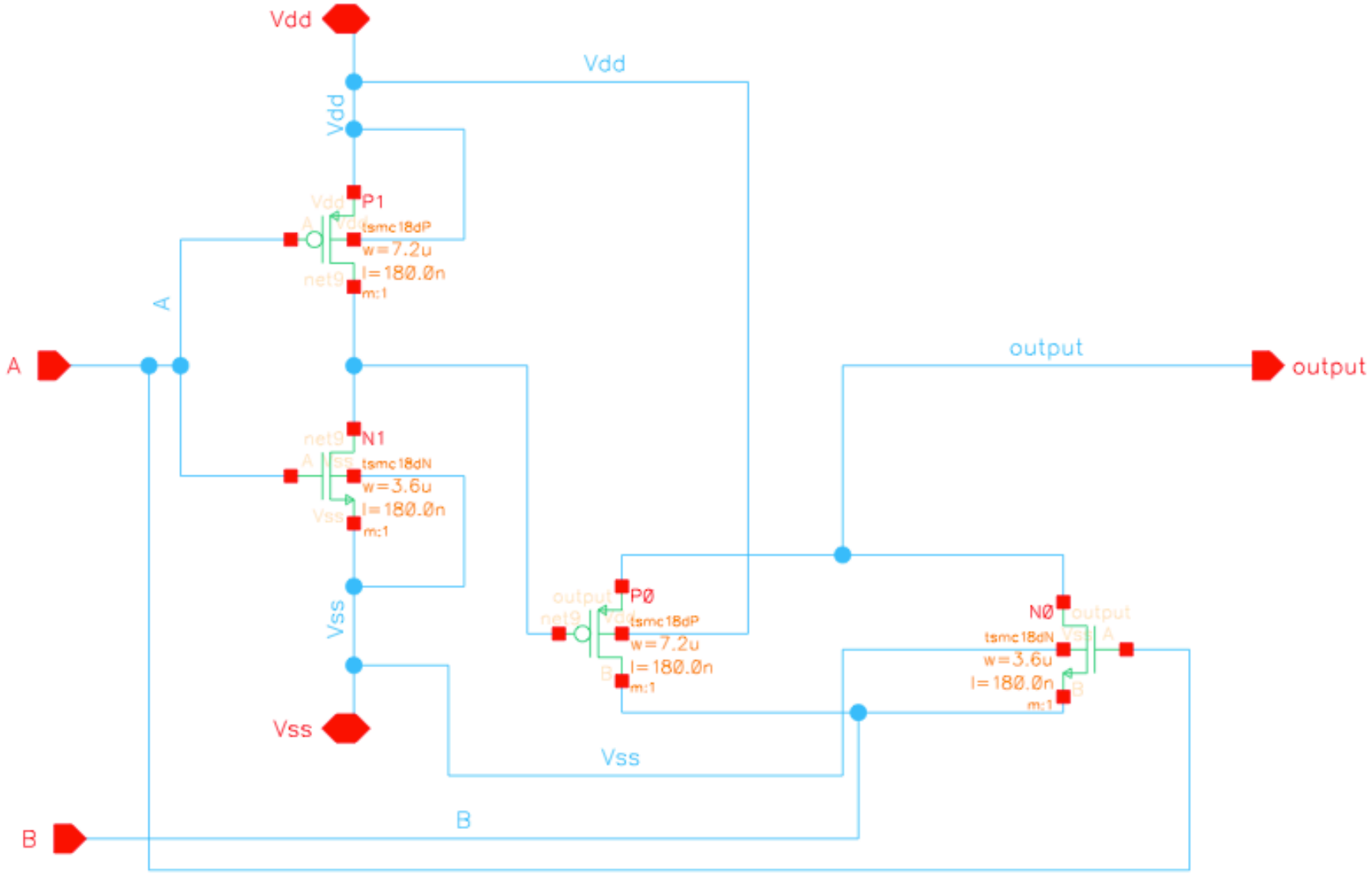
2-Input NOR Gate Testbench Waveform



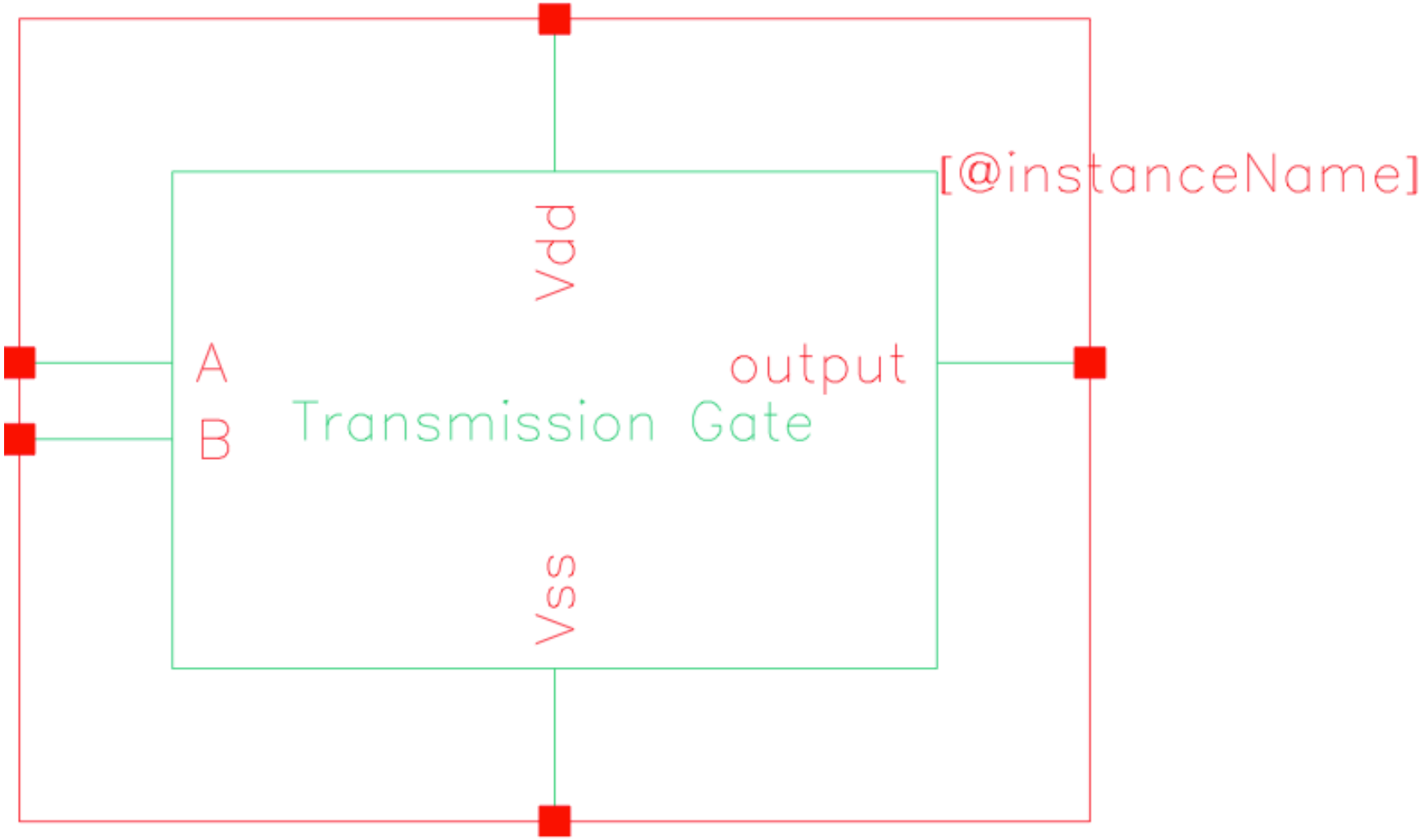
Transmission Gate

$(W/L)_n = 3.6/0.18$
$(W/L)_p = 7.2/0.18$

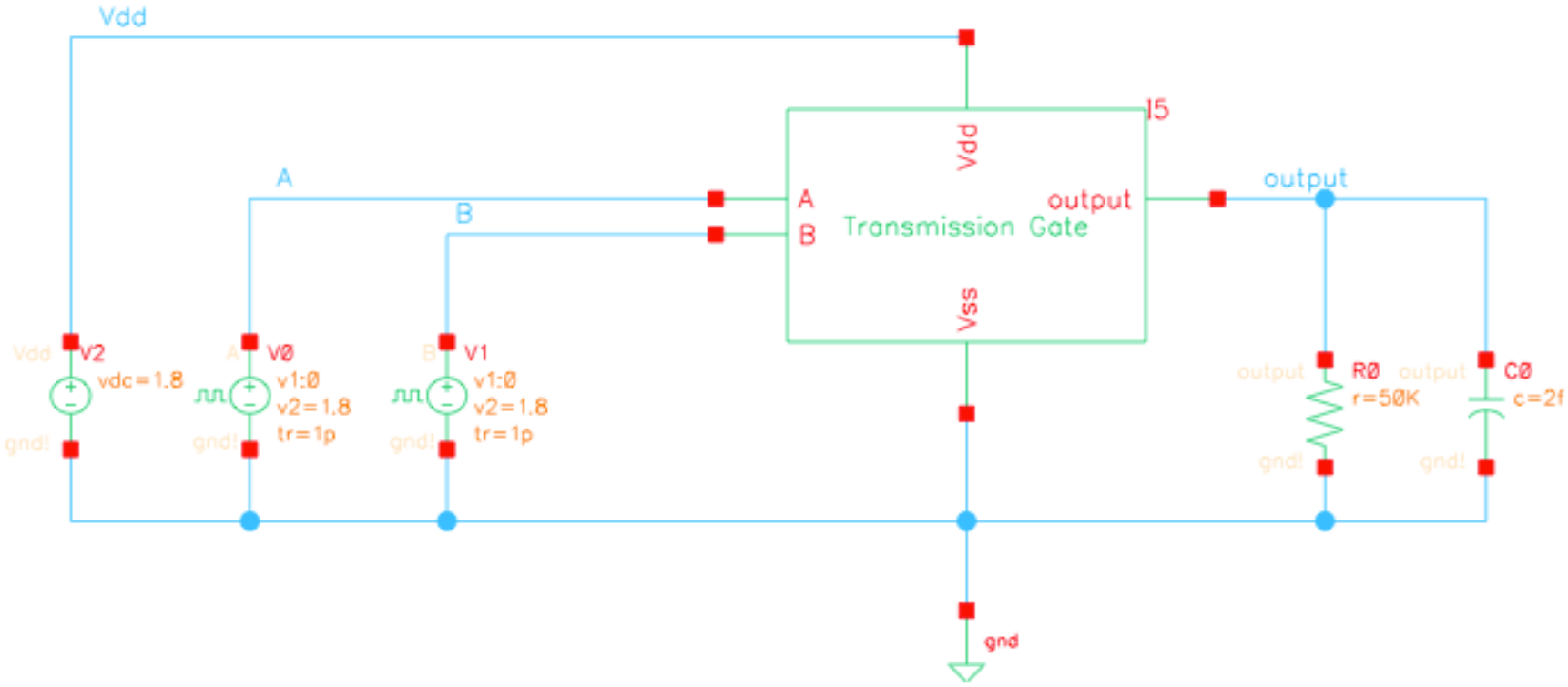
Transmission Gate Schematic



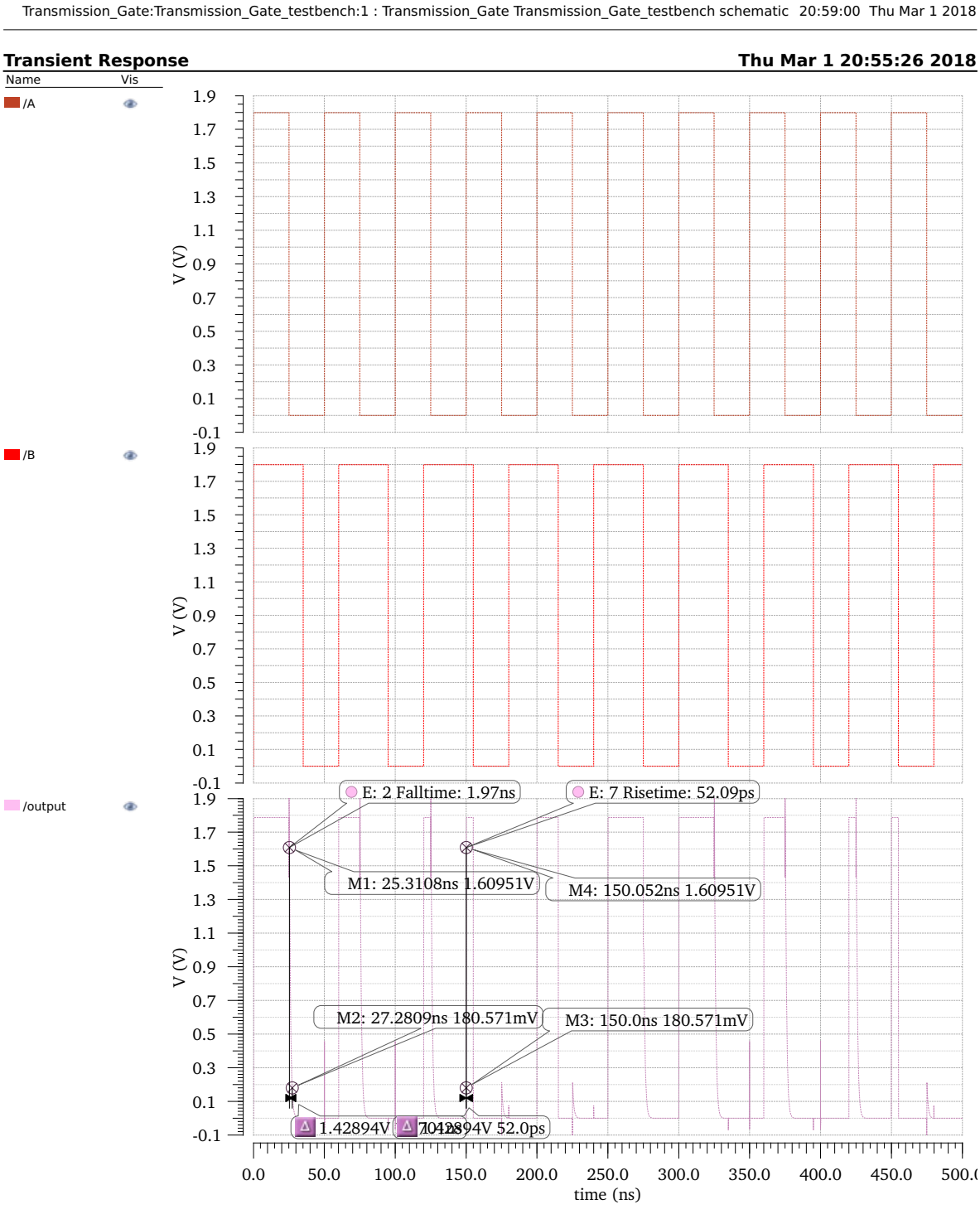
Transmission Gate Symbol



Transmission Gate Testbench



Transmission Gate Testbench Waveform



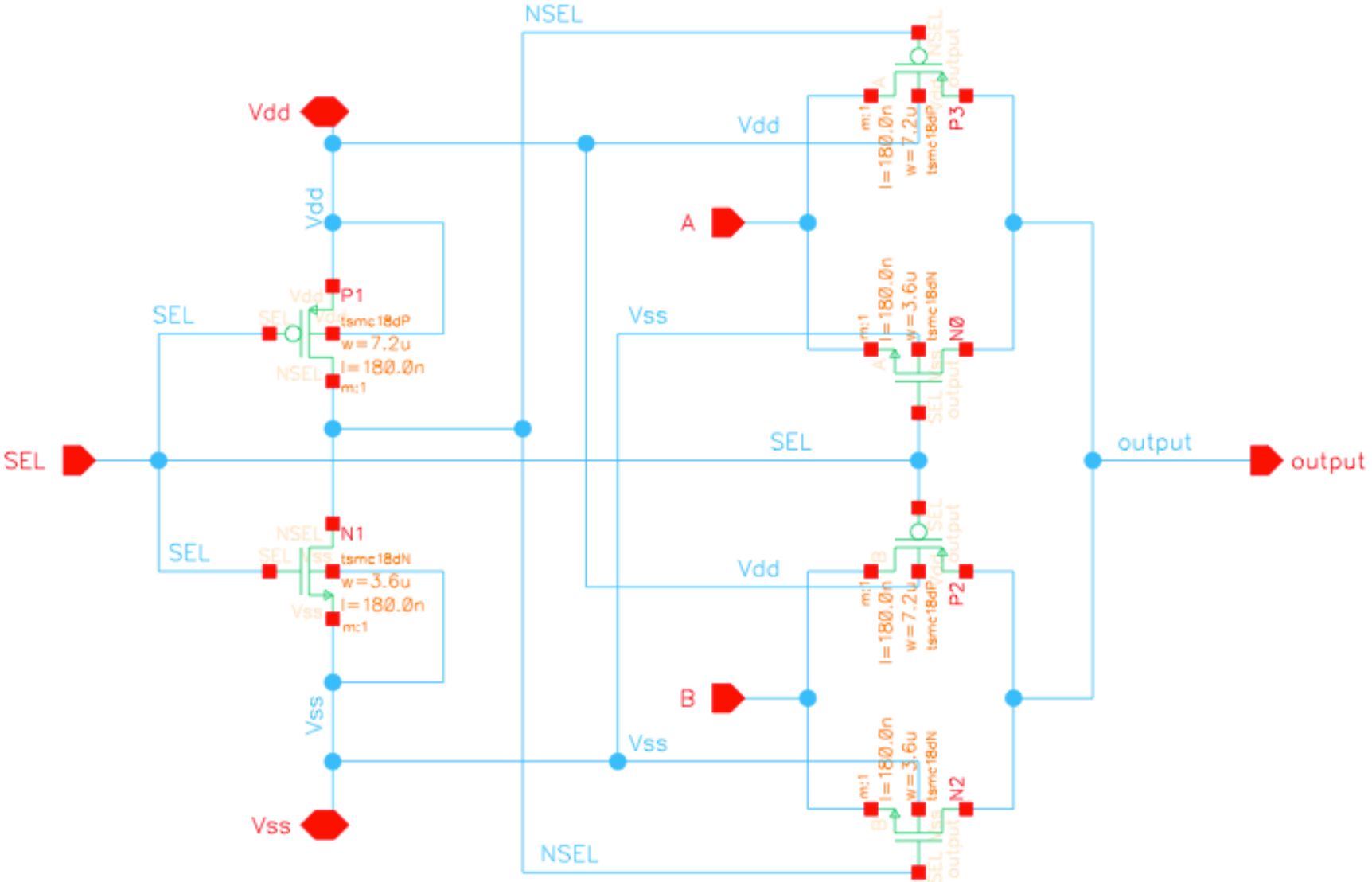
2:1 MUX

From Transmission Gate

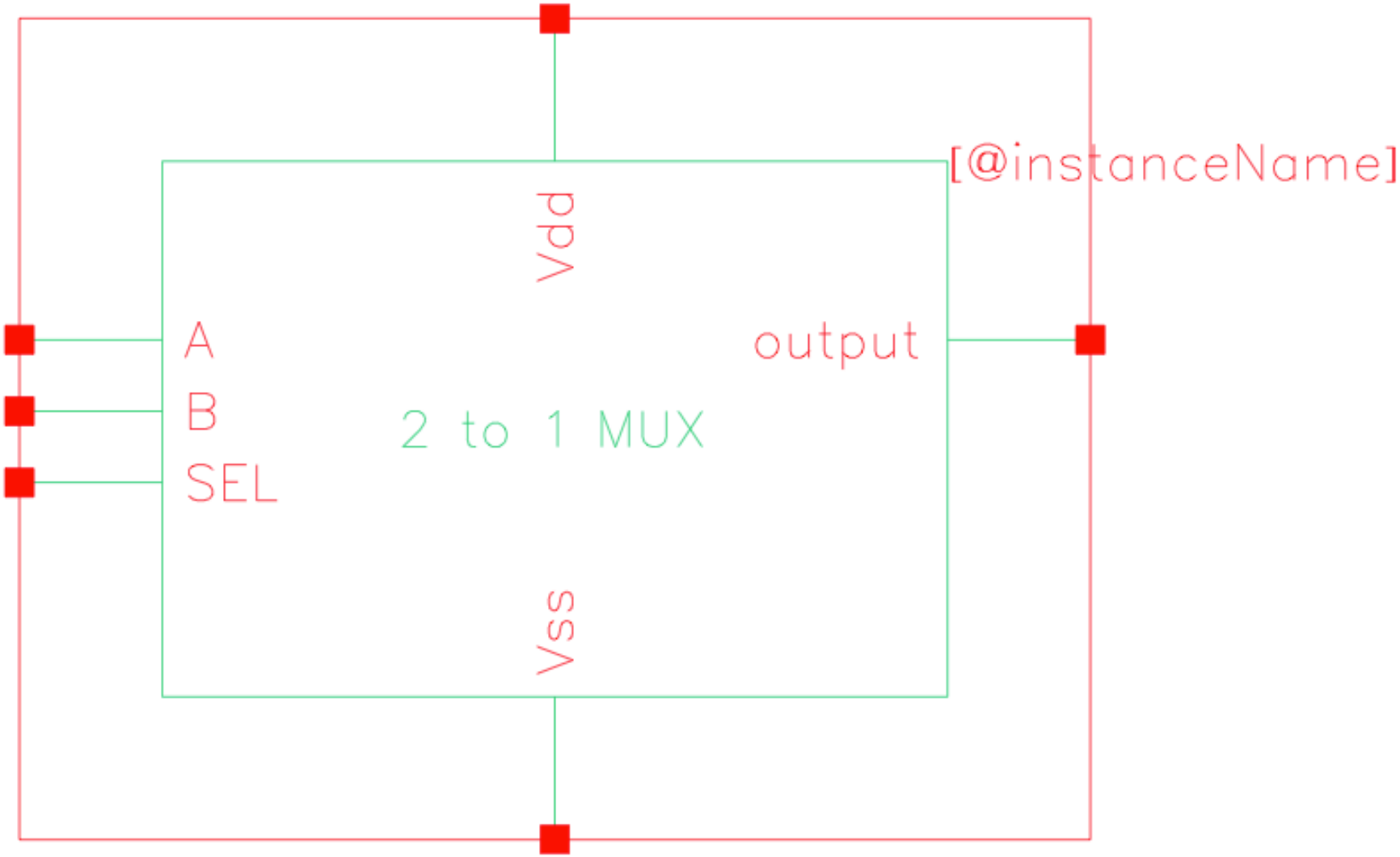
$(W/L)_n = 3.6/0.18$

$(W/L)_p = 7.2/0.18$

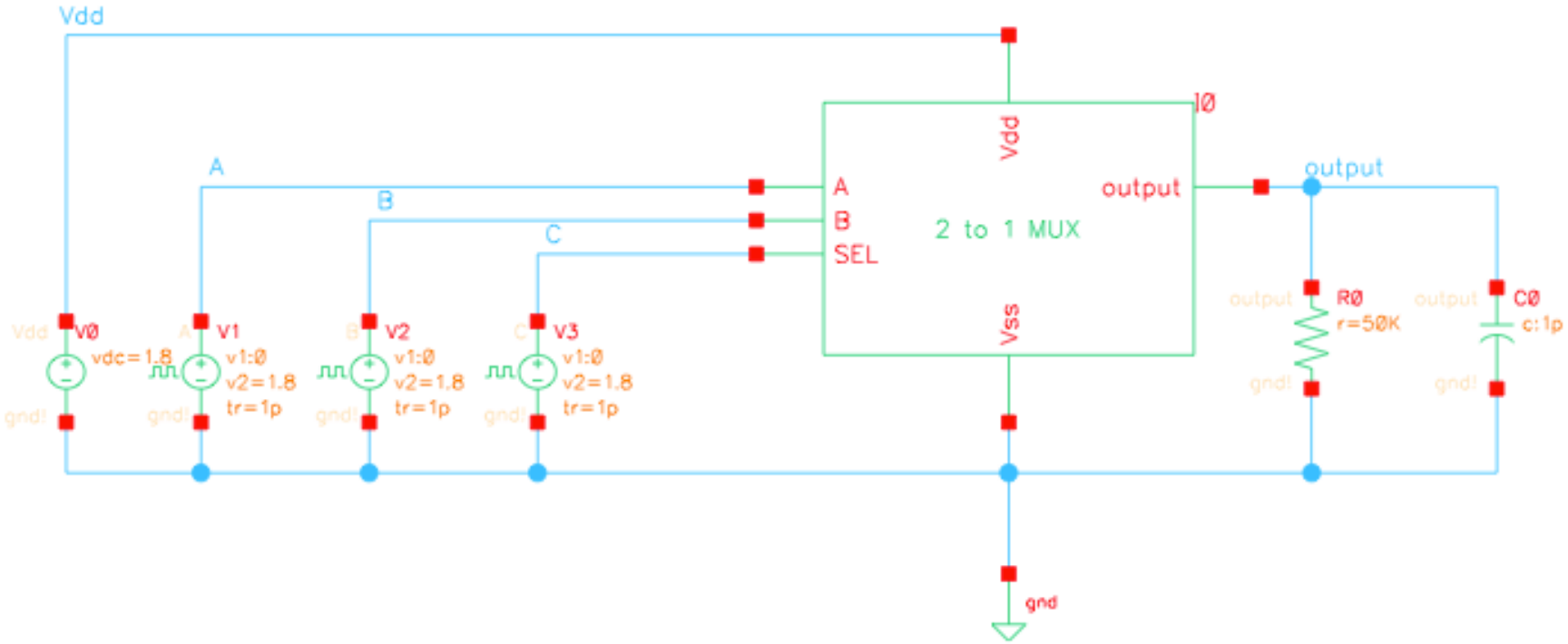
2:1 MUX Schematic



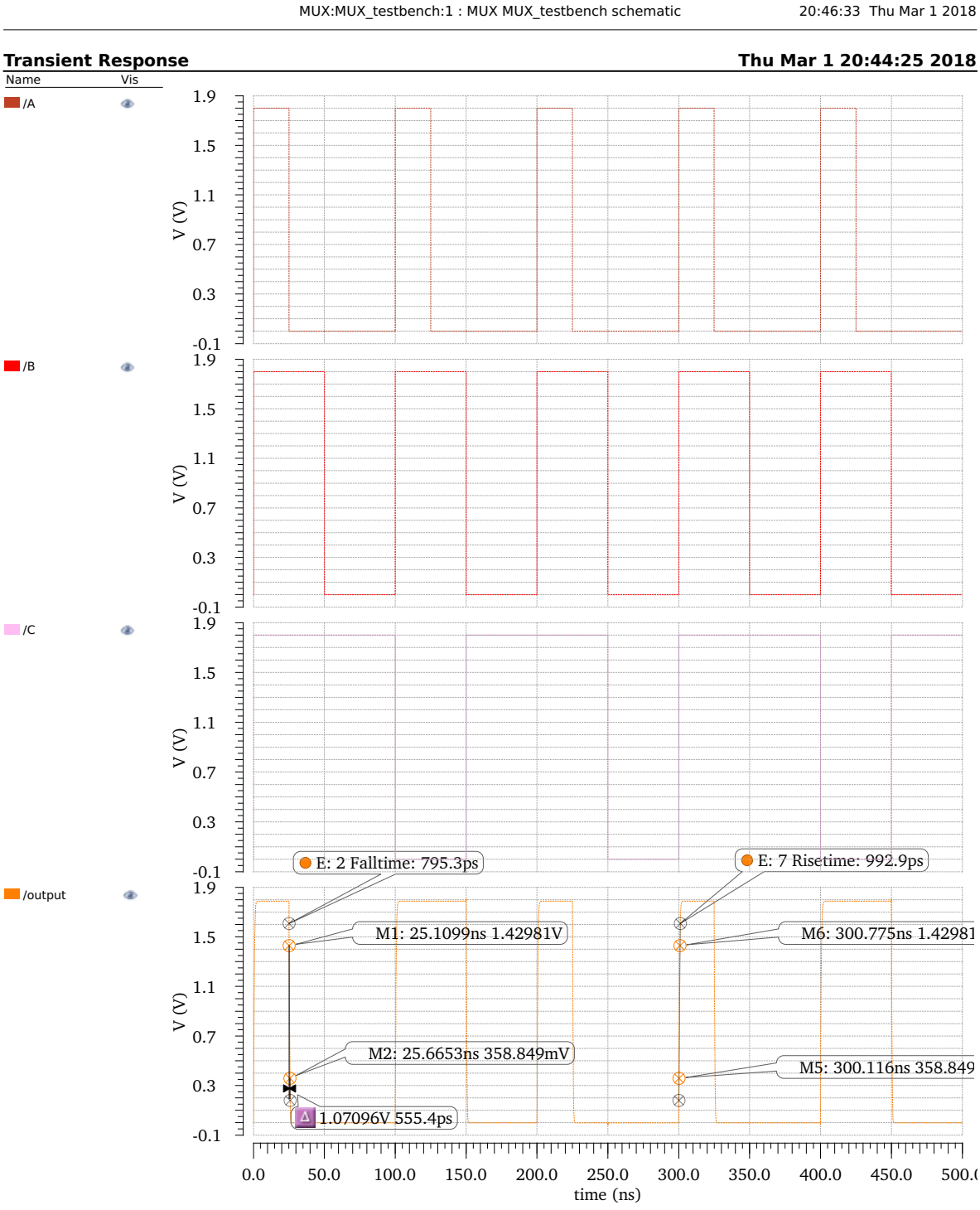
2:1 MUX Symbol



2:1 MUX Testbench



2:1 MUX Testbench Waveform



Conclusion

S. No.	Description	Rise Time (μs)	Fall Time (μs)	Delay Time (μs)
1	Inverter	0.000236	0.00018	-0.000056
2	3-Input NAND Gate	0.000057	0.000036	-0.000021
3	2-Input NOR Gate	0.002172	0.000838	-0.001334
4	Transmission Gate	0.000052	0.00197	0.001918
5	2:1 MUX	0.000993	0.000795	-0.000198