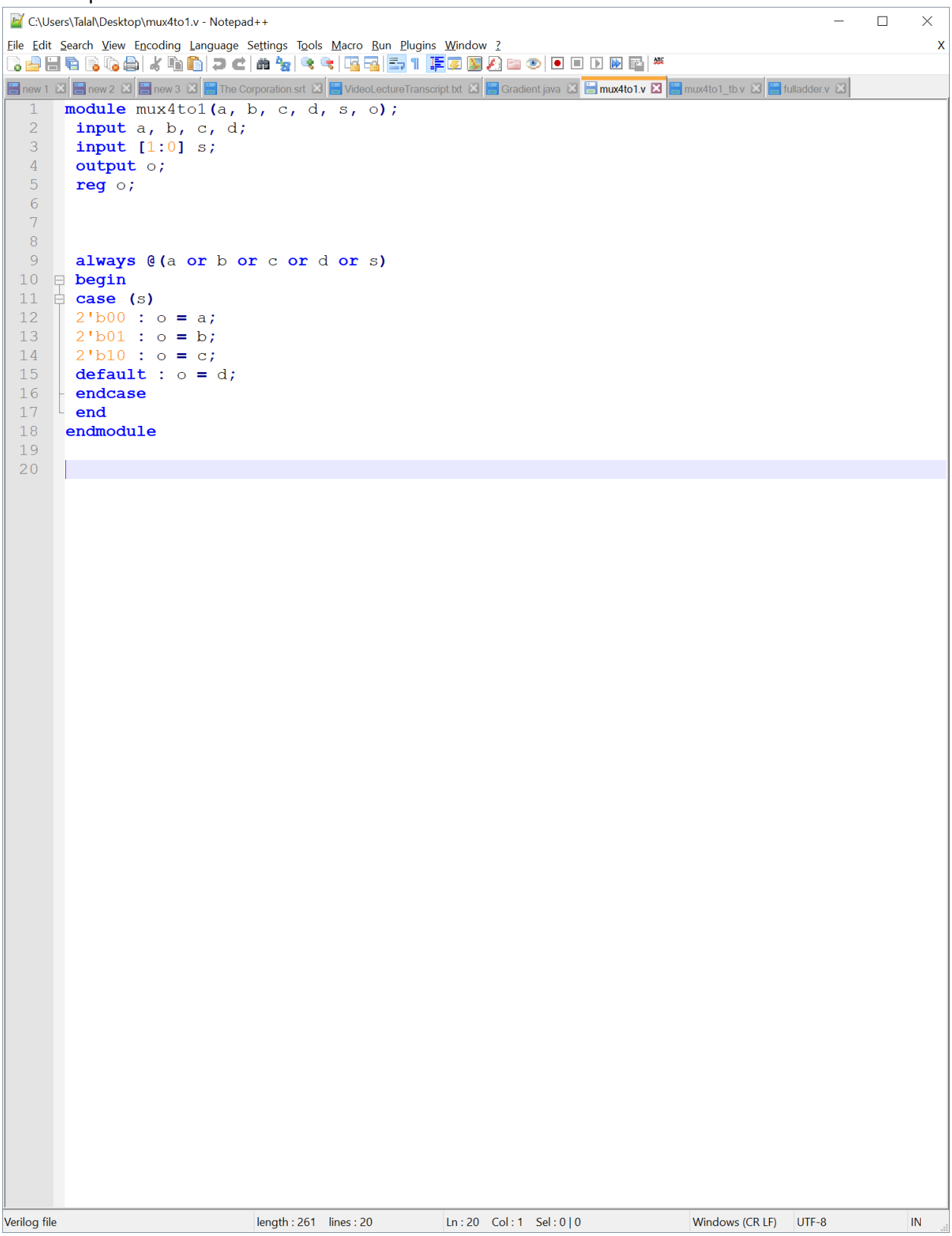
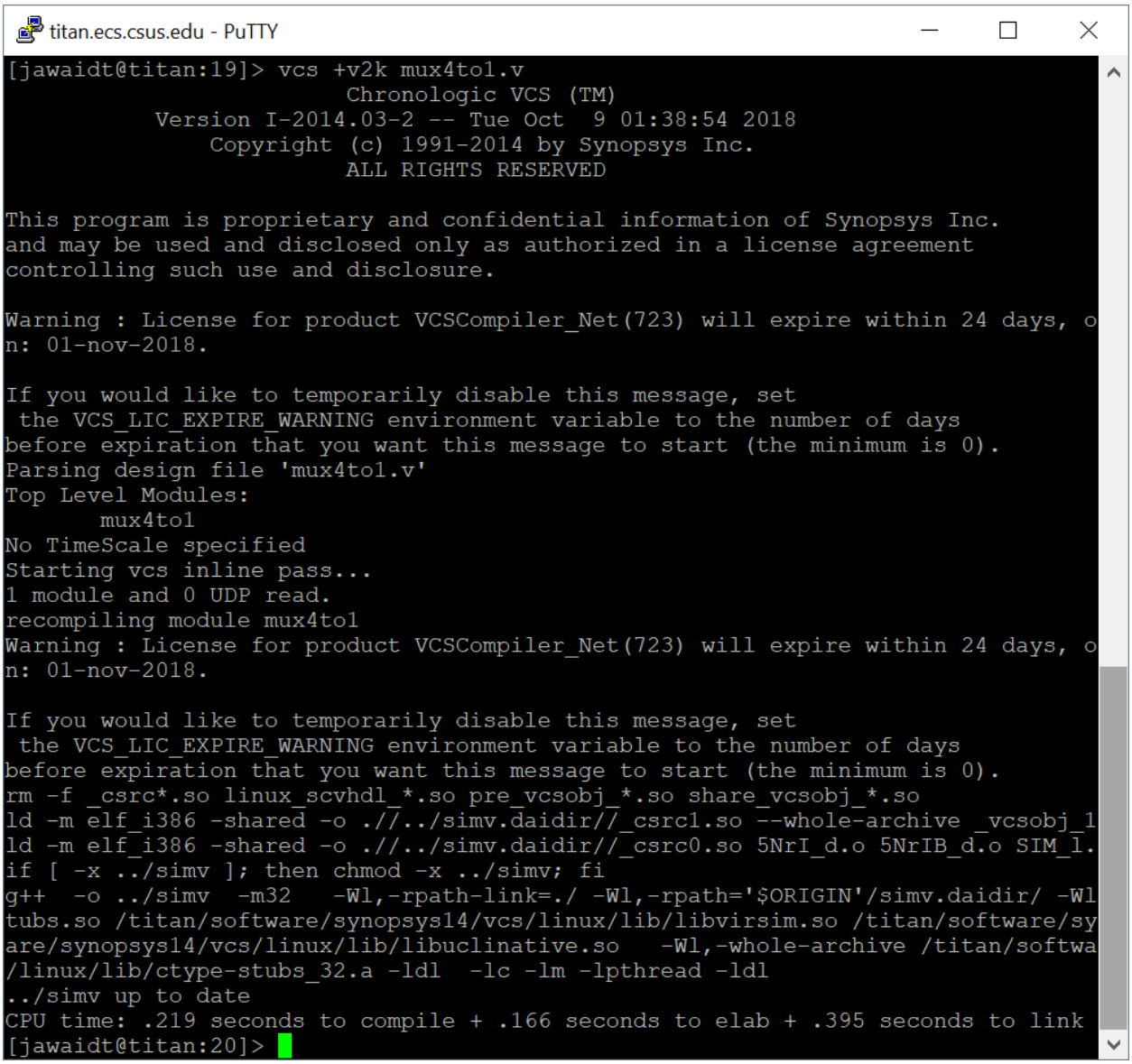
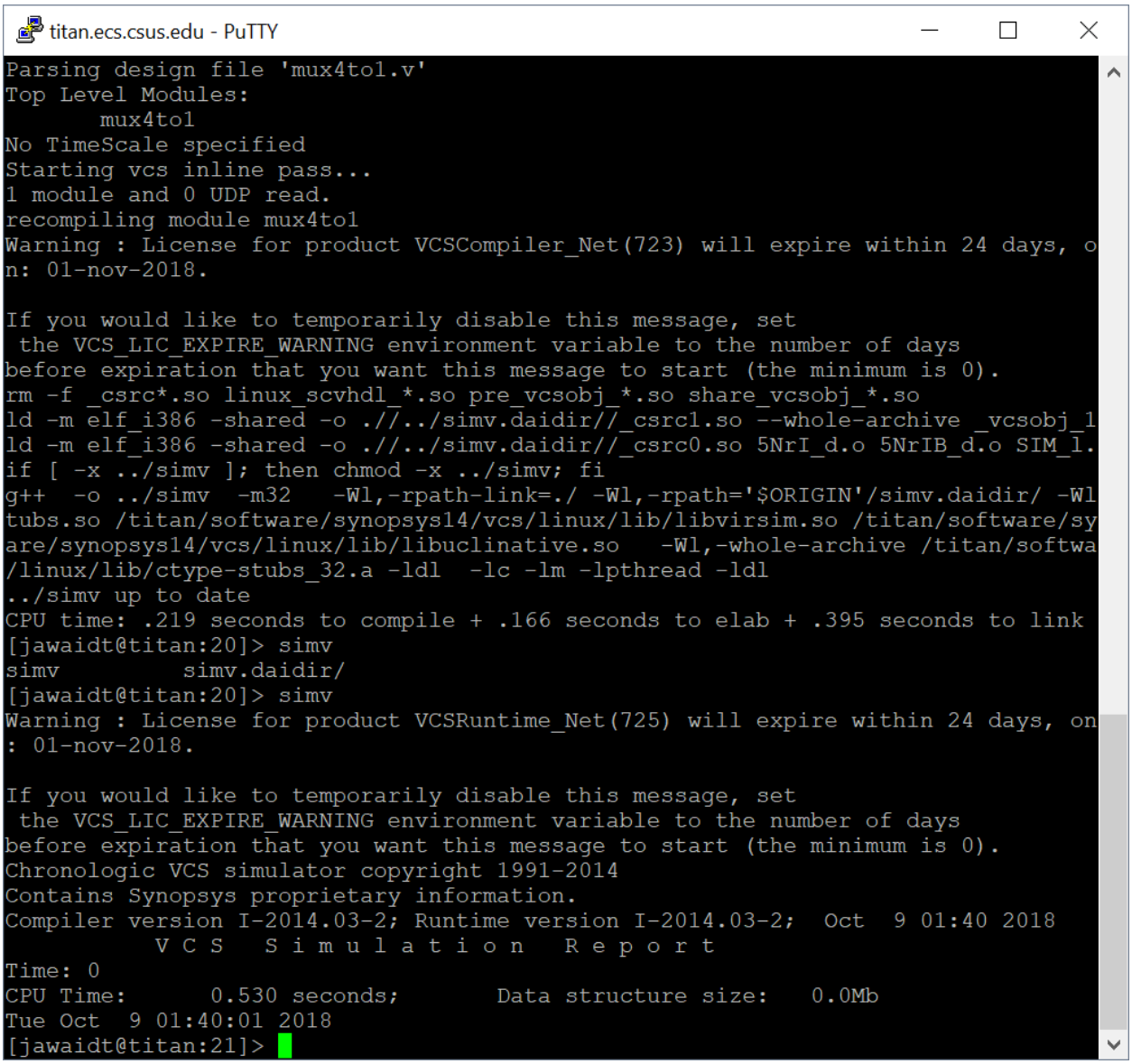
4x1 Multiplexer

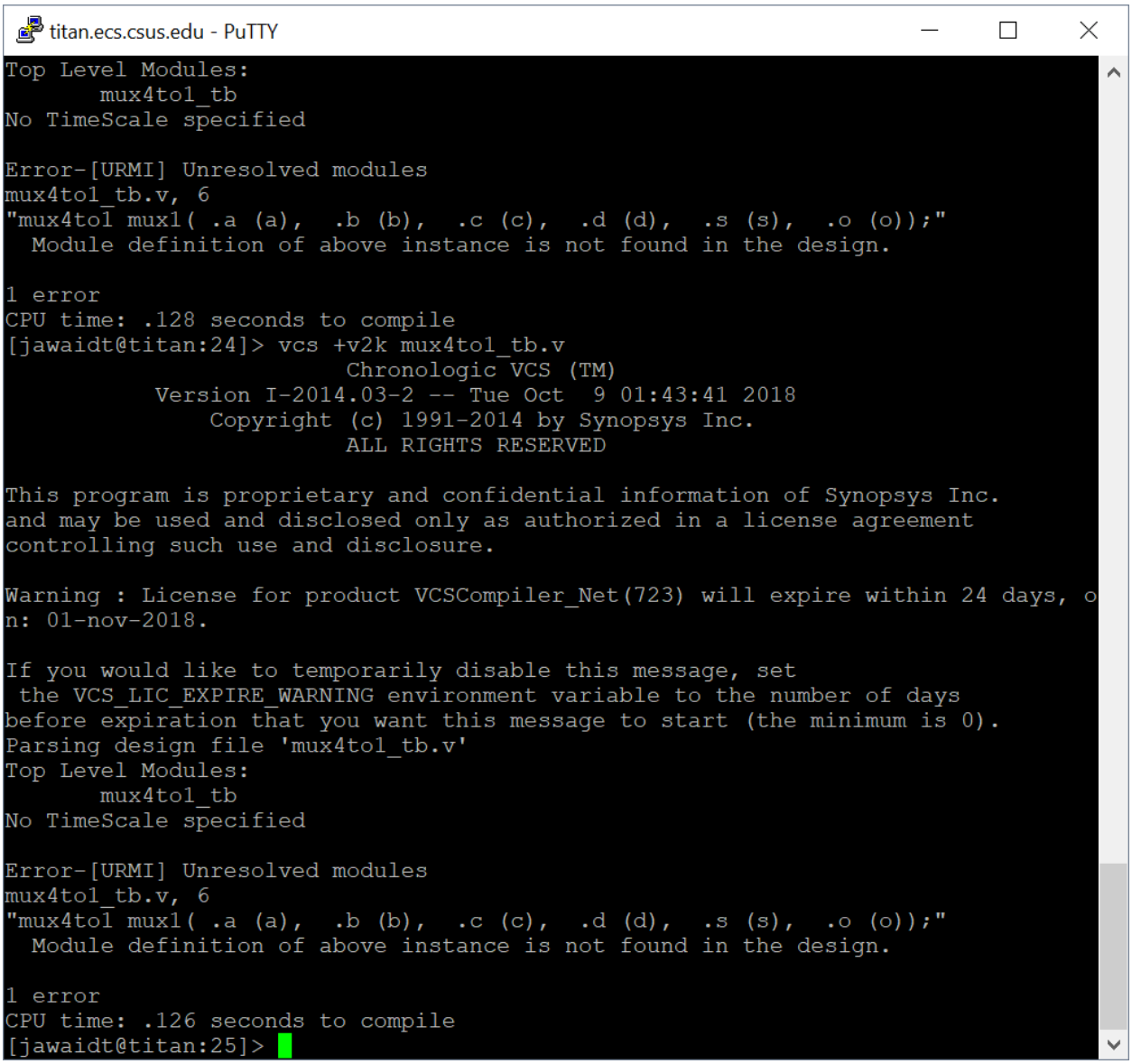


Attempting to compile


titan.ecs.csus.edu - PuTTY
[jawaidt@titan:19]> vcs +v2k mux4to1.v
Chronologic VCS (TM)
Version I-2014.03-2 -- Tue Oct 9 01:38:54 2018
Copyright (c) 1991-2014 by Synopsys Inc.
ALL RIGHTS RESERVED
This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.
Warning : License for product VCSCompiler_Net(723) will expire within 24 days, o
n: 01-nov-2018.
If you would like to temporarily disable this message, set
the VCS_LIC_EXPIRE_WARNING environment variable to the number of days
before expiration that you want this message to start (the minimum is 0).
Parsing design file 'mux4to1.v'
Top Level Modules:
mux4to1
No TimeScale specified
Starting vcs inline pass...
1 module and 0 UDP read.
recompiling module mux4to1
Warning : License for product VCSCompiler_Net(723) will expire within 24 days, o
n: 01-nov-2018.
If you would like to temporarily disable this message, set
the VCS_LIC_EXPIRE_WARNING environment variable to the number of days
before expiration that you want this message to start (the minimum is 0).
rm -f _csrc*.so linux_scvhdl_*.so pre_vcsobj_*.so share_vcsobj_*.so
ld -m elf_i386 -shared -o .//../simv.daidir//_csrc1.so --whole-archive _vcsobj_1
ld -m elf_i386 -shared -o .//../simv.daidir//_csrc0.so 5NrI_d.o 5NrIB_d.o SIM_l.
if [-x ../simv]; then chmod -x ../simv; fi
g++ -o ../simv -m32 -Wl,-rpath-link=./ -Wl,-rpath='$ORIGIN'/simv.daidir/ -Wl
tubs.so /titan/software/synopsys14/vcs/linux/lib/libvirsim.so /titan/software/sy
are/synopsys14/vcs/linux/lib/libuclinative.so -Wl,-whole-archive /titan/softwa
/linux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .219 seconds to compile + .166 seconds to elab + .395 seconds to link
[jawaidt@titan:20]>

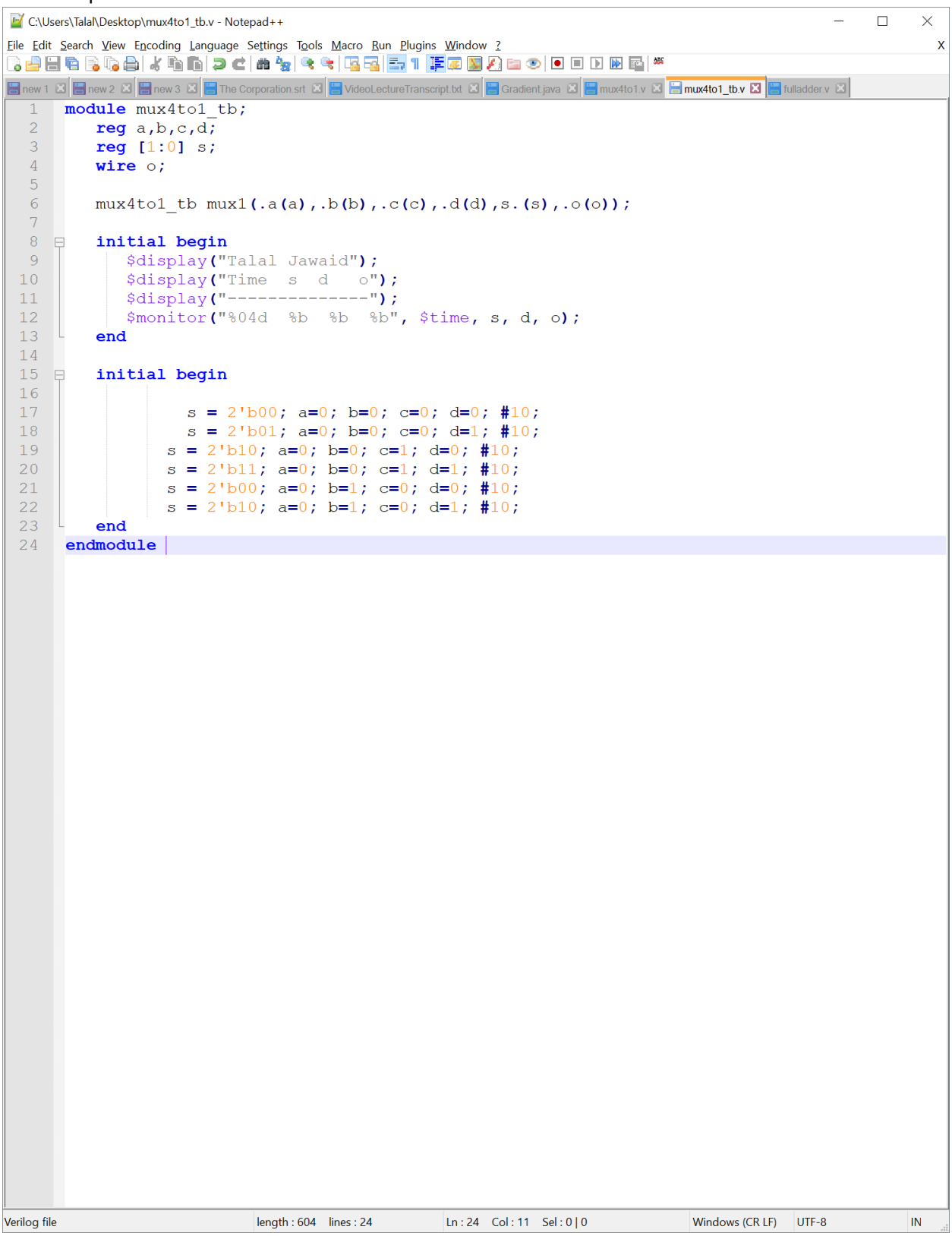


Attempting to run via simv

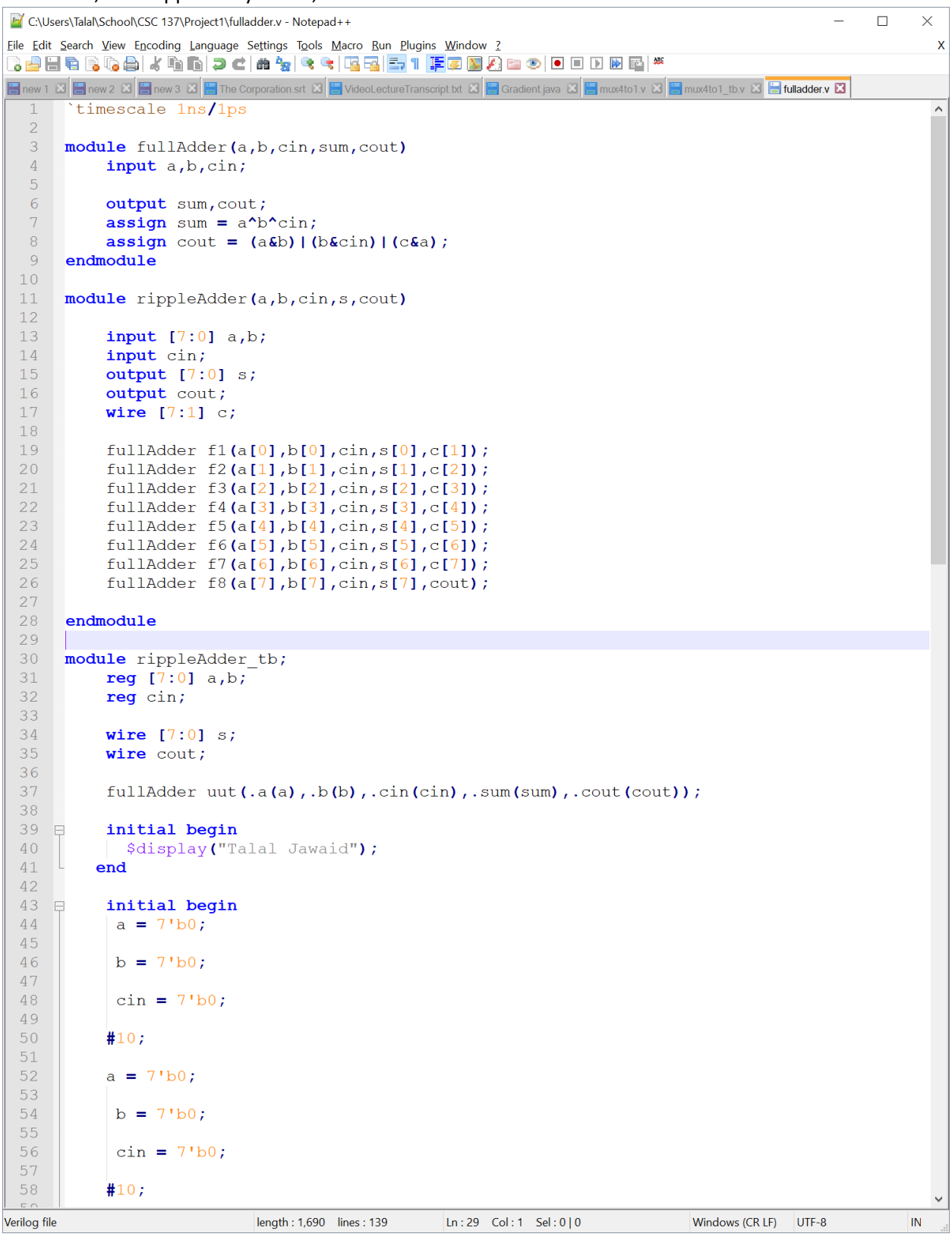


Attempting to compile mux4to1_tb

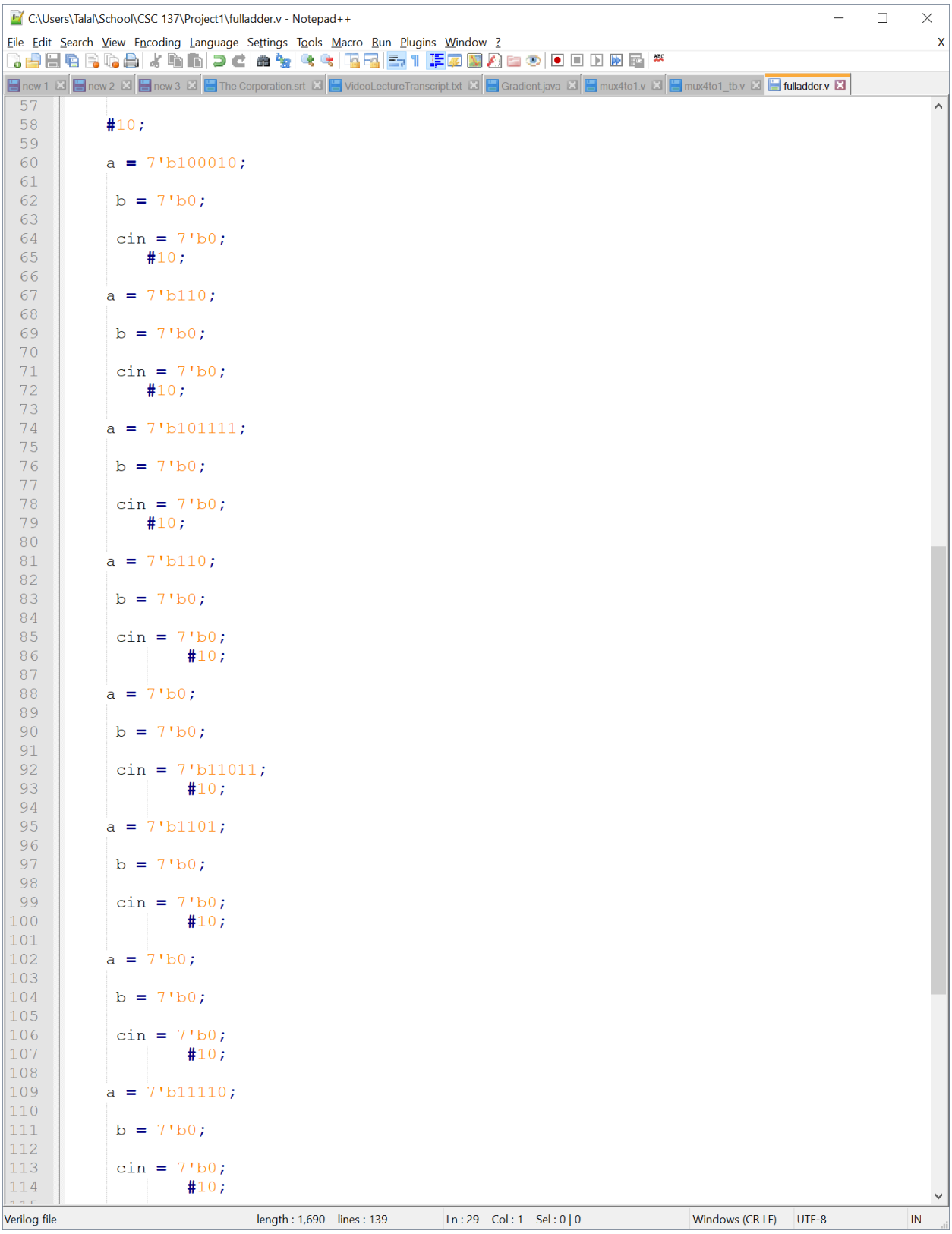
4x1 Multiplexer test bench

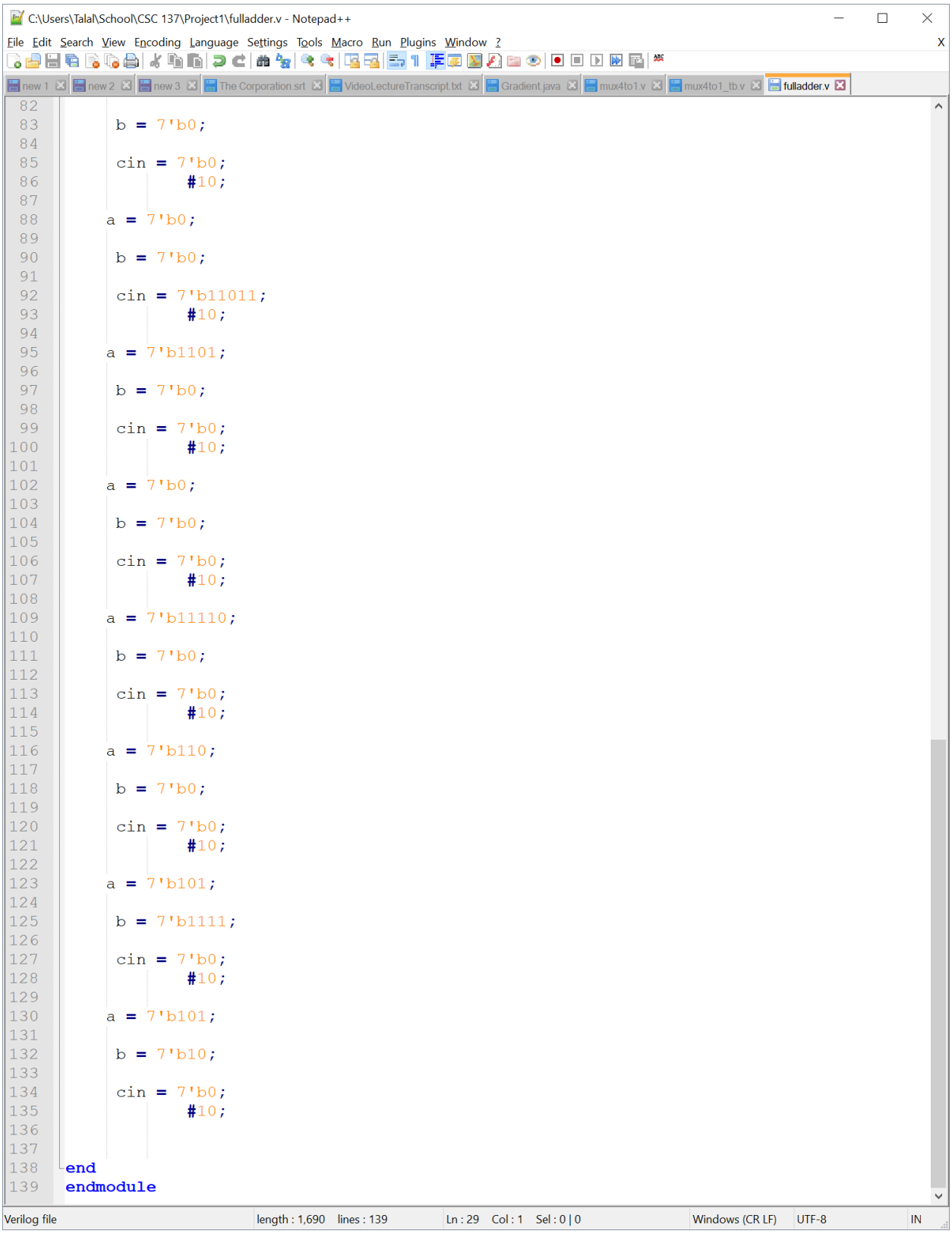


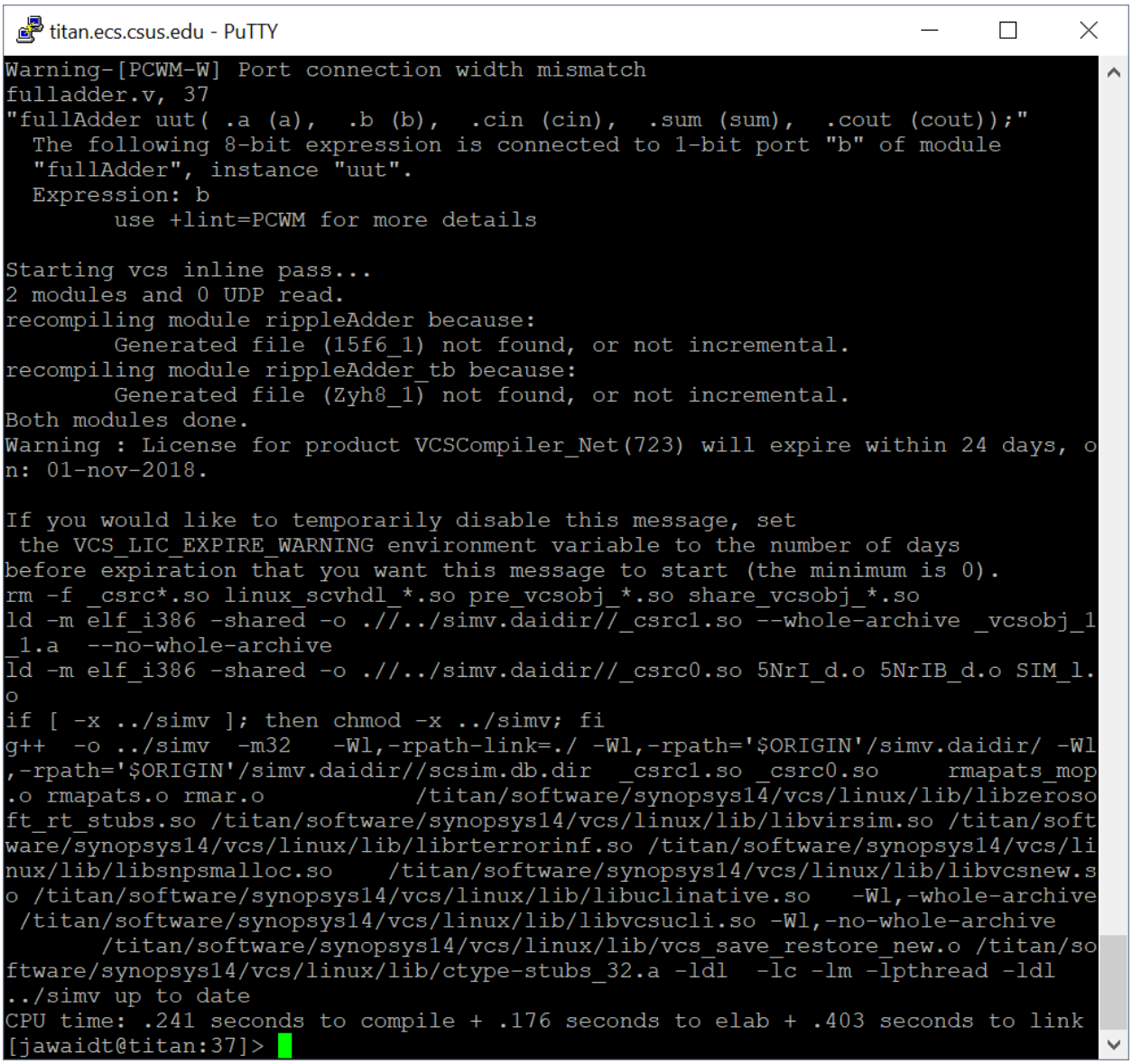
Full Adder, 8 bit ripple carry adder, test bench



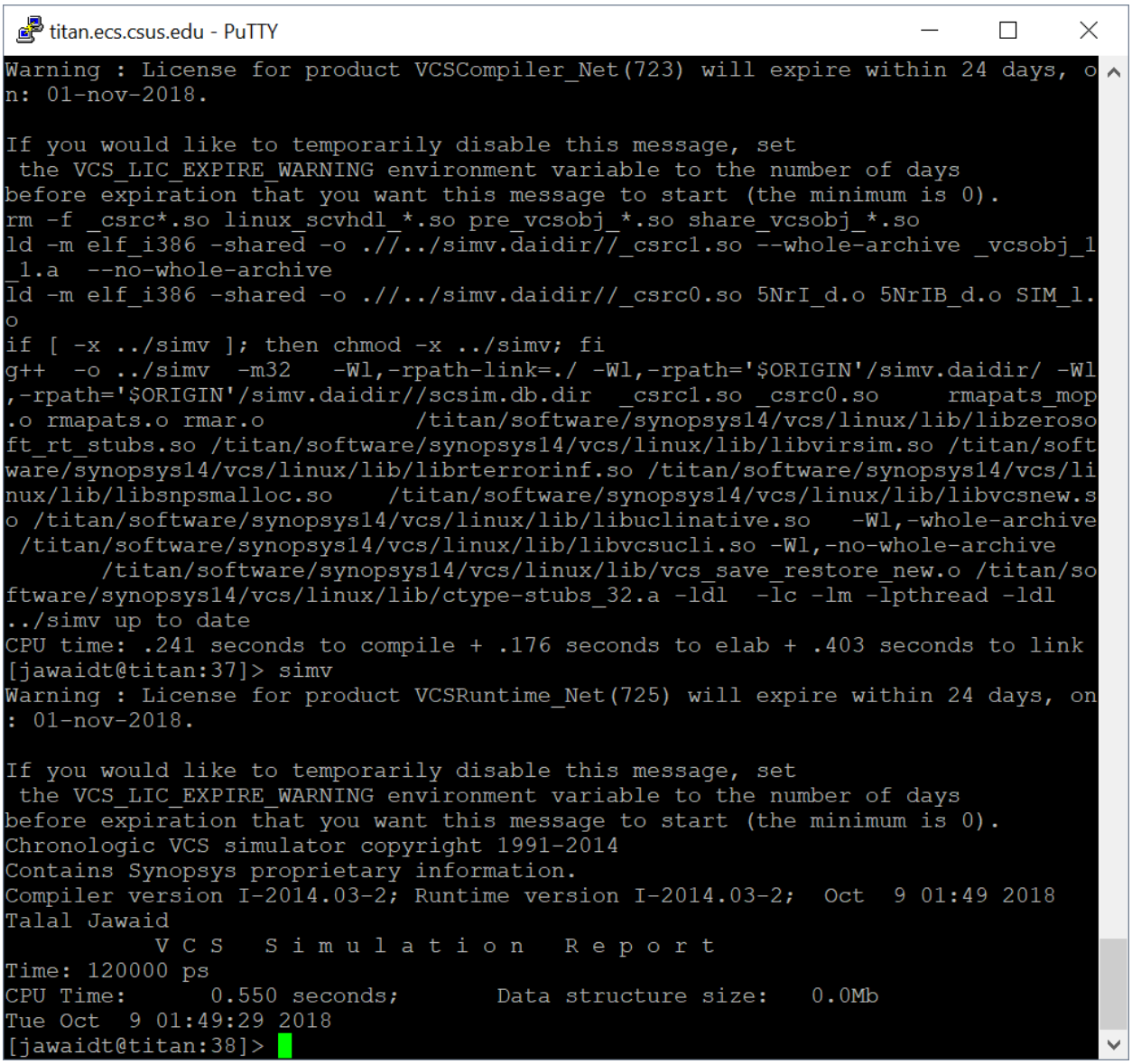

```
1  `timescale 1ns/1ps
2
3  module fullAdder(a,b,cin,sum,cout)
4      input a,b,cin;
5
6      output sum,cout;
7      assign sum = a^b^cin;
8      assign cout = (a&b)|(b&cin)|(c&a);
9  endmodule
10
11 module rippleAdder(a,b,cin,s,cout)
12
13     input [7:0] a,b;
14     input cin;
15     output [7:0] s;
16     output cout;
17     wire [7:1] c;
18
19     fullAdder f1(a[0],b[0],cin,s[0],c[1]);
20     fullAdder f2(a[1],b[1],cin,s[1],c[2]);
21     fullAdder f3(a[2],b[2],cin,s[2],c[3]);
22     fullAdder f4(a[3],b[3],cin,s[3],c[4]);
23     fullAdder f5(a[4],b[4],cin,s[4],c[5]);
24     fullAdder f6(a[5],b[5],cin,s[5],c[6]);
25     fullAdder f7(a[6],b[6],cin,s[6],c[7]);
26     fullAdder f8(a[7],b[7],cin,s[7],cout);
27
28 endmodule
29
30 module rippleAdder_tb;
31     reg [7:0] a,b;
32     reg cin;
33
34     wire [7:0] s;
35     wire cout;
36
37     fullAdder uut(.a(a),.b(b),.cin(cin),.sum(sum),.cout(cout));
38
39     initial begin
40       $display("Talal Jawaid");
41    end
42
43     initial begin
44      a = 7'b0;
45
46      b = 7'b0;
47
48      cin = 7'b0;
49
50     #10;
51
52     a = 7'b0;
53
54      b = 7'b0;
55
56      cin = 7'b0;
57
58     #10;
```


C:\Users\Talal\School\CSC 137\Project1\fulladder.v - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
new 1
new 2
new 3
The Corporation.srt
VideoLectureTranscript.txt
Gradient.java
mux4to1.v
mux4to1_tb.v
fulladder.v
#10;
a = 7'b100010;
b = 7'b0;
cin = 7'b0;
#10;
a = 7'b110;
b = 7'b0;
cin = 7'b0;
#10;
a = 7'b101111;
b = 7'b0;
cin = 7'b0;
#10;
a = 7'b110;
b = 7'b0;
cin = 7'b0;
#10;
a = 7'b0;
b = 7'b0;
cin = 7'b11011;
#10;
a = 7'b1101;
b = 7'b0;
cin = 7'b0;
#10;
a = 7'b0;
b = 7'b0;
cin = 7'b0;
#10;
a = 7'b11110;
b = 7'b0;
cin = 7'b0;
#10;
Verilog file
length : 1,690 lines : 139
Ln : 29 Col : 1 Sel : 0 | 0
Windows (CR LF)
UTF-8
IN


C:\Users\Talal\School\CSC 137\Project1\fulladder.v - Notepad++
File Edit Search View Encoding Language Settings Tools Macro Run Plugins Window ?
new 1
new 2
new 3
The Corporation.srt
VideoLectureTranscript.txt
Gradient.java
mux4to1.v
mux4to1_tb.v
fulladder.v
b = 7'b0;
cin = 7'b0;
#10;
a = 7'b0;
b = 7'b0;
cin = 7'b11011;
#10;
a = 7'b1101;
b = 7'b0;
cin = 7'b0;
#10;
a = 7'b0;
b = 7'b0;
cin = 7'b0;
#10;
a = 7'b11110;
b = 7'b0;
cin = 7'b0;
#10;
a = 7'b110;
b = 7'b0;
cin = 7'b0;
#10;
a = 7'b101;
b = 7'b1111;
cin = 7'b0;
#10;
a = 7'b101;
b = 7'b10;
cin = 7'b0;
#10;
end
endmodule
Verilog file
length : 1,690 lines : 139
Ln : 29 Col : 1 Sel : 0 | 0
Windows (CR LF)
UTF-8
IN



Compiling fulladder.v



Attempting to run via simv

All files compiled, synthesized, and ran through Quartus and Vivado. Not sure why VCS and SIMV weren't working. Test benches did not correctly work in Quartus or Vivado.