Course Name: CPE 142
Cours

Instructor
Assign
Due Date
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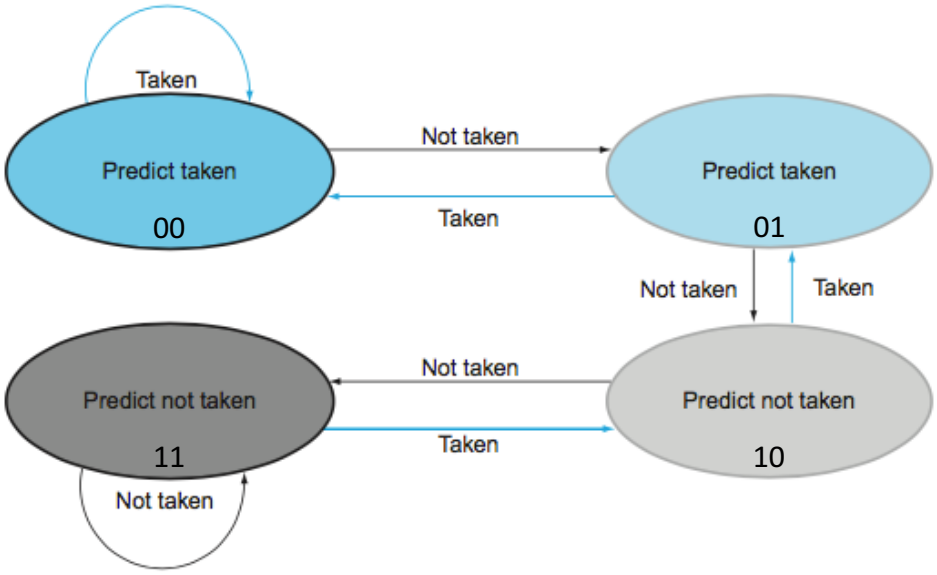
Na

4.16.2: What is the accuracy of the two-bit predictor for the first 4 branches in this pattern, assuming that the predictor starts off in the bottom left state from Figure 4.63 (predict not taken)?



Actual	Current State	Prediction	Next State
T	NT(11)	NT	NT(10)
NT	NT(10)	NT	NT(11)
T	NT(11)	NT	NT(10)
T	NT(10)	NT	T(01)

$$Accuracy\ of\ Predictor = \frac{Number\ of\ Hits}{Total\ Branches}$$

One out of four hit therefore, $\frac{1}{4} = 25\%\ hit\ rate$

5.6: In this exercise, we will look at the different ways capacity affects overall performance. In general, cache access time is proportional to capacity. Assume that main memory accesses take 70 ns and that memory access are 36% of all instructions. The following table shows data for L1 caches attached to each of two processors, P1 and P2.

	L1 Size	L1 Miss Rate	L1 Hit Time
P1	2 KiB	8.0%	0.66 ns
P2	4 KiB	6.0%	0.90 ns

5.6.1: Assuming that the L1 hit time determines the cycle times for P1 and P2, what are their respective clock rates?

$$Clock\ Rate = \frac{1}{L1\ Hit\ Time}$$

P1: $\frac{1}{0.66\ ns} = 1.5152\ GHz$

P2: $\frac{1}{0.90\ ns} = 1.1111\ GHz$

5.6.2: What is the Average Memory Access Time for P1 and P2?

$$Average\ Memory\ Access\ Time = (Hit\ Rate \times Hit\ Time) + (Miss\ Rate \times Miss\ Time)$$

P1: $(92\% \times 0.66\ ns) + (8\% \times 70\ ns) = (0.6072 + 5.6) = 6.2072\ ns$

P2: $(94\% \times 0.90\ ns) + (6\% \times 70\ ns) = (0.846 + 4.2) = 5.046\ ns$

5.6.3: Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 and P2? Which processor is faster?

$$Miss\ Cycles = (IC)(Memory\ Access\ Frequency)(\frac{Main\ Memory\ Access}{L1\ Hit\ Time})$$

$$Total\ Cycles = (1.0)(IC) + Miss\ Cycles$$

$$CPI = \frac{Total\ Cycles}{IC}$$

$$CPU\ Time\ with\ Stalls = (IC)(CPI)(L1\ Hit\ Time)$$

P1:

$$Miss\ Cycles = IC \times (0.36) \times (0.08) \times \left(\frac{70}{0.66}\right) = 3.0545 \times IC$$

$$Total\ Cycles = (1.0)(IC) + (3.0545)(IC) = (4.0545)(IC)$$

$$CPI = \frac{(4.0545)(IC)}{IC} = 4.0545$$

$$CPU\ Time\ with\ Stalls = IC \times 4.0545 \times 0.66ns = (2.676 \times IC)ns$$

P2:

$$Miss\ Cycles = IC \times (0.36) \times (0.06) \times \left(\frac{70}{0.90}\right) = 1.68 \times IC$$

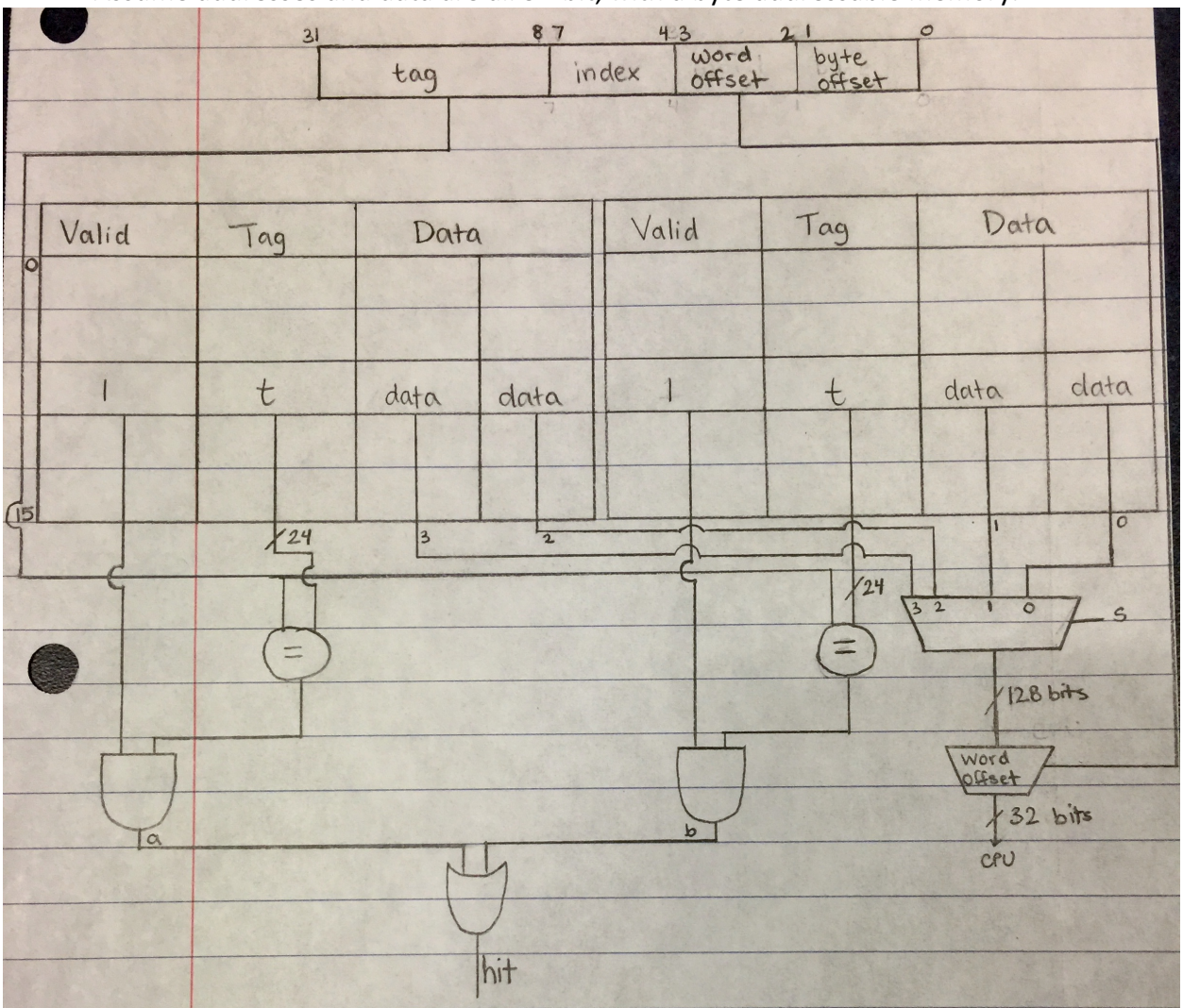
$$Total\ Cycles = (1.0)(IC) + (1.68)(IC) = (2.68)(IC)$$

$$CPI = \frac{(2.68)(IC)}{IC} = 2.68$$

$$CPU\ Time\ with\ Stalls = IC \times 2.68 \times 0.90ns = (2.412 \times IC)ns$$

From the above calculations, we can conclude that P2 is faster than P1.

1 Provide the block diagram for a 2-way set associative cache with 32 four-word blocks. Assume addresses and data are all 32-bit, with a byte addressable memory.



$32 \times 32 \times 4 = 4096 \div 8 = 512$ bytes

$$\frac{512 \text{ bytes}}{\text{cache}} \times \frac{1 \text{ word}}{4 \text{ bytes}} \times \frac{1 \text{ block}}{4 \text{ words}} \times \frac{1 \text{ set}}{2 \text{ block}} = 16 \frac{\text{sets}}{\text{cache}}$$

width of index: $\log_2 16 = 4$ bits

width of word offset: $\log_2 4 = 2$ bits

width of byte offset: $\log_2 4 = 2$ bits

a	b	miss/hit	s
0	0	miss	x
0	1	hit in b	0 or 1
1	0	hit in a	2 or 3

2 Consider the following address trace: 2, 3, 11, 16, 21, 13, 64, 48, 19, 11, 3, 32, 22, 4, 27, 6, and 11. Assume the cache is initially empty. Label each reference in the list with hit or miss and show the final content of the cache.

Block 0 = {0, 1, 2, 3}
Block 1 = {4, 5, 6, 7}
Block 2 = {8, 9, 10, 11}
Block 3 = {12, 13, 14, 15}
Block 4 = {16, 17, 18, 19}
Block 5 = {20, 21, 22, 23}
Block 6 = {24, 25, 26, 27}
Block 7 = {28, 29, 30, 31}
Block 8 = {32, 33, 34, 35}
Block 9 = {36, 37, 38, 39}
Block 10 = {40, 41, 42, 43}
Block 11 = {44, 45, 46, 47}
Block 12 = {48, 49, 50, 51}
Block 13 = {52, 53, 54, 55}
Block 14 = {56, 57, 58, 59}
Block 15 = {60, 61, 62, 63}

Index	2	3	11	16	21	13	64	48	19	11	3	32	22	4	27	6	11
Data	0	0	2	4	5	3	16	12	4	2	0	8	5	1	6	1	2
Set	0	0	2	4	5	3	0	12	4	2	0	8	5	1	6	1	2
Hit/Miss	M	H	M	M	M	M	M	M	H	H	M	M	H	M	M	H	H