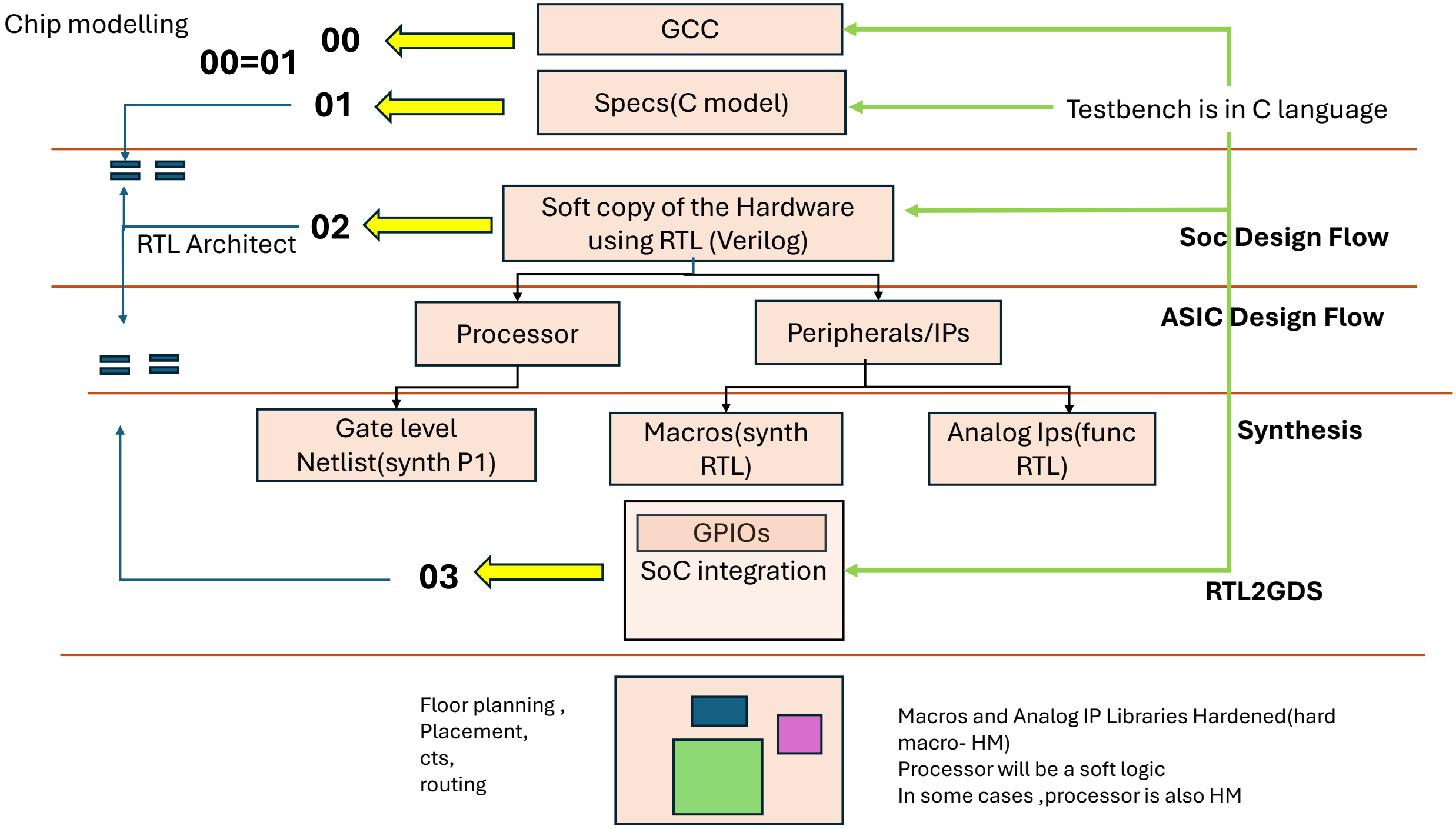
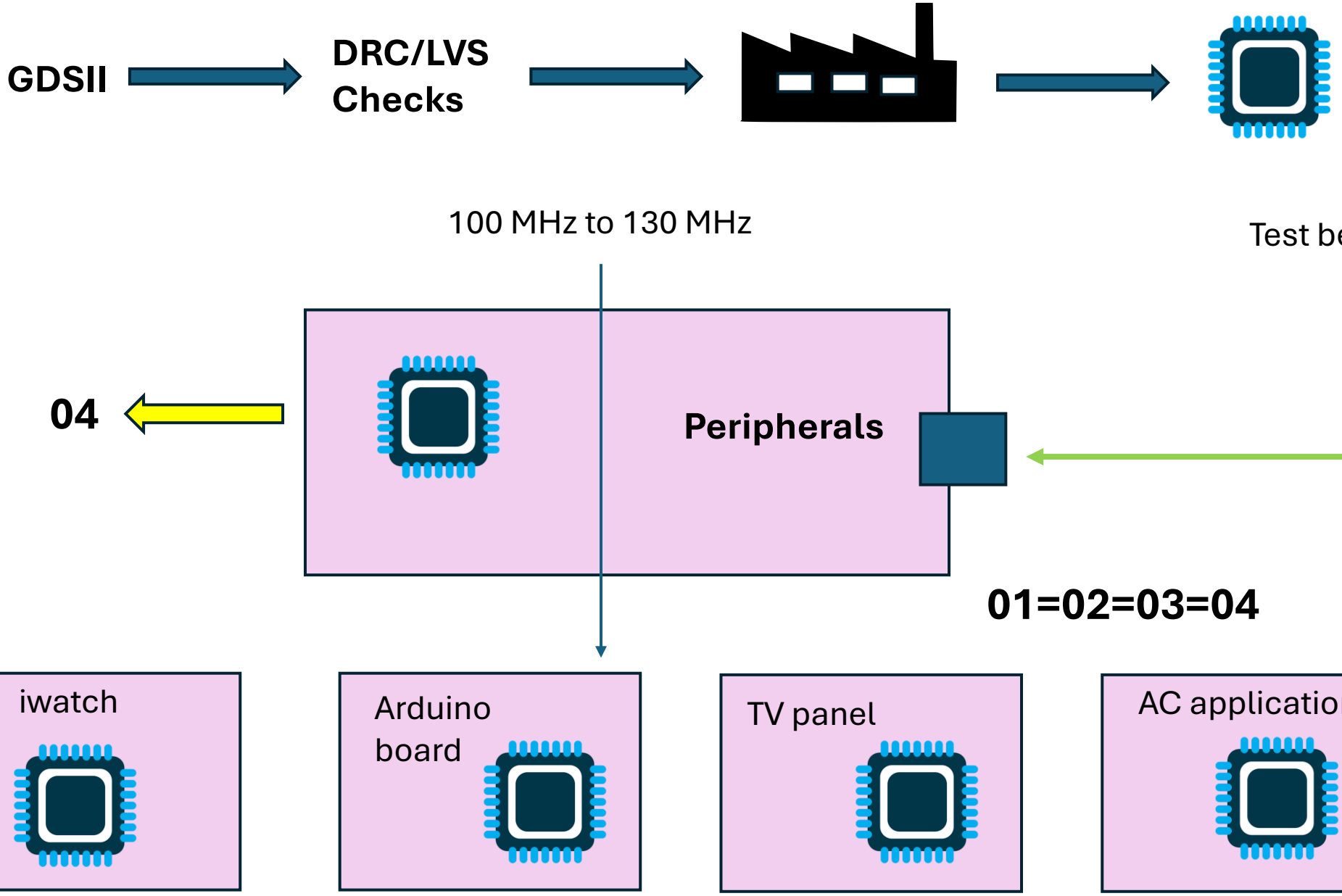

Chip modelling
00=01
00
GCC
01
Specs(C model)
Testbench is in C language
RTL Architect
02
Soft copy of the Hardware using RTL (Verilog)
Soc Design Flow
Processor
Peripherals/IPs
ASIC Design Flow
Gate level Netlist(synth P1)
Macros(synth RTL)
Analog Ips(func RTL)
Synthesis
GPIOs
SoC integration
03
RTL2GDS
Floor planning ,
Placement,
cts,
routing
Macros and Analog IP Libraries Hardened(hard macro- HM)
Processor will be a soft logic
In some cases ,processor is also HM


GDSII
DRC/LVS
Checks
100 MHz to 130 MHz
Test bench in C language
04
Peripherals
01=02=03=04
iwatch
Arduino
board
TV panel
AC application