

# A Three Stage Comparator And Its Modified Version With Fast Speed And Low Kickback

A Project Work

Submitted in partial fulfilment of Requirements for the award of the

Degree of

BACHELOR OF TECHNOLOGY

IN

ELECTRONICS AND COMMUNICATION ENGINEERING

By

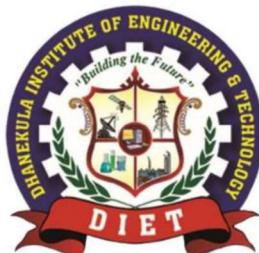
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Certified by ISO 9001-2015, Accredited by NBA

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**CERTIFICATE**

This is to certify that the project work entitled “ A THREE STAGE COMPARATOR AND ITS MODIFIED VERSION WITH FAST SPEED AND LOW KICKBACK ” is bonafide record of project work done jointly by S. Divya Sri (198T1A04E3), S. Leela Durga Prasad (198T1A04E5), Sachin Jha (198T1A04E1), B.A.K.Venkatesh (208T5A0401), under my guidance and supervision and is submitted in partial fulfillment for the award of the degree of Bachelor of Technology in Electronics & Communication Engineering by Jawaharlal Nehru Technological University, Kakinada during the academic year 2022-2023

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## DECLARATION

I declare that this project report titled **A Three Stage Comparator And Its Modified Version With Fast Speed And Low kickback** submitted in partial fulfillment of the degree of B. Tech in Electronics and Communication Engineering is a record of original work carried out by us under the supervision of Dr. M. Vamshi Krishna and has not formed the basis for the award of any other degree or diploma, in this or any other Institution or University. In keeping with the ethical practice in reporting scientific information, due acknowledgments have been made wherever the findings of others have been cited.

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## **DHANEKULA INSTITUTE OF ENGINEERING AND TECHNOLOGY**

### **Department of Electronics & Communications Engineering**

#### **VISION-MISSION-PEOs**

##### **VISION/MISSION/PEOs**

Institute Vision	Pioneering Professional Education through Quality
Institute Mission	<ul style="list-style-type: none"><li>• Providing Quality Education through state-of-art infrastructure, laboratories, and committed staff.</li><li>• Moulding Students as proficient, competent, and socially responsible engineering personnel with ingenious intellect.</li><li>• Involving faculty members and students in research and development works for the betterment of society.</li></ul>
Department Vision	Be a model in the arena of Electronics and Communication Engineering Education & Research to Elevate Rural Community
Department Mission	<ul style="list-style-type: none"><li>• Imparting professional education endowed with ethics and human values to transform students to be competent and committed electronics engineers.</li><li>• Adopting best pedagogical methods to maximize knowledge transfer.</li><li>• Having adequate mechanisms to enhance understanding of theoretical concepts through practice.</li><li>• Establishing an environment conducive for lifelong learning and entrepreneurship development.</li><li>• To train as effective innovators and deploy new technologies for service of society.</li></ul>
Program Educational Objectives (PEO's)	<p><b>PEO1:</b> Shall have professional competency in electronics and communications with strong foundation in science, mathematics and basic engineering.</p> <p><b>PEO2:</b> Shall design, analyze and synthesize electronic circuits and simulate using modern tools.</p> <p><b>PEO3:</b> Shall Discover practical applications and design innovative circuits for Lifelong learning</p> <p><b>PEO4:</b> Shall have effective communication skills and practice the ethics consistent with a sense of social responsibility.</p>

DHANEKULA INSTITUTE OF ENGINEERING AND TECHNOLOGY

Department of Electronics & Communications Engineering

POs/PSOs

PROGRAM OUTCOMES

1	<b>Engineering Knowledge:</b> Apply the knowledge of mathematics, science, engineering fundamentals, and engineering programs.
2	<b>Problem analysis:</b> Identify, formulate, review research literature, and analyze complex Engineering problems reaching substantiated conclusions using first principles of Mathematics, natural sciences, and engineering sciences
3	<b>Design/development of solutions:</b> Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, and societal considerations.
4	<b>Conduct investigations of complex problems:</b> Use research-based knowledge and research methods including design of experiments, analysis, and synthesis of the information to provide valid conclusions.
5	<b>Modern tool usage:</b> Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6	<b>The engineer and society:</b> Apply to reason informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues, and the consequent responsibilities relevant to the professional engineering practice.
7	<b>Environment and sustainability:</b> Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8	<b>Ethics:</b> Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9	<b>Individual and teamwork:</b> Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10	<b>Communication:</b> Communicate effectively on complex engineering activities with the Engineering community and with society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11	<b>Project management and finance:</b> Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12	<b>Lite-long learning:</b> Recognize the need for and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

## **PROGRAM SPECIFIC OUTCOMES (PSO's)**

**PSO1:** Make use of specified software tool for designing and developing VLSI and Embedded Systems.

**PSO2:** Innovate and Design application specific electronic circuits for modern wireless communication.

**Project vs. POs Mapping**

Project title	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12
A Three Stage Comparator And Its Modified Version With Fast Speed And Low Kickback												

3-High

2-Medium

1-Low

### **Justification of Mapping of Project with Program Outcomes:**

1. The knowledge of mathematics, science, engineering fundamentals, and engineering Programs are strongly correlated to all course outcomes.
2. Application of Ethical principles is not correlated to all course outcomes.

**Project vs. PSOs Mapping**

Project Title	PSO1	PSO2
A Three Stage Comparator And Its Modified Version With Fast Speed And Low Kickback		

3-High

2-Medium

1-Low

### **Justification of Mapping of Project with Program Specific Outcomes:**

This project is related to Communications area, which helps to expertise in the Corresponding area by applying engineering fundamentals are correlated to all course outcomes.

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## **A Three-Stage Comparator and Its Modified Version With Fast Speed and Low Kickback**

## ABSTRACT

This brief presents a three-stage comparator and its modified version to improve the speed and reduce the kickback noise. Compared to the traditional two-stage comparators, the three-stage comparator in this work has an extra amplification stage, which enlarges the voltage gain and increases the speed. Unlike the traditional two-stage structure that uses pMOS input pair in the regeneration stage, the three-stage comparator makes it possible to use nMOS input pairs in both the regeneration stage and the amplification stage, further increasing the speed. Furthermore, in the proposed modified version of three-stage comparator, a CMOS input pair is adopted at the amplification stage. This greatly reduces the kickback noise by canceling out the nMOS kickback through the pMOS kickback. It also adds an extra signal path in the regeneration stage, which helps increase the speed further. For easy comparison, both the conventional two-stage and the proposed three-stage comparators are implemented in the same 45nm CMOS process.

## **CHAPTER-1**

### **INTRODUCTION**

#### **Introduction:**

Nowadays, many applications such as signal filtering and processing are processed digitally. Designers of digital integrated circuit (IC) need to develop a fast analog to digital converter (ADC) circuit because ADC will influence the overall performance of the applications [1]. In these applications, the power consumption and processing time is very critical. Most ADCs use a comparator as part of their building blocks. Hence the comparator must have a high speed and consume less power. Comparator is used to compare two analog signals and will give the output in binary signal based on the comparison [2]- [3]. Since the input signals are usually low in amplitude, a preamplifier circuit is needed for the comparator. A differential amplifier with active loads is usually the first stage of the preamplifier. The differential amplifier will produce a very high gain. It amplifies the difference between two input voltages. The output of the preamplifier is connected to the decision-making circuit or latch. The decision-making circuit determines which signal is greater by comparing the signals. A flash and pipeline ADC architecture usually use the preamplifier based comparators [4]. A preamplifier based comparator is a regenerative comparator, it uses back to back latch stage and positive feedback [5, 6]. The preamplifier in a comparator with latch is used to reduce the kickback effect [1]-[5]. This will help in eliminating noise. A latch is defined as the memory unit that stores a charge on the gate capacitance of an inverter [4]. A commonly used architecture in analog circuits is a dynamic latch because it provides excellent speed along with an acceptable accuracy. A dynamic latch circuit can be constructed using a cross coupled pair of PMOS and NMOS transistors [6]-[7]. The latch works in two phases which is governed by a clock (CLK) level either low or high.

#### **Importance of Low power:**

Demand for devices with portable battery is increasing rapidly and the crux of matter is low power design methodologies for high speed applications. This power reduction is achieved by voltage scaling. The voltage scaling results in subthreshold region of operation and these increasing demands need to meet in results in new architectures and innovative circuits. As we step features the performance is affected by process variation. This exists in certain applications

like window comparators, analog to digital converters and others. Comparators are the heart of all these applications. Overall performance of comparator is influenced by its design [1]. The important function of the comparator is to compare certain values versus the reference value.

### **Importance of comparator in ADC:**

Analog-to-digital converters (ADC) have become a significant element driving the semiconductor industry over the past few years. Increased integration of different functional blocks within a single chip makes ADCs more conventional and they are able to provide high speed with low power dissipation. In addition, some features of ADCs like small size processes, low power indulgences, and a reduced propagation delay make them more acceptable to the semiconductor industry. However, it is not straightforward to scale down transistor dimensions, as it requires high channel doping, gate-induced drain leakage, and band to band tunneling across the junction. The difficulty of short channel effects also needs to be controlled [1]. Moreover, analog circuit design happens to be more complex to carry out the necessity of reliability, where supply voltages need to be decreased according to the small dimensions of the transistors [2]. All these concerns apply to the most usable representative of the ADCs: the comparator.

The comparator is the key building block in the design process for ADCs. The comparators measure the smallest voltage differences in ADC's inputs, resolving the performance and the precision of any ADCs. An application that requires digital information recovery from analog signals, such as I/O receivers and radio frequency identification (RFID) memory circuits, widely uses high performance comparators to intensify a little input voltage to a big voltage level [3, 4]. Moreover, digital logic circuits can detect these signals within a short period. Therefore, a faster and precision-making comparator requires high gain and high bandwidth [5, 6].

Several structures of high-speed comparators exist, such as the multistage open loop comparator, the preamplifier latch comparator, and the regenerative latch comparator. Among the different structures, high resolution and high speed can be obtained easily by using the multistage open loop comparator. On the other hand, the latch-type comparator is the most usable one in the abovementioned applications due to its high-speed and low power consumption features. Latch-type comparators are able to accomplish decisions more rapidly with no static power indulgence and strong positive feedback [13]. Moreover, latch-type comparators are able to generate high

gain in regeneration mode due to their positive feedback features. However, to design circuits for low voltage operations capable of decreasing the dynamic range of the inputs and the corresponding differential process [2, 14], the power dissipations in rail-to-rail operations are often increased. Consequently, the most vital limitations of the dynamic latch comparator are the kickback noises generated by high transmission currents [15]. In addition, employing a transmission gate can also induce spikes at the differential input voltage signals, which affects the performance of the dynamic latch comparator due to random noise, input offset voltages, and component mismatch.

### **Latch Based Comparators:**

Latch based comparators are used for low power design and high speed. The latch based comparator consists of 2 stages. The preamplifier stage of comparator improves the sensitivity of comparator from noise generated by feedback stage[2].The latch stage senses the small difference between the inputs and detects the larger input. The output buffer provides amplified outputs. An input referred latch offset voltage, resulting from threshold voltage VTH, current factor  $\beta$  ( $= \mu COXW/L$ ) and parasitic load capacitance mismatches, limits the accuracy of comparators [1]. The design of these stages is very important so as to achieve an efficient performance. In [3], double tail comparator it is proposed where the conventional comparator is changed for low power and quick operation as delay is reduced by adding few more transistors. Common mode input voltage is limited by low power operation. Comparators with high performance are required to amplify small inputs to signals with sufficient level to be detected by various systems [8]. In the proposed design of the comparator as in [1], a fully differential with an enhanced reset architecture using transmission gates to increase the speed has been used for sample and hold less ADC. A fast comparator with high accuracy is key element for ADC [9]. Apart from technological amendments, designing new circuits for low voltage operation and shunning stacking of transistors between the rails is preferred. In systems designed for testing and fault detection, window comparators are utilized. They are also required to meet the demand of low power design. The conventional window comparator [4]with voltage hysteresis property operating in noisy conditions employs comparators along with AND gate. Comparators are the vital elements of many electronic systems and it must be optimized to achieve higher performance.

In these days, Analog-Digital converters (ADCs) require high speed and more power efficient comparators. Because of this, design of high speed and low power comparators becomes more demanding in the CMOS manufacturing industry. Particularly, latch type dynamic comparator is preferred due to its high input impedance and very low static power consumption. [1] Today's modern comparators use dynamic pre-amplification process as the first stage in the comparison process. After pre-amplification stage, the output of pre-amplification stage is carried into regenerative stage. At the earlier developing stage, single-stage dynamic comparators were designed. In single-stage dynamic comparators, a latch circuit is connected in series followed with a preamplifier circuit. But this design possessed a drawback. The kick-back noise which is produced by the means of capacitive path between output and input nodes. This kick-back noise is the reason why the single-stage dynamic comparators preferred as less power effective when compared to later develop more power efficient dynamic comparators. These dynamic comparators can be designed using energy efficient gates as mentioned in [1]. Dynamic comparators have developed in various types in due course of time. One of these types was strong arm latch type of comparators. These strong arm type latch comparators are more popularly used as regenerative comparators [2]. This strong arm type of comparator has less static power due to its strong positive feedback. This type comparator has only one stage design. Because of the one stage design, strong arm latch type comparators have large voltage headroom as mentioned in [3]. Two-stage dynamic comparators were introduced to get control of kick-back noise. Two stage dynamic comparator consists of two stages. The first stage in the two-stage dynamic comparator is called pre-amplifier stage[10-15]. The other stage of two-stage dynamic comparator is called latching stage. In the first stage, preamplifier circuit amplifies the given input signal. Pre-amplifier amplifies the given input signal to minimize the comparison time and therefore increase the comparison speed. The second stage, latching circuit is generally a circuit with inverters back to back[16-18] .The second stage carries out the comparison process in the two-stage dynamic comparator circuit.

The latch based comparator circuit being designed consists of a preamplifier and a dynamic latch.

### **Comparator:**

In electronics, a comparator is used to compare two voltages and it will specify which input is higher by stating the output in digital form [1]. A block diagram of a comparator is illustrated in Figure 1. Two terminals at the input are the analogue inputs indicated by  $V_+$  and  $V_-$  and the output in digital form is  $V_o$ .

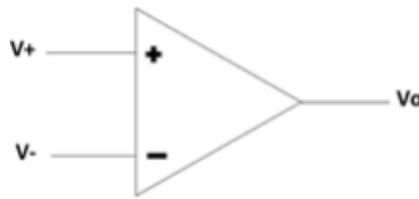


Figure 1: Block diagram of a comparator

Referring to Figure 1, when the input voltage at the positive terminal ( $V_+$ ) is greater than the input voltage at the negative terminal ( $V_-$ ), the output will be a positive value or logic 1. However, when the input at the negative terminal is greater, the output voltage will be negative or logic 0.

### **Preamplifier:**

The preamplifier is used to amplify the input signal. This is done by inputting the signal to the first stage of the preamplifier circuit which is a differential amplifier with active loads. This is followed by a circuit to minimize kickback noise and to reduce the effect of offset voltage error caused by device mismatch [5]. The output of the preamplifier is connected to the decision-making circuit. The decision-making circuit compares the signals and determines which signal is greater. The output of the decision-making circuit is then converted into a logic signal [2] by an output buffer circuit. The preamplifier used here is self-biased differential circuit with active loads in order to reduce the effect of offset voltage error caused because of device mismatch [8].

### **Latch:**

A dynamic latch stage is a second stage of the comparator circuit. In the circuit, two inverters connected back-to-back is used to form a differential comparator. NMOS transistors are also

used and placed between the two differential nodes of the latch. The latch stage will amplify the difference between input signals after determining which of the input signals is greater. The output of the latch will be in digital output level indicating whether the differential input signal is positive or negative.

## CHAPTER 2

### LITERATURE REVIEW

**Babayan-Mashhadi, S., & Lotfi, R. (2014). Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 22(2), 343–352.**

The need for ultra low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional doubletail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18- $\mu$ m CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced.

Summary: Although transistor count is more delay and power consumption are reduced.

**Khorami, A., & Sharifkhani, M. (2016). High-speed low-power comparator for analog to digital converters. AEU - International Journal of Electronics and Communications.**  
Low-power high-speed ADCs are natural candidates for portable electronic devices. Comparators play an important role in efficiency of commonly used ADCs, such as Flash and SAR ADCs. Static comparators have been used in the past, however, they are impractical for portable applications because of their limited speed and significant amounts of power consumption. One-stage dynamic comparators were proposed to reduce the power consumption and improve the speed. These comparators, however, suffer from an inherent trade-off between the power consumption and offset voltage . Moreover, one-stage dynamic comparators suffer from kick-back noise caused through the capacitive path from the output

nodes to the input nodes of the comparator . Two-stage dynamic comparators were proposed to mitigate the kickback noise and decouple the offset versus speed trade-off of the single-stage dynamic comparators. In the two-stage dynamic comparators, the input transistors are chosen large enough to achieve a given offset voltage. In fact, the overall offset of the comparator is almost dominated by the first stage. Using large transistors at the input leads to large parasitic capacitors at the output of the first stage of the comparator. Consequently, there is an inherent trade-off between power consumption and offset voltage. Recently some methods are reported to enhance the speed and reduce power consumption, or offset voltage.

**Summary:** Although transistor count is more delay and power consumption are reduced. In this paper, A low-power high-speed two-stage dynamic comparator is presented. In this circuit, the voltage swing of the first stage of the comparator, pre-amplifier stage, is limited to  $V_{dd}/2$  in order to reduce the first stage power consumption. Also, this voltage swing limitation provides a strong drive at the evaluation phase for the second stage to enhance the comparison speed. Analytical derivations along with post layout simulation results prove that the proposed method speeds up the conventional circuit by a factor of two in the same budget of power consumption and offset voltage. Furthermore, the proposed circuit offers a wide input common mode range as large as the supply voltage while employing PMOS transistors at the input of the comparator.

**Summary:** By employing PMOS the power although  $v_{cm}$  is reduced, the delay is more

**Neethu Prakash, SAR ADC Using Low Power High Speed Comparator for Precise Applications, journal of Emerging Technologies and Innovative Research.**

Now a days, low-power high-speed ADCs are integral parts of a variety of applications such as handheld devices. Comparators are the key building blocks of different types of ADCs. Several years ago, CMOS amplifiers were used as static comparators, although they suffer from very high power consumption (since they are always on) and inherent limited speed. In the proposed comparator, pMOS latch and pMOS preamplifier in addition to a small cross-coupled circuit are used with a special clocking pattern to adjust the preamplifier gain. The clocking pattern provides enough preamplifier gain; since pMOS transistors are used at the input of the latch, and the cross-coupled circuit is employed to keep the common mode voltage of the preamplifier outputs at a low level. It is shown that the proposed comparator

reduces the power consumption by half while increasing the speed. Moreover, it operates at large input common-mode voltages close to VDD, although pMOS transistors are used at the input of the comparator. As another benefit, the preamplification delay can be set to its optimum value to have a better comparison speed and reduce excess power consumption. However, in the conventional and other comparators, this delay is fixed to a value which is far from its optimum point. As a result, the proposed comparator is a good candidate for precise low power high-speed applications. Deactivating the preamplifier after the optimum delay reduces the power consumption significantly. Therefore, it reduces the power consumption and improves the speed. The proposed structure can also be implemented using nMOS transistors, i.e., latch and preamplifier with input Nmos transistors. This will result in a higher speed because of the inherent superiority of nMOS transistors over pMOS ones. Using this comparator an SAR ADC is made. The tool used is Cadence

Summary: speed is improved in this method.

**Lu, J., & Holleman, J. (2013). A Low-Power High-Precision Comparator With Time-Domain Bulk-Tuned Offset Cancellation. IEEE Transactions on Circuits and Systems,**

A novel time-domain bulk-tuned offset cancellation technique is applied to a low-power high-precision dynamic comparator to reduce its input-referred offset with minimal additional power consumption and delay. The offset cancellation scheme does not introduce observable offset or noise, and can achieve fast and robust convergence with a wide range of common mode input. Operating at a supply of 5 V and clock frequency of 200 kHz, the comparator together with the OC circuitry consumes Less energy comparison

**Ata Khorami, Mohammad Sharifkhani,Excess power elimination in high-resolution dynamic comparators, Microelectronics Journal, Volume 64, 2017, Pages 45-52, ISSN 0026-2692,**

A method is presented to reduce the power consumption of the two-stage dynamic comparators. In the two-stage dynamic comparators, the first stage (pre-amplifier stage) amplifies the input differential voltage. Then the second stage (latch stage) is activated and

finishes the comparison. When the comparison is about to finish, the balance of the positive feedback of the latch stage tends to tilt toward one of the outputs; after this, to the end of the comparison, there is no need for additional pre-amplification gain which causes excess power consumption. In this paper, a method is proposed to eliminate this part of power consumption. It is shown that while reducing the power consumption significantly, the method does not affect the dynamic behavior of the comparator such as speed or offset voltage. This method reduces the power consumption.

**M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, “A low noise self-calibrating dynamic comparator for high-speed ADCs,” in Proc. IEEE Asian Solid-State Circuits .** This paper presents a low offset voltage, low noise dynamic latched comparator using a self-calibrating technique. The new calibration technique does not require any amplifiers for the offset voltage cancellation and quiescent current. It achieves low offset voltage in low power consumption, Furthermore the proposed comparator requires only one phase clock while conventionally two phase clocks were required leading to relaxed clock. Moreover, a low input noise of 0.6 mV at 1 sigma, three times lower than the conventional one, is obtained.

**Masaya Miyahara, Yusuke Asada, Daehwa Paik, & Akira Matsuzawa. (2008). A low-noise self-calibrating dynamic comparator for high-speed ADCs. 2008 IEEE Asian Solid-State Circuits Conference**

A design for an on-chip high-speed clocked-comparator for high frequency signal digitization. The comparator consists of two stages, amplification and regenerative, comprising a total of 10 MOS transistors. The design is implemented in 65nm CMOS technology. Also, the paper presents a new cost effective technique for measuring the maximum speed of the clocked comparator. The measurement and simulation results show that the proposed design has higher speed and less active area than the conventional Comparator design largely depends on the target application. In this paper, we present a design for an on-chip high-speed clocked comparator for high-frequency low-swing signal

test applications. The comparator is attractive for the applications where speed is of the highest priority and the common mode range is limited, for examples, testing of on-chip high frequency signals, high-speed data link and ADCs of moderate number of bits. In addition, a cost-effective technique is presented for measuring the highest possible clock frequency that can be applied to the comparator while keeping correct operation.

**Amaya, A., Villamizar, R., & Roa, E. (2016). An offset reduction technique for dynamic voltage comparators. 2016 12th Conference on Ph.D. Research in Microelectronics and Electronics**

Comparator is one of the fundamental building blocks in Analog-to-digital converters. designing high speed comparator is more challenging when the supply voltage is smaller. in other words to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. This paper presents a technique to reduce offset voltage of a dynamic comparator. Contrary to conventional way of measuring offset, the proposed technique is based on phase measurement of comparator output. A full-digital implementation is used to measure phase without impacting offset accuracy. Simulation results show a reduction of more than ten times in the comparator offset with a small increment in power consumption. The technique can be used during normal operation requiring less delay to finish calibration, so that there is not need to break the communication link associated to the comparator.

**Shilpi Singh, A novel cmos dynamic latch comparator for low power and high speed, International Journal of Microelectronics Engineering (IJME), Vol. 1, No.1, 2015**

The power problem is one of the most serious limitations in high performance VLSI's and battery backed-up systems. High speed and low power comparators are the essential building blocks of many analog circuits such as high speed analog-to-digital converters (ADCs), memory sense amplifiers and data receivers. In analog to-digital converters, the comparator plays a vital role on the overall performance of the converter. A fast and accurate comparator is a crucial element in any high resolution and high speed data converters. There are two main types of comparator based on their structure and operation: amplifier chain type and

latch type. Amplifier chain-type comparators use a set of cascade amplifiers to generate the output in response to small difference between input signal and reference signal. On the other hand, latch type comparators provide higher speed and lower power consumption. This paper presents a novel dynamic latched comparator that consumes lower power and higher speed than the conventional dynamic latched comparators. This paper also provides a comprehensive review of a variety of comparator designs in terms of power and delay. The comparators and the proposed circuit are designed and simulated their transient responses in Tanner EDA suite using 180 nm CMOS technology and 1V power supply voltage and it demonstrates Less power consumption and higher speed than the conventional latched comparators.

## **CHAPTER 3**

### **EXISTING METHOD**

In modern communication systems high-speed analog-to-digital converters (ADCs), as the interface between the digital processors with the analog world, digitize the signal at the front-end receive paths [1]. One of the fastest analog-to-digital converters is the flash analog-to-digital converter, and usually an N-bit flash analog-to-digital converter employs  $2N - 1$  comparators to quantize input signals into corresponding digital signals. Thus the performance of comparators decides the converting speed and quantization precision of ADCs. An ideal latched comparator is composed of a preamplifier with infinite gain and a digital latch circuit. Since the amplifiers used in comparators need not to be either linear or closed-loop, they can incorporate positive feedback to attain virtually infinite gain [2].

Considering the limited gain in the implementation of actual preamplifier design, the actual latched comparators employ an amplifier circuit with finite gain and a positive feedback dynamic latched circuit. Because of its special architecture, working process of a latched comparator could be divided in two stages: tracking and latching stages. In tracking stage the following dynamic latch circuit is disabled, and the input analog differential voltages are amplified by the preamplifier. In the latching stage while the preamplifier is disabled, the latch circuit regenerates the amplified differential signals into a pair of full-scale digital signals with a positive feedback mechanism and latches them at output ends. While the latch circuits regenerate the difference signals, the large voltage variations on regeneration nodes will introduce the instantaneous large currents. Through parasitic gate-source and gate-drain capacitances of transistors, the instantaneous currents are coupled to the inputs of the comparators, making the disturbances unacceptable. It is so-called kickback noise influence. In flash ADCs where a large number of comparators are switched on or off at the same time, the summation of variations came from regeneration nodes may become unexpectedly large and directly results in false quantization code output [3].

High-speed, low-offset, low-power consumption comparator is very attractive for many applications, such as memory sensing circuits, analog to digital converters and data receivers. While the technology scaling of MOS transistors enables high-speed and low-power operation, the offset voltage of the comparator is increased due to the transistor mismatch. In conventional designs, pre-amplifiers are used to reduce offset voltage [1]. However, these techniques require high voltage gain to reduce the offset voltage and loosing effectiveness with the reduction of the drain resistance due to the technology scaling. Moreover, large power consumption of the amplifier is inevitable for realizing a wide bandwidth amplifier. On the other hand, a dynamic comparator which has the offset compensation function was proposed [2]. In this method the same input signal of each comparator as the reference voltage is given in flash type ADC, and the load capacitances of the output node of each comparator are controlled digitally so that the output of the comparator may reach the ideal value. However, the calibration time greatly increases if the resolution of the ADC is increased. Moreover, the speed of the comparator is slowed down due to the increase of added capacitances. Additionally, the considerably large size circuits to control the calibration are necessary for each comparator. Therefore this topology is improper for the design of high resolution flash type ADCs. Moreover, a comparator noise determines the signal to noise ratio of ADCs. This is especially true for a high resolution successive approximation ADC which requires a sufficiently low noise comparator to prevent conversion errors [3]

Preamplifier latch based comparator circuit consists of a preamplifier followed by a latch. The major drawback of the latch comparator is the offset error caused by transistor mismatch [7] and unbalanced charge residues .To overcome this a preamplifier circuit is used. The basic principle of the preamplifiers is that it amplifies the input signal and feeds it to the input of latch which is designed by using back to back inverter [8]. Fig.1 shows the block diagram of a comparator.

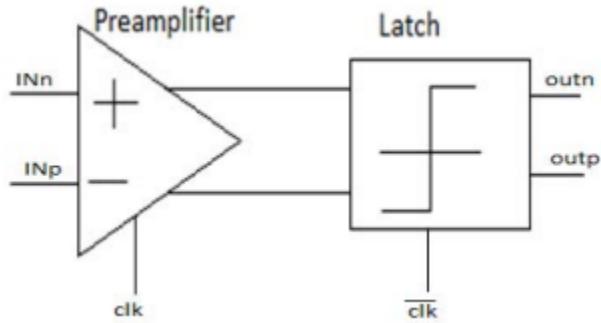


Fig.1.Block Diagram of comparator

As a key building block, the comparator plays an important role in various types of analog-to-digital converters (ADCs). Especially, in high-speed high-resolution SAR ADCs, the ADC sampling rate and accuracy are limited by the comparator speed, kickback noise, input referred noise, and offset. Under this circumstance, it is important to design a high-performance comparator. High performance comparators are needed to amplify a small input (or the difference between the input voltage and a reference voltage) to a level large enough to be detected by digital logic circuits within a very short time.

In this method a latch based comparator which has a preamplifier and latch stage is proposed.

The block diagram of latch based comparator is shown below.

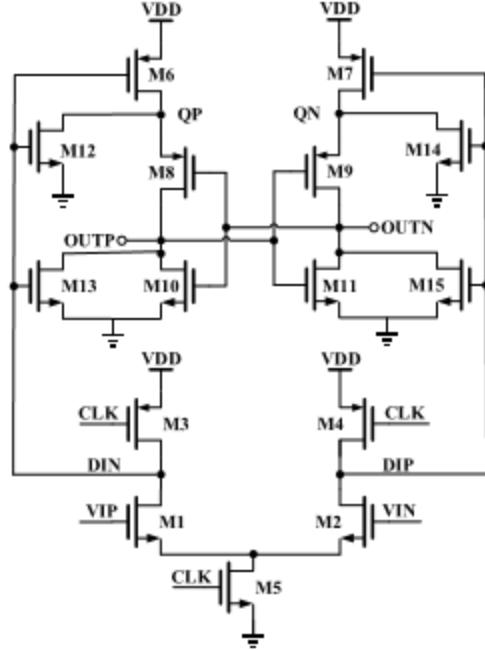


Fig. 2. Miyahara's two-stage comparator.

Fig. 2 shows the Miyahara's two-stage comparator. There are three phases of operation, namely the reset phase, the amplification phase, and the regeneration phase. In the reset phase ( $\text{CLK} = 0$ ), the comparator is reset. In the amplification phase ( $\text{CLK} = 1$ ), the input signal  $\text{VIP}$ – $\text{VIN}$  is amplified and sent to the latch stage. In the regeneration phase,  $\text{OUTP}$  and  $\text{OUTN}$  regenerate to  $\text{VDD}$  or  $\text{GND}$ . As mentioned before, such a structure has the limitation of pMOS input pair in the latch stage.

Although the Miyahara's two-stage comparator increases the speed, its speed can be further improved in the following way. As can be seen in Fig. 2, its latch input pair  $\text{M}_6$ – $\text{M}_7$  are pMOS transistors, and the pMOS hole mobility is small (2–3 times smaller than the nMOS electron mobility), limiting the regeneration speed. Thus, our goal is to use nMOS transistors instead for the latch input pair, so that the regeneration speed could be greatly improved. Meanwhile, we must maintain the nMOS transistors for the preamplifier input pair.

## CHAPTER 4

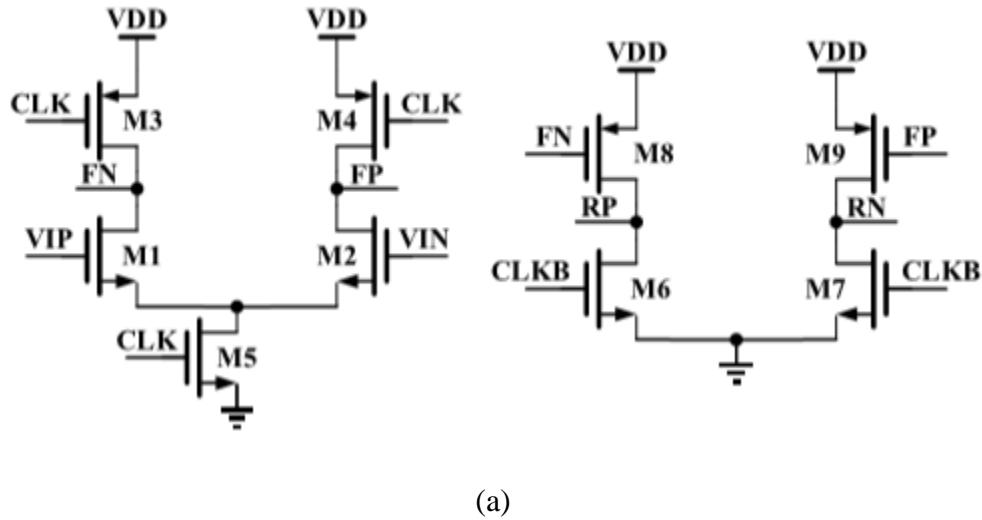
### PROPOSED METHOD

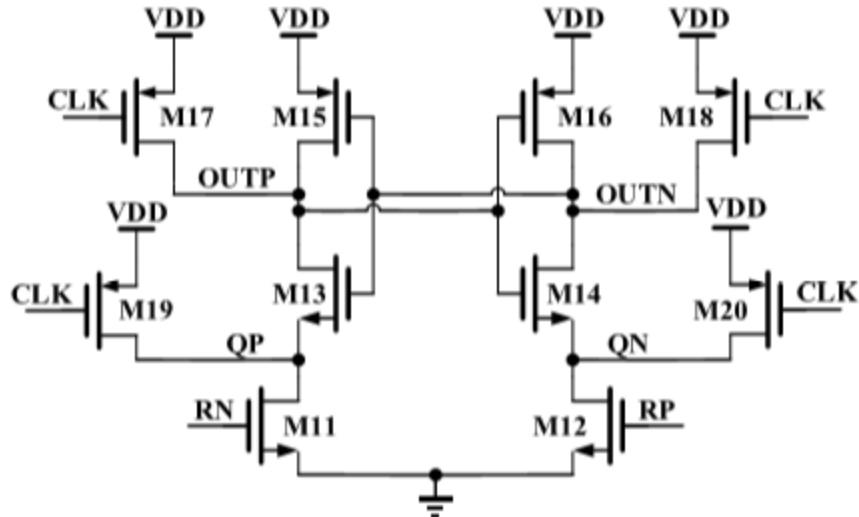
Digital wireless communication applications such as Ultra Wide-Band (UWB) and Wireless Personal Area Network (WPAN) need low-power high-speed ADCs to convert Radio Frequency /Intermediate Frequency signals into digital form for baseband processing. Comparator is an important device widely used in ADC [1]. Comparators are used in ADCs, data transmission, switching power regulators, and many other applications. The comparator design plays a vital role in high speed ADCs. Power consumption & speed are key metrics in comparator design [2]. The comparator is the critical building block for all high speed ADCs, regardless of the architecture, which in large measure determines the overall performance of data converters. It includes the maximum sampling rate, bit resolution, and total power consumption.

Comparators may be the most underrated and underutilized monolithic linear component. This is unfortunate because comparators are one of the most flexible and universally applicable components available. In large measure the lack of recognition is due to the IC op amp, whose versatility allows it to dominate the analog design world. Comparators are frequently perceived as devices, which crudely express analog signals in digital form—a 1-bit A/D converter. Strictly speaking, this viewpoint is correct. It is also wastefully constrictive in its outlook. Comparators don't just compare" in the same way that op amps don't "just amplify". Comparators, in particular high speed comparators, can be used to implement linear circuit functions which are as sophisticated as any op amp-based circuit. Judiciously combining a fast comparator with op amps is a key to achieving high performance results. In general, opamp based circuits capitalize on their ability to close a feedback loop with precision. Ideally, such loops are maintained continuously over time. Conversely, comparator circuits are often based on speed and have a discontinuous output over time. While each approach has its merits, a fusion of both yields the best circuits.

Fig. 3 shows the three-stage comparator in this work. The three stages are connected one after another. Compared with the Miyahara's comparator, the major difference is that one extra preamplifier (the second stage) is added. This extra preamplifier acts as an inverter, and makes the latch stage able to use nMOS input pair M11–12 instead of pMOS input pair, which leads to

increased speed. The extra preamplifier also provides voltage gain, thus improving the regeneration speed and suppressing the input referred offset and noise. Although the extra preamplifier helps increase the speed, this extra stage itself incurs extra delay, because the amplified signal has to go through two stages, rather than one stage, before arriving at the latch stage. Thus, it is necessary to discuss whether this extra delay overwhelms the benefit it brings about. As can be seen in Fig. 3, after the first-stage amplification, its outputs FP and FN fall to GND. This makes the second-stage input pair M8–9 have a large gate–source voltage equal to VDD. As a result, the current on M8–9 is large enough for quickly pulling up RP and RN. This means that the extra delay incurred by the second stage is small (about 20 ps in post-layout simulation) compared to the large delay of the latch stage (about 200 ps in post-layout simulation). This makes sense because the second stage is actually a dynamic inverter which does not incur much delay. Furthermore, compared to the first-stage output load in the Miyahara's comparator (M6–7 and M12–15 in Fig. 3), the first-stage output load in the three-stage comparator is only M8–9 in Fig. 3. The output load is reduced by several times, improving the amplification speed.

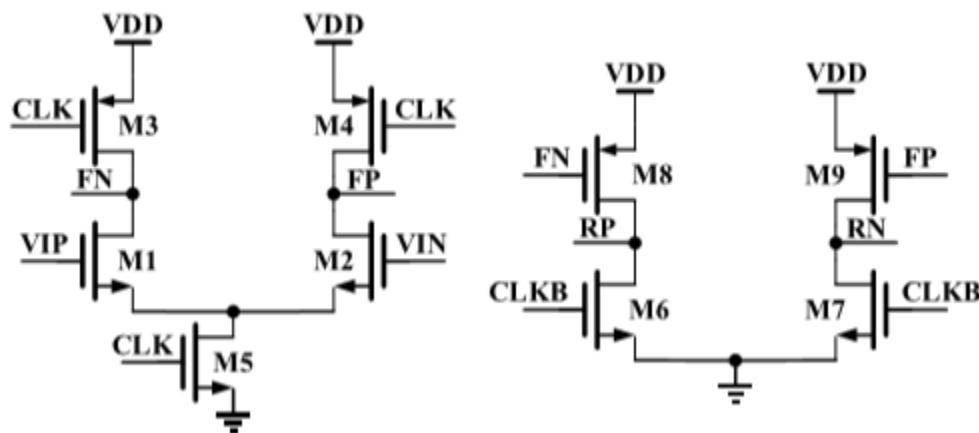




(b)

Fig. 3. Three-stage comparator in this work. (a) First two stages (preamplifiers). (b) Third stage (latch stage).

In order to reduce the kickback noise and further improve the speed, this brief proposes a modified version of three-stage comparator, as shown in Fig. 4. Compared to the original version in the previous section, the only difference is that the modified version has the extra first two stages of Fig. 4(b) and extra paths M29–32 in the latch stage of Fig. 4(c). The extra first two stages use pMOS input pair.



(a)

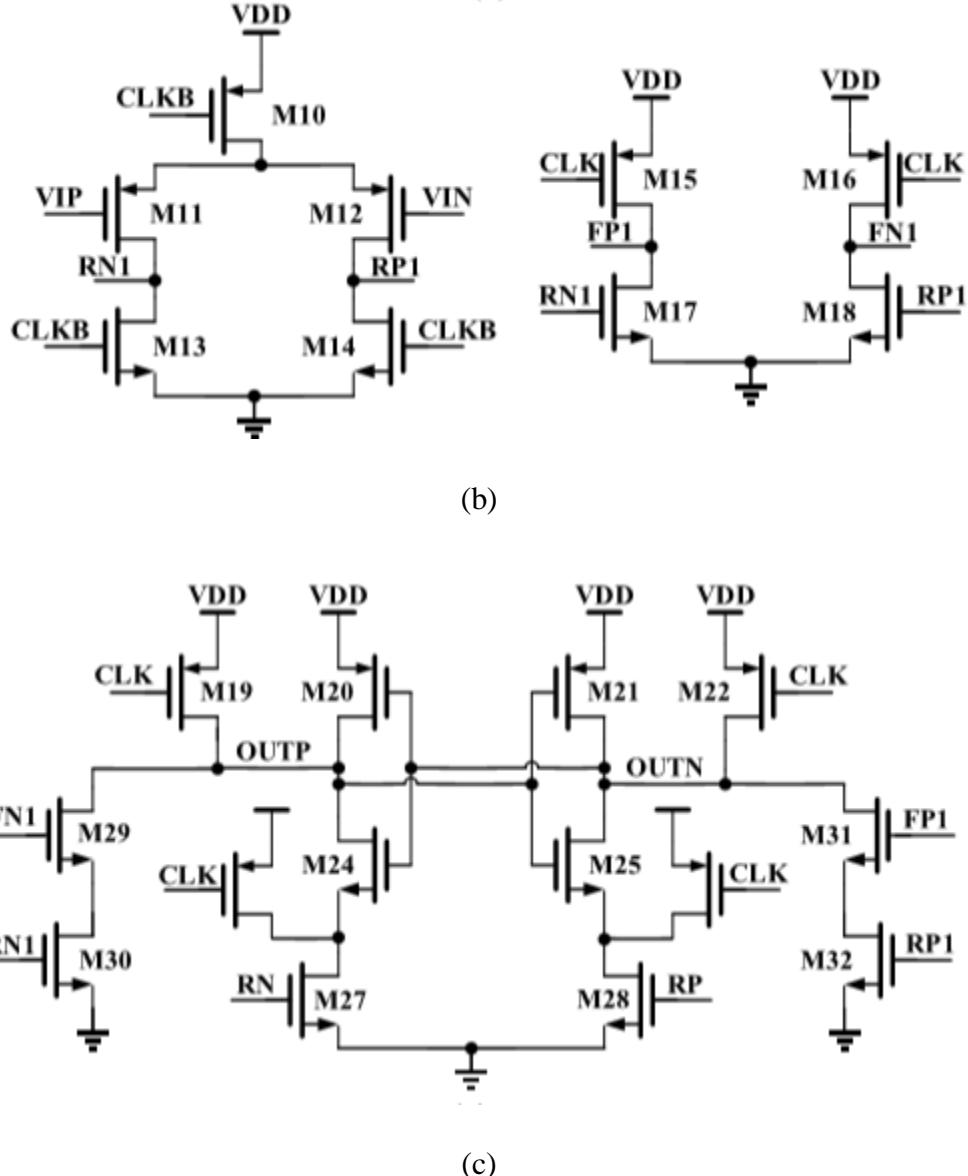


Fig. 4. Proposed modified version of three-stage comparator. (a) Original first two stages (preamplifiers) with nMOS input pair. (b) Extra first two stages (preamplifiers) with pMOS input pair. (c) Third stage (latch stage).

M11–12 to cancel out the nMOS input pair M1–2 kickback noise. Besides, the extra paths M29–32 apply extra signal onto the latching nodes OUTP and OUTN, thus the regeneration speed is increased further, and the input referred offset and noise are suppressed further. The operation of these extra circuits is as follows. In the reset phase, CLK is 0 and CLKB is 1. The RP1 and RN1 in Fig. 4(b) are reset to GND, while FP1 and FN1 are reset to VDD. This turns off M30 and M32 in Fig. 4(c), ensuring that there is no static current in the extra path M29–32.

In the amplification phase, CLK rises to 1 and CLKB falls to 0. RP1 and RN1 in Fig. 4(b) rise to VDD (R stands for rise). Then, FP1 and FN1 fall to GND (F stands for fall). Because the rising of RP1 and RN1 occurs before the falling of FP1 and FN1, the extra paths in Fig. 4(c) are turned on for a limited time, drawing a differential current from the latching nodes OUTP and OUTN. This generates a differential voltage at OUTP and OUTN, which helps speedup the regeneration phase afterward and suppress the comparator input referred offset and noise. After FP1 and FN1 fall to GND, the extra paths in Fig. 4(c) are turned off again to prevent the static current

Overall, the modified version of three-stage comparator has the advantages of faster speed, lower input referred offset and noise, and lower kickback noise..

## **ADVANTAGES:**

- In the proposed method, The extra first two stages use pMOS input pair M11–12 to cancel out the nMOS input pair M1–2 kickback noise. Besides, the extra paths M29–32 apply extra signal onto the latching nodes OUTP and OUTN, thus the regeneration speed is increased further.

## **APPLICATIONS:**

There are several applications of Comparator

- They are used in Audio/Video devices.
- They are used in Cell Phones.
- They are widely used in CMOS Image sensors for mobile applications.
- They are used in Medical Instrumentation and medical imaging.

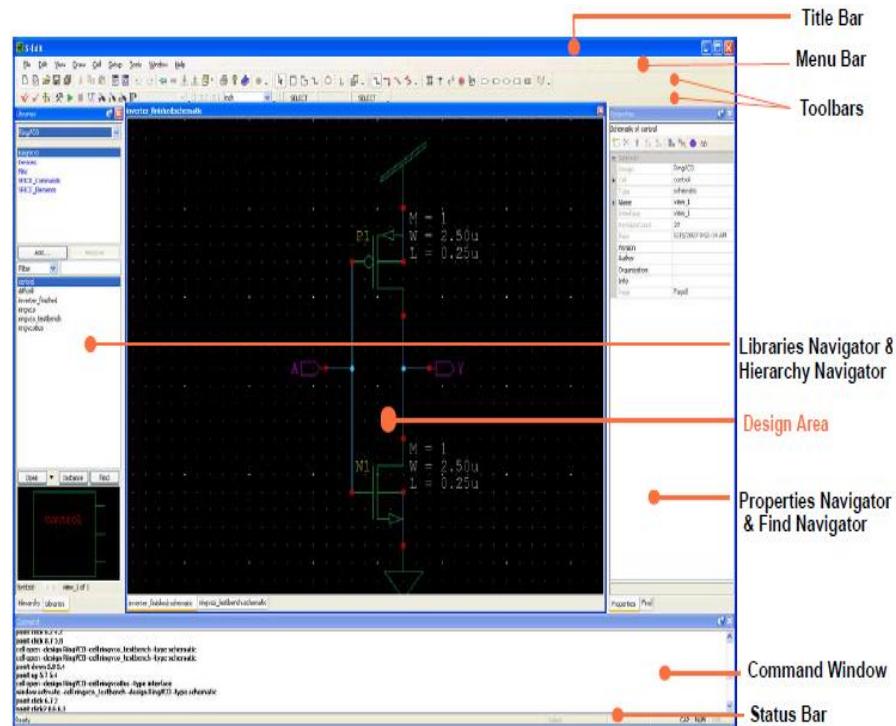
## TANNER TOOL

### Launching S-Edit

To launch S-Edit, double-click on the S-Edit icon.



The user interface consists of the elements shown below. Unless you explicitly retrieve a setup file, the position, docking status and other display characteristics are saved with a design and will be restored when the design is loaded.



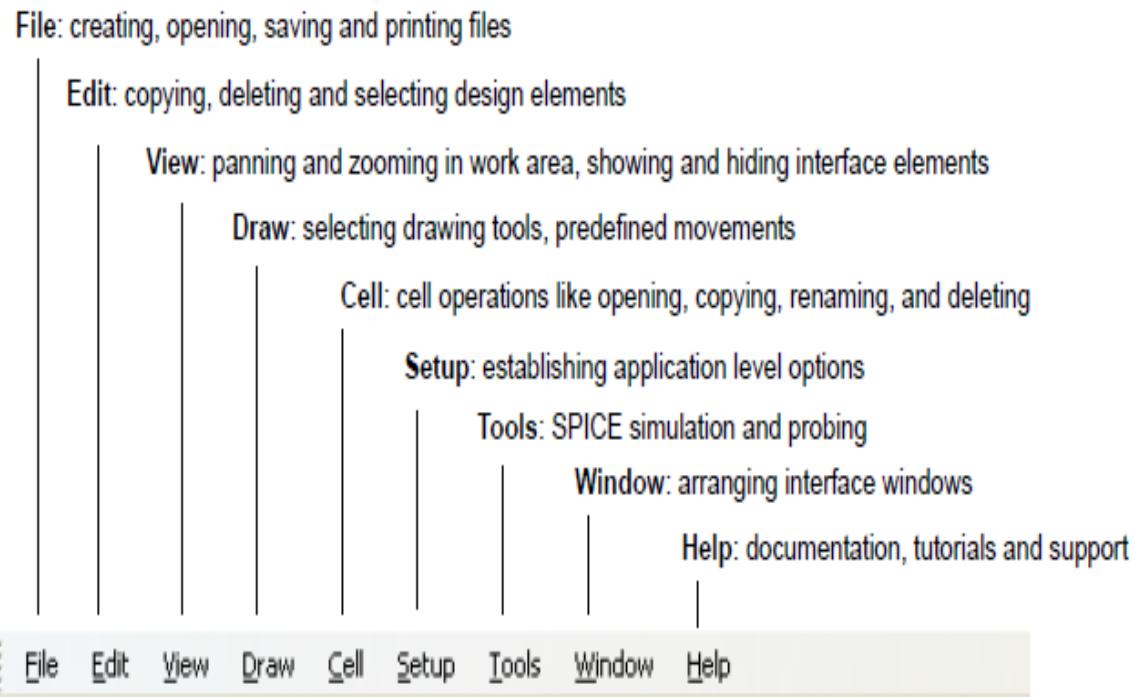
### Parts of the User Interface

## Title Bar

The title bar shows the name of the current cell and the view type (symbol, schematic, etc.).

## Menu Bar

The menu bar contains the S-Edit menu titles. The menu displayed may vary depending on the view type that is active. See “Shortcuts for Cell and View Commands” on page 70 for the various methods S-Edit provides for executing commands.



## Menu List Filtering

Most S-Edit menus and dialogs allow for filtering to speed the process of selecting from a drop-down list. So, when you enter a character, S-Edit will jump to the first list item that begins with that character. For example, typing **g** highlights the first list item beginning with that letter and filters the display to show only items that begin with **g**. Typing a **u** after the **g** highlights the first list item beginning with **gu**, and filters the display to show only items that begin with **gu**, and so on. The search procedure is case-insensitive.

## Toolbars

You can display or hide individual toolbars using the **View > Toolbars** command, or by right-clicking in the toolbar region. Toolbars can be relocated and docked as you like. For added convenience, S-Edit displays a tool tip when the cursor hovers over an icon.

### **Standard Toolbar**

The Standard toolbar provides buttons for commonly used file and editing commands, as well as operations specific to S-Edit such as “View Symbol.”



### **Draw Toolbar**

The Draw toolbar provides tools used to create non-electrical objects, such as rectangles, circles, and lines, for illustrating and documenting a design.



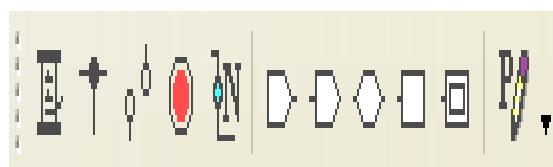
### **Segment Toolbar**

The Segment toolbar provides tools with which you limit the degree of angular freedom allowed when you are drawing wires.



### **Electrical Toolbar**

The Electrical toolbar provides the tools used to create wires, nets, and ports, and to add properties.



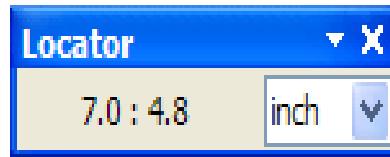
### **SPICE Simulation Toolbar**

The SPICE Simulation toolbar lets you extract connectivity, select and probe nets, launch T-Spice and select evaluated properties.



### Locator Toolbar

The Locator toolbar displays the coordinates of the mouse cursor and allows you to quickly change the units of measurement application-wide.



### Mouse Buttons Toolbar

The Mouse Buttons toolbar shows the current functions of the mouse buttons.



Mouse buttons vary in function according to the tool that is active. The **Shift**, **Ctrl** and **Alt** keys can further change the function. For two-button mice, the middle-button function is accessed by clicking the left and right buttons at the same time, or by pressing **Alt** while clicking the left mouse button.

### Customizing Toolbars

You can add buttons for existing commands to existing S-Edit toolbars, add entirely new toolbars, and add new buttons for entirely new commands to either new or existing toolbars.

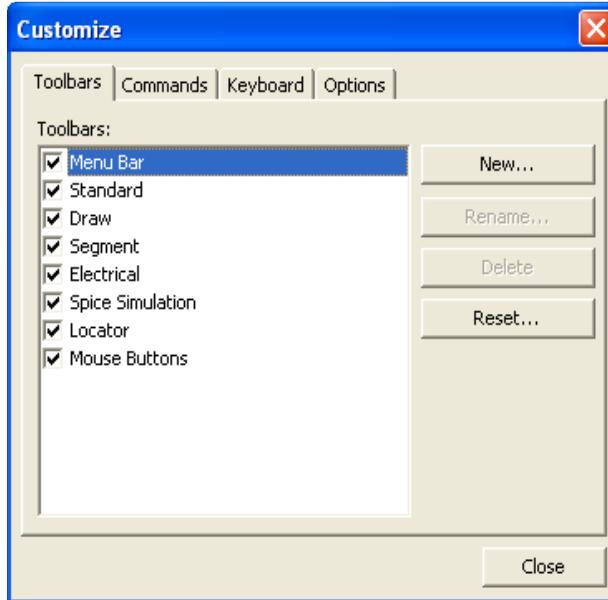
To customize toolbars, right-click anywhere in the toolbar area and click on **Customize** in the

context-sensitive menu.



This opens the **Customize** dialog, to the **Toolbars** tab. Note that in this dialog the checkmarks control only whether or not a toolbar is displayed. The buttons apply only to the toolbar that is highlighted, and will be applied even if a toolbar is not currently displayed.

All toolbars are checked, so all are displayed. Only Menu Bar is highlighted, so any of the button actions (ex. Reset) will act only on the Menu Bar.

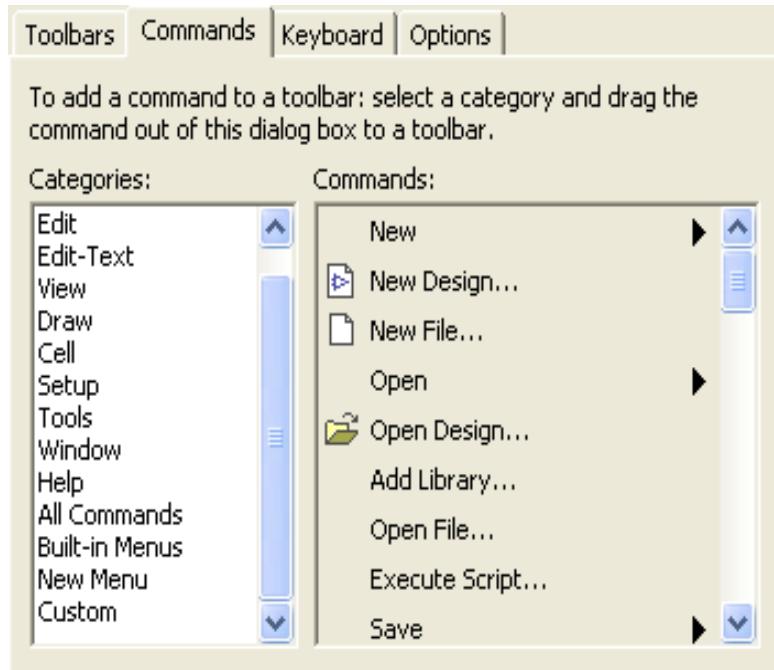


**Reset** returns an existing toolbar to the default display settings for aspects such as icon size, tooltips, etc.—and its original button contents.

The **New**, **Rename** and **Delete** functions apply only to custom toolbars

## Adding a Command to a Toolbar

Use the **Commands** tab to add a button for an existing command to any toolbar.



[1] Right-click in the toolbar area, select **Customize** and then the **Commands** tab.

[2] Pick the desired command from the **Categories** list (or use All Commands for a complete list of available commands), then simply click-and-drag the command from the right column to the desired toolbar.

[3] S-Edit will insert a button displaying the command text, or an icon if one is already defined.

## Adding a New Menu

[1] You can also use the **Commands** tab to add a new menu category to the menu bar.

[2] In the Commands tab, scroll down to **New Menu** at the end of the **Categories** list.

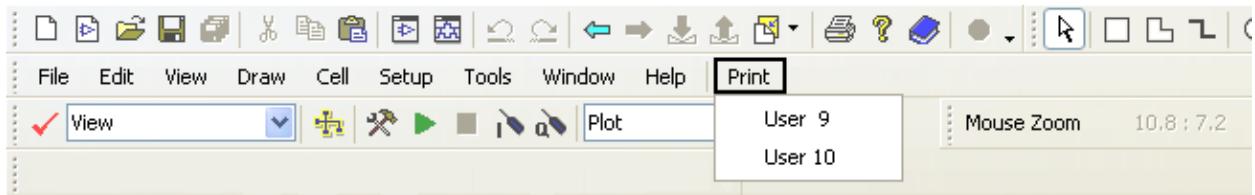
[3] Click-and-drag **New Menu** from the right column to the Menu bar in the interface.



[4] Right-click on the New Menu button you have just placed to open the control menu, where you can rename it, then check **Begin a Group** to populate the menu with pull-down commands.



[5] Select the new menu button in the interface to open the pull-down group, then click-and-drag from the Commands tab to add the desired command(s). Make sure to drop the commands within the group area.



## Schematic design of Inverter

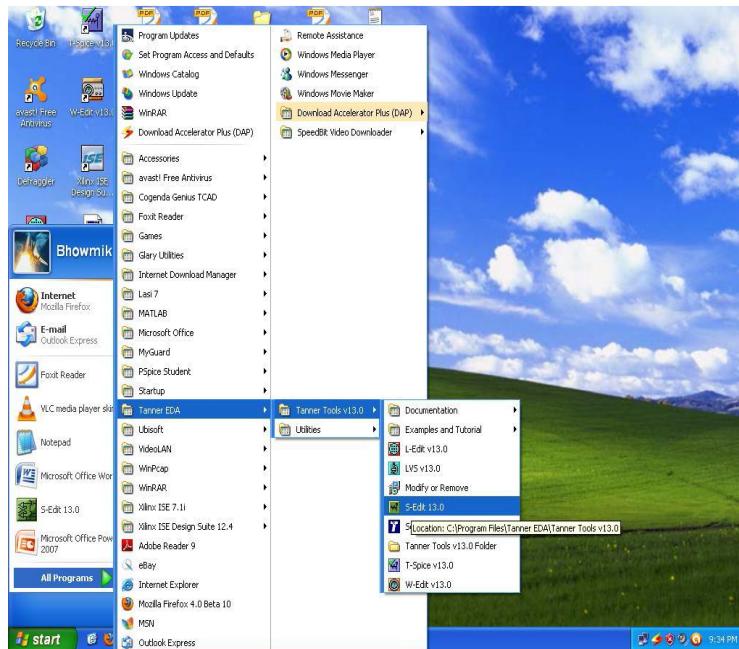
**What is schematic Design:** There are many phases or progressions of a design. A common term you will hear when working with a Designer is “Schematic Design”. This phase is early in the design process. Schematic Design establishes the general scope, conceptual ideas, the scale and relationship of the various program elements. The primary objective of schematic design is to arrive at a clearly defined feasible concept based on the most promising design solutions.

Opening S-edit platform:

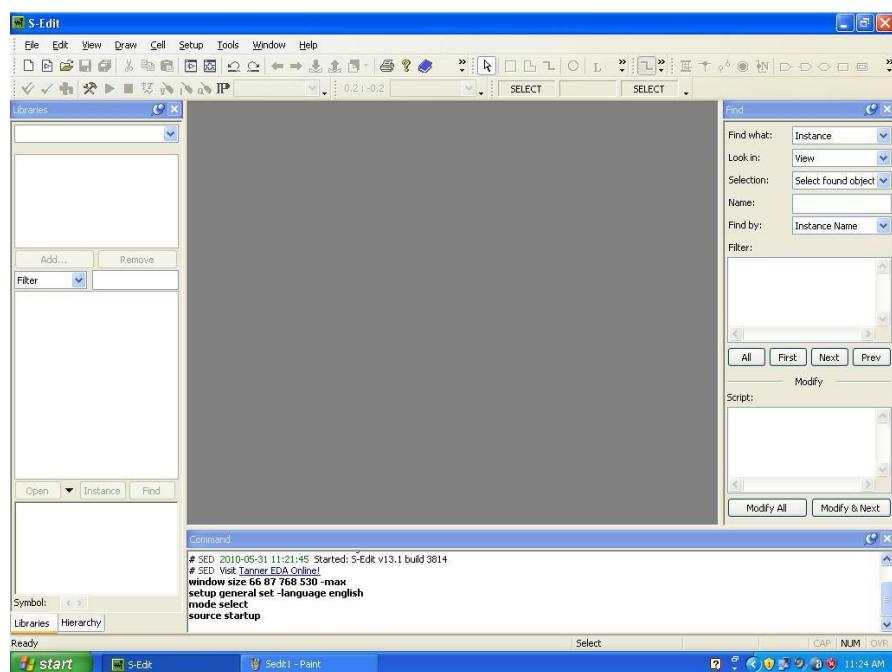
First of all double click on the icon of s-edit on the desktop

or

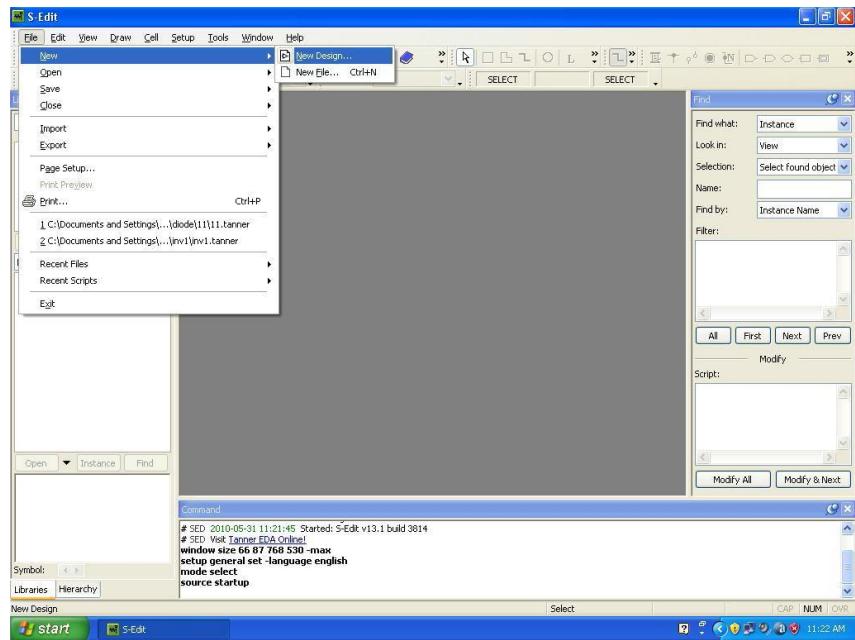
Go to the start menu >>All Programs >>Tanner EDA >>Tanner Tool v 13.0 >> S-Edit v 13.0



A new window will open



Go to >>file >> New >> New Design  
Select New Design

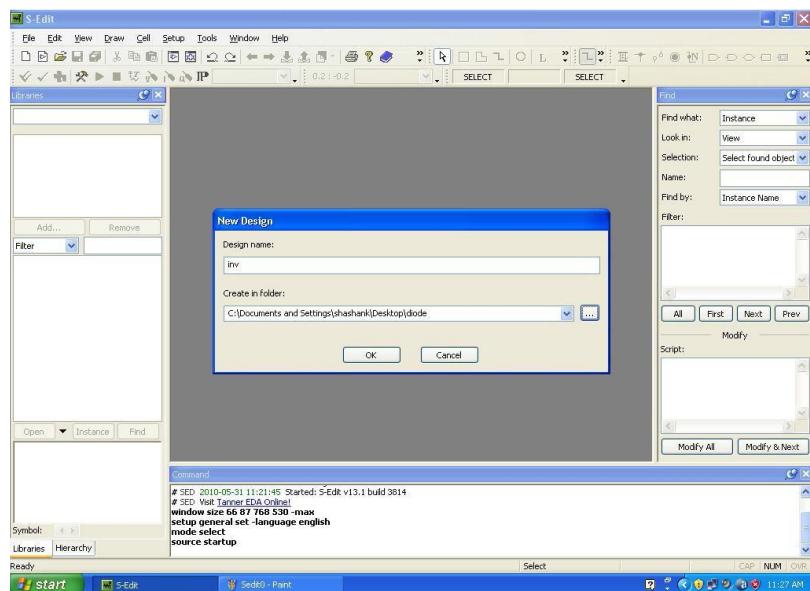


One dialog box will appear

Design Name : Give the name your design as you wish

Create a Folder : Give the path where you want to save the S-Edit Files.

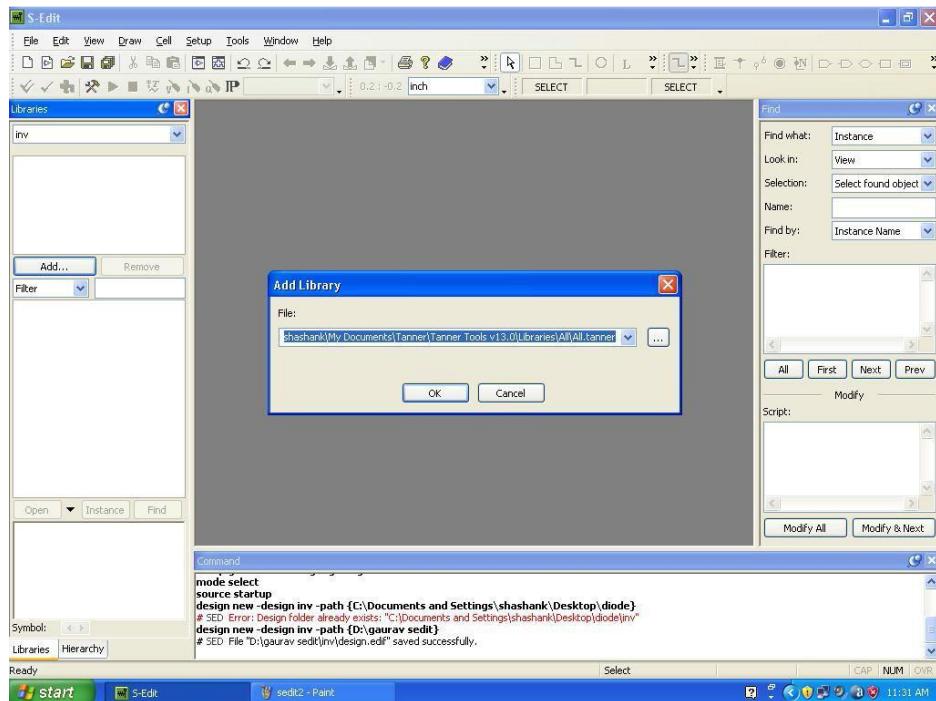
Then Click on 'OK'



Now to add libraries in your work click on **Add** , left on the library window.

Give the path where Libraries are stored . As for example

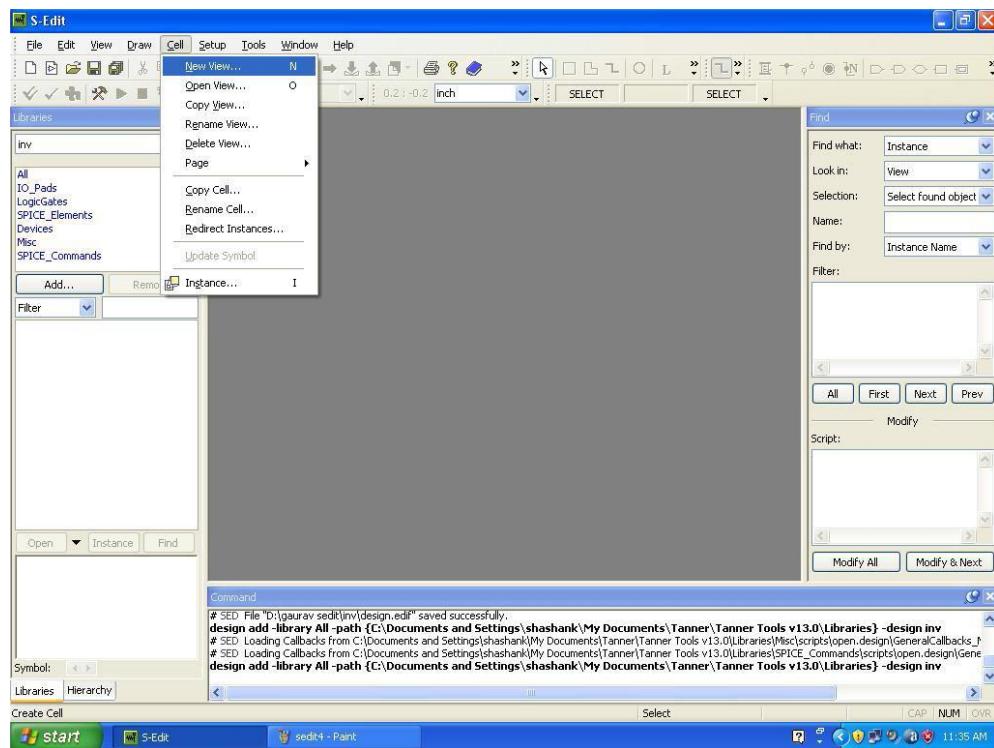
C:\Documents and Settings\Bhowmik.IIIT-3AC288AD0A\My Documents\Tanner EDA\Tanner Tools v13.0\Libraries>All\All.tanner



Now to create new cell

Go to cell menu >> New view --

Select 'New view'



The new cell will appear like below:

Design = your design name

Cell = cell no. ( cell no you can change but your design name **inv** will be same for different cell.

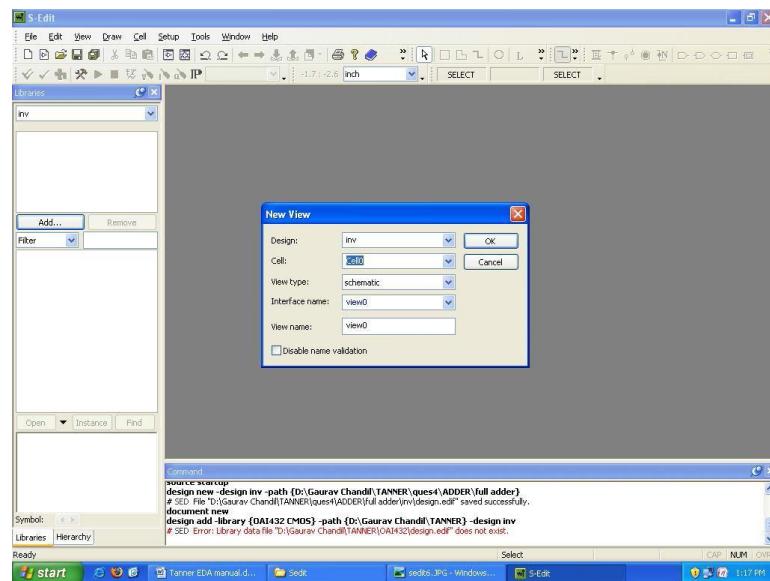
Design name should be changed only when you are going to design another circuit)

View type = schematic

Interface name = “by default”

View name = “by default”

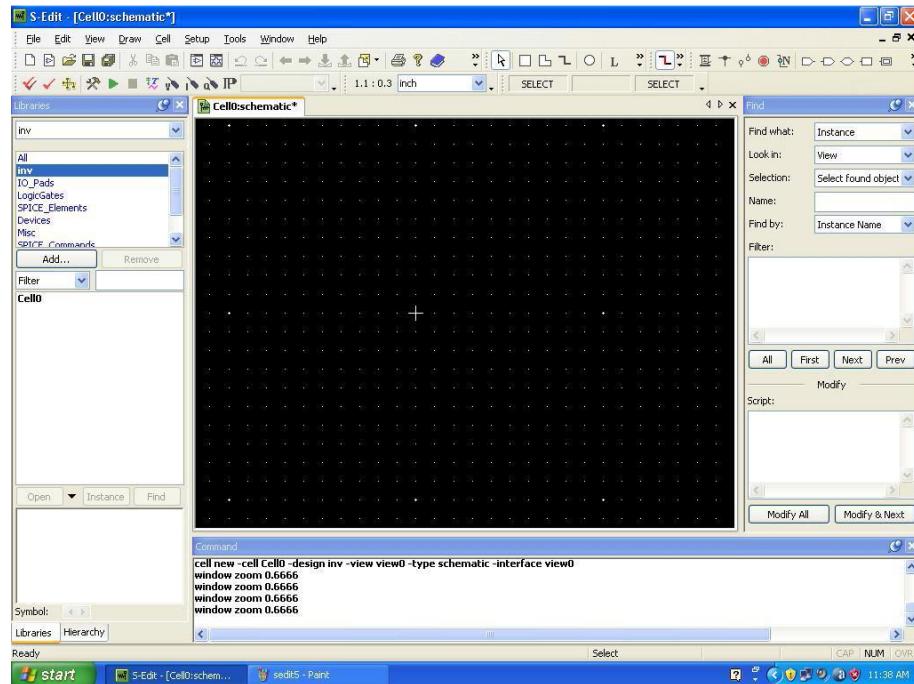
Then press “OK”.



Then a cell will be appeared where we can draw the schematic of any circuit.

In the black window you have seen some white bubble arranged in specific order. This is called grid. You can change grid distance by clicking on black screen and then scroll the mouse.

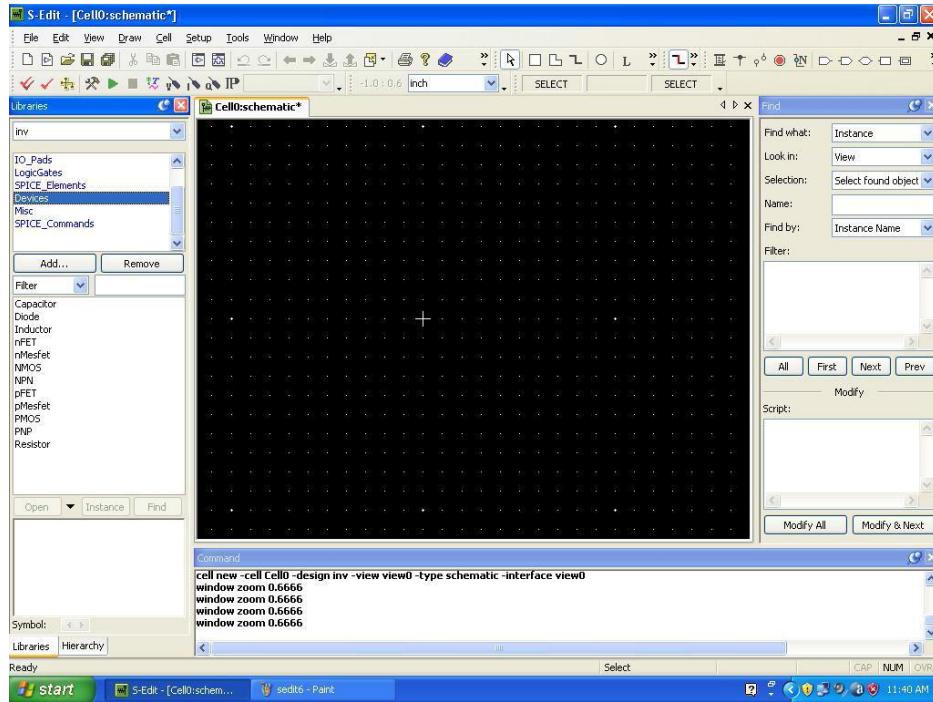
If you want your screen big enough for design space , then you can close the **Find & command window**. You can again bring these window from **view menu bar**.



To make any circuit schematic .

for example inverter

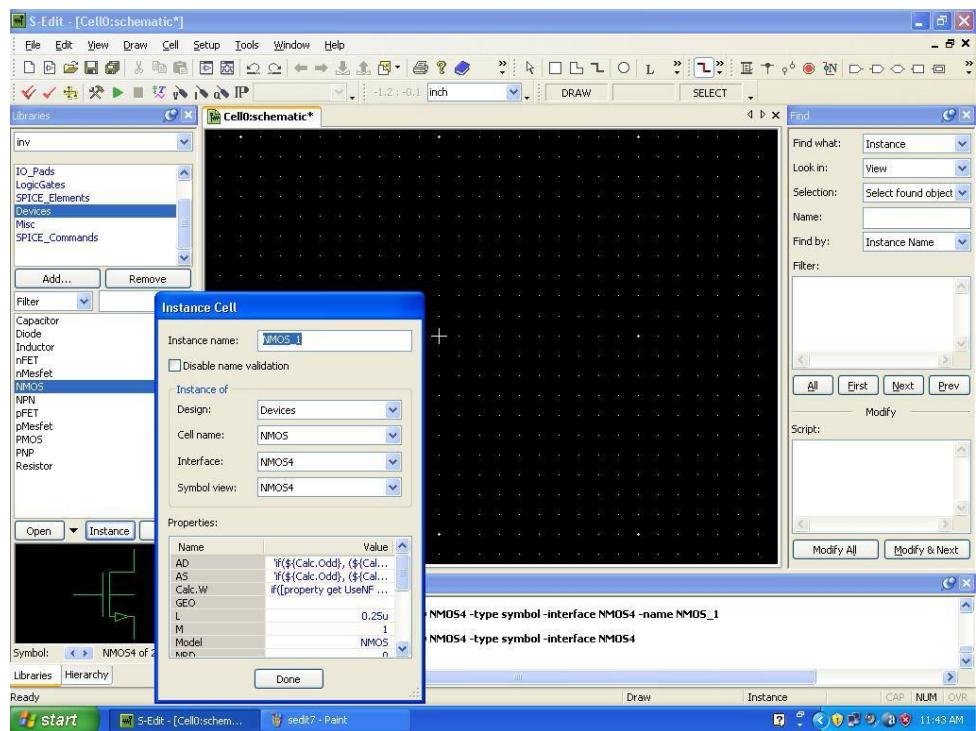
a) Go to >>libraries & click on device then all device will be open.



b) Select any device

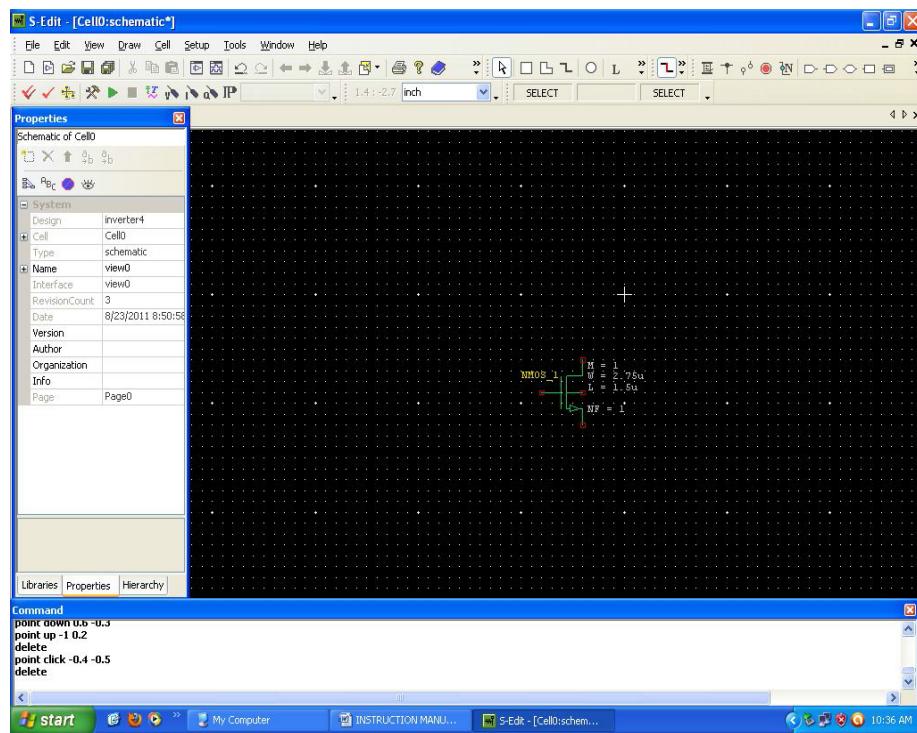
e.g. :- NMOS Device, then click on , instance

(then the dialog box instance cell will appear.)



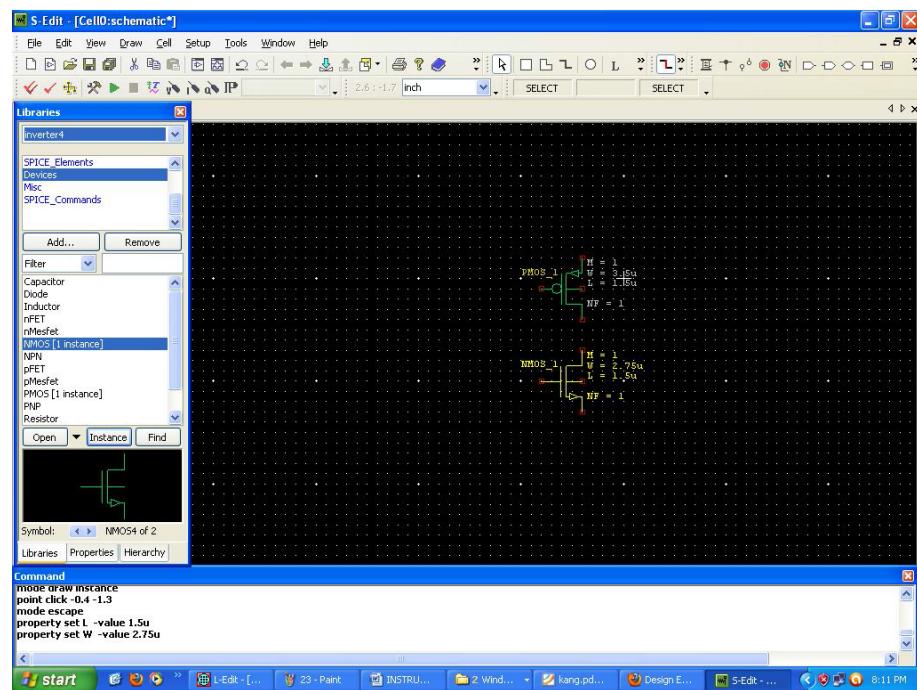
## In instance cell

- You can change the values of various device parameters according to your requirements.
  - Go to properties >> change the parameter values as your requirement.
  - Now before clicking **DONE** you have to DRAG the selected device into the cell and drop it where you want it to **FIX**.
- Then click **DONE** or press **ESC**.



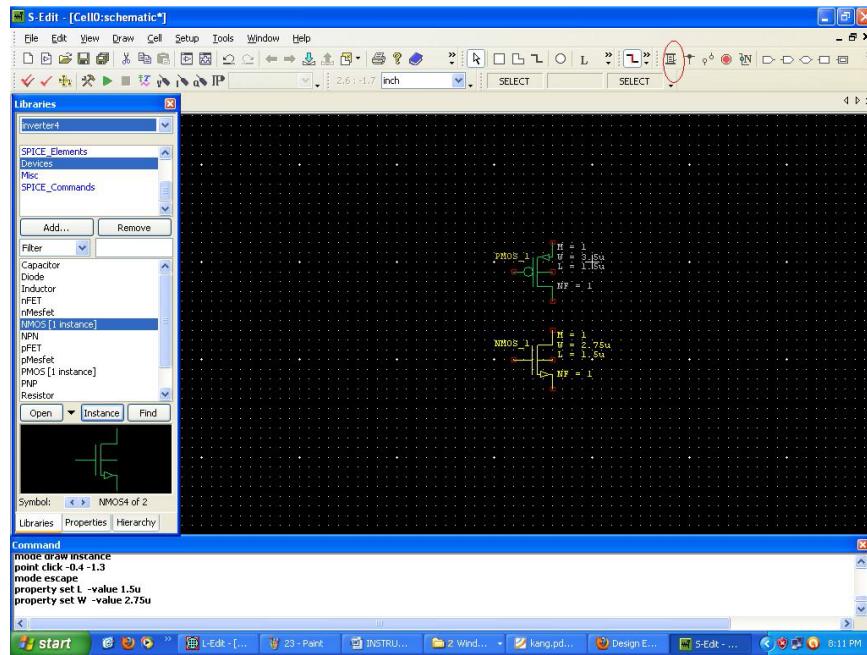
Similarly you can DRAG & DROP any device into the cell for draw your schematic circuit.

For inverter we need another Pmos.

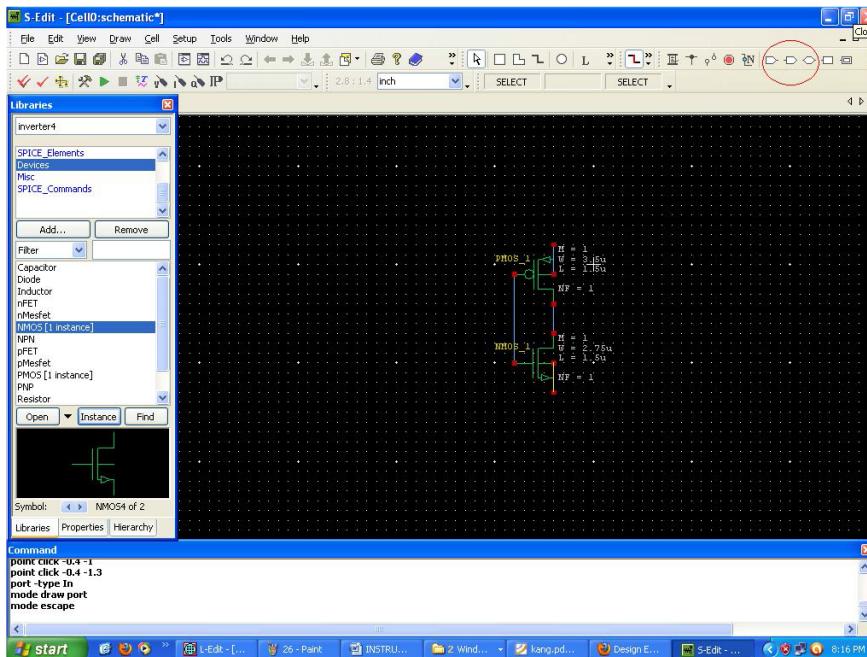


Now connect two device with wire.

Go to tool bar and select wire.

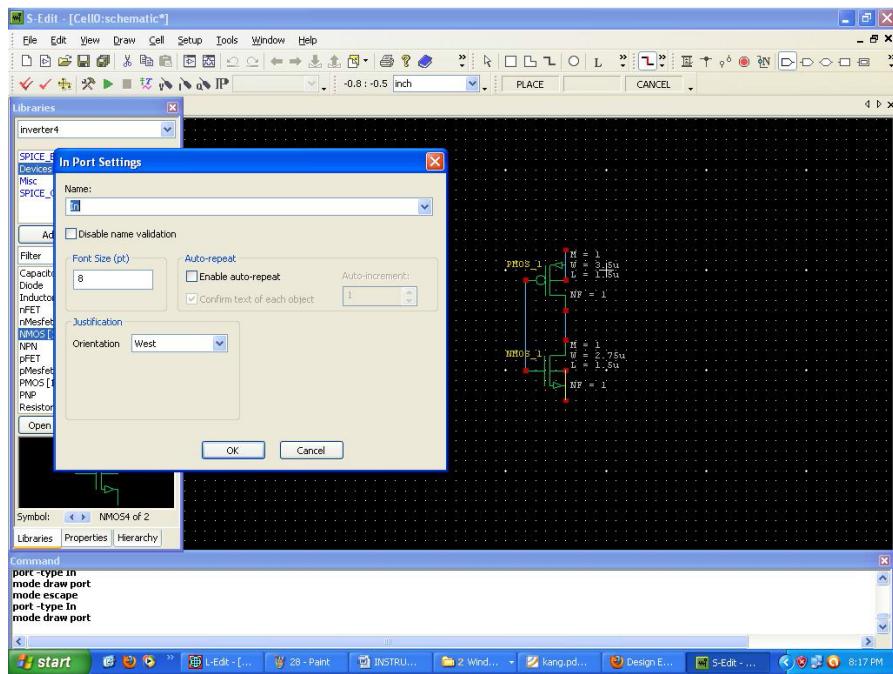


Similarly to give input & output port in the circuit , select input port that shown by red ellipse.



Now you can give Port name as you wish in the dialog box.

Then click OK

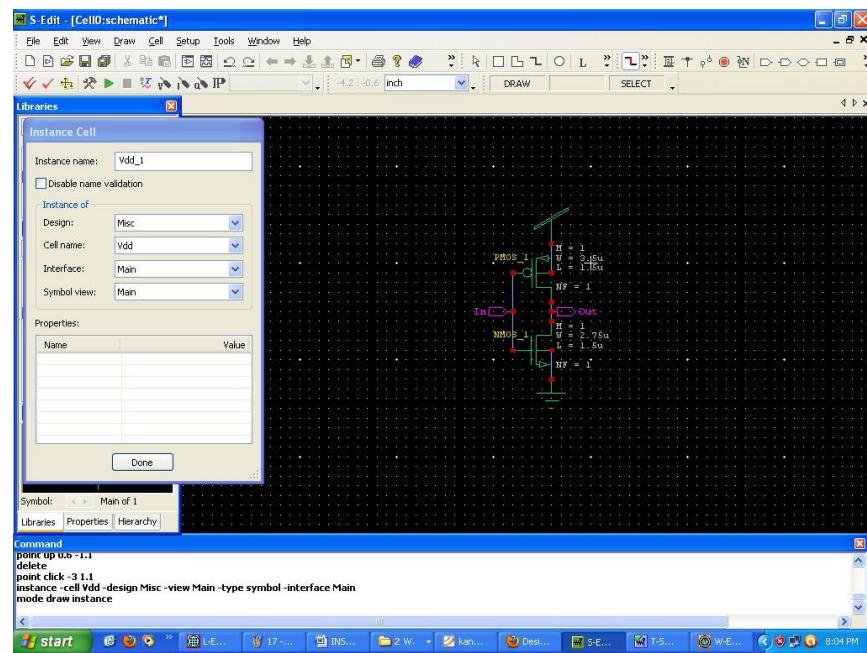


Similarly give Output Port name.

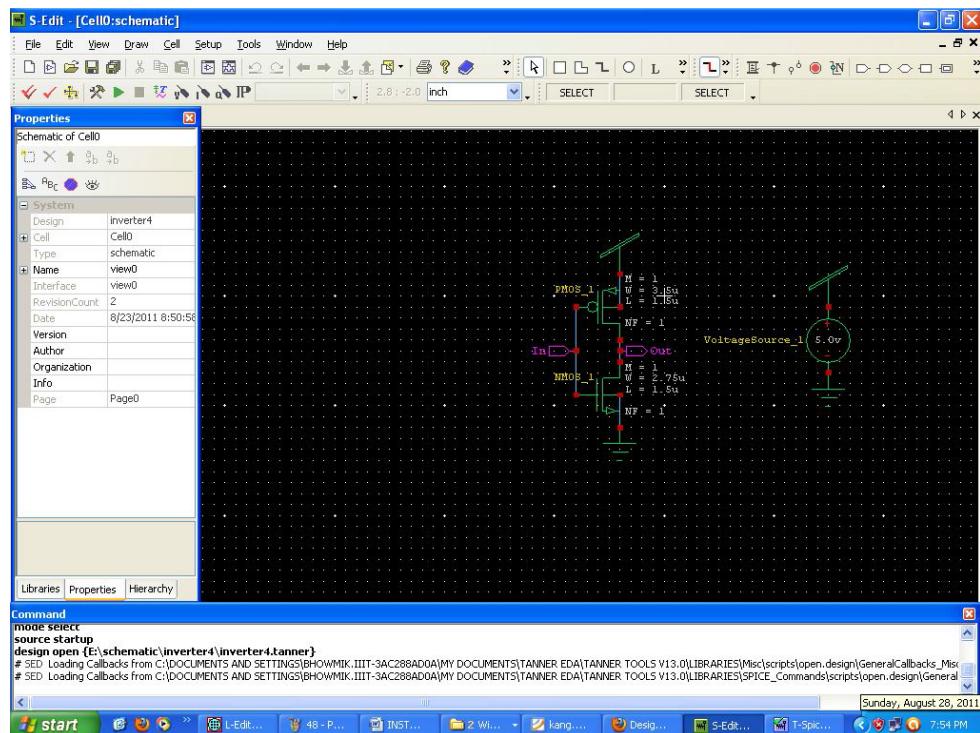
**NOTE :** you can rotate the port (short cut key “R”).

Now, after completed these steps, you should give the supply (VDD) & ground (GND).

For that Go to libraries >> MISC >>Select VDD or GND



Now you have to create a source of VDD. For that go to libraries >>spice\_element >> and then select voltage source of type DC . you can give any value in vdd .lets take vdd =5v.

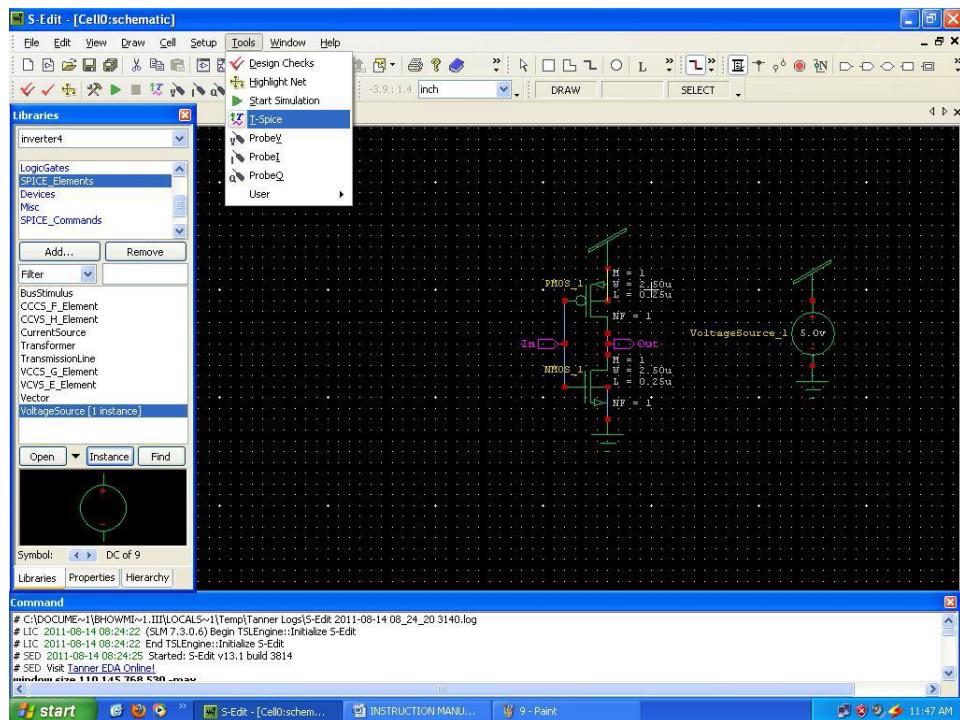


By doing all the above steps you have completed schematic of Inverter

### Pre layout simulation

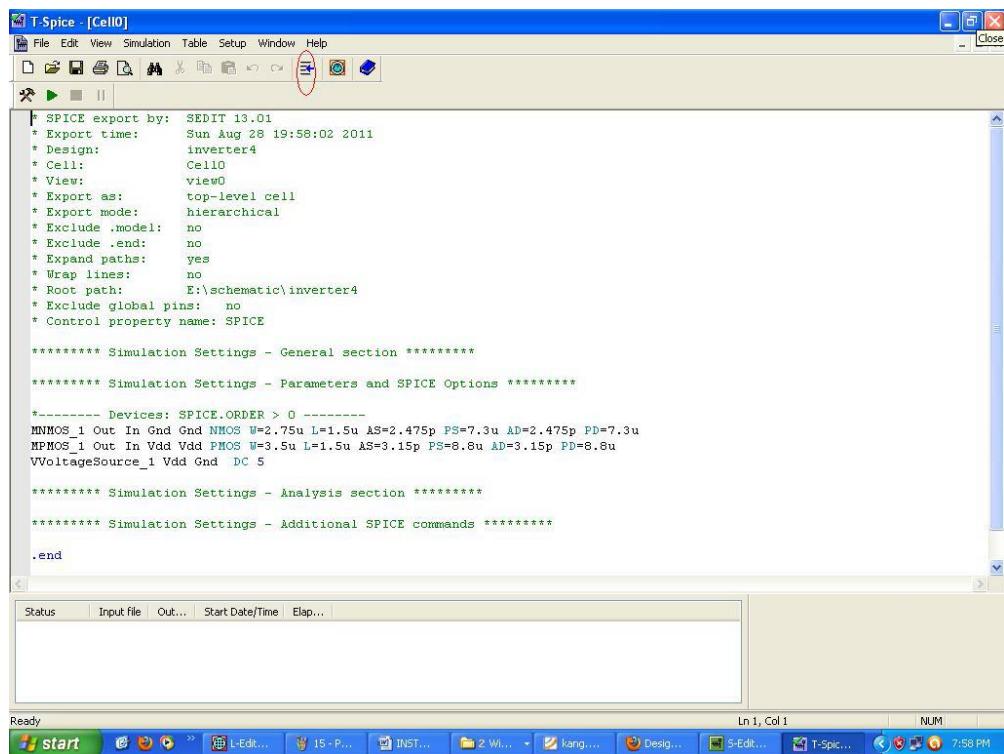
After schematic design you have to check whether your design match with the specification required or not . That's why you need to simulate the design which is called Pre layout simulation.

For simulation go to>> tools>> T-spice>> ‘ok’



A T-spice window will open.

Then click on the bar shown by red ellipse



```

T-Spice - [Cell0]
File Edit View Simulation Table Setup Window Help
[Icons] [Close]

* SPICE export by: SEDIT 13.01
* Export time: Sun Aug 28 19:58:02 2011
* Design: inverter4
* Cell: Cell0
* View: view0
* Export as: top-level cell
* Export mode: hierarchical
* Exclude .model: no
* Exclude .end: no
* Expand paths: yes
* Wrap lines: no
* Root path: E:\schematic\inverter4
* Exclude global pins: no
* Control property name: SPICE

***** Simulation Settings - General section *****

***** Simulation Settings - Parameters and SPICE Options *****

***** Devices: SPICE.ORDER > 0 *****
MNMOS_1 Out In Gnd Gnd NMOS W=2.75u L=1.5u AS=2.475p PS=7.3u AD=2.475p PD=7.3u
MPMOS_1 Out In Vdd Vdd PMOS W=3.5u L=1.5u AS=3.15p PS=8.8u AD=3.15p PD=8.8u
VVoltageSource_1 Vdd Gnd DC 5

***** Simulation Settings - Analysis section *****

***** Simulation Settings - Additional SPICE commands *****

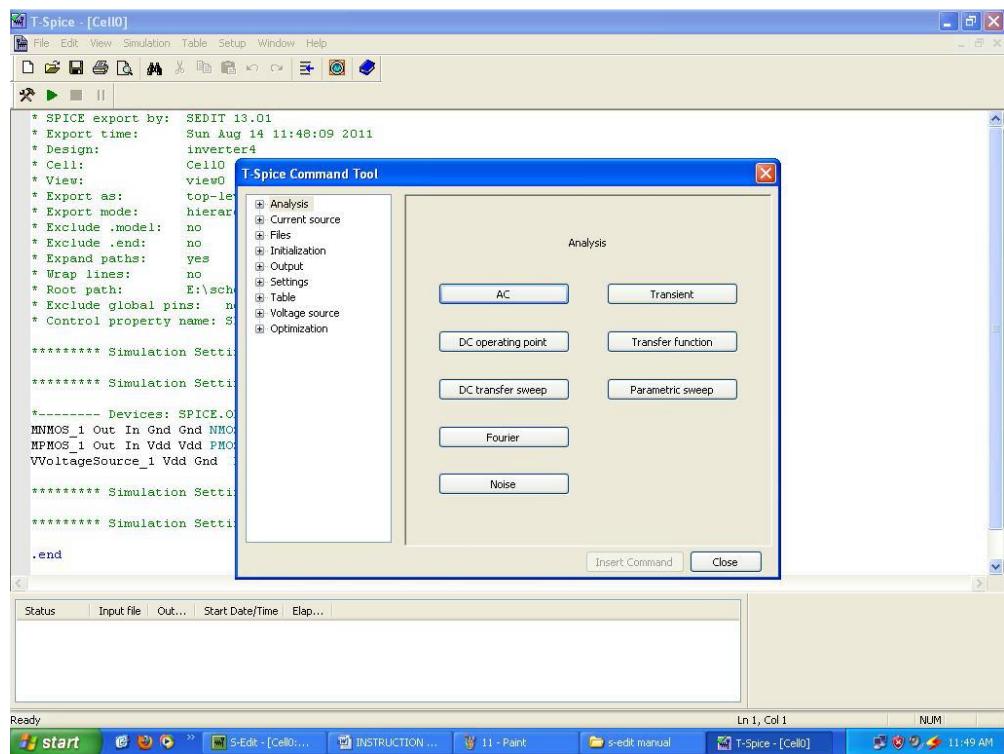
.end

```

Status Input file Out... Start Date/Time Elap... Ready Ln 1, Col 1 NUM

start I-Edit... 15 - P... INST... 2 Wi... Kang... Desig... S-Edit... T-Spice... 7:58 PM

A “T-spice command Tool “ dialog box will open as shown below.



On the T-spice command you can see in the left hand side  
 Analysis,  
 Current source  
 Files  
 Initialization,  
 Output  
 Settings  
 Table  
 Voltage source  
 Optimization

Lets start doing transient analysis of Inverter.

Step 1 : You have to include TSMC 0.25  $\mu\text{m}$  Technology file .

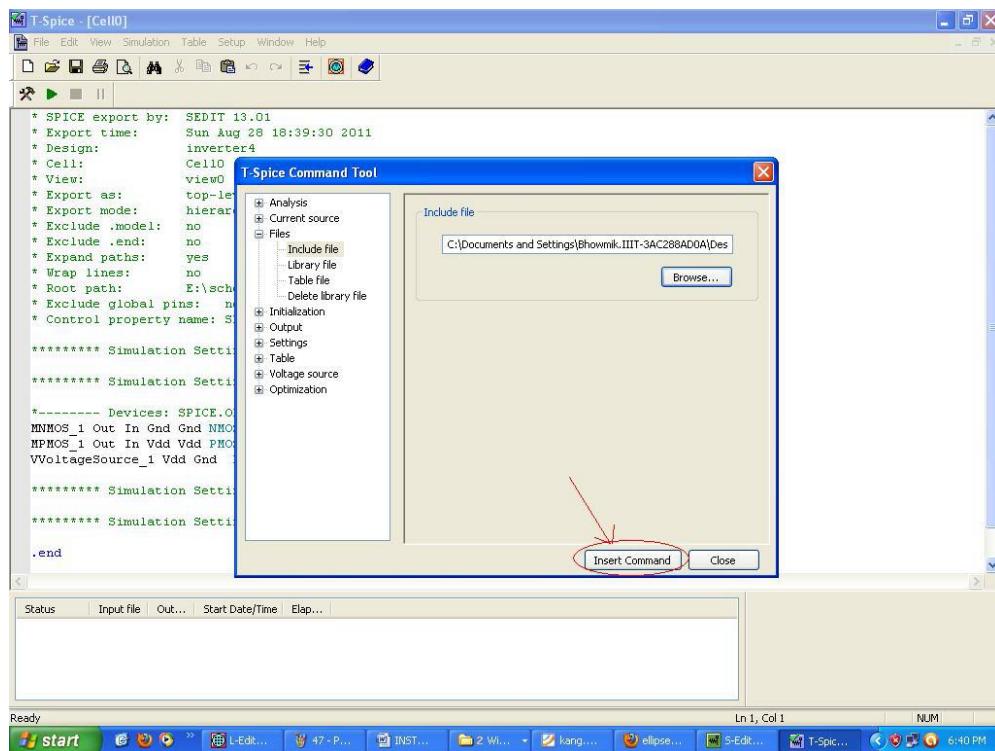
For that

Go to >> T-spice command tool >> Files >> Include >> browse TSMC .25 $\mu\text{m}$  files

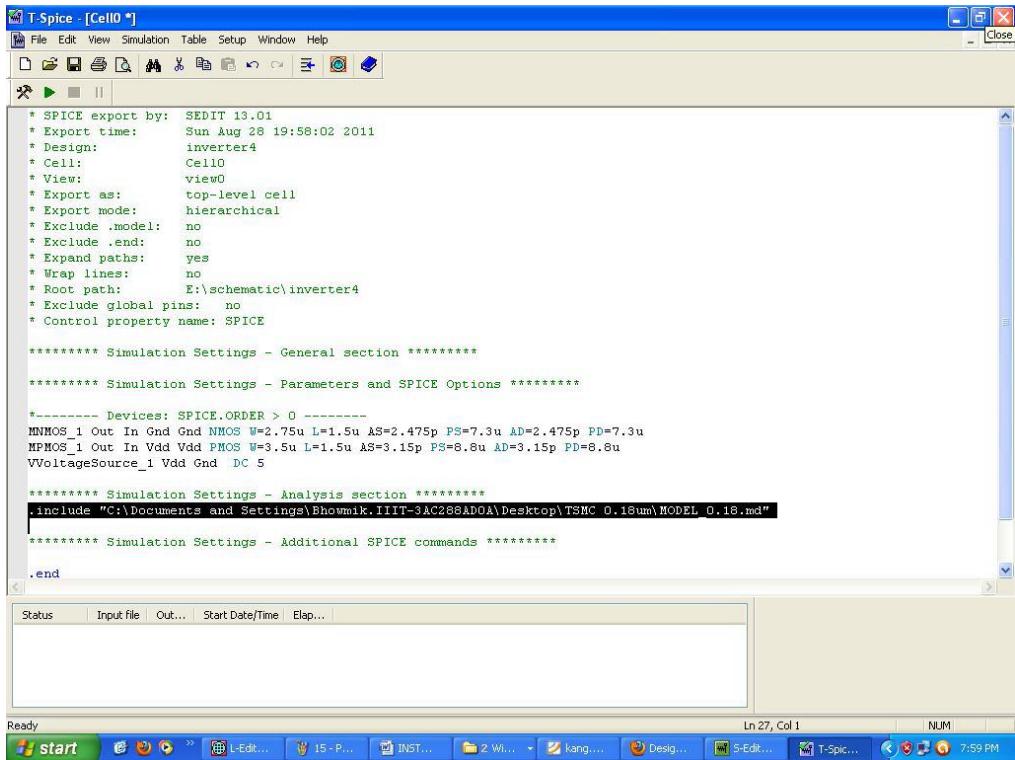
>> Insert command.

C:\Documents and Settings\Bhowmik.IIIT-3AC288AD0A\Desktop\TSMC

0.25um\MODEL\_0.25.md



File is included shown by highlight.



```
* SPICE export by: SEDIT 13.01
* Export time: Sun Aug 28 19:58:02 2011
* Design: inverter4
* Cell: Cell0
* View: view0
* Export as: top-level cell
* Export mode: hierarchical
* Exclude .model: no
* Exclude .end: no
* Expand paths: yes
* Wrap lines: no
* Root path: E:\schematic\inverter4
* Exclude global pins: no
* Control property name: SPICE

***** Simulation Settings - General section *****

***** Simulation Settings - Parameters and SPICE Options *****

----- Devices: SPICE.ORDER > 0 -----
NNMOS_1 Out In Gnd Gnd W=2.75u L=1.5u AS=2.475p PS=7.3u AD=2.475p PD=7.3u
MPMOS_1 Out In Vdd Vdd PMOS W=3.5u L=1.5u AS=3.15p PS=8.8u AD=3.15p PD=8.8u
VVoltageSource_1 Vdd Gnd DC 5

***** Simulation Settings - Analysis section *****
.include "C:\Documents and Settings\Bhowmik.IIIT-3AC288ADOA\Desktop\TSMC 0.18um\MODEL 0.18.md"

***** Simulation Settings - Additional SPICE commands *****

.end

Status | Input file | Out... | Start Date/Time | Elap...
Ready
```

Step2 : Then to give Input

T-spice command tool >> Voltage source >> select type of input you want to give(lets take **bit**) >> Insert command

Step 3: Analysis

T-spice command tool >> Analysis >> select type of analysis you want to give(lets take **transient**) >> Insert command

step 4: Output

T-spice command tool >> Output >> which output you want to see >> Insert Command

The total spice netlist will come like this.

T-Spice - [Cell0]

File Edit View Simulation Table Setup Window Help

Exclude .end: no  
 Expand paths: yes  
 Wrap lines: no  
 Root path: E:\schematic\inverter4  
 Exclude global pins: no  
 Control property name: SPICE

\*\*\*\*\* Simulation Settings - General section \*\*\*\*\*  
 \*\*\*\*\* Simulation Settings - Parameters and SPICE Options \*\*\*\*\*  
 \*\*\*\*\* Devices: SPICE\_ORDER > 0 \*\*\*\*\*  
 MNMOS\_1 Out In Gnd Gnd NMOS W=2.75u L=1.5u AS=2.475p PS=7.3u AD=2.475p PD=7.3u  
 PMOS\_1 Out In Vdd Vdd PMOS W=3.5u L=1.5u AS=3.15p PS=8.8u AD=3.15p PD=8.8u  
 VVoltageSource\_1 Vdd Gnd DC 5

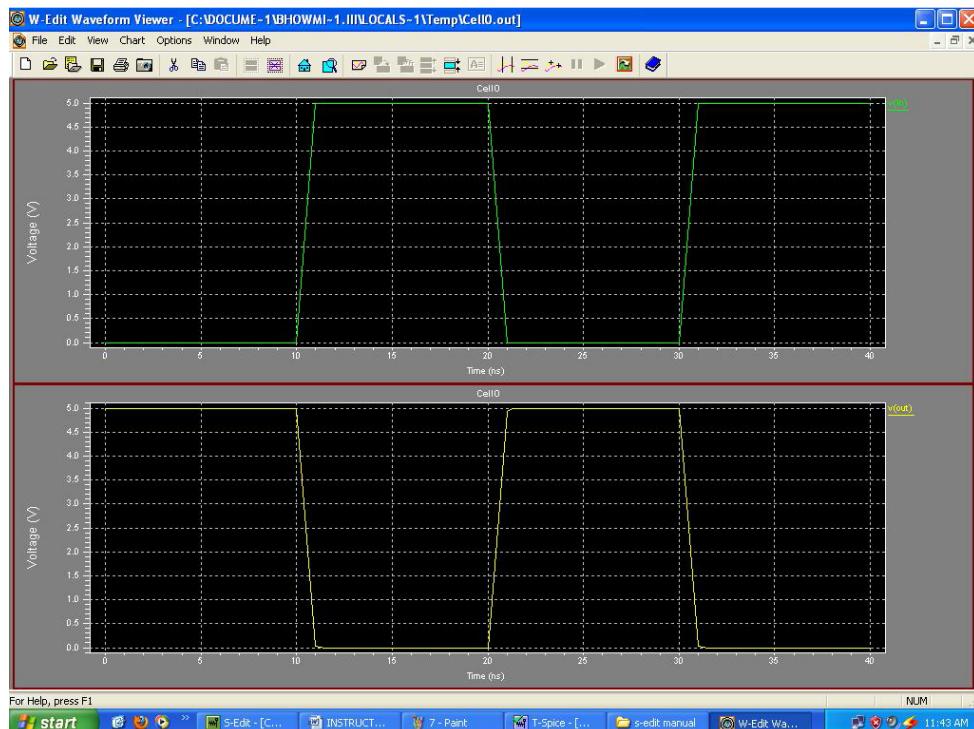
\*\*\*\*\* Simulation Settings - Analysis section \*\*\*\*\*  
 include "C:\Documents and Settings\Bhowmik.IIIT-3AC288ADOA\Desktop\TSMC 0.18um\MODEL\_0.18.mdf"  
 .v1 In Gnd Bit ((0101))  
 .tran 5n 40n  
 .print v(out) v(in)

\*\*\*\*\* Simulation Settings - Additional SPICE commands \*\*\*\*\*  
 .end

Status Input file Out... Start Date/Time Elap...  
 Finished Cell0.sp C... August 29, ... 00...

Now save it .

Then Run by clicking red ellipse shown on left above corner.Output of Pre layout simulation of Inverter



## **SIMULATION TOOL**

The tool used for simulation purpose for the entire research work is Tanner EDA tool version 13.0. The features and functionality of this tool has been described below:

### **SIMULATION TOOL**

The design cycle for the development of electronic circuits includes an important pre-fabrication verification phase. Because of the expense and time pressures associated with the fabrication step, accurate verification is crucial to efficient design. The role of EDA tool is to help design and verify a circuit's operation by numerically solving the differential equations describing the circuit. These simulation results allow circuit designers to verify and fine-tune designs before submitting them for fabrication. Tanner EDA tool is a complete circuit design and analysis system that includes:

- **Schematic Editor (S-Edit):** Schematic editor is a powerful design capture and analysis package that can generate netlist directly usable in T-Spice simulations.
- **T-Spice Circuit Simulator:** T-Spice performs fast and accurate simulation of analog and mixed analog/digital circuits. The simulator includes the latest and best device models available, as well as coupled line models and support for userdefined device models via tables or C functions. T-Spice uses an extended version of the SPICE input language that is compatible with all industry standard SPICE simulation programs. All of SPICE's device models are incorporated, as well as resistors, capacitors, inductors, mutual inductors, single and coupled transmission lines, current sources, voltage sources, controlled sources, and a full complement of the latest advanced semiconductor device models from Berkeley and Philips Labs.
- **Waveform Editor (W-Edit):** W-Edit displays T-Spice simulation output waveforms as they are being generated during simulation. Visualizing the complex numerical data resulting from VLSI circuit simulation is critical to testing, understanding, and improving those circuits. W-Edit is a waveform viewer that provides ease of use, power, and speed in a flexible environment designed for graphical data presentation.
- **Layout Editor (L-Edit):** Tanner EDA tool includes L-Edit for layout editing, • Interactive DRC for real-time design rule checking during editing, Standard DRC for hierarchical

DRC, Standard Extract for netlist extraction, Standard LVS for layout versus schematic, Node Highlighting for highlighting all geometry associated with a node and SPR for standard cell place & route.

## T-SPICE

To transform your ideas into designs, you must be able to simulate large circuits quickly and with a high degree of accuracy. That means you need a simulation tool that offers fast run times, integrates with your other design tools, and is compatible with industry standards. Tanner T-Spice Circuit Simulator puts you in control of simulation jobs with an easy-to-use graphical interface and a faster, more intuitive design environment. With key features such as multi-threading support, device state plotting, real-time waveform viewing and analysis, and a command wizard for simpler SPICE syntax creation, T-Spice saves you time and money during the simulation phase of your design flow.

T-Spice enables more accurate simulations by supporting the latest transistor models—including BSIM4 and the Penn State Philips (PSP) model. Given that T-Spice is compatible with a wide range of design solutions and runs on Windows and Linux platforms, it fits easily and cost effectively into your current tool flow.

T-Spice incorporates numerous innovations and improvements not found in other SPICE and SPICE-compatible simulators:

- **Speed:** T-Spice provides highly optimized code for evaluating device models, formulating the systems of linear equations, and solving those systems. In addition to the standard direct model evaluation, T-Spice also provides the option of table-base transistor model evaluation, in which the results of device model evaluations are stored in tables and reused. Because evaluation of device models can be computationally expensive, this technique can yield dramatic simulation speed increases.
- **Convergence:** T-Spice uses advanced mathematical methods to achieve superior numerical stability. Large circuits and feedback circuits, impossible to analyze with other SPICE products, can be simulated in T-Spice.
- **Accuracy:** T-Spice uses very accurate numerical methods and charge conservation to achieve superior simulation accuracy.

- **Macro modeling:** T-Spice simulates circuits containing “black box” macro devices. A macro device can directly use experimental data as its device model. Macro devices can also represent complex devices, such as logic gates, for which only the overall transfer characteristics, are of interest.
- **Input language extensions:** The T-Spice input language is an enriched version of the standard SPICE language. It contains many enhancements, including parameters, algebraic expressions, and a powerful bit and bus input wave specification syntax.
- **External model interface:** You can develop custom device models using C or C++.
- **Runtime waveform viewing:** The W-Edit waveform viewer displays graphical results during simulation. T-Spice analysis results for voltages, currents, charges, and power can be written to single or multiple files.

T-Spice also supports foundry extensions, including HSPICE foundry extensions to models.

- Supports PSP, BSIM3.3, BSIM4.6, BSIM SOI 4.0, EKV 2.6, MOS 9, 11, 20, 30, 31, 40, PSP, RPI a-Si & Poly-Si TFT, VBIC, Modella, and MEXTRAM models.
- Includes two stress effect models, from the Berkeley BSIM4 model and from TSMC processes, in the BSIM3 model to provide more accuracy in smaller geometry processes.
- Supports gate and body resistance networks in RF modeling.
- Performs non-quasi-static (NQS) modeling.
- Supports comprehensive geometry-based parasitic models for multi-finger devices.
- Models partially depleted, fully depleted, and unified FD-PD SOI devices.
- Models self-heating and RF resistor networks.
- Performs table-based modeling for using measured device data to model a device.
- Includes enhanced diode and temperature equations to improve compatibility with many foundry model libraries.

### **Work in a faster, easier design environment**

T-Spice helps integrate your design flow from schematic capture through simulation and waveform viewing. An easy-to-use point-and-click environment gives you complete control over the simulation process for greater efficiency and productivity.

- Enables easy creation of syntax-correct SPICE through a command wizard.

- Highlights SPICE Syntax through a text editor.
- Provides Fast, Accurate, and Precise options to enable optimal balance of accuracy and performance.
- Enables you to link from syntax errors to the SPICE deck by double clicking.
- Supports Verilog-A for analog behavioral modeling, allowing designers to prove system level designs before doing full device level design.
- Provides “.alter” command for easy what-if simulations with netlist changes.

### **Perform sophisticated analysis**

T-Spice uses superior numerical techniques to achieve convergence for circuits that are often impossible to simulate with other SPICE programs. The types of circuit analysis it performs include:

- DC and AC analysis.
- Transient analysis with Gear or trapezoidal integration.
- Enhanced noise analysis.
- Monte Carlo analysis over unlimited variables and trials with device and lot variations.
- Virtual measurements with functions for timing, error, and statistical analysis including common measurements such as delay, rise time, frequency, period, pulse width, settling time, and slew rate.
- Parameter sweeping using linear, log, discrete value, or external file data sweeps.
- 64-bit engine for increased capacity and higher performance.

### **With T-Spice, you can**

- Optimize designs with variables and multiple constraints by applying a Levenberg-Marquardt non-linear optimizer.
- Perform Safe Operating Area (SOA) checks to create robust designs.
- Use bit and bus logic waveform inputs.

### **Benefit from flexible licensing**

When you purchase a new design tool, licensing options can greatly affect your total cost of ownership. T-Spice is available in node-locked and networked configurations offering you the most flexible licensing possible. With a single solution, T-Spice will work whenever and wherever meeting the design needs of your main workgroup and remote workers. If you offshore design projects, T-Spice does not have geographic restriction on its licenses, thus, lowering your total cost of ownership.

## **SCHEMATIC EDITOR**

Schematic Editor (S-Edit) is an easy-to-use PC-based design environment for schematic capture. It gives you the power you need to handle your most complex full custom IC design capture. S-Edit is tightly integrated with Tanner EDA's T-Spice simulation, L-Edit layout, and HiPer verification tools. S-Edit helps you meet the demands of today's fast-paced market by optimizing your productivity and speeding your concepts to silicon. Its efficient design capture process integrates easily with third-party tools. S-Edit enables you to explore design choices and provides an easy-to-use view into the consequences of those choices. A faster design cycle gives you more flexibility in moving to an optimal solution—freeing up more time and resources for process corner validation. The results are less risk downstream, higher yield, and quicker time to market.

### **Schematic capture for the most complex full custom IC design**

- Bus support speeds the creation of mixed signal designs.
- Advanced array support enables easy creation and editing of memory, imaging, or circuits with repetitive blocks.
- Rubber band connectivity editing enables faster design modifications.
- S-Edit displays evaluated parameters in real time over the course of the design process. Parameters with formulas based on other circuit parameters can be displayed or evaluated.
- Auto symbol generation enables you to easily create symbols from schematics, and synchronize any changes.
- All actions are fully scriptable through the TCL/ Tk command language.

- Recordable scripts enable you to automate tasks or expand the tool for application-specific needs.
- Replay-able logs permit recovery if there is an unexpected network or hardware failure.
- S-Edit performs net highlighting and keeps the net highlighted as you move through the hierarchy.
- Cross probe from SPICE net lists and LVS to highlighting nets or devices.
- Schematic ERC enables you to check your design for common errors such as undriven nets, unconnected pins and multiple output pins connected together. The design checks are fully configurable, including custom validation scripts.

### **Tight integration with simulation**

- S-Edit is tightly integrated with simulation. You can drive the simulator from within the schematic capture environment, viewing operating point results directly on the schematic and performing waveform cross-probing to view node voltages and device terminal currents or charges.
- S-Edit creates an efficient flow for the iterative loop of design, simulation, analysis, and tweaking of circuit parameters. The IC designer can focus on the design and not on data processing—thereby speeding up the design process.

### **Easy interoperability with third party tools and legacy data**

- S-Edit imports schematics via EDIF from third party tools, including Cadence®, Mentor, Laker and View Draw with automatic conversion of schematics and properties for seamless integration of legacy data.
- Net lists can be exported in flexible, user-configurable formats, including SPICE and CDL variants, EDIF, structural Verilog, and structural VHDL.
- Library support in S-Edit maximizes the reuse of IP developed in previous projects, or imported from third-party vendors.

### **Powerful and easy-to-use interface**

- S-Edit brings to front-end design capture the ease-of-use and design productivity for which Tanner Tools are known.
- A fully user-programmable design environment allows you to remap hotkeys, create new toolbars, and customize the view to your preference—all in a streamlined GUI.

- The complete user interface is available in multiple languages. S-Edit currently supports English, Japanese, Simplified and Traditional Chinese.
- S-Edit provides Unicode support. All user data can be entered in international character sets.

### **Cost-effective**

- S-Edit provides an ideal performance to-cost ratio, allowing you to maximize the number of designers on a project.
- Since S-Edit is Windows-based, designers can work on cost-effective workstations or laptops. This means you can take your work with you anywhere—even home—and continue working to meet time-to-market pressures.
- Available in two configurations—full schematic editor, and schematic viewer.

### **Easy to manage**

- Human-readable technology files and design databases are revision-control system-compatible.
- CAD managers can control distribution and access rights to the technology or design. The format allows revision control systems to manage revisions over the course of the design process.

### **Benefit from flexible licensing**

When you purchase a new design tool, licensing options can greatly affect your total cost of ownership. S-Edit is available in node-locked and networked configurations offering you the most flexible licensing possible. With a single solution, S-Edit will work whenever and wherever meeting the design needs of your main workgroup and remote workers. If you offshore design projects, S-Edit does not have geographic restriction on its licenses, thus, lowering your total cost of ownership.

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