

SIVARAM PADMASOLA

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[Github](#) [Linkedin](#) [Website](#)

OBJECTIVE

Being a researcher in the field of VLSI and/or semiconductors.

EDUCATION

Bachelor of Engineering, Electronics and Communication Engineering Expected August 2024

Birla Institute of Technology and Sciences, Pilani – Hyderabad Campus

- Relevant Coursework: Analog and Digital VLSI Design, Microelectronic Circuits, Electronic Devices, Digital Design, Modelling of Field Effect Nano Devices, Computer Architecture, Analog Electronics, FPGA-based System Design Lab, Microprocessor Programming and Interfacing

12th Grade graduation (SSC certification) Completed June 2020
FIITJEE Junior College, Miyapur

10th Grade graduation (CBSE certification) Completed June 2018
CHIREC International School, Kondapur

SKILLS & ABILITIES

Programming Languages

- C/C++, Python, Java, Verilog, Assembly (8086 instruction set)

Software and environments

- MATLAB and Code Composer Studio
- LTSPICE, HSPICE and Vivado
- Rizin and Ghidra

EXPERIENCE

Summer intern May 2022 to July 2022

Shris Infotech Pvt Ltd, Hyderabad

- Developed a C/C++ implementation of `at_lookup` and `/ or at_client` (without persistence) at a minimum allowing a C/C++ programmer to create application code.
- Done for [The Atsign Foundation](#)

PROJECT AND RESEARCH WORK

Design of Ternary Logic Circuits

- Ongoing academic coursework project (informal) under [Dr. Syed Ershad Ahmed](#)
- Design of Ternary Logic Circuits is done using CNTFETs in HSPICE

[Design and Fabrication of 3 dB 180-degree Hybrid Coupler](#)

- Completed academic coursework project under [Dr. Harish V Dixit](#)
- Design was done in AWR Microwave Office using FR-4 substrate

[Music Genre Predictor](#) using transfer learning

- Completed academic coursework project under [Dr. Paresh Saxena](#)
- Improvement was done on an existing project using Mixup Training and Test Time Augmentation

Ongoing coursework project for FPGA-based System Design Lab