Chapter 2
Introduction

This section provides high-level descriptions of the modules available on the devices covered by this document.

2.1 Introduction

The KW39/38/37 wireless microcontrollers (MCU), which includes the KW39, KW38 and KW37 families of devices, are highly integrated single-chip devices that enable Bluetooth Low Energy (Bluetooth LE) and Generic FSK connectivity for automotive and industrial embedded systems. To meet the stringent requirements of automotive applications, the KW39/38/37 is fully AEC Q100 Grade 2 Automotive Qualified. The target applications center on wirelessly bridging the embedded world with mobile devices to enhance the human interface experience, share embedded data between devices and the cloud and enable wireless firmware updates. Leading the automotive applications is the Digital Key, where a smartphone can be used by the owner as an alternative to the key FOB for unlocking and personalizing the driving experience. For a car sharing experience, the owner can provide selective, temporary authorization for access to the car allowing the authorized person to unlock, start and operate the car using their mobile device using Bluetooth LE.

The KW39/38/37 Wireless MCU integrates an Arm® Cortex®-M0+ CPU with up to 512 KB flash and 64 KB SRAM and a 2.4 GHz radio that supports Bluetooth LE 5.0 and Generic FSK modulations. The Bluetooth LE radio supports up to 8 simultaneous connections in any master/slave combination.

The KW38 includes an integrated FlexCAN module enabling seamless integration into a cars in-vehicle or industrial CAN communication network. The FlexCAN module can support CAN's flexible data-rate (CAN FD) protocol for increased bandwidth and lower latency required by many automotive applications.

The KW39/38/37 devices can be used as a "BlackBox" modem in order to add Bluetooth LE or Generic FSK connectivity to an existing host MCU or MPU (microprocessor), or may be used as a standalone smart wireless sensor with embedded application where no host controller is required.

The RF circuit of the KW39/38/37 is optimized to require very few external components, achieving the smallest RF footprint possible on a printed circuit board. Extremely long battery life is achieved through the efficiency of code execution in the Cortex-M0+ CPU core and the multiple low power operating modes of the KW39/38/37. For power critical applications, an integrated DC-DC converter enables operation from a single coin cell or Li-ion battery with a significant reduction of peak receive and transmit current consumption.

2.2 Block Diagram

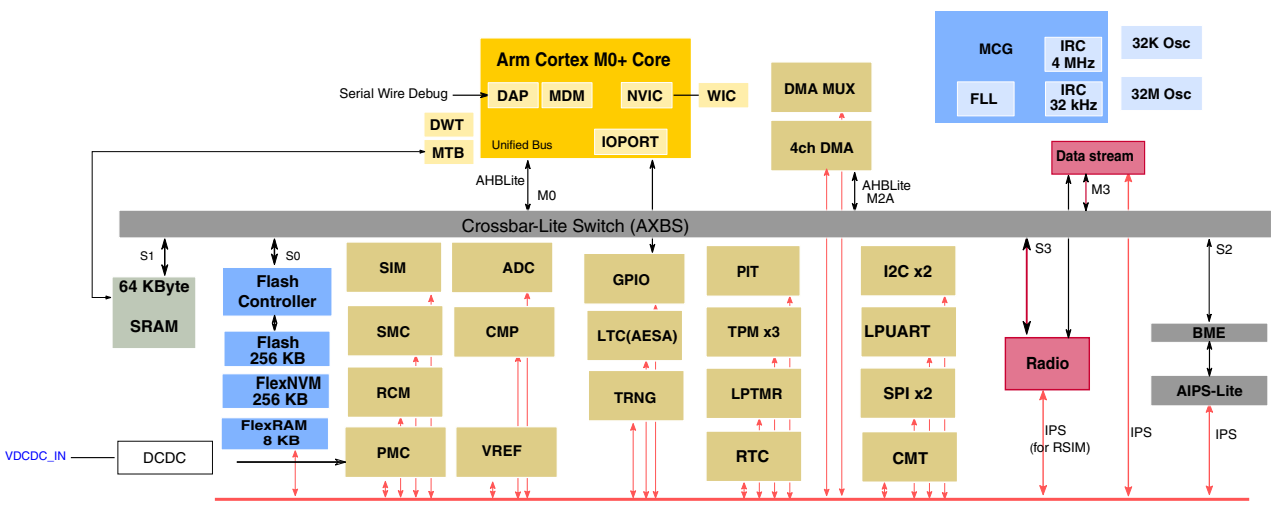

Figure 2-1. KW39 Detailed Block Diagram

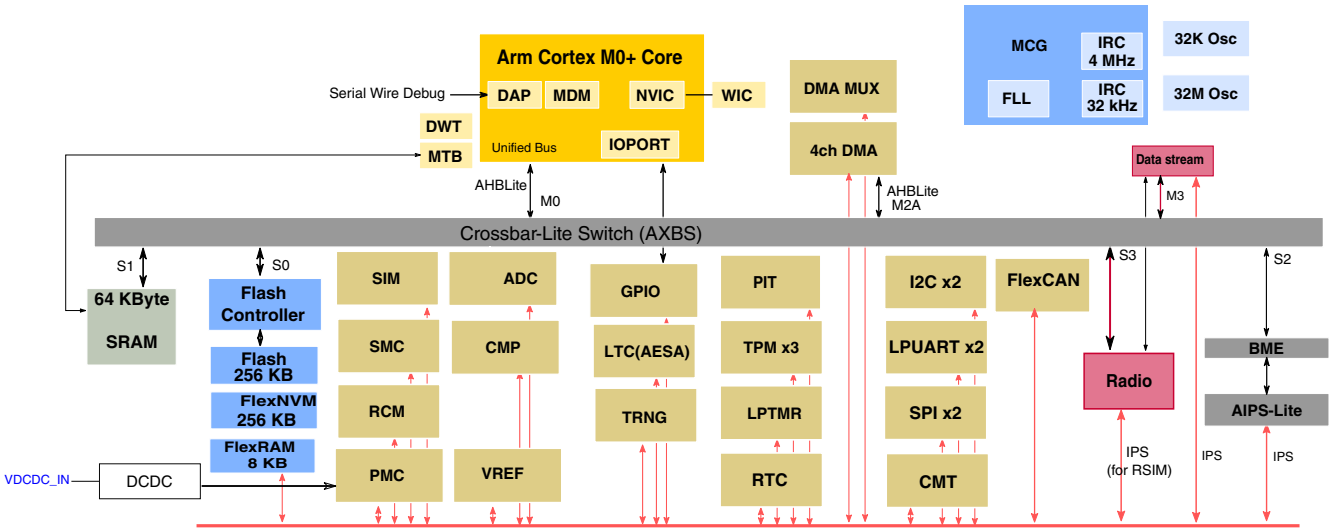

Figure 2-2. KW38 Detailed Block Diagram

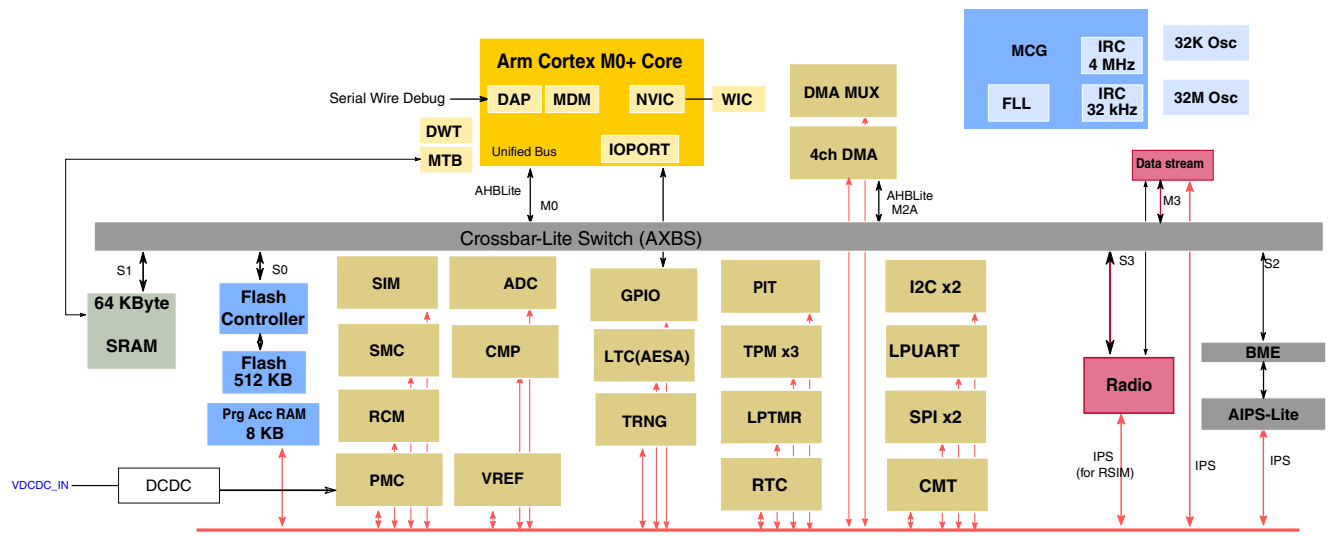

Figure 2-3. KW37 Detailed Block Diagram

Table 2-1. List of IPs in block diagrams

Acronym	Definition
ADC	Analog-to-Digital Converter
AESA	Advanced Encryption Standard Accelerator
AIPS	Peripheral Bridge
BME	Bit Manipulation Engine
CMP	Comparator
CMT	Carrier Modulator Timer
DAP	Debug Access Port
DMA	Direct Memory Access

Table continues on the next page...

Table 2-1. List of IPs in block diagrams (continued)

Acronym	Definition
DMAMUX	Direct Memory Access Multiplexer
DWT	Data Watchpoint and Trace
FLL	Frequency-Locked Loop
GPIO	General Purpose Input/Output
I2C	Inter-integrated Circuit
IRC	Internal Reference Clock
LPTMR	Low-Power Timer
LPUART	Low-Power UART
LTC	LP Trusted Cryptography
MCG	Multipurpose Clock Generator
MDM	Miscellaneous Debug Module
MTB	Micro Trace Buffer
NVIC	Nested Vectored Interrupt Controller
OSC	Oscillator
PIT	Periodic Interrupt Timer
PMC	Power Management Control
PORT	Port Control and Interrupt
Prg Acc RAM	Flash Programming Acceleration RAM
RCM	Reset Control Module
RSIM	Radio System Integration Module
RTC	Real-Time Clock
SIM	System Integration Module
SMC	System Mode Controller
SPI	Serial Peripheral Interface
TRNG	True Random Number Generator
VREF	Voltage Reference

2.3 Feature Summary

The following table lists the features integrated on device.

Table 2-2. Feature Summary

Feature	Device
Hardware Characteristics	
Package	48-pin HVQFN (7 X 7 mm, 0.5 mm pitch) with wettable flanks
Voltage range	DCDC in Buck configurations supports 2.1 V to 3.6 V
	Bypass configuration: 1.71 V to 3.6 V (1.45-3.6 V for RF and OSC supplies)

Table continues on the next page...

Table 2-2. Feature Summary (continued)

Feature	Device
Temperature range	T_A: -40° C to +105° C T_J: -40° C to +125° C
System	
Central processing unit (CPU)	Arm Cortex-M0+ core (32-bit)
Max. CPU frequency	48 MHz (4 MHz in VLPR mode)
Max. Bus frequency	24 MHz (1 MHz in VLPR mode)
Nested vectored Interrupt controller (NVIC)	32 vectored interrupts 4 programmable interrupt priority levels
Low Power Modes	Wait, Stop and Partial Stop Compute operation mode Very low power run (VLPR), wait (VLPW), and stop (VLPS) Low Leakage Stop (LLS3, LLS2) Very Low Leakage Stop (VLLS3,VLLS2, VLLS1, VLLS0)
DMA	4 channel eDMA
DMA request multiplex	Yes Supports up to 64 DMA requests
Low-leakage Wakeup Unit (LLWU)	External wake-up pins with digital glitch filter as well as internal wake-up sources
Non-maskable interrupt (NMI)	Yes
Software COP (COP)	Yes
Debug and Trace	2-pin serial wire debug (SWD) Micro trace buffer (MTB) + Data Watchpoint and Trace (DWT)
Unique Identification (ID) Numbers	80-bit unique device ID Additional 40-bit unique value for creating MAC address
Memory	
Flash memory	KW39/38 sub-family: 256 KB P-Flash with ECC, 256 KB FlexNVM, and 8 KB FlexRAM KW37 sub-family: 2 x 256 KB P-Flash with ECC and 8 KB Program Acceleration RAM
Random-access memory (RAM)	64 KB
System Register File	32 bytes
Clocks	
Reference crystal oscillator or resonator	Crystal reference oscillator, ability to bypass oscillator with external clock. Supports 26 MHz or 32 MHz crystals
32 kHz External crystal oscillator	Supports 32 kHz or 32.768 kHz crystal/resonator, or external 32/32.768kHz clock
Internal clock references	31.25 to 39.063 kHz oscillator with ±3% max. deviation across temperature 4 MHz oscillator with ±11% max. deviation across temperature 1 kHz oscillator
Frequency-locked loop (FLL)	20 - 48 MHz
Human-Machine Interface (HMI)	
General-purpose input/output (GPIO)	Default to disabled (no leakage) Hysteresis and configurable pull up/down device on all input pins

Table continues on the next page...

Table 2-2. Feature Summary (continued)

Feature	Device
	Configurable drive strength and/or slew rate on some pins up to 12 pins (package dependent) with 20 mA high current drive ability Single cycle GPIO control via IOPORT
General Purpose Analog	
Power management controller (PMC)	Low voltage warning and detect with selectable trip points 1 kHz LPO
16-bit analog-to-digital converter (ADC)	5 pure single end input channels, plus either one single end input channel (DP) or a pair of differential input channel (DP/DM) Linear successive approximation algorithm Internal Temp Sensor and Battery Monitor DMA support
High speed comparator (HSCMP) with internal 6-bit digital-to-analog converter (DAC)	Up to 5 external channels
Voltage Reference(VREF1)	Supply an accurate 1.2 V voltage output
Timers	
16-bit TPM timer (LPTPM x3)	One 4-channel without quadrature decode Two 2-channel with quadrature decode basic Timer/Pulse-Width Modulator (TPM) function PWM generation built in
32-bit Programmable interrupt timer (PIT)	2 channel
Real-time clock (RTC)	32-bit seconds counter 16-bit prescaler with compensation
Low-power Timer (LPTMR)	1-channel, 16-bit pulse counter or periodic interrupt functional in all power modes
Communication Interfaces	
Serial peripheral interface (2x SPI)	Two SPI with 4-entry TX/CMD and RX FIFOs Master mode and slave mode functions Supports multiple chip selects in master mode Programmable transfer lengths DMA Support
Inter-Integrated Circuit (2x I2C)	Two I2C modules
Low power universal asynchronous receiver/transmitter (2x LPUART)	Two LPUART modules for KW38 and one LPUART module for KW37 and KW39 Supports LIN break detection Tx pin pseudo open drain with enable/disable programmable configurable x4 to x32 oversampling Functional in STOP/VLPS modes Hardware Flow Control (RTS/CTS)

Table continues on the next page...

Table 2-2. Feature Summary (continued)

Feature	Device
	DMA Support
Carrier Modulation Timer (CMT)	Direct drive of IR LED
FlexCAN	Includes a CAN (FlexCAN0) module that supports Flexible Data-rate (CAN FD) feature (supported in KW38 only)
Radio	
Operating Frequency range	ISM: 2400 - 2483.5 MHz MBAN: 2360 - 2400 MHz
Antenna and RF match support	Support for External, PCB and Ceramic chip antenna
Common Rx/Tx antenna terminals	Use 1 single end pin for Rx and Tx
Extended range options	Capable of supporting an external PA of +30 dB gain Supports +10 dB external LNA Supports AoA/AoD
Security Support	
Encryption	AES-128 Accelerator supporting ECB, CBC, CTR, CCM and CCM*, CMAC, and XCBC-MAC modes
TRNG	True Random Number Generator
ESD/EFT	
Human Body Model (HBM) JEDEC STD 2, method A114	>+ / -2000 V All package pins,including RF pins.
Charge Device Model (CDM) JEDEC STD 2, method C101	+ / -500 V All package pins,including RF pins.

2.4 Features Overview

The following section lists the features of the devices.

32-bit Cortex M0+ (enhanced M0) Central Processor Unit (CPU)

- Up to 48 MHz core frequency across temperature range of –40 °C to 105 °C
- Supports up to 32 interrupt request sources
- 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Bit Manipulation Engine (BME) for improved bit handling of peripheral modules
- Binary compatible instruction set architecture with the Cortex M0+ core
- Thumb instruction set combines high code density with 32-bit performance
- Serial Wire Debug (SWD) reduces the number of pins required for debugging
- Micro Trace Buffer (MTB) provides lightweight program trace capabilities using system RAM as the destination memory

Input Voltage operation

- DCDC in Buck configuration supports 2.1 V to 3.6 V
- Bypass Mode 1.71 V to 3.6 V (1.5 V - 3.6 V for the RF and 32 MHz OSC supplies)

On-chip Memory

- 512 KB of flash memory (KW39/38 has 1x256 KB flash plus 1x256 KB FlexNVM that can execute program code, store data or back up emulated EEPROM data and KW37 has 2x256 KB flash), read/program/erase over full operating voltage and temperature
- 64 KB of Low Power Random access memory (SRAM), memory retention in most low power modes
- Security circuitry to prevent unauthorized access to SRAM and Flash contents

Power-Saving

- Multiple power modes including low leakage state-retention and memory-retention modes
- Peripheral clock enable registers can disable clocks to unused modules, reducing currents

System Clock Source Options

- Reference Oscillator — crystal reference oscillator supporting 32 MHz or 26 MHz crystals
- 32 kHz Oscillator — 32.768 kHz crystal reference oscillator
- Multipurpose Clock Generator(MCG)
  - Frequency-locked loop (FLL) controlled by internal or external reference
    - 20 MHz to 48 MHz FLL output
  - Internal reference clocks — Can be used as a clock source for other on-chip peripherals
    - On-chip RC oscillator range of 31.25 kHz to 39.0625 kHz with 3% accuracy across full temperature range
    - On-chip 4 MHz oscillator with 11% accuracy across full temperature range

System Protection

- Standard Watchdog reset with option to run from dedicated 1 kHz internal clock source or bus clock
- Low-voltage detection with reset or interrupt; selectable trip points
- HardFault exception on attempts to execute undefined instructions or access to undefined memory space
- LOCKUP reset resource from core

- Flash Read\Write protection
- Firmware distribution protection: Flash can be marked execute-only on a per-segment (8 KB in KW39/38/37) basis to prevent firmware contents from being read by third parties.

Development Support

- Two-wire Serial Wire Debug interface
- Breakpoint unit supporting up to 2 hardware breakpoints
- Watchpoint unit supporting up to 2 watchpoints
- Micro Trace Buffer provides program trace capabilities

Peripherals

- DMA — 4-channel DMA. Bus master provides very configurable source-to-destination data movement capabilities supporting either software-triggered or peripheral-paced transfers.
- ADC — up to 5 external channels, 16-bit resolution analog-to-digit converter, fully functional in the entire voltage range. Performance for the ADC depends on package pinout.
- VREF — Voltage reference supply accurate voltage output that can be trimmed in 0.5 mV steps
- HSCMP — high speed comparator with internal 6-bit DAC
- PIT — 2-channel 32-bit timer module that can be used to assert interrupts or to provide one more time base
- LPTPM — One 4-channel, and two 2-channel; Basic TPM function. Timer/Pulse-Width Modulator Module supporting input capture, output compare.
- LPTMR — Low Power Timer that can wakeup CPU from all low power modes
- RTC — Robust 32-bit Real Timer Clock with hardware compensation
- CMT — Carrier Modulation Timer used to drive IR communications
- AESA — AES-128 Accelerator with DMA support
- TRNG — True Random Number Generator
- LPUART — Serial Communication Interface with DMA support and hardware flow control (RTS\CTS). Supports LIN break detection. KW38 has two LPUARTs and KW39/37 has one LPUART.
- SPI — Two Serial Peripheral Interfaces with DMA support
- I2C — Two Inter-Integrated Circuit modules with SMBUS 2.0 and DMA support
- GPIO — Port interrupt capability on all the GPIO pins
- FlexCAN — Includes a CAN (FlexCAN0) module that supports Flexible Data-rate (CAN FD) feature (supported in KW38 only)

Radio

- 2.4GHz ISM band (2400-2483.5 MHz) and MBAN 2360-2400 MHz operation

- Supported Standards
  - Bluetooth Low Energy 5
  - Generic FSK modulation capability
- Bluetooth Low Energy Link Layer hardware supporting up to 8 simultaneous connections in any master/slave combination
- 26 MHz or 32 MHz crystal reference oscillator
- Generic FSK Link Layer hardware
- Single RF port shared by both transmit and receive
- Low external component count
- Supports external PA and LNA
- Supports AoA/AoD

NOTE

Refer to the latest version of product datasheet for receiver and transmitter performance and other specifications.

2.5 Orderable Part Numbers

Table 2-3. KW39/38/37 Part Numbers

Device	Qualification Tier	CAN FD	512 KB P-Flash	256 KB P-FLASH/256 KB FlexNVM	Second LPUART with LIN	8 KB FlexRAM EEPROM	Package
MKW39A512VFT4	Auto AEC-Q100 Grade 2	N	N	Y	N	Y	7X7 mm 48-pin "Wettable" HVQFN
MKW38A512VFT4	Auto AEC-Q100 Grade 2	Y	N	Y	Y	Y	
MKW38Z512VFT4	Industrial	Y	N	Y	Y	Y	
MKW37A512VFT4	Auto AEC-Q100 Grade 2	N	Y	N	N	N	
MKW37Z512VFT4	Industrial	N	Y	N	N	N	

Chapter 3
Signal Multiplexing and Pin Assignment

3.1 Signal Multiplexing and Signal Descriptions

This section illustrates which of this device's signals are multiplexed on which external pin.

3.2 KW39/37 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control and Interrupt module is used to select the functionality for each GPIO pin. ALT0 is reserved for analog functions on some GPIO pins. ALT1 – ALT9 are assigned to the available digital functions on each GPIO pin. GPIO pins with a default of "disabled" are high impedance after reset – their input and output buffers are disabled.

48 "Wettable" HVQFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
1	PTA0	SWD_DIO		PTA0/ RF_ACTIVE	SPI0_PCS1			TPM1_CH0		SWD_DIO		
2	PTA1	SWD_CLK		PTA1/ RF_STATUS	SPI1_PCS0			TPM1_CH1		SWD_CLK		
3	PTA2	RESET_b		PTA2				TPM0_CH3		RESET_b		
4	PTA16	DISABLED		PTA16/ LLWU_P4	SPI1_SOUT			TPM0_CH0				
5	PTA17	DISABLED		PTA17/ LLWU_P5	SPI1_SIN			TPM_ CLKIN1				
6	PTA18	DISABLED		PTA18/ LLWU_P6	SPI1_SCK			TPM2_CH0				
7	PTA19	ADC0_SE5	ADC0_SE5	PTA19/ LLWU_P7	SPI1_PCS0			TPM2_CH1				
8	PSWITCH	PSWITCH	PSWITCH									

48 "Wettable" HVQFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
9	DCDC_CFG/ VDCDC_IN	DCDC_CFG/ VDCDC_IN	DCDC_CFG/ VDCDC_IN									
10	DCDC_LP	DCDC_LP	DCDC_LP									
11	DCDC_GND	DCDC_GND	DCDC_GND									
12	DCDC_LN	DCDC_LN	DCDC_LN									
13	VDD_ 1P8OUT	VDD_ 1P8OUT	VDD_ 1P8OUT									
14	DCDC_LN	DCDC_LN	DCDC_LN									
15	VDD_ 1P5OUT_ PMCIN	VDD_ 1P5OUT_ PMCIN	VDD_ 1P5OUT_ PMCIN									
16	PTB0	DISABLED		PTB0/ LLWU_P8/ RF_RFOSC_ EN		I2C0_SCL	CMP0_OUT	TPM0_CH1		CLKOUT		
17	PTB1	ADC0_SE1/ CMP0_IN5	ADC0_SE1/ CMP0_IN5	PTB1/ RF_ PRIORITY	DTM_RX	I2C0_SDA	LPTMR0_ ALT1	TPM0_CH2		CMT_IRO		
18	PTB2	ADC0_SE3/ CMP0_IN3	ADC0_SE3/ CMP0_IN3	PTB2/ RF_NOT_ ALLOWED/ LLWU_P9		DTM_TX	TPM0_CH0	TPM1_CH0			TPM2_CH0	
19	PTB3	ADC0_SE2/ CMP0_IN4	ADC0_SE2/ CMP0_IN4	PTB3/ ERCLK32K/ RF_ACTIVE		TPM0_CH1	CLKOUT	TPM1_CH1		RTC_ CLKOUT	TPM2_CH1	
20	VDD_0	VDD_0	VDD_0									
21	PTB16	EXTAL32K	EXTAL32K	PTB16		I2C1_SCL		TPM2_CH0				
22	PTB17	XTAL32K	XTAL32K	PTB17		I2C1_SDA		TPM2_CH1				
23	PTB18	NMI_b	ADC0_SE4/ CMP0_IN2	PTB18		I2C1_SCL	TPM_ CLKIN0	TPM0_CH0		NMI_b		
24	ADC0_DP0	ADC0_DP0/ CMP0_IN0	ADC0_DP0/ CMP0_IN0									
25	ADC0_DM0	ADC0_DM0/ CMP0_IN1	ADC0_DM0/ CMP0_IN1									
26	VREFL/ VSSA	VREFL/ VSSA	VREFL/ VSSA									
27	VREFH/ VREF_OUT	VREFH/ VREF_OUT	VREFH/ VREF_OUT									
28	VDDA	VDDA	VDDA									
29	XTAL_OUT	XTAL_OUT	XTAL_OUT									
30	EXTAL	EXTAL	EXTAL									
31	XTAL	XTAL	XTAL									
32	VDD_RF3	VDD_RF3	VDD_RF3									
33	ANT	ANT	ANT									

48 "Wettable" HVQFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
34	GANT	GANT	GANT									
35	VDD_RF2	VDD_RF2	VDD_RF2									
36	VDD_RF1	VDD_RF1	VDD_RF1									
37	PTC1	DISABLED		PTC1/ RF_EARLY_ WARNING	ANT_B	I2C0_SDA	LPUART0_ RTS_b	TPM0_CH2			SPI1_SCK	
38	PTC2	DISABLED		PTC2/ LLWU_P10	TX_SWITCH	I2C1_SCL	LPUART0_ RX	CMT_IRO		DTM_RX	SPI1_SOUT	
39	PTC3	DISABLED		PTC3/ LLWU_P11	RX_SWITCH	I2C1_SDA	LPUART0_ TX	TPM0_CH1		DTM_TX	SPI1_SIN	
40	PTC4	DISABLED		PTC4/ LLWU_P12/ RF_ACTIVE	ANT_A	EXTRG_IN	LPUART0_ CTS_b	TPM1_CH0		I2C0_SCL	SPI1_PCS0	
41	PTC5	DISABLED		PTC5/ LLWU_P13/ RF_NOT_ ALLOWED/ RF_ PRIORITY		LPTMR0_ ALT2	LPUART0_ RTS_b	TPM1_CH1				
42	PTC6	DISABLED		PTC6/ LLWU_P14/ RF_RFOSC_ EN		I2C1_SCL	LPUART0_ RX	TPM2_CH0				
43	PTC7	DISABLED		PTC7/ LLWU_P15	SPI0_PCS2	I2C1_SDA	LPUART0_ TX	TPM2_CH1				
44	VDD_1	VDD_1	VDD_1									
45	PTC16	DISABLED		PTC16/ LLWU_P0/ RF_STATUS	SPI0_SCK	I2C0_SDA	LPUART0_ RTS_b	TPM0_CH3				
46	PTC17	DISABLED		PTC17/ LLWU_P1/ RF_EXT_ OSC_EN	SPI0_SOUT	I2C1_SCL	LPUART0_ RX			DTM_RX		
47	PTC18	DISABLED		PTC18/ LLWU_P2	SPI0_SIN	I2C1_SDA	LPUART0_ TX			DTM_TX		
48	PTC19	DISABLED		PTC19/ LLWU_P3/ RF_EARLY_ WARNING	SPI0_PCS0	I2C0_SCL	LPUART0_ CTS_b					
49	Ground	NA										

3.3 KW38 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control and Interrupt module is used to select the functionality for each GPIO pin. ALT0 is reserved for analog functions on some GPIO pins. ALT1 – ALT9 are assigned to the available digital functions on each GPIO pin. GPIO pins with a default of “disabled” are high impedance after reset – their input and output buffers are disabled.

48 "Wettable" HVQFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
1	PTA0	SWD_DIO		PTA0/ RF_ACTIVE	SPI0_PCS1			TPM1_CH0		SWD_DIO		
2	PTA1	SWD_CLK		PTA1/ RF_STATUS	SPI1_PCS0			TPM1_CH1		SWD_CLK		
3	PTA2	RESET_b		PTA2				TPM0_CH3		RESET_b		
4	PTA16	DISABLED		PTA16/ LLWU_P4	SPI1_SOUT	LPUART1_ RTS_b		TPM0_CH0				
5	PTA17	DISABLED		PTA17/ LLWU_P5	SPI1_SIN	LPUART1_ RX	CAN0_TX	TPM_ CLKIN1				
6	PTA18	DISABLED		PTA18/ LLWU_P6	SPI1_SCK	LPUART1_ TX	CAN0_RX	TPM2_CH0				
7	PTA19	ADC0_SE5	ADC0_SE5	PTA19/ LLWU_P7	SPI1_PCS0	LPUART1_ CTS_b		TPM2_CH1				
8	PSWITCH	PSWITCH	PSWITCH									
9	DCDC_CFG/ VDCDC_IN	DCDC_CFG/ VDCDC_IN	DCDC_CFG/ VDCDC_IN									
10	DCDC_LP	DCDC_LP	DCDC_LP									
11	DCDC_GND	DCDC_GND	DCDC_GND									
12	DCDC_LN	DCDC_LN	DCDC_LN									
13	VDD_ 1P8OUT	VDD_ 1P8OUT	VDD_ 1P8OUT									
14	DCDC_LN	DCDC_LN	DCDC_LN									
15	VDD_ 1P5OUT_ PMCIN	VDD_ 1P5OUT_ PMCIN	VDD_ 1P5OUT_ PMCIN									
16	PTB0	DISABLED		PTB0/ LLWU_P8/ RF_RFOSC_ EN		I2C0_SCL	CMP0_OUT	TPM0_CH1		CLKOUT	CAN0_TX	
17	PTB1	ADC0_SE1/ CMP0_IN5	ADC0_SE1/ CMP0_IN5	PTB1/ RF_ PRIORITY	DTM_RX	I2C0_SDA	LPTMR0_ ALT1	TPM0_CH2		CMT_IRO	CAN0_RX	

48 "Wettable" HVQFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
18	PTB2	ADC0_SE3/ CMP0_IN3	ADC0_SE3/ CMP0_IN3	PTB2/ RF_NOT_ ALLOWED/ LLWU_P9		DTM_TX	TPM0_CH0	TPM1_CH0			TPM2_CH0	
19	PTB3	ADC0_SE2/ CMP0_IN4	ADC0_SE2/ CMP0_IN4	PTB3/ ERCLK32K/ RF_ACTIVE	LPUART1_ RTS_b	TPM0_CH1	CLKOUT	TPM1_CH1		RTC_ CLKOUT	TPM2_CH1	
20	VDD_0	VDD_0	VDD_0									
21	PTB16	EXTAL32K	EXTAL32K	PTB16	LPUART1_ RX	I2C1_SCL		TPM2_CH0				
22	PTB17	XTAL32K	XTAL32K	PTB17	LPUART1_ TX	I2C1_SDA		TPM2_CH1				
23	PTB18	NMI_b	ADC0_SE4/ CMP0_IN2	PTB18	LPUART1_ CTS_b	I2C1_SCL	TPM_ CLKIN0	TPM0_CH0		NMI_b		
24	ADC0_DP0	ADC0_DP0/ CMP0_IN0	ADC0_DP0/ CMP0_IN0									
25	ADC0_DM0	ADC0_DM0/ CMP0_IN1	ADC0_DM0/ CMP0_IN1									
26	VREFL/ VSSA	VREFL/ VSSA	VREFL/ VSSA									
27	VREFH/ VREF_OUT	VREFH/ VREF_OUT	VREFH/ VREF_OUT									
28	VDDA	VDDA	VDDA									
29	XTAL_OUT	XTAL_OUT	XTAL_OUT									
30	EXTAL	EXTAL	EXTAL									
31	XTAL	XTAL	XTAL									
32	VDD_RF3	VDD_RF3	VDD_RF3									
33	ANT	ANT	ANT									
34	GANT	GANT	GANT									
35	VDD_RF2	VDD_RF2	VDD_RF2									
36	VDD_RF1	VDD_RF1	VDD_RF1									
37	PTC1	DISABLED		PTC1/ RF_EARLY_ WARNING	ANT_B	I2C0_SDA	LPUART0_ RTS_b	TPM0_CH2			SPI1_SCK	
38	PTC2	DISABLED		PTC2/ LLWU_P10	TX_SWITCH	I2C1_SCL	LPUART0_ RX	CMT_IRO		DTM_RX	SPI1_SOUT	
39	PTC3	DISABLED		PTC3/ LLWU_P11	RX_SWITCH	I2C1_SDA	LPUART0_ TX	TPM0_CH1		DTM_TX	SPI1_SIN	CAN0_TX
40	PTC4	DISABLED		PTC4/ LLWU_P12/ RF_ACTIVE	ANT_A	EXTRG_IN	LPUART0_ CTS_b	TPM1_CH0		I2C0_SCL	SPI1_PCS0	CAN0_RX
41	PTC5	DISABLED		PTC5/ LLWU_P13/ RF_NOT_ ALLOWED/		LPTMR0_ ALT2	LPUART0_ RTS_b	TPM1_CH1				

48 "Wettable" HVQFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	ALT8	ALT9
				RF_PRIORITY								
42	PTC6	DISABLED		PTC6/LLWU_P14/RF_RFOSC_EN		I2C1_SCL	LPUART0_RX	TPM2_CH0				
43	PTC7	DISABLED		PTC7/LLWU_P15	SPI0_PCS2	I2C1_SDA	LPUART0_TX	TPM2_CH1				
44	VDD_1	VDD_1	VDD_1									
45	PTC16	DISABLED		PTC16/LLWU_P0/RF_STATUS	SPI0_SCK	I2C0_SDA	LPUART0_RTS_b	TPM0_CH3			LPUART1_RTS_b	
46	PTC17	DISABLED		PTC17/LLWU_P1/RF_EXT_OSC_EN	SPI0_SOUT	I2C1_SCL	LPUART0_RX			DTM_RX	LPUART1_RX	
47	PTC18	DISABLED		PTC18/LLWU_P2	SPI0_SIN	I2C1_SDA	LPUART0_TX			DTM_TX	LPUART1_TX	
48	PTC19	DISABLED		PTC19/LLWU_P3/RF_EARLY_WARNING	SPI0_PCS0	I2C0_SCL	LPUART0_CTS_b				LPUART1_CTS_b	
49	Ground	NA										

3.4 KW39/38/37 Pinouts

KW39/38/37 device pinouts are shown in the figure below.

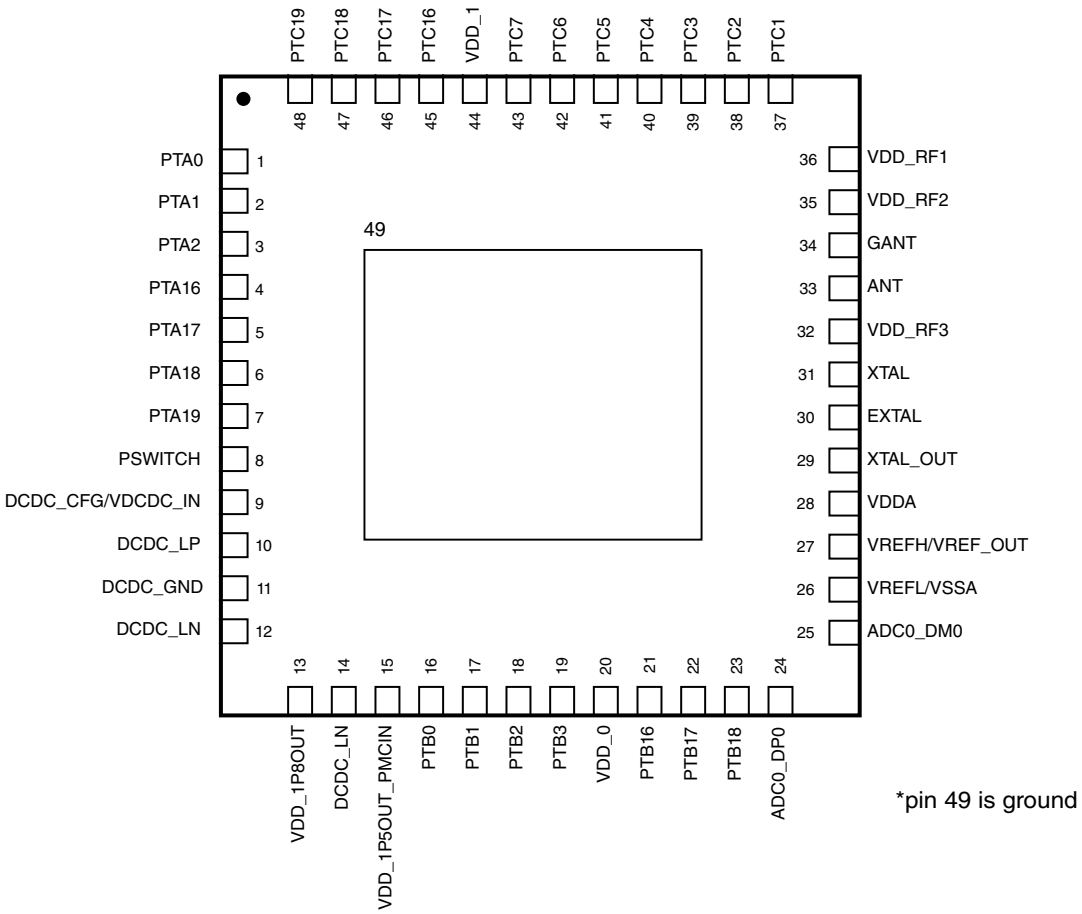

Figure 3-1. 48-pin "Wettable" HVQFN pinout diagram

3.5 KW39/38/37 Signal Descriptions

Table 3-1. KW39/38/37 Signal Descriptions

Signal Name	Description	Type
ADC0_DM0	ADC Channel 0 Differential Input Negative	A
ADC0_DP0	ADC Channel 0 Differential Input Positive	A
ADC0_SE1	ADC Channel 0 Single-ended Input 1	A
ADC0_SE2	ADC Channel 0 Single-ended Input 2	A

Table continues on the next page...

Table 3-1. KW39/38/37 Signal Descriptions (continued)

Signal Name	Description	Type
ADC0_SE3	ADC Channel 0 Single-ended Input 3	A
ADC0_SE4	ADC Channel 0 Single-ended Input 4	A
ADC0_SE5	ADC Channel 0 Single-ended Input 5	A
ANT	Antenna	A
ANT_A	Antenna selection A for Front End Module support	D
ANT_B	Antenna selection B for Front End Module support	D
RF_ACTIVE	Signal to indicate future Radio activity.	D
CLKOUT	Internal Clocks Monitoring	D
CMP0_IN0	Comparator0 Input 0	A
CMP0_IN1	Comparator0 Input 0	A
CMP0_IN2	Comparator0 Input 0	A
CMP0_IN3	Comparator0 Input 0	A
CMP0_IN4	Comparator0 Input 0	A
CMP0_IN5	Comparator0 Input 0	A
CMP0_OUT	Comparator0 Output	D
CMT_IRO	Carrier Modulator Transmitter Infrared Output	D
DCDC_CFG	DCDC Switch Mode Select	D
DCDC_GND	DCDC Switch Ground	G
DCDC_LN	DCDC Switch Inductor Input Negative	A
DCDC_LP	DCDC Switch Inductor Input Positive	A
DTM_RX	Direct Test Mode Receive	D
DTM_TX	Direct Test Mode Transmit	D
EXTAL	26 MHz or 32 MHz Crystal Input	A
EXTAL32K	32kHz Crystal Input	A
EXTRG_IN	TPM or ADC External Trigger Input	D
GANT	Antenna ground	A
I2C0_SCL	I2C0 SCL	D
I2C0_SDA	I2C0 SDA	D
I2C1_SCL	I2C1 SCL	D
I2C1_SDA	I2C1 SDA	D
LPTMR0_ALT1	Low Power Timer0 ALT1	D
LPTMR0_ALT2	Low Power Timer0 ALT2	D
NMI_b	Non Maskable Interrupt Request	D
PSWITCH	DCDC Switch Enable	D
PTA0	GPIO Port A0	D
PTA1	GPIO Port A1	D
PTA16	GPIO Port A16	D
PTA17	GPIO Port A17	D
PTA18	GPIO Port A18	D

Table continues on the next page...

Table 3-1. KW39/38/37 Signal Descriptions (continued)

Signal Name	Description	Type
PTA19	GPIO Port A19	D
PTA2	GPIO Port A2	D
PTB0	GPIO Port B0	D
PTB1	GPIO Port B1	D
PTB16	GPIO Port B16	D
PTB17	GPIO Port B17	D
PTB18	GPIO Port B18	D
PTB2	GPIO Port B2	D
PTB3	GPIO Port B3	D
PTC1	GPIO Port C1	D
PTC16	GPIO Port C16	D
PTC17	GPIO Port C17	D
PTC18	GPIO Port C18	D
PTC19	GPIO Port C19	D
PTC2	GPIO Port C2	D
PTC3	GPIO Port C3	D
PTC4	GPIO Port C4	D
PTC5	GPIO Port C5	D
PTC6	GPIO Port C6	D
PTC7	GPIO Port C7	D
RESET_b	MCU Reset	D
RF_EARLY_WARNING	Bluetooth LE LL generated signal which can be used to wake an external sensor to make a measurement before a Bluetooth LE event.	D
RF_EXT_OSC_EN	Internal request to turn on an external oscillator for use by the internal Radio. The request can also be from the SoC if it is using the RF oscillator as its clock.	D
RF_PRIORITY	An output that notifies to the external WiFi device that the Radio event is a high priority and needs access to the 2.4 GHz antenna.	D
RF_STATUS	An output which indicates when the Radio is in an RX or a TX event; software can also control this signal directly.	D
RTC_CLKOUT	RTC Clock Out	D
RF_NOT_ALLOWED	Input signal that allows the external chip (eg. WiFi Chip) to signal the 2.4 GHz radio when BTLE and Generic FSK LL radio operations are not allowed.	D
RF_RFOSC_EN	External request to turn on the Radio's internal RF oscillator.	D
RX_SWITCH	Supports Front End Module (FEM)	D
SPI0_PCS0	SPI0 PCS0	D
SPI0_PCS1	SPI0 PCS1	D
SPI0_PCS2	SPI0 PCS2	D
SPI0_SCK	SPI0 Clock	D
SPI0_SIN	SPI0 Input	D

Table continues on the next page...

Table 3-1. KW39/38/37 Signal Descriptions (continued)

Signal Name	Description	Type
SPI0_SOUT	SPI0 Output	D
SPI1_PCS0	SPI1 PCS0	D
SPI1_SCK	SPI1 Clock	D
SPI1_SIN	SPI1 Input	D
SPI1_SOUT	SPI1 Output	D
SWD_CLK	Serial Wire Debug Clock	D
SWD_DIO	Serial Wire Debug Data Input and Output	D
TPM_CLKIN0	TPM Clock Input 0	D
TPM_CLKIN1	TPM Clock Input 1	D
TPM0_CH0	TPM0 Channel 0	D
TPM0_CH1	TPM0 Channel 1	D
TPM0_CH2	TPM0 Channel 2	D
TPM0_CH3	TPM0 Channel 3	D
TPM1_CH0	TPM1 Channel 0	D
TPM1_CH1	TPM1 Channel 1	D
TPM2_CH0	TPM2 Channel 0	D
TPM2_CH1	TPM2 Channel 1	D
TX_SWITCH	Supports Front End Module (FEM)	D
LPUART0_CTS_b	LPUART0 Clear To Send	D
LPUART0_RTS_b	LPUART0 Request To Send	D
LPUART0_RX	LPUART0 Receive	D
LPUART0_TX	LPUART0 Transmit	D
LPUART1_CTS_b	LPUART1 Clear To Send	D
LPUART1_RTS_b	LPUART1 Request To Send	D
LPUART1_RX	LPUART1 Receive	D
LPUART1_TX	LPUART1 Transmit	D
VDCDC_IN	DCDC Switch Main Supply	P
VDD_0	Power Supply 0	P
VDD_1	Power Supply 1	P
VDD_1P5OUT_PMCIN	DCDC Pulsed Output 1.5 V Regulated Output or PMC Input when DCDC in bypass mode	P
VDD_1P8OUT	DCDC Pulsed 1.8 V Regulated Output	P
VDDA	Power Supply - Analog	P
VREFH	ADC reference voltage	P
VSSA	ADC ground	G
XTAL	26 MHz or 32 MHz Crystal Input	A
XTAL32K	32 kHz Crystal Input	A

Legend

- A - Analog

- D - Digital
- P - Power Supply
- G - Ground

3.6 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the chapter of the module. They also briefly describe the signal function and direction.

3.6.1 Core Modules

This section contains tables describing the core module signal descriptions.

Table 3-2. SWD Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
SWD_DIO	SWD_DIO	Serial Wire Debug Data Input/ Output[1]	I/O
SWD_CLK	SWD_CLK	Serial Wire Clock[2]	I

1. Pulled up internally by default
2. Pulled down internally by default

3.6.2 Radio Modules

This section contains tables describing the radio signals.

Table 3-3. Radio Module Signal Descriptions

Module Signal Name	Pin Direction	Pin Name	Pin Description
ANT	O	ANT	Antenna
ANT_A	O	ANT_A	Antenna selection A for Front End Module support
ANT_B	O	ANT_B	Antenna selection B for Front End Module support
RF_ACTIVE	O	RF_ACTIVE	An output which is asserted prior to any Radio event and remains asserted for the duration of the event.
DTM_RX	I	DTM_RX	Direct Test Mode Receive
DTM_TX	O	DTM_TX	Direct Test Mode Transmit
GANT	I	GANT	Antenna ground
RF_STATUS	O	RF_STATUS	An output which indicates when the Radio is in an Rx or Tx event; software can also control this signal directly.

Table continues on the next page...

Table 3-3. Radio Module Signal Descriptions (continued)

Module Signal Name	Pin Direction	Pin Name	Pin Description
RF_PRIORITY	O	RF_PRIORITY	An output which indicates to the external WiFi device that the Radio event is a high priority and it needs access to the 2.4 GHz antenna.
RF_EARLY_WARNING	O	RF_EARLY_WARNING	Bluetooth LE LL generated signal which can be used to wake an external sensor to make a measurement before a Bluetooth LE event.
RF_NOT_ALLOWED	I	RF_NOT_ALLOWED	External signal which causes the internal Radio to cease radio activity.
RF_TX_CONF	I	RF_TX_CONF	Signal from an external Radio which indicates the availability of the 2.4 GHz antenna to the internal Radio. **NOTE:** This is a GPIO, not a dedicated PIN.
RX_SWITCH	O	RX_SWITCH	Front End Module receive mode signal.
TX_SWITCH	O	TX_SWITCH	Front End Module transmit mode signal.

Table 3-4. Radio Module Miscellaneous Pin Descriptions

Pin Name	Pad Direction	Pin Name	Pin Description
RF_INT_OSC_EN	I	RF_RFOSC_EN	External request to turn on the Radio's internal RF oscillator.
RF_EXT_OSC_EN	O	RF_EXT_OSC_EN	Internal request to turn on an External oscillator for use by the internal Radio. The request can also be from the SoC if it is using the RF oscillator as its clock.

3.6.3 System Modules

This section contains tables describing the system signals.

Table 3-5. System Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
NMI_b	—	Non-maskable interrupt	I
RESET_b	—	Reset bidirectional signal	I/O
VDD_[1:0]	VDD	Power supply	I
Ground	VSS	Ground	I
VDD_RF[3:1]	VDD_RF	Radio power supply	I
VDCDC_IN	VDCDC_IN	VDCDC_IN	I
VDD_1P8OUT	VDD_1P8	DC-DC 1.8 V Regulated Output / Input in bypass	I/O
VDD_1P5OUT_PMCIN	VDD_1P5/VDD_PMC	DC-DC 1.5 V Regulated Output / PMC Input in bypass	I/O

Table continues on the next page...

Table 3-5. System Module Signal Descriptions (continued)

SoC Signal Name	Module Signal Name	Description	I/O
PSWITCH	PSWITCH	DC-DC enable switch	I
DCDC_CFG	DCDC_CFG	DC-DC switch mode select	I
DCDC_LP	DCDC_LP	DC-DC inductor input positive	I/O
DCDC_LN	DCDC_LN	DC-DC inductor input negative	I/O
DCDC_GND	DCDC_GND	DC-DC ground	I

Table 3-6. LLWU Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
LLWU_P[15:0]	LLWU_P[15:0]	Wake-up inputs	I

3.6.4 Clock Modules

This section contains tables for Clock signal descriptions.

Table 3-7. Clock Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
EXTAL	EXTAL	26 MHz/32 MHz External clock/Oscillator input	I
XTAL	XTAL	26 MHz/32 MHz Oscillator input	I
XTAL_OUT	XTAL_OUT	26 MHz/32 MHz Clock output	O
XTAL_OUT_EN	XTAL_OUT_ENABLE	26 MHz/32 MHz Clock output enable for XTAL_OUT	I
EXTAL32K	EXTAL32K	32 kHz External clock/ Oscillator input	I
XTAL32K	XTAL32K	32 kHz Oscillator input	I
CLKOUT	CLKOUT	Internal clocks monitor	O

3.6.5 Analog Modules

This section contains tables for Analog signal descriptions.

Table 3-8. ADC0 Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
ADC0_DM0	DADM0	ADC Channel 0 Differential Input Negative	I
ADC0_DP0	DADP0	ADC Channel 0 Differential Input Positive	I
ADC0_SE[5:1]	AD[5:1]	ADC Channel 0 Single-ended Input n	I
VREFH	V_{REFSH}	Voltage Reference Select High	I
VDDA	V_{DDA}	Analog Power Supply	I
VSSA	V_{SSA}	Analog Ground	I

Table 3-9. CMP0 Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
CMP0_IN[5:0]	IN[5:0]	Analog voltage inputs	I
CMP0_OUT	CMP0	Comparator output	O

Table 3-10. VREF Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
VREF_OUT	VREF_OUT	Internally generated voltage reference output	O

3.6.6 Timer Modules

This section contains tables describing timer module signals.

Table 3-11. TPM0 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock	I
TPM0_CH[3:0]	TPM_CH[3:0]	TPM channel	I/O

Table 3-12. TPM1 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock	I
TPM1_CH[1:0]	TPM_CH[1:0]	TPM channel	I/O

Table 3-13. TPM2 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
TPM_CLKIN[1:0]	TPM_EXTCLK	External clock	I
TPM2_CH[1:0]	TPM_CH[1:0]	TPM channel	I/O

Table 3-14. LPTMR0 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
LPTMR0_ALT[2:1]	LPTMR0_ALT[2:1]	Pulse counter input pin	I

Table 3-15. RTC Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
RTC_CLKOUT	RTC_CLKOUT	1 Hz square-wave output	O

3.6.7 Communication Interfaces

This section contains tables for the signal descriptions for the communication modules.

Table 3-16. SPI0 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
SPI0_PCS0	PCS0/SS	Chip Select/Slave Select	I/O
SPI0_PCS[2:1]	PCS[2:1]	Chip Select	O
SPI0_SCK	SCK	Serial Clock	I/O
SPI0_SIN	SIN	Data In	I
SPI0_SOUT	SOUT	Data Out	O

Table 3-17. SPI1 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
SPI1_PCS0	SPI1_PCS0	Chip Select/Slave Select	I/O
SPI1_SCK	SCK	Serial Clock	I/O
SPI1_SIN	SIN	Data In	I
SPI1_SOUT	SOUT	Data Out	O

Table 3-18. I2C0 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
I2C0_SCL	SCL	I2C serial clock line	I/O
I2C0_SDA	SDA	I2C serial data line	I/O

Table 3-19. I2C1 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
I2C1_SCL	SCL	I2C serial clock line	I/O
I2C1_SDA	SDA	I2C serial data line	I/O

Table 3-20. CAN0 Signal Descriptions (KW38 only)

SoC Signal Name	Module Signal Name	Description	I/O
CAN0_RX	CAN RX	CAN Receive Pin	I
CAN0_TX	CAN TX	CAN Transmit Pin	O

Table 3-21. LPUART0 Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
LPUART0_CTS_b	LPUART CTS	Clear To Send	I
LPUART0_RTS_b	LPUART RTS	Request To Send	O
LPUART0_RX	LPUART RxD	Receive Data	I
LPUART0_TX	LPUART TxD	Transmit Data[1]	I/O

1. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data

Table 3-22. LPUART1 Module Signal Descriptions (KW38 only)

SoC Signal Name	Module Signal Name	Description	I/O
LPUART1_CTS_b	LPUART CTS	Clear To Send	I
LPUART1_RTS_b	LPUART RTS	Request To Send	O
LPUART1_RX	LPUART RxD	Receive Data	I
LPUART1_TX	LPUART TxD	Transmit Data[1]	I/O

1. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data

3.6.8 Human-Machine Interfaces(HMI)

This section contains tables describing the HMI signals.

Table 3-23. GPIO Module Signal Descriptions

SoC Signal Name	Module Signal Name	Description	I/O
PTA[19:16][2:0]	PORTA19-16, 2-0	General Purpose Input/Output	I/O
PTB[18:16][3:0]	PORTB18-16, 3-0	General Purpose Input/Output	I/O
PTC[19:16][7:1]	PORTC19-16, 7-1	General Purpose Input/Output	I/O