The Chinese University of Hong Kong

Department of Computer Science and Engineering

ENGG2020 Digital Logic & Systems

Lab 2 BCD to 7-segment Decoder

Instructions

- Before the lab session, please
  - Print out the Lab Answer Sheet
  - Find and read the IC datasheets on the web
  - Read the CUHK CSE FPGA Board User Guide in Blackboard
- Submit your Lab Answer Sheet within your lab session in **hard copy**
- Late submission will **not** be accepted

Objectives

- Understand Binary Coded Decimal (BCD) and 7-segment display
- Understand the use of BCD to 7-segment Decoder
- Implement basic combinational logic circuit

Components & tools

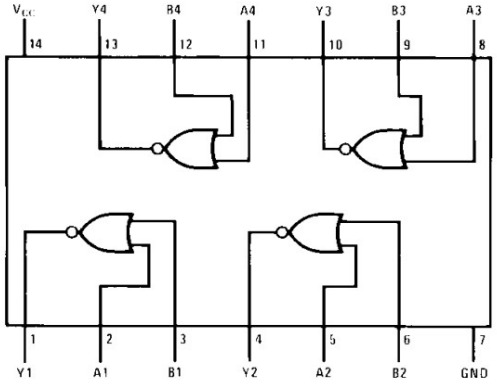
- CUHK CSE FPGA Board x 1
- 74LS02 x 1 (Four NOR gates)
- Connecting wires

Components and Tools Overview

In this lab, we are going to use 74LS08, 74LS32, and 74LS86 to construct a 1-bit full adder and use 7447A to decode the result for 7-segment display.

1. 74LS02

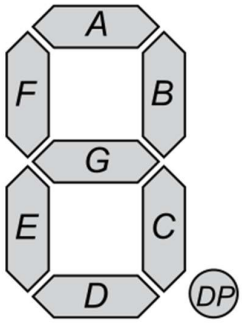
74LS02 consists of four NOR gates. The output of an NOR gate is at logic level 1 only when all the inputs are at logic level 0. The pin assignment is shown below:



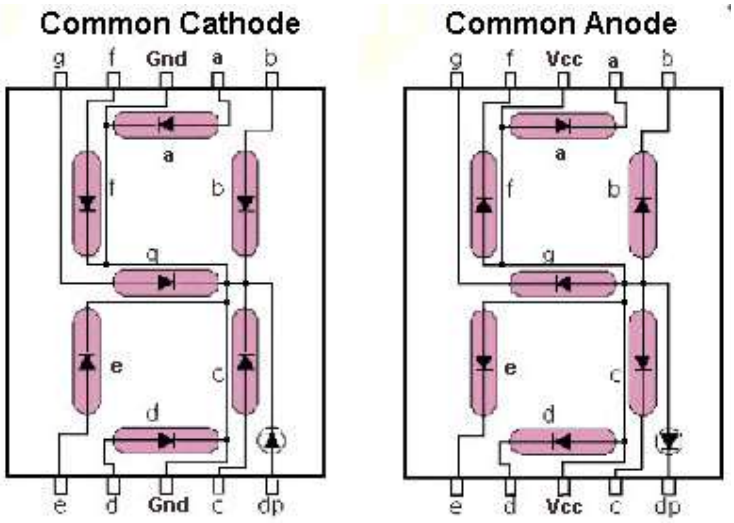
2. 7-segment Display

Although individual LEDs are able to display the gate outputs and the states of flip-flops, they are not suitable for displaying decimal numbers. In many digital devices, 7-segment display is used to display numbers or characters.

We use seven LEDs to display the output numbers of the full adder, in addition, there is an extra LED for the decimal point (DP). The LEDs are labeled from A to G as below:

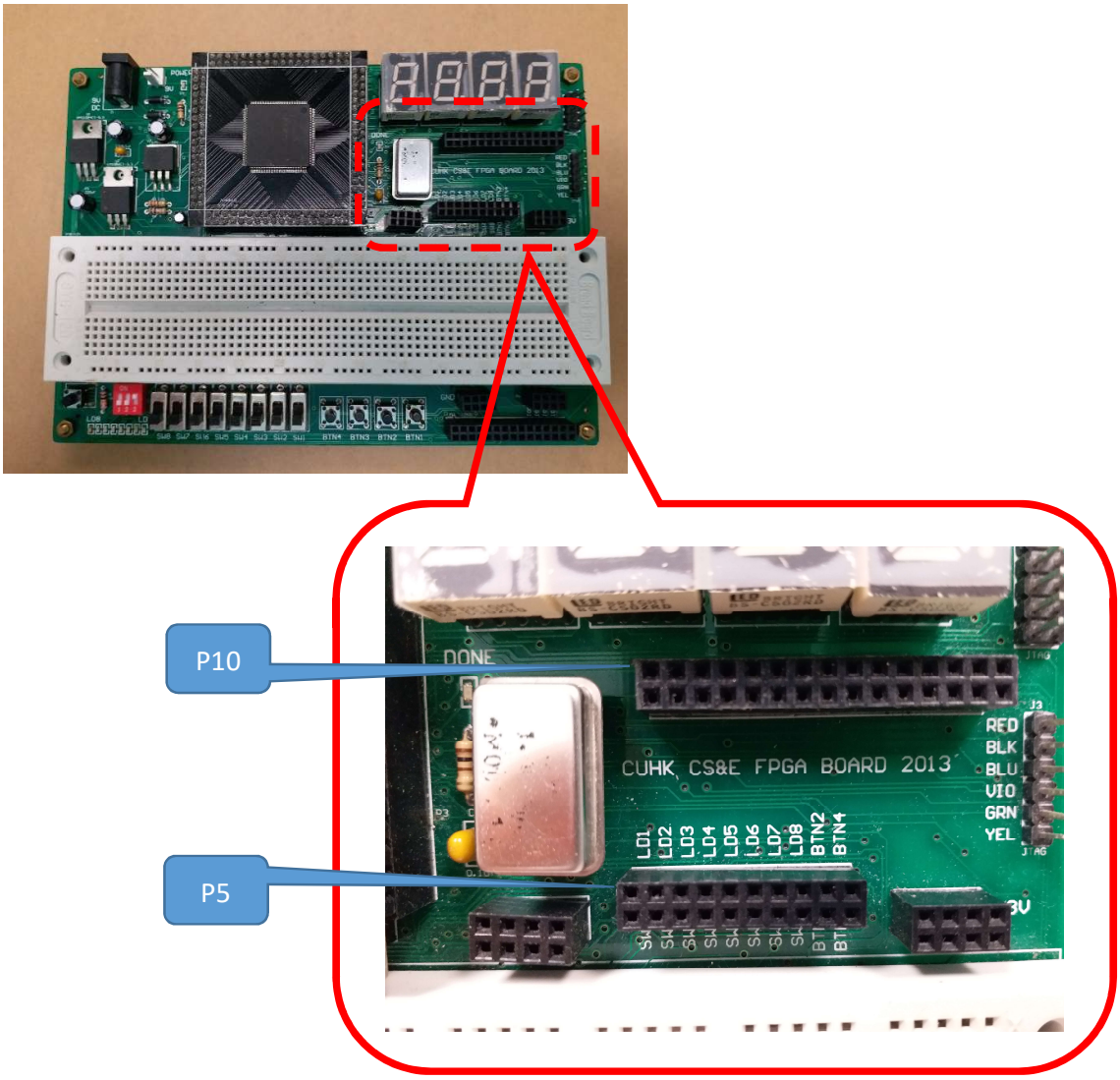


There are two types of 7-segment display. They are a) Common Cathode, and b) Common Anode. The Common Cathode type is used in the FPGA board of this experiment. In order to light up a LED, a logic level 1 is required.



3. CUHK CSE FPGA Board

The CUHK CSE FPGA Board and the pin assignment of P5 and P10 are shown below.



P10 Pin Assignment for Display 1

b	d	f												
a	c	e	g											

P5 Pin Assignment for LEDs, switches and buttons

LD1	LD2	LD3	LD4	LD5	LD6	LD7	LD8	BTN2	BTN4
SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	BTN1	BTN3

Procedures

In this lab, you are required to construct a combinational logic circuit for a simplified version of BCD to 7-segment Display.

1. Truth Table of BCD to 7-segment Decoder

Binary Coded Decimal (BCD) use four bits to represent a decimal digit. As shown below, the decimal digit 0 to 9 are represented by the four input bits/lines A, B, C, and D. In order to show the decimal digital on a 7-segment display, the BCD will be converted to 7 output bits/lines by a combinational logic circuit.

In this lab, we will focus on implementing the decoding circuit for decimal digits from 1 to 4 only.

set 0,5-15 as dont care term

for b, b=1 (all output are 1,including dont care)

c=B+D=C'+D

e=(B+D)'=(C'+D)' by grouping 0 ,ie c is complement of e, just a not gate

in NOR implement: target: make it into (A+B)' form so c=B+D=(B+D)"

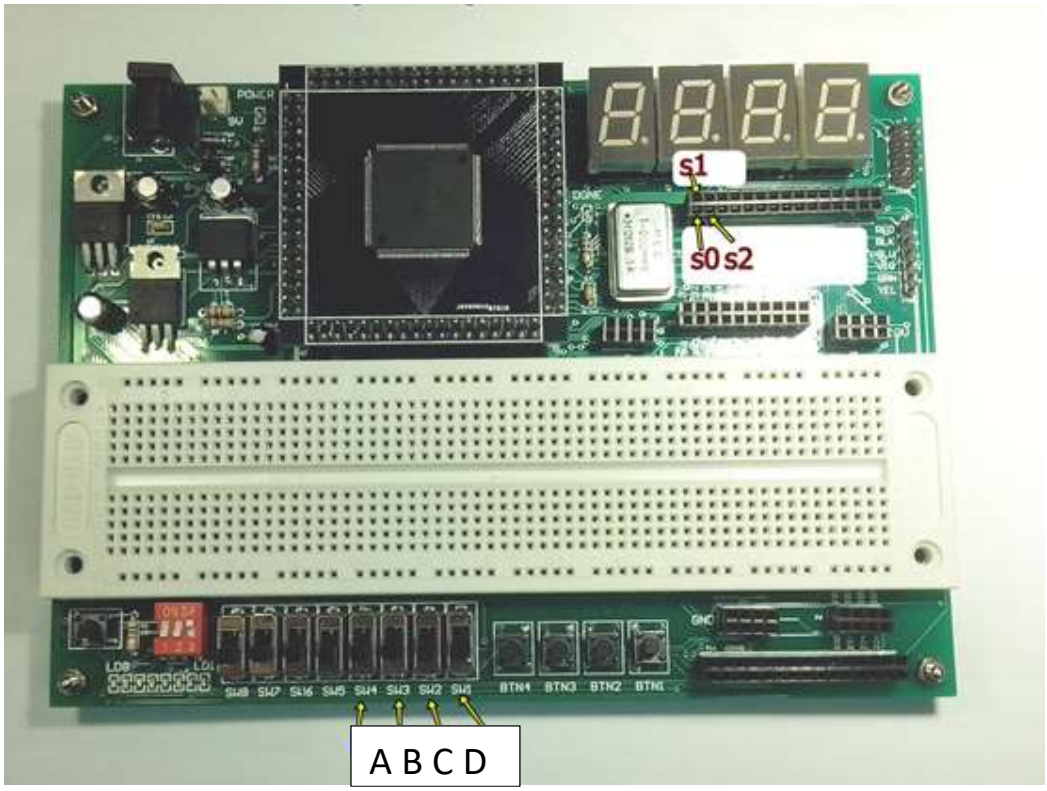
Decimal Digit	Input lines				Output lines							Display pattern
	A	B	C	D	a	b	c	d	e	f	g	
0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	1
2	0	0	1	0	1	1	0	1	1	0	1	2
3	0	0	1	1	1	1	1	1	0	0	1	3
4	0	1	0	0	0	1	1	0	0	1	1	4
5	0	1	0	1	1	0	1	1	0	1	1	5
6	0	1	1	0	1	0	1	1	1	1	1	6
7	0	1	1	1	1	1	1	0	0	0	0	7
8	1	0	0	0	1	1	1	1	1	1	1	8
9	1	0	0	1	1	1	1	1	0	1	1	9

Table 1: Truth Table of BCD to 7-segment Decoder

if your output finally depends on a dont care term, just write down the dont care term name eg A=0, B=dont care , A+B=B

2. Decoder Design

Before you construct the physical circuit on the board, write down the logic functions on the Answer Sheet for Question 1 and 2.



3. Decoder Implementation

In our simplified decoder (for decimal digits 1 to 4 only), there are 4 input lines and 7 output lines.

Please connect the input A, B, C, and D to SW4, SW3, SW2, and SW1 respectively.

Please connect the output a, b, c, d, e, f, and g to Pin 1 to 7 of P10 socket respectively.

Lab 2 BCD to 7-segment Decoder
Answer Sheet

Name: _____ Student ID: _____

Name: _____ Student ID: _____

Session (Time): _____ Group Number: _____

1. Determine the simplified logic functions of the 7 segments of LED outputs in terms of inputs A, B, C, and D **directly** in terms of minterms from the truth table in Table 1 for decimal digits from 1 to 4 only. [30 marks]

   a = _____

   b = _____

   c = _____

   d = _____

   e = _____

   f = _____

   g = _____

2. Convert the **simplified** logic functions in part 1) to another set of logic functions which are using maximum 4x NOR gates only. [30 marks]

   a = _____

   b = _____

   c = _____

   d = _____

   e = _____

   f = _____

   g = _____

3. Construct the circuit on the board and demonstrate the decoding functions to the instructor or TA. [40 marks]