ENGG2020 DIGITAL LOGIC AND SYSTEMS

CHAPTER 4B: COMBINATIONAL LOGIC

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CONTENTS

- Combinational logic circuit
- Adder and Subtractor
- Comparator
- Decoder and Encoder
- Multiplexer and Demultiplexer
- Tri-state Buffer

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COMPARATORS

4-BIT COMPARATOR

- Consider a 4-bit comparator to compare the magnitude of two 4-bit binary numbers, A and B
- After comparison, only one of the following three outputs will be HIGH
- D1 represents A = B
- D2 represents A > B
- D3 represents A < B

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4-BIT COMPARATOR

- Assume A = $A_3A_2A_1A_0$ and B = $B_3B_2B_1B_0$
- If A=B, D1 is HIGH if and only if A_3=B_3, A_2=B_2, A_1=B_1, and A_0=B_0
- In Boolean function, if A=B, x_i = 1 for i = 0,1,2,3

$$x_i = A_iB_i + \bar{A}_i\bar{B}_i$$

$$D_1 : (A = B) \Rightarrow x_3x_2x_1x_0$$

If A_i = B_i, x_i =1

If A = B, x_0 = x_1 = x_2 = x_3, and D_1 = 1

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4-BIT COMPARATOR

- D2 or D3 implies the comparison of the magnitudes of A and B at different bits
- Starting from the most significant bit
  - Find the first position when $A_i \neq B_i$
  - If A_i=1, then A_i>B_i
- We have:

$$D_2 : (A > B) \Rightarrow$$

$$A_3\bar{B}_3 + x_3A_2\bar{B}_2 + x_3x_2A_1\bar{B}_1 + x_3x_2x_1A_0\bar{B}_0$$

x3=1 if a3=b3

$$D_3 : (A < B) \Rightarrow$$

$$\bar{A}_3B_3 + x_3\bar{A}_2B_2 + x_3x_2\bar{A}_1B_1 + x_3x_2x_1\bar{A}_0B_0$$

If A_3=1 and B_3=0, A>B, and D_2 = 1

If A_3=0 and B_3=1, A<B, and D_3 = 1

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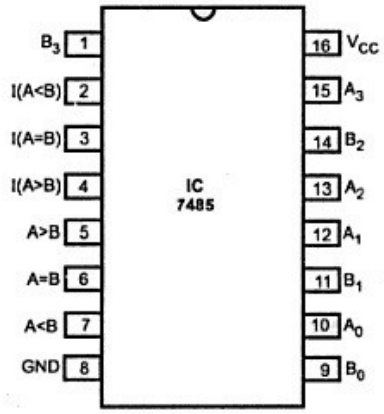
COMMERCIAL PACKAGE OF COMPARATOR

- A commercial IC 7485 is a 4-bit comparator
- To compare two 1-byte binary numbers, two 7485 can be cascaded with each other



(a) Pin diagram (IC 7485)

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8 DECODER AND ENCODER

DECODER AND ENCODER

- They are a pair of widely used devices essentially for two reasons
  - Valuable messages are to be transmitted through public channels without being noticed by parties other than the intended ones – special codes are generated (encoding)
  - Once codes are received the original messages must be revealed as accurately as possible (decoding)
- What are the conditions to achieve these requirements?
  - Encryption, decryption, efficient transmission, and error detection and correction

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DECODER

- A process of systematically rearranging some code words such that the original message or information can be realized
- Decoding is the conversion of a n-bit input coder to a m-bit output code, such that each valid input code word produces a unique output code

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2-BIT DECODER (ACTIVE-HIGH)

- For a 2-bit decoder, there are 2 input bits and 2^2 unique output patterns
- The truth table of a 2-bit decoder:

X0	X1	A	B	C	D
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Active-HIGH outputs

- For each combination of X0 and X1, there is only one Active-HIGH output

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2-BIT DECODER (ACTIVE-HIGH)

- In order to make an efficient hardware implementations, we have modified the truth table as below, by adding the complements of X0 and X1

Active-HIGH outputs

X0	X1	X0'	X1'	A	B	C	D
0	0	**1**	**1**	1	0	0	0
0	**1**	**1**	0	0	1	0	0
1	0	0	**1**	0	0	1	0
1	**1**	0	0	0	0	0	1

- By making such modification, only 4 AND gates and 2 NOT gates are required

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ACTIVE-HIGH VS. ACTIVE-LOW

- Active-HIGH

X0	X1	X0'	X1'	A	B	C	D
0	0	**1**	**1**	1	0	0	0
0	**1**	**1**	0	0	1	0	0
1	0	0	**1**	0	0	1	0
1	**1**	0	0	0	0	0	1

- Active-LOW

X0	X1	X0'	X1'	A'	B'	C'	D'
0	0	**1**	**1**	0	1	1	1
0	**1**	**1**	0	1	0	1	1
1	0	0	**1**	1	1	0	1
1	**1**	0	0	1	1	1	0

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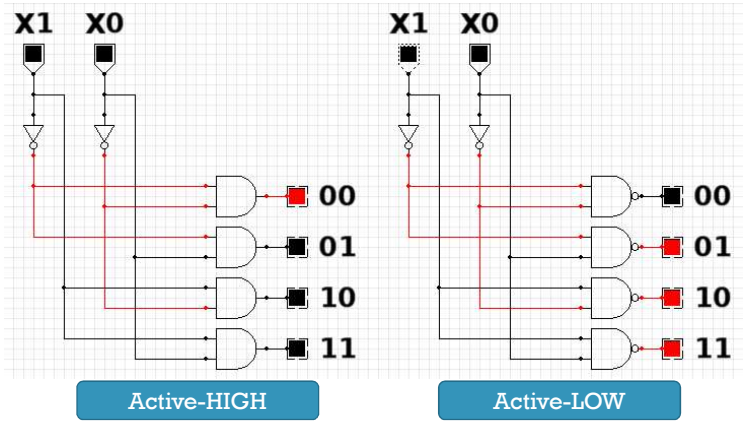
2-BIT DECODER

- The logic circuits of 2-bit decoder:



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3-BIT DECODER

X0	X1	X2	X0'	X1'	X2'	A	B	C	D	E	F	G	H
0	0	0	**1**	**1**	**1**	1	0	0	0	0	0	0	0
0	0	**1**	**1**	**1**	0	0	1	0	0	0	0	0	0
0	**1**	0	**1**	0	**1**	0	0	1	0	0	0	0	0
0	**1**	**1**	**1**	0	0	0	0	0	1	0	0	0	0
1	0	0	0	**1**	**1**	0	0	0	0	1	0	0	0
1	0	**1**	0	**1**	0	0	0	0	0	0	1	0	0
1	**1**	0	0	0	**1**	0	0	0	0	0	0	1	0
1	**1**	**1**	0	0	0	0	0	0	0	0	0	0	1

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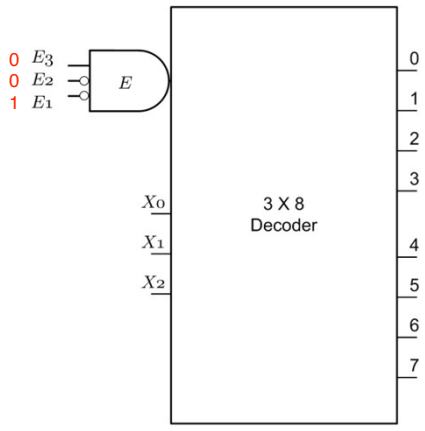
COMMERCIAL PACKAGE OF 3X8 DECODER

- 74138 is a 3x8 decoder
  - 3-bit code input
  - 8-bit Active-LOW output
- In addition, there are 3 enabling bits which is used to provide an external control to the device
  - Chip selection
  - Reset



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TRUTH TABLE OF 3X8 DECODER

* or X = Don't Care

commercial encodeing have so many pins(dont care) with no reason

Disabled

001
correct encode

Enabled

E1	E2	E3	X0	X1	X2	0	1	2	3	4	5	6	7
H	*	*	*	*	*	H	H	H	H	H	H	H	H
*	H	*	*	*	*	H	H	H	H	H	H	H	H
*	*	L	*	*	*	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

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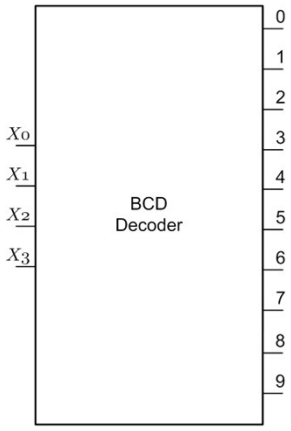
COMMERCIAL PACKAGE OF BCD DECODER

- 7442 is a BCD to DEC decoder
  - 4-bit code input
  - 10-bit Active-LOW output



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TRUTH TABLE OF BCD DECODER

X3	X2	X1	X0	0	1	2	3	4	5	6	7	8	9
L	L	L	L	**L**	H	H	H	H	H	H	H	H	H
L	L	L	H	H	**L**	H	H	H	H	H	H	H	H
L	L	H	L	H	H	**L**	H	H	H	H	H	H	H
L	L	H	H	H	H	H	**L**	H	H	H	H	H	H
L	H	L	L	H	H	H	H	**L**	H	H	H	H	H
L	H	L	H	H	H	H	H	H	**L**	H	H	H	H
L	H	H	L	H	H	H	H	H	H	**L**	H	H	H
L	H	H	H	H	H	H	H	H	H	H	**L**	H	H
H	L	L	L	H	H	H	H	H	H	H	H	**L**	H
H	L	L	H	H	H	H	H	H	H	H	H	H	**L**
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

Invalid inputs ALL OUTPUTS SET HIGH

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ENCODER

- Encoding performs the inverse process of decoding by arranging the input message such that
  - The message is not recognized if intercepted during the transmission (e.g. encryption)
  - The code can be corrected if corrupted during the transmission (e.g. error detection and correction)
- Given a specified arrangement of message in an encoder,
  - the received code cannot be exactly restored unless that special arrangement is exactly known
  - Which is a unique KEY and LOCK in encryption mechanism

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TRUTH TABLE OF 8X3 ENCODER

change the direction of decoder

- This is the truth table of 3x8 decoder actually.

Decoder Inputs OR Encoder Outputs

X0	X1	X2	A	B	C	D	E	F	G	H
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Decoder Outputs OR Encoder Inputs

- By changing the input/output directions, we have the truth table of 8x3 encoder

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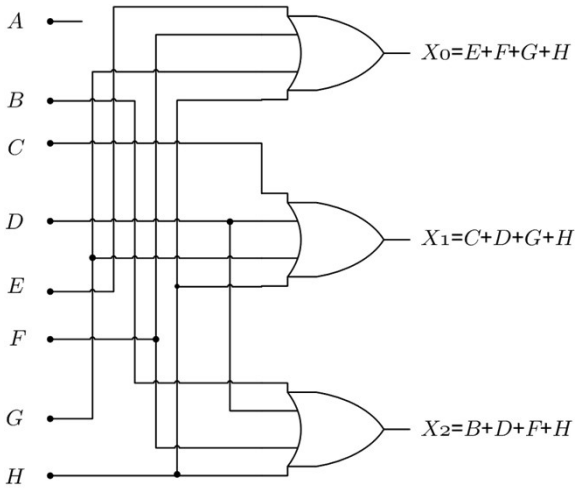
LOGIC CIRCUIT OF 8X3 ENCODER



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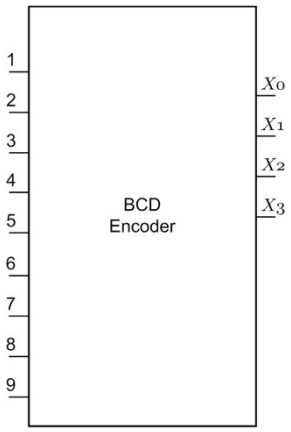
COMMERCIAL PACKAGE OF ENCODER

- 74147 is a commercial package of a DEC to BCD encoder
- 10 decimal inputs from 0 to 9 (Active-LOW)
- 4 bits BCD output (Active-LOW)
- Priority Encoder
  - When there are more than one inputs active, higher priority will be given to the larger decimal input.



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TRUTH TABLE OF 74147

eg code :low 1 1 1 1 1 1 1 1 L-> first row(L11L), coz 9 is low

1	2	3	4	5	6	7	8	9	X3	X2	X1	X0
H	H	H	H	H	H	H	H	H	H	H	H	H
*	*	*	*	*	*	*	*	L	L	H	H	L
*	*	*	*	*	*	*	L	H	L	H	H	H
*	*	*	*	*	*	L	H	H	H	L	L	L
*	*	*	*	*	L	H	H	H	H	L	L	H
*	*	*	*	L	H	H	H	H	H	L	H	L
*	*	*	L	H	H	H	H	H	H	L	H	H
*	*	L	H	H	H	H	H	H	H	H	L	L
*	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

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MULTIPLEXER AND DEMULTIPLEXER

application:
share channel
span spectrum in different time slot

MULTIPLEXER AND DEMULTIPLEXER

- Multiplexing means transmitting a large number of information over a smaller number of channels or lines
  - Data selection is involved by a control signal
  - Implemented in the transmitting end
- Demultiplexing means distributing a single source of information from a large number of channels or lines
  - Work like a decoder
  - Implemented in the receiving end
- Given a multiplexer circuit, the information cannot be accurately demultiplexed, unless exact knowledge of the multiplex circuit is known

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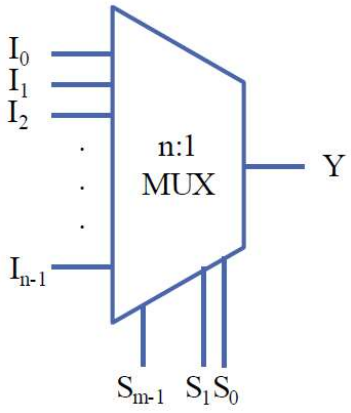
MULTIPLEXER (MUX)

- The symbol of a nx1 MUX:



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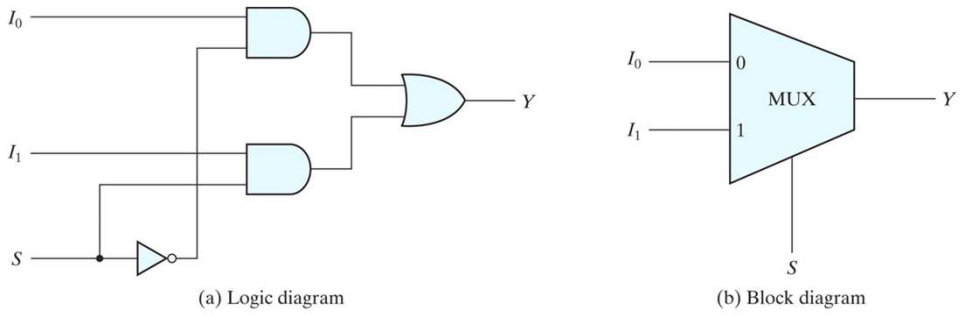
2X1 MULTIPLEXER

- The logic circuit and symbol of a 2x1 MUX



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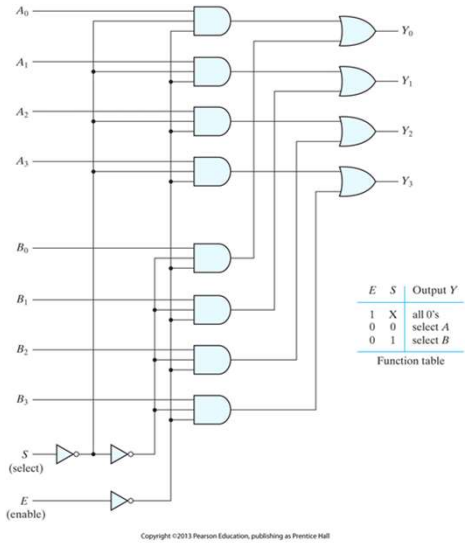
QUADRUPLE 2X1 MULTIPLEXER

- The logic circuit and truth table of a quadruple 2x1 MUX



E	S	Output Y
1	X	all 0's
0	0	select A
0	1	select B

Function table

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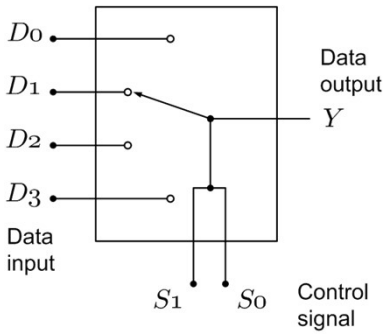
4X1 MULTIPLEXER

- Consider a 4-input MUX
  - 4 inputs: D0 to D3
  - 1 output: Y
- Only one input is selected/read/sent to the output



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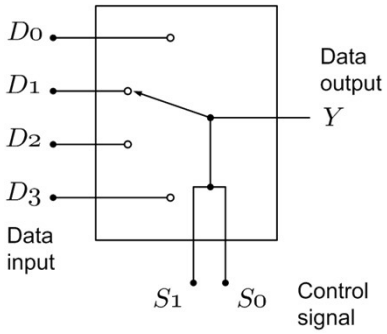
4X1 MULTIPLEXER

- The selection is performed by control signals
  - 2 control signals: S0 and S1
- The truth table of the 4X1 MUX

S1	S0	Y
0	0	D0
0	1	D1
1	0	D2
1	1	D3

- NO two inputs will be selected at a time



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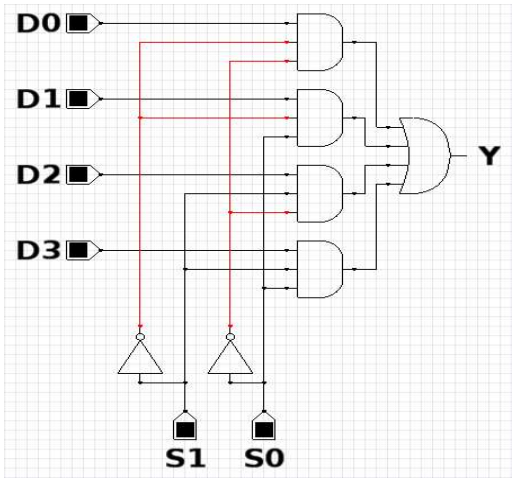
4X1 MULTIPLEXER

- The logic circuit of 4x1 MUX:



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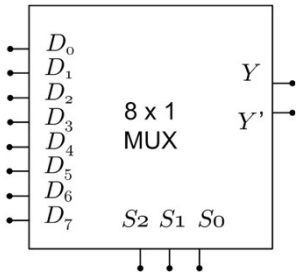
COMMERCIAL PACKAGE OF 8X1 MUX

- 74151 is a commercial package of 8x1 MUX
- The block diagram and truth table of 8x1 MUX:



S2	S1	S0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

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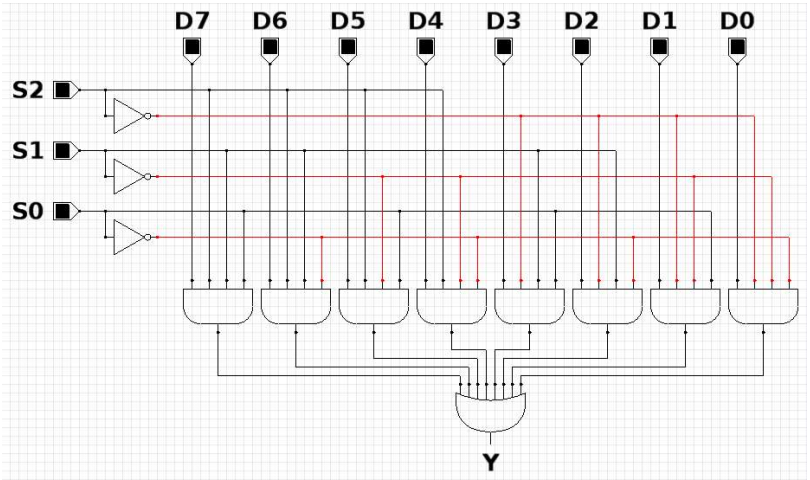
COMMERCIAL PACKAGE OF 8X1 MUX



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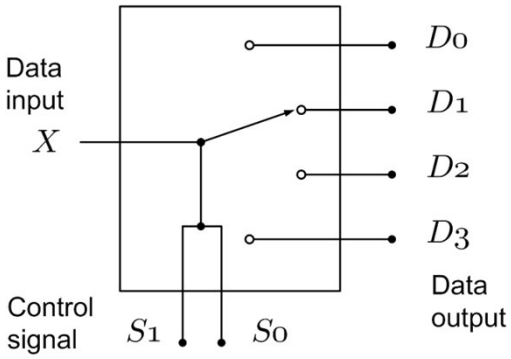
DEMULTIPLEXER (DEMUX)

- Consider a 4-output DEMUX
  - 4 outputs: D0 to D3
- Only one output is selected and assigned the value of X
- The selection is performed by control signals, S0 and S1



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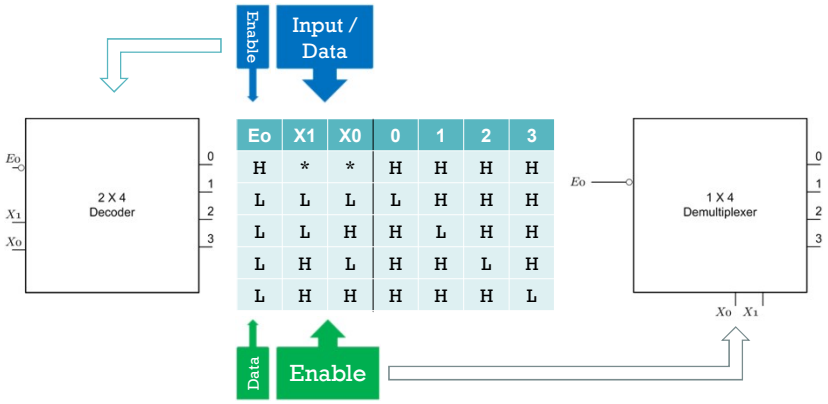
USE DECODER AS DEMUX

- A DEMUX can be implemented by a decoder



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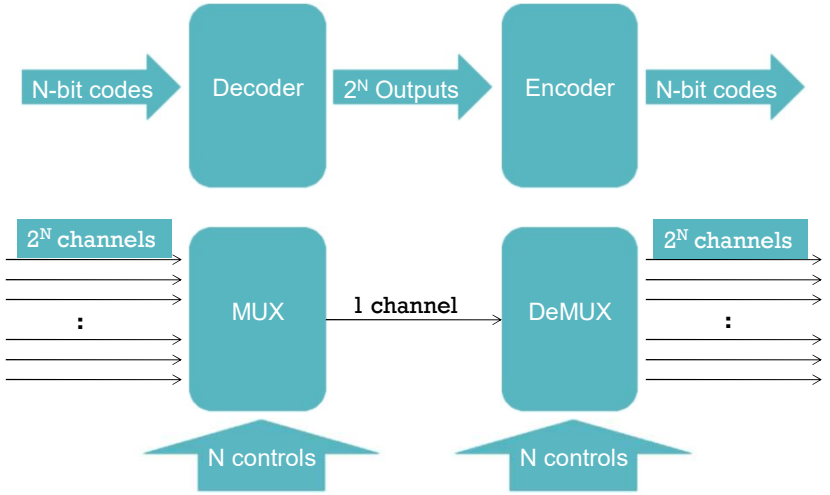
SUMMARY OF ENCODER/DECODER/MUX/DEMUX



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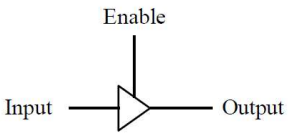
APPENDIX: TRI-STATE BUFFER

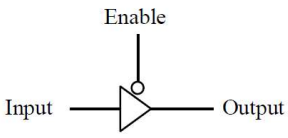
TRI-STATE BUFFER

- Tri-State logic allows an output port to assume a high impedance state in addition to the 0 and 1 logic levels
- High impedance state effectively remove the device's influence from the rest of the circuit
- This allows multiple circuits to share the same output line(s)



Active-High Enable

Active-High Enable	Input	Output
0	0	Z
0	1	Z
1	0	0
1	1	1



Active-Low Enable

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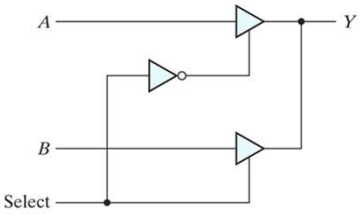
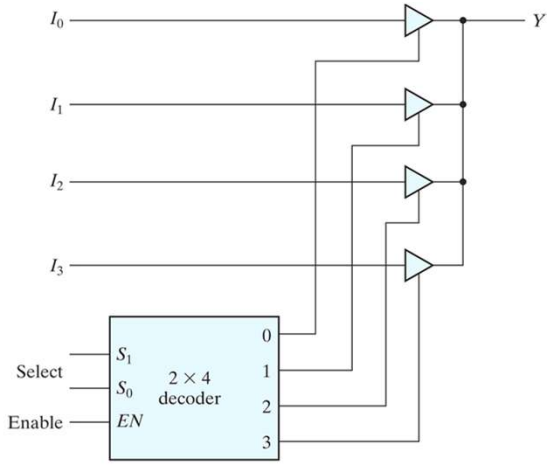
TRI-STATE BUFFER

- MUX with tri-state buffers



(a) 2-to-1-line mux



(b) 4-to-1-line mux

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ANY QUESTIONS ?

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