Latch (Level-Sensitive) Timing Diagrams

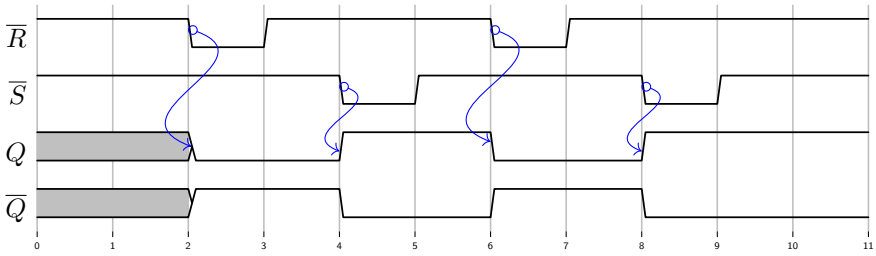

Figure 1: RS Latch

The Q (and $\overline{Q}$) output will change if either of the $\overline{R}$ or $\overline{S}$ input signals change.

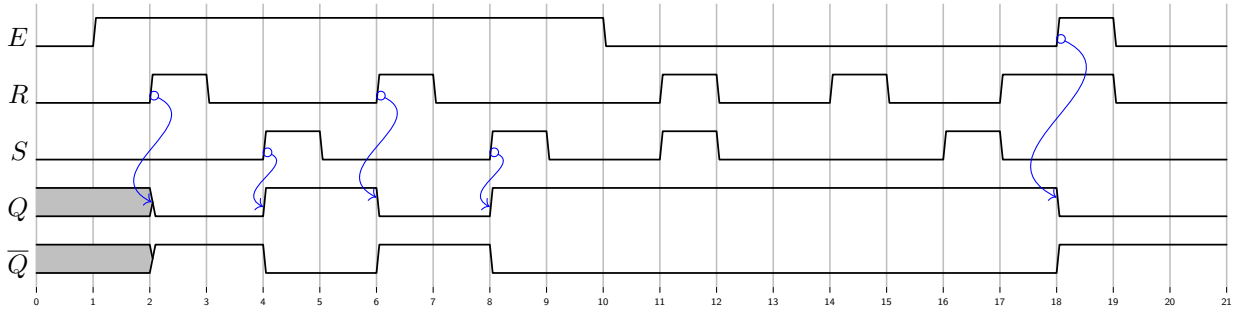

Figure 2: RS Latch w/Enable

The Q (and $\overline{Q}$) output will change if either of the R or S input signals change when the E input signal is high (or becomes high.)

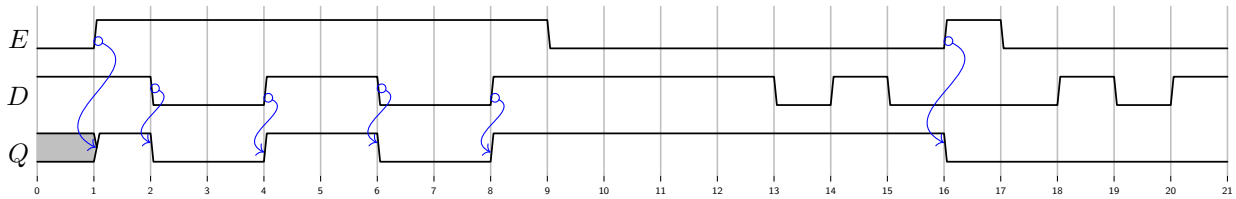

Figure 3: D Latch

The Q output will change to match the D input signal any time that the E input signal is high.

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jwinans@niu.edu 2020-09-16 16:04:17 -0500 v2.0-676-gbee1b8f

Flip-Flop (Edge-Sensitive) Timing Diagrams

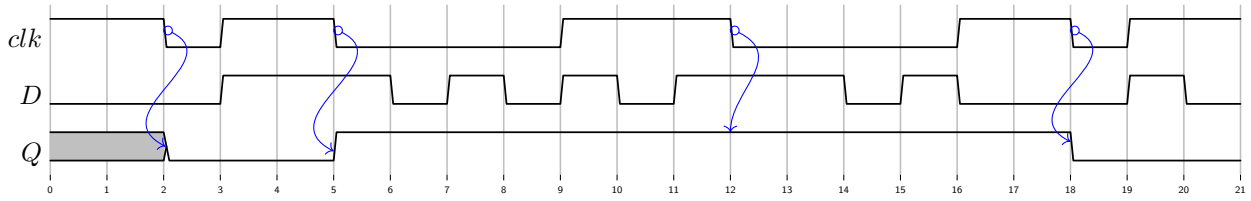

Figure 4: D Flip-Flop (falling-edge triggered)

The Q signal will be set to match that of the D signal when ever a falling edge on clk occurs.
(The *only* time that the Q output can change as a result of a falling edge on the clk signal line.)

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