

LETTER

Low-power high-performance 32-bit RISC-V microcontroller on 65-nm silicon-on-thin-BOX (SOTB)

Trong-Thuc Hoang^{1, 2, a), b)}, Ckristian Duran¹, Khai-Duy Nguyen^{1, 3}, Tuan-Kiet Dang^{1, 3}, Quynh Nguyen Quang Nhu³, Phuc Hong Than⁴, Xuan-Tu Tran⁵, Duc-Hung Le⁶, Akira Tsukamoto², Kuniyasu Suzaki^{2, 7}, and Cong-Kha Pham^{1, c)}

Abstract In this paper, a 32-bit RISC-V microcontroller in a 65-nm Silicon-On-Thin-BOX (SOTB) chip is presented. The system is developed based on the VexRiscv Central Processing Unit (CPU) with the Instruction Set Architecture (ISA) extensions of RV32IM. Besides the core processor, the System-on-Chip (SoC) contains 8KB of boot ROM, 64KB of on-chip memory, UART controller, SPI controller, timer, and GPIOs for LEDs and switches. The 8KB of boot ROM has 7KB of hard-code in combinational logics and 1KB of a stack in SRAM. The proposed SoC performs the Dhrystone and Coremark benchmarks with the results of 1.27 DMIPS/MHz and 2.4 Coremark/MHz, respectively. The layout occupies 1.32-mm² of die area, which equivalents to 349,061 of NAND2 gate-counts. The 65-nm SOTB process is chosen not only because of its low-power feature but also because of the back-gate biasing technique that allows us to control the microcontroller to favor the low-power or the high-performance operations. The measurement results show that the highest operating frequency of 156-MHz is achieved at 1.2-V supply voltage (V_{DD}) with +1.6-V back-gate bias voltage (V_{BB}). The best power density of 33.4- μ W/MHz is reached at 0.5-V V_{DD} with +0.8-V V_{BB} . The least current leakage of 3-nA is retrieved at 0.5-V V_{DD} with -2.0-V V_{BB} .

Keywords: 32-bit microcontroller, back-gate bias, RISC-V, RV32IM, Silicon-on-Insulator, SOTB.

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

From the beginning of the 21st century, the Reduced Instruction Set Computer (RISC) architecture was already dominant in the mobile marketplace because of its low-power and low-cost characteristics [1]. For example, there were RISC-based

Central Processing Units (CPUs) like ARM CPUs in most of the hand-held devices [2], and MIPS-based CPUs in most of the gaming consoles [3]. And very recently, the emerging of the open-source RISC-V Instruction Set Architecture (ISA) was challenging even the most senior Integrated Circuit (IC) design companies. The development of RISC-V was expanding and turning the silicon industry to more efficiently than ever. Comparing to the conventional IC development flow, the RISC-V ecosystem is like “one barbarian is at the gates with a refurbished siege engine” [4].

RISC-V is an open-source ISA that was first presented by the Berkeley architecture group in 2014 [5], and now it is maintaining by the RISC-V Foundation group [6]. The primary goal of the RISC-V Foundation is to provide a completely open ISA to support the research, development, and education in both academia and industry areas. The ISA can support 32-bit, 64-bit, and 128-bit address spaces. It was designed specially to avoid the “over-architecting” in microarchitecture by implementing only the small base integer of ISA [7]. Then based on the bases, the ISA can be extended with many of standard extensions like “M” for multiplication and division, “A” for atomic, “F” for floating-point, “D” for double, “C” for compressed instruction sets, and more [7]. Finally, the RISC-V ecosystem is developed, and the toolchains such as assemblers, linkers, compilers, and operating systems are provided by the RISC-V Foundation to suit all of the above standard ISA extensions [8]. As a result, the way of designing and the time for developing a highly customized processor have become much more efficient and robust.

Up to now, there are plenty of RISC-V processors that have been presented in both academic and industrial forums. The IP cores, the System-on-Chips (SoCs), and the development kits were proposed and developed in both Field-Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs) [9, 10, 11, 12, 13]. Some worth-mention works are the highly customizable Rocket cores of the Berkeley architecture group [14], the high-performance 32-bit E-core series [15] and 64-bit U-core series [16] of the SiFive Inc., and the 32-bit RI5CY cores [17] and 64-bit Ariane cores [18] of the PULP-platform research group. For small low-power energy-efficient 32-bit RISC-V microprocessors, although there were plenty of IP cores presented in FPGAs as reviewed by R. Höller *et al.* in June 2019 [19], silicon proof publications were still limited. The worth-mention 32-bit RISC-V chip measurement publications can be listed are the Parallel Ultra-

¹ University of Electro-Communications (UEC), Tokyo 182-8585, Japan

² National Institution of Advanced Industrial Science and Technology (AIST), Tokyo 135-0064, Japan

³ The University of Danang, University of Science and Technology (DUT), 54 Nguyen Long Bang St., Danang, Vietnam

⁴ Duy Tan University (DTU), 3 Quang Trung, Hai Chau Dist., Danang, Vietnam

⁵ University of Engineering and Technology (VNU-UET), 144 Xuan Thuy St., Cau Giay Dist., Hanoi, Vietnam

⁶ University of Science (VNU-HCMUS), 227 Nguyen Van Cu St., Dist. 5, Hochiminh City, Vietnam

⁷ Technology Research Association of Secure IoT Edge application based on RISC-V Open architecture (TRASIO), Tokyo 135-0064, Japan

a) thuc@vlsilab.ee.uec.ac.jp

b) trongthuc.hoang@aist.go.jp

c) phamck@uec.ac.jp

DOI: 10.1587/elex.17.20200282

Received August 19, 2020

Accepted September 4, 2020

Publicized October 6, 2020

Copyedited October 25, 2020

Low Power (PULP) SoC in 2016 [20], PULPv2 SoC in 2017 [21], the low-power microcontroller intended for Internet of Things (IoT) in 2016 [22] and 2017 [23], the FE310-G000 in 2017 [24], and the FE310-G002 in 2019 [25].

In this paper, a 32-bit RISC-V microcontroller is presented and measured. The core processor is the VexRiscv CPU [26] with the RV32IM ISA extensions. Then based on the CPU, the completed SoC is built, including 8KB of boot ROM with 1KB of a stack in SRAM and 7KB of hard-code in combinational logics, 64KB of SRAM on-chip memory, UART controller, SPI controller, timer, and GPIOs. The 65-nm Silicon-On-Thin-BOX (SOTB) process was chosen due to its low-power feature [27]. Furthermore, it can provide the chip with the back-gate biasing technique, which allows us to enhance the chip performances further [28]. The chip layout sits on a die area of 1.32-mm², which equivalents to 349,061 of NAND2 gate-counts. The core power supply (V_{DD}) was measured from 0.5-V to 1.2V, and the I/O V_{DD} was fixed at 3.3-V. The peak performance of 156-MHz maximum operating frequency (F_{Max}) was achieved at 1.2-V V_{DD} with +1.6-V of back-gate bias voltage (V_{BB}). The best power density of 33.4- μ W/MHz was reached at 0.5-V V_{DD} with +0.8-V V_{BB} . At sleep mode, when the clock is cut off, the lowest value of 3-nA current leakage was achieved at 0.5-V V_{DD} with -2.0-V V_{BB} . The completed SoC was benchmarked with the Dhrystone and Coremark tests, and the results were 1.27 DMIPS/MHz and 2.4 Coremark/MHz, respectively.

The remainder of this paper is organized as follows. Section 2 describes the architecture of the proposed SoC chip. Section 3 gives details of the measurement results. Finally, Section 4 concludes the paper.

2. Architecture

Fig. 1 shows the proposed architecture of the microcontroller. The core processor is the VexRiscv CPU generated with full options [26], including cache trashing, cache exceptions, single cycle barrel shifter, debug module via JTAG, dynamic branching, and Memory Management Unit (MMU). Comparing to the original design from the SpinalHDL [26], for better fitting in the chip, the caches sizes were increased a little bit to 4.5KB for each of the data and instruction caches.

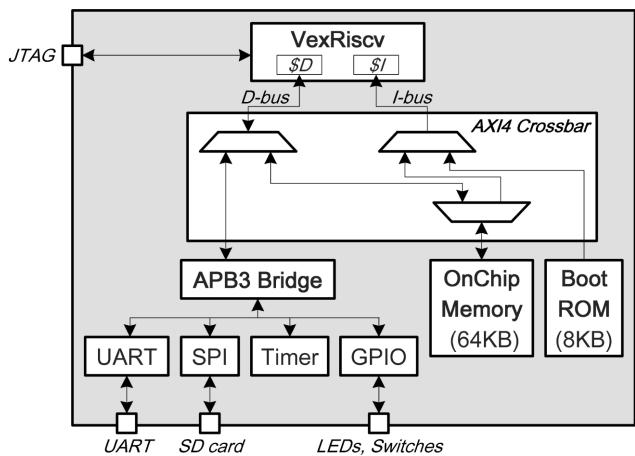


Fig. 1 The microcontroller architecture.

The SPI controller was added for the usage of the SD-card. The GPIO has 16 LEDs and 16 switches. The 64KB size of the on-chip memory was chosen due to the size limitation of the intended fabricated chip. The 8KB of boot ROM contains 7KB of hard-code in combinational logics and 1KB of a stack in SRAM. The 1KB of SRAM stack can be used later after boot. The 7KB hard-code boot ROM initis the Control/Status Registers (CSRs) in the CPU, prints the initial text to the UART, starts the SD-card, loads the program from the SD-card to the on-chip memory, and jumps to the on-chip memory and executes there. With this boot flow, the microcontroller can self-boot to run any desired software in the SD-card for an embedded application. The source codes and guide for replicating this proposed microcontroller are published in the given repository [29].

3. Evaluation

3.1 Silicon-on-thin-BOX (SOTB)

Fig. 2 shows the structure of the SOTB Complementary Metal Oxide Semiconductor (CMOS) with the triple wells of deep N-well, N/P-well, and N+/P+, the Shallow Trench Isolations (STIs), and the ultrathin Buried-OXide (BOX) layers. SOTB technology is one of the Fully-Depleted Silicon-On-Insulator (FD-SOI) technology families with the key innovation of the ultrathin BOX layer. The layer that allows an appropriate back-gate bias voltage to be applied, thus increasing the control of transistors much more efficiently [28]. Furthermore, SOTB devices are good candidates for low-voltage operation due to the low impurity concentration in the channel regions that leads to small variation [27]. By changing the back-gate bias voltage, the operation of the SOTB CMOS can be fine-tuned to satisfy either the low-power or the high-performance requirements. To be specific, when the reverse back-gate bias voltage is applied, the leakage current can be reduced significantly. And when the forward back-gate bias voltage is deployed, the maximum operating frequency can be increased profoundly. Therefore, a SOTB microcontroller chip can be used for a wide range of embedded applications.

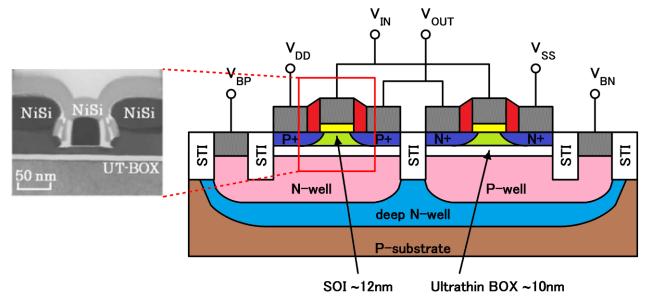


Fig. 2 Cross-section of the SOTB CMOS (modified from [28]).

3.2 Measurement result

The fabricated chips used 160-pin QFP packages. The PCB test boards with necessary accessories were built to test the chips. Fig. 3 shows a PCB platform with a chip inside the socket, a built-in USB-to-UART interface, programmable

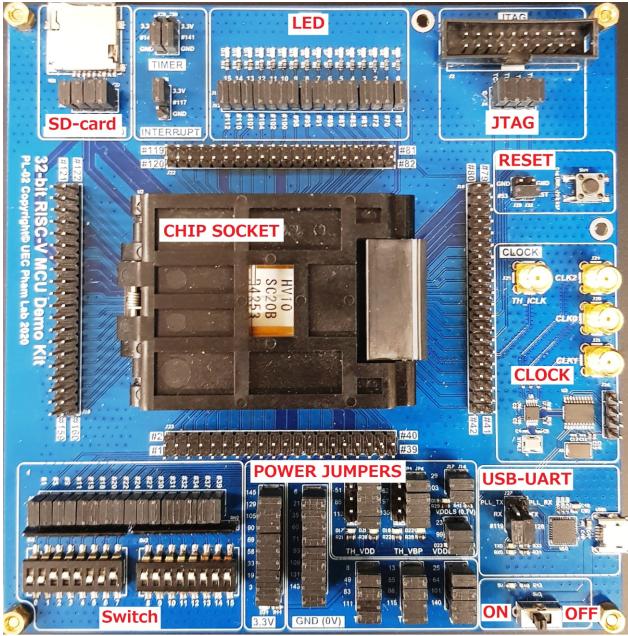


Fig. 3 Test board (PCB) with the chip inside the socket.

clocks provided by a clock generator chip, and other peripherals such as SD-card socket, JTAG header, LEDs, and switches. The power supplies can be drawn directly from the USB interface or external power sources by using or not using the power jumpers. The operating clock also can be feed from an external source via the SMA connector.

The chip micrograph is given in Fig. 4. It can be seen that the four 16KB SRAM macros made up a total of 64KB on-chip memory for the system. The 16KB SRAM macro was chosen because it is the largest SRAM macro available in the 65-nm SOTB process. The 8KB of boot ROM also contains one 1KB SRAM macro for the stack. As shown in Fig. 4, there is one VexRiscv core placed in the bottom with two caches of instruction and data that sit right next to its left and right. Each cache contained four 1KB SRAM macros and one 512B SRAM macro, thus 4.5KB in total. The layout was $1,436.24\text{-}\mu\text{m}$ in width and $921.6\text{-}\mu\text{m}$ in height that sits on the $1.5\times 1.0\text{-mm}^2$ die.

The main features of the chip are highlighted in Table I.

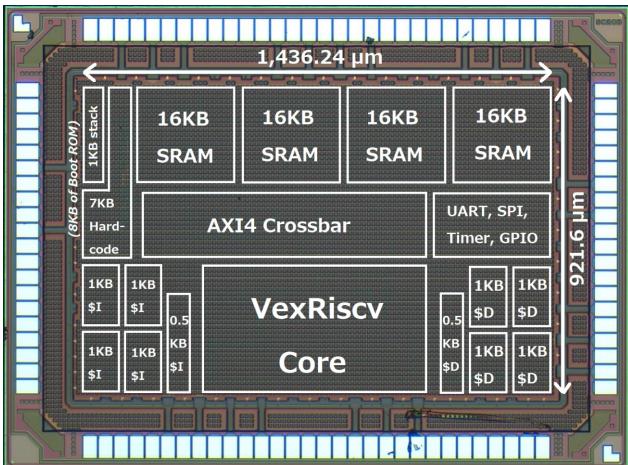


Fig. 4 The chip micrograph with floorplan.

Table I Chip features summary.

Technology	65-nm SOTB
Layout size	$1,323,640\text{-}\mu\text{m}^2 \approx 1.32\text{-mm}^2$
Gate-count	349,061
I/O V_{DD}	3.3-V
Core V_{DD}	0.5-V to 1.2-V
Benchmarks	1.27 DMIPS/MHz 2.4 Coremark/MHz
Peak performance	at 1.2-V V_{DD} with +1.6-V V_{BB} : $F_{Max} = 156\text{-MHz}$ $P_{Active} = 269.54\text{ }\mu\text{W/MHz}$
Best power density	at 0.5-V V_{DD} with +0.8-V V_{BB} : $F_{Max} = 15\text{-MHz}$ $P_{Active} = 33.4\text{-}\mu\text{W/MHz}$
Best leakage current	at 0.5-V V_{DD} with 0-V V_{BB} : 4.33- μA at 0.5-V V_{DD} with -2.0-V V_{BB} : 3-nA

The layout size was about 349,061 gate-counts on a 1.32-mm^2 of die area. The I/O V_{DD} was fixed at 3.3-V while the core V_{DD} can operate in the range of 0.5-V to 1.2-V. The processor achieved the benchmark results of 1.27 DMIPS/MHz and 2.4 Coremark/MHz. According to the table, at the high-performance operating mode, the chip can perform at 156-MHz with the highest V_{DD} and a forward V_{BB} . The best power density was $33.4\text{-}\mu\text{W/MHz}$ with the lowest operating V_{DD} . At the sleep mode, the clock is cut off, and a reversed V_{BB} is applied; the lowest leakage current of 3-nA was achieved, as shown in the table.

Fig. 5 shows the changes in F_{Max} corresponding to V_{DD} and V_{BB} . Overall, the F_{Max} performances increased almost linear with the increment of V_{DD} . To be specific, with no bias (i.e., $V_{BB} = 0\text{-V}$), F_{Max} values ranged from 12-MHz at 0.6-V V_{DD} to 104-MHz at 1.2-V V_{DD} ; the changes were about 15-MHz per 0.1-V of V_{DD} . For V_{BB} from -2.0-V to +0.8-V, F_{Max} values also increased nearly linear; there was about 18-MHz improvement in F_{Max} for each 0.4-V increment of V_{BB} . However, when a $V_{BB} \geq 1.2\text{V}$ was applied, the F_{Max} increment became very little to none, as seen in the figure. The maximum F_{Max} value of 156-MHz was achieved at 1.2-V V_{DD} with +1.6-V V_{BB} . At -2.0-V V_{BB} , the microcontroller can function only with $V_{DD} \geq 0.9\text{-V}$.

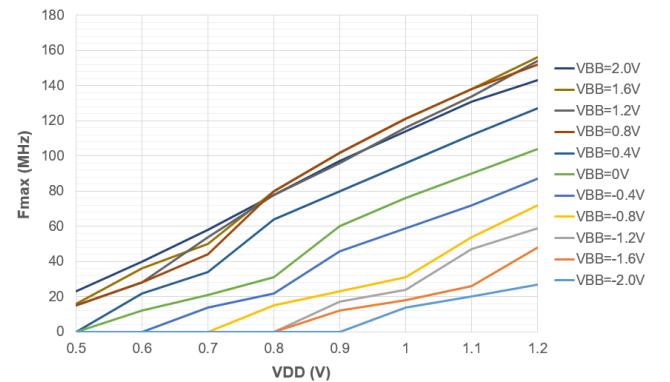


Fig. 5 Maximum operating frequency (F_{Max}) vs. supply voltages.

Fig. 6 gives the variations in power consumption corresponding to V_{DD} and V_{BB} . Overall, the changes were

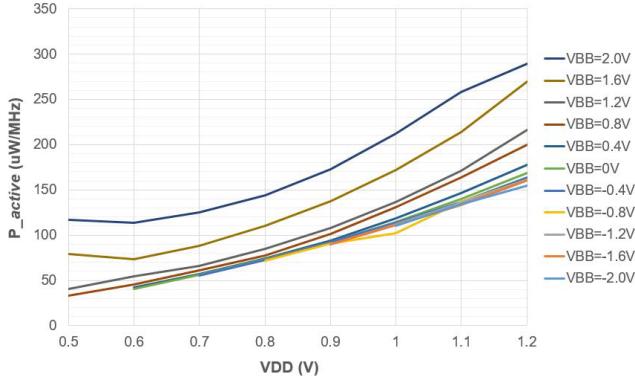


Fig. 6 Operating power consumption (P_{active}) vs. supply voltages.

almost linear with the V_{DD} increment. For no bias, the power consumptions ranged from $40.8\text{-}\mu\text{W}/\text{MHz}$ at 0.6-V V_{DD} to $169.04\text{-}\mu\text{W}/\text{MHz}$ at 1.2-V V_{DD} ; the changes were about $21\text{-}\mu\text{W}/\text{MHz}$ for each 0.1-V increment of V_{DD} . At reversed back-gate bias, there were only tiny reductions in consumptions, as seen in the figure. In contrast, P_{Active} values increased quite a lot with forwarding back-gate bias. Comparing to the no bias power consumption line, the $+2.0\text{-V}$ V_{BB} power consumption line was about $1.86\times$ higher at all range of V_{DD} . The best power density of $33.4\text{-}\mu\text{W}/\text{MHz}$ was achieved at the lowest operating point of 0.5-V V_{DD} with $+0.8\text{-V}$ V_{BB} .

Fig. 7 shows the changes in leakage current corresponding to V_{DD} and V_{BB} . The leakage current values were measured at sleep mode when the clock is cut off. At no bias, I_{leak} values ranged from $4.33\text{-}\mu\text{A}$ at 0.5-V V_{DD} to $25\text{-}\mu\text{A}$ at 1.2-V V_{DD} . From $+0.8\text{-V}$ to -1.2-V V_{BB} , the I_{leak} values reduced roughly about one order of magnitude per 0.4-V V_{BB} reduction. However, the $V_{\text{BB}} \leq -1.6\text{-V}$ lines can not result in further reduction of leakage currents due to the Gate-Induced Drain Leakage (GIDL) phenomenon [28]. The best leakage current was 3-nA with 0.5-V V_{DD} and -2.0-V V_{BB} .

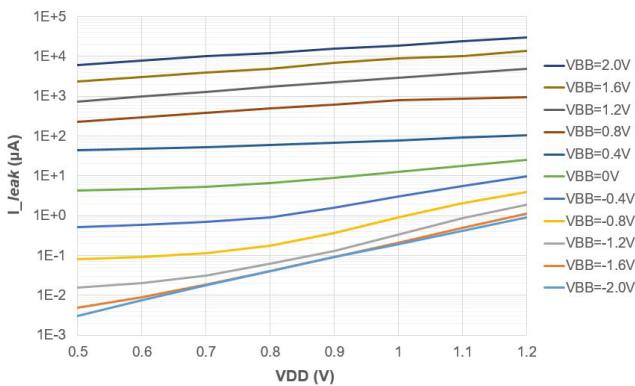


Fig. 7 Leakage current (I_{leak}) vs. supply voltages.

3.3 Comparison and discussion

For the comparison, Table II gives the results of this work and two other recent 32-bit RISC-V microcontrollers. To provide a better point-of-view, the results of PULPv2 [21] and Duran *et al.* [23] were scaled to the equivalent results of a 65-nm node by using the equations from [30]. It is noted that

Table II Comparison with other 32-bit RISC-V microcontrollers.

Design	Duran <i>et al.</i> (2017) [23]	PULPv2 (2017) [21]	This work (2020)
ISA	RV32IM	RV32IMC	RV32IM
No. of cores	1	4	1
Core V_{DD} (V)	1.2	0.32 to 1.15	0.5 to 1.2
Process	130-nm	28-nm	65-nm
F_{Max} (MHz)	160	825	156
P_{Active} ($\mu\text{W}/\text{MHz}$)	167	20.7	33.4
Leakage power (mW) *			
running	N/A	0.37	0.4
idle (clock-gated)	N/A	N/A	0.003
<i>Scaled to 65-nm by using equations [30]</i>			
Process	65-nm	65-nm	65-nm
F_{Max} (MHz)	304.88	388.68	156
P_{Active} ($\mu\text{W}/\text{MHz}$)	23.05	126.6	33.4
Leakage power (mW) *			
running	N/A	2.22	0.4
idle (clock-gated)	N/A	N/A	0.003

* measured at 0.6-V V_{DD} & no bias.

because the equations in [30] did not have the parameters for the 28-nm process, the scaled values of PULPv2 [21] were calculated by using the settings of the 32-nm process instead.

Although the F_{Max} in this work is the lowest value in the table, the comparison may not reflect the true nature of the architecture. The reason is that for those designs without integrated Phase-Locked Loop (PLL) or Frequency-Locked Loop (FLL), the operating frequencies heavily depended on the I/O circuits. For example, the chip in [21] had integrated FLL while those chips in [23] and in this work had not. Therefore, the operating frequency in [21] could easily go higher than 500-MHz, while those in [23] and in this work were limited by the general digital I/Os, as seen in the table.

For the dynamic power consumption of P_{Active} , the result of this work was measured while running the Dhrystone test, while the result in [23] was measured while running three while loops. Therefore, if the microcontroller in [23] was running the Dhrystone test when being measured, the value of $23.05\text{-}\mu\text{W}/\text{MHz}$ should be a bit higher. For the result of [21], it can be argued that if with a single-core processor, its power consumption will be much less. Hence, the power density of a single-core of PULPv2 can be roughly approximated by $126.6/4 = 31.65\text{-}\mu\text{W}/\text{MHz}$, closes to the value of $33.4\text{-}\mu\text{W}/\text{MHz}$ of this work.

For leakage power comparison, the PULPv2 chip [21] reported 0.37-mW while running at 0.6-V V_{DD} with no bias (i.e., $V_{\text{BB}} = 0\text{-V}$). Scaling to the equivalent result of the 65-nm node, 0.37-mW became 2.22-mW. With a similar argument about single-core versus multi-core, the leakage power of a single-core could be roughly estimated to about $2.22/4 = 0.555\text{-mW}$. Thus, the 0.4-mW result of this work still yields the best performance in the table. It is also noted that the best values of leakage powers in this work were not brought to the comparison table because the results with reserved back-gate bias voltages were not reported in those papers [21, 23]. Furthermore, the results at sleep-mode with

the applied clock-gating technique were also not presented in the papers [21, 23]. For this work, the leakage power with clock-gating reduced nearly $133.33 \times$ to $3\text{-}\mu\text{W}$ compared to the without clock-gating result at the same operating condition.

To conclude, a truly fair comparison between implementations were hard to achieve due to the complex nature of microcontroller architecture. Table II has already brought a proper perspective for the comparison, but yet, it may not ultimately reflect all of the pros and cons of all implementations. However, it can be said that the proposed microcontroller chip in this paper has achieved average performances of F_{Max} and P_{Active} and a genuinely good leakage power value. With the powerful tool of back-gate biasing, the proposed microcontroller can be used for a wide range of embedded applications in both means of low-power and high-performance settings.

4. Conclusion

The 32-bit RISC-V microcontroller based on RV32IM VexRiscv CPU was presented in this paper. The completed system-on-chip was built and fabricated with the 65-nm SOTB technology. Its measurement results were presented and discussed with other recent silicon-proof publications. The proposed SoC was benchmarked by using the Dhrystone and Coremark tests, and the results were 1.27 DMIPS/MHz and 2.4 Coremark/MHz, respectively. The layout occupied 1.32-mm² of die area with 349,061 gate-counts. The core V_{DD} range is 0.5-V to 1.2V, and the core back-gate bias voltage range is -2.0-V to +2.0-V. The measurement results show the highest operating frequency was 156-MHz, the lowest operating V_{DD} was 0.5-V, the best power density was 33.4- $\mu\text{W}/\text{MHz}$, and the best current leakage was 3-nA. The SOTB technology gave not only the astonishing ultra-low-power characteristic but also the flexibility of operating modes. As a result, with back-gate bias voltage control, the proposed implementation can be suited for a wide range of embedded applications nowadays in both needs of low-power or high-performance microcontroller systems.

Acknowledgments

This paper is based on results obtained from a project, JPNP16007, commissioned by the New Energy and Industrial Technology Development Organization (NEDO). This work is also supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc., Cadence Design Systems, Inc., Renesas Electronics Corp., and Nippon Systemware Co., Ltd.

References

- [1] S.P. Dandamudi: *Guide to RISC Processors: for Programmers and Engineers* (Springer-Verlag, New York, 2005) 1 (DOI: 10.1007/b139084).
- [2] Wikipedia: ARM architecture (2020) https://en.wikipedia.org/wiki/ARM_architecture.
- [3] Wikipedia: Reduced instruction set computer (2020) https://en.wikipedia.org/wiki/Reduced_instruction_set_computer.
- [4] R. Goodwins: Chips that pass in the night: How risky is RISC-V to Arm, Intel and the others? Very (2020) https://www.theregister.co.uk/2020/03/09/risc_v_intel_amd_arm/.
- [5] A. Waterman, *et al.*: The RISC-V instruction set manual, vol. I, ver. 2.0, UCB/EECS-2014-54, EECS Department, University of California, Berkeley (2014) <https://www2.eecs.berkeley.edu/Pubs/TechRpts/2014/EECS-2014-54.pdf>.
- [6] RISC-V Foundation (2020) <https://riscv.org/risc-v-foundation/>.
- [7] A. Waterman and K. Asanović: The RISC-V instruction set manual, vol. I, ver. 2.2, SiFive Inc. and EECS Department, University of California, Berkeley (2017) <https://content.riscv.org/wp-content/uploads/2017/05/riscv-spec-v2.2.pdf>.
- [8] RISC-V Foundation: RISC-V software status (2020) <https://riscv.org/software-status/>.
- [9] Y. Wang and N. Tan: “An application-specific microprocessor for energy metering based on RISC-V,” IEEE Int. Conf. on IC Design and Tech. (ICICDT) (2019) 1 (DOI: 10.1109/ICICDT.2019.8790918).
- [10] A. Munir, *et al.*: “Fast reliable verification methodology for RISC-V without a reference model,” Int. Workshop on Microprocessor and SOC Test, Security and Verification (MTV) (2018) 12 (DOI: 10.1109/MTV.2018.00012).
- [11] E. Gur, *et al.*: “FPGA implementation of 32-bit RISC-V processor with web-based assembler-disassembler,” Int. Symp. on Fundamentals of Electrical Engi. (ISFEE) (2018) 1 (DOI: 10.1109/ISFEE.2018.8742406).
- [12] D.K. Dennis, *et al.*: “Single cycle RISC-V micro architecture processor and its FPGA prototype,” Int. Symp. on Embedded Computing and System Design (ISED) (2017) 1 (DOI: 10.1109/ISED.2017.8303926).
- [13] K. Patsidis, *et al.*: “A low-cost synthesizable RISC-V dual-issue processor core leveraging the compressed instruction set extension,” Microprocessors and Microsystems **61** (2018) 1 (DOI: 10.1016/j.micpro.2018.05.007).
- [14] K. Asanović, *et al.*: The rocket chip generator, UCB/EECS-2016-17, EECS Department, University of California, Berkeley (2016) <http://www2.eecs.berkeley.edu/Pubs/TechRpts/2016/EECS-2016-17.html>.
- [15] SiFive, Inc.: SiFive E31 manual, v19.08p0 (2019) <https://sifive.cdn.prismic.io/sifive%2Fc89f6e5a-cf9e-44c3-a3db-04420702dcc1-sifive+e31+manual+v19.08.pdf>.
- [16] SiFive, Inc.: SiFive U54 manual, v19.08p2p0 (2019) https://sifive.cdn.prismic.io/sifive%2Fe05812-e9cd-4553-bfef-c7e715088055_sifive_coreip_U54MC_AXI4_rtl_v19_08p2p0_release_manual.pdf.
- [17] M. Gautschi, *et al.*: “Near-threshold RISC-V core with DSP extensions for scalable IoT endpoint devices,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **25** (2017) 2700 (DOI: 10.1109/TVLSI.2017.2654506).
- [18] F. Zaruba and L. Benini: “The cost of application-class processing: energy and performance analysis of a Linux-ready 1.7-GHz 64-Bit RISC-V core in 22-nm FDSOI technology,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **27** (2019) 2629 (DOI: 10.1109/TVLSI.2019.2926114).
- [19] R. Holler, *et al.*: “Open-source RISC-V processor IP cores for FPGAs — overview and evaluation,” Mediterranean Conf. on Embedded Computing (MECO) (2019) 1 (DOI: 10.1109/MECO.2019.8760205).
- [20] F. Conti, *et al.*: “PULP: a ultra-low power parallel accelerator for energy-efficient and flexible embedded vision,” Journal of Signal Processing Systems **84** (2016) 339 (DOI: 10.1007/s11265-015-1070-9).
- [21] D. Rossi, *et al.*: “Energy-efficient near-threshold parallel computing: the PULPv2 cluster,” IEEE Micro **37** (2017) 20 (DOI: 10.1109/MM.2017.3711645).
- [22] C. Duran, *et al.*: “A 32-bit RISC-V AXI4-lite bus-based microcontroller with 10-bit SAR ADC,” IEEE Latin American Symp. on Circ. and Syst. (LASCAS) (2016) 315 (DOI: 10.1109/LASCAS.2016.7451073).
- [23] C. Duran, *et al.*: “A system-on-chip platform for the internet of things featuring a 32-bit RISC-V based microcontroller,” IEEE Latin American Symp. on Circ. and Syst. (LASCAS) (2017) 1 (DOI: 10.1109/LASCAS.2017.8126878).
- [24] SiFive, Inc.: SiFive FE310-G000 preliminary datasheet, v1p5 (2017) https://sifive.cdn.prismic.io/sifive%2Ffeb6f967-ff96-418f-9af4-a7f3b7fd1dfc_fe310-g000-ds.pdf.

- [25] SiFive, Inc.: SiFive FE310-G002 preliminary datasheet, v1p0 (2019) https://sifive.cdn.prismic.io/sifive%2F3d777659-a0dd-49ed-a011-5bebba17aecf_fc310-g002-ds.pdf.
- [26] SpinalHDL: A FPGA friendly 32-bit RISC-V CPU implementation (2020) <https://github.com/SpinalHDL/VexRiscv>.
- [27] H. Okuhara, *et al.*: “Power optimization methodology for ultralow power microcontroller with silicon on thin BOX MOSFET,” IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **25** (2017) 1578 (DOI: [10.1109/TVLSI.2016.2635675](https://doi.org/10.1109/TVLSI.2016.2635675)).
- [28] T. Ishigaki, *et al.*: “Effects of device structure and back biasing on HCI and NBTI in silicon-on-thin-BOX (SOTB) CMOSFET,” IEEE Trans. Electron Devices **58** (2011) 1197 (DOI: [10.1109/TED.2011.2107520](https://doi.org/10.1109/TED.2011.2107520)).
- [29] T.-T. Hoang: VexRiscv 32-bit MCU (2020) <https://github.com/thuchoang90/VexRiscv>.
- [30] A. Stillmaker and B. Baas: “Scaling equations for the accurate prediction of CMOS device performance from 180 nm to 7 nm,” Integration **58** (2017) 74 (DOI: [10.1016/j.vlsi.2017.02.002](https://doi.org/10.1016/j.vlsi.2017.02.002)).