Analog Output Subsystem: OPA192 & OPA197 Integration

1. Introduction

This document presents a detailed design for the analog output stage of a Data Acquisition (DAQ) system, ensuring accurate signal conditioning, stability, and robustness.

The DAQ outputs are classified into two voltage stages:

- DAC0-3 (3.3V Stage)
    - Uses OPA192 as the buffer op-amp.
    - Output range: 0V to 3.3V.
- DAC4-7 (±12V Stage)
    - Uses OPA197 for high-voltage amplification.
    - Output range: -12V to +12V.

1.1. Design Objectives

The core objectives of this design include:

1. Accurate DAC output scaling
2. Ensuring stability with capacitive loads
3. Consistent bandwidth (~100 kHz) across both stages
4. Minimized voltage drop across R_ISO
5. Optimized resistor values for precise scaling

2. DAC8568 Output Scaling for 3.3V and ±12V Stages

The DAC8568 generates a 0V to 2.5V output, which must be amplified and shifted to match the respective voltage stages.

2.1. Output Calculation

For a generalized output scaling formula, the output voltage is given by:

$$V_{OUT} = \left(1 + \frac{R_{FB}}{R_{G2}} + \frac{R_{FB}}{R_{G1}}\right) V_{DAC} - \left(\frac{R_{FB}}{R_{G2}}\right) V_{REF}$$

Where:

- $V_{DAC} =$ DAC output voltage (0 to 2.5V)
- $V_{REF} =$ 2.5V DAC reference
- $R_{FB} =$ Feedback resistor
- $R_{G1}, R_{G1} =$ Gain resistors

The resistor network is designed separately for each voltage stage.

3. DAC8568 Output Scaling for 3.3V Stage

The 3.3V stage (DAC0-3) uses OPA192 in a non-inverting amplifier configuration.

3.1. Gain Calculation

The gain is:

$$G = \frac{V_{OUT_{max}} - V_{OUT_{min}}}{V_{DAC_{max}} - V_{DAC_{min}}}$$

$$G = \frac{3.3V - 0V}{2.5V - 0V} = 1.32$$

3.2. Resistor Selection

For a non-inverting amplifier, the gain is:

$$G = 1 + \frac{R_F}{R_G}$$

Choosing $R_G = 10\text{k}\Omega$:

$$1.32 = 1 + \frac{R_F}{10\text{k}\Omega}$$

$$R_F = (1.32 - 1) \cdot 10\text{k}\Omega = 3.2\text{k}\Omega$$

3.3. Output Resolution Calculation

- DAC resolution:

$$Resolution_{DAC} = \frac{V_{REF}}{2^{16}} = \frac{2.5V}{65536} \approx 0.038mV$$

- Scaled output resolution:

$$Resolution_{OUT} = Resolution_{DAC} \cdot G = 0.038mV \cdot 1.32 \approx \mathbf{0.05}\boldsymbol{mV}$$

3.4. Final Resistor Values

Component	Value
R_F	$3.2\text{k}\Omega$
R_G	$10\text{k}\Omega$

4. DAC8568 Output Scaling for ±12V Stage

The ±12V stage (DAC4-7) uses OPA197 to achieve high-voltage amplification.

4.1. Gain Calculation

The gain is:

$$G = \frac{V_{OUT_{max}} - V_{OUT_{min}}}{V_{DAC_{max}} - V_{DAC_{min}}}$$

$$G = \frac{12V - (-12V)}{2.5V - 0V} = \frac{24V}{2.5V} = 9.6$$

4.2. Resistor Selection

For a non-inverting amplifier, the gain is:

$$G = 1 + \frac{R_F}{R_G}$$

Choosing $R_G = 10\text{k}\Omega$:

$$9.6 = 1 + \frac{R_F}{10\text{k}\Omega}$$

$$R_F = (9.6 - 1) \cdot 10\text{k}\Omega = 86\text{k}\Omega$$

4.3. Output Resolution Calculation

Scaled output resolution:

$$Resolution_{OUT} = Resolution_{DAC} \cdot G = 0.038mV \cdot 9.6 \approx \mathbf{0.3648mV}$$

4.4. Final Resistor Values

Component	Value
R_F	$86\text{k}\Omega$
R_G	$10\text{k}\Omega$

5. Stability Considerations

5.1. OPA192 (3.3V Stage)

- Low-power op-amp with 1 MHz GBW.
- Requires R_{ISO} for stability with higher capacitive loads.
- Chosen values:
    - $R_{ISO} = 68\Omega$
    - $C_{LOAD} = 20nF$

5.2. OPA197 (±12V Stage)

- Precision op-amp with 2.5 MHz GBW.
- Stabilized by R_ISO for capacitive loads.
- Chosen values:
    - $R_{ISO} = 110\Omega$
    - $C_{LOAD} = 12nF$

6. Load Stability & Voltage Drop Analysis

The cutoff frequency for stability is:

$$f_c = \frac{1}{2\,\pi\,R_{ISO}\,C_{LOAD}}$$

For the 3.3V stage:

$$f_c = \frac{1}{2 \cdot \pi \cdot\ 68\ \cdot 20nF} \approx 117\ kHz$$

For the ±12V stage:

$$f_c = \frac{1}{2 \cdot \pi \cdot 110\ \cdot 12nF} \approx 120\ kHz$$

Voltage drop across R_{ISO}:

$$V_{drop} = I_{load} \cdot R_{ISO}$$

For 5mA output current:

- OPA192 (3.3V Stage, $R_{ISO} = 68\Omega$)

$$V_{drop_{3V3}} = 5mA \cdot 68\Omega = 0.34\text{V}$$

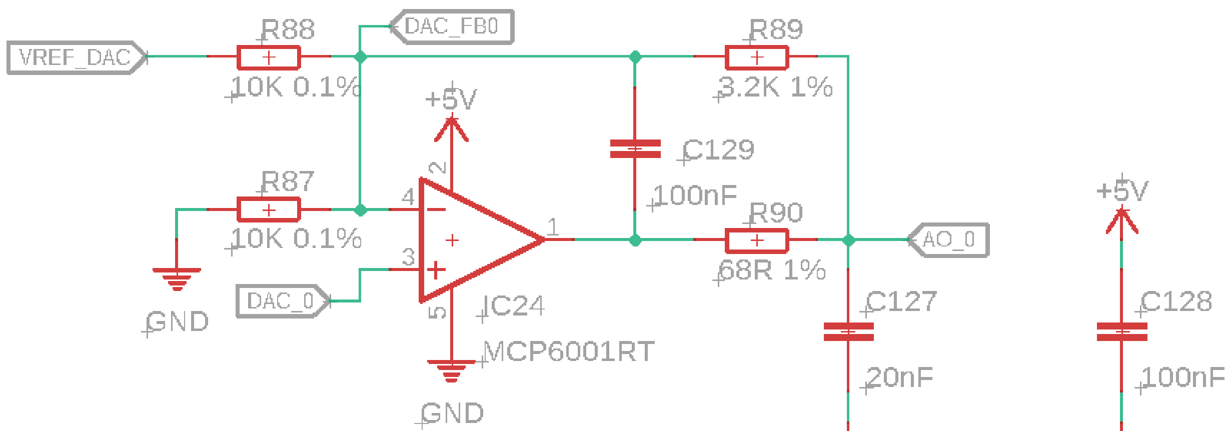
- OPA197 (±12V Stage, $R_{ISO} = 110\Omega$)

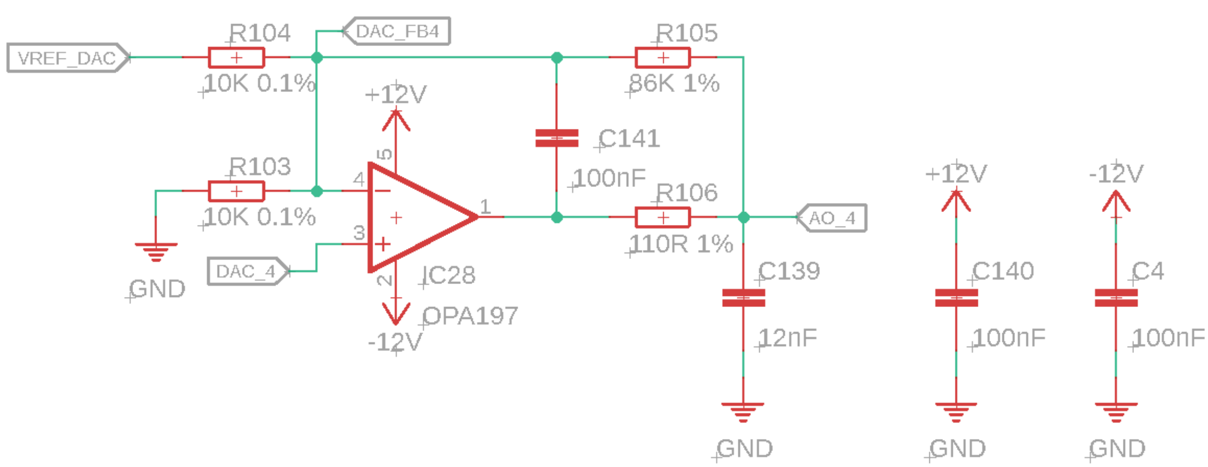
$$V_{drop_{12V}} = 5mA \cdot 110\Omega = 0.55\text{V}$$

7. Final Optimized Circuit

7.1. Parameter Summary

DAC Channel	Op-Amp	Supply Voltage	Output Voltage Range	R_{ISO}	C_{LOAD}	Cutoff Frequency (kHz)
DAC0-3	OPA192	5V	0V to 3.3V	68Ω	20nF	117 kHz
DAC4-7	OPA197	±12V	-12V to +12V	110Ω	12nF	120 kHz





8. Purpose of the 10kΩ Pulldown Resistors

The pulldown resistors serve a critical role in ensuring signal stability by preventing the op-amp's inverting input from floating if the DAC output becomes high impedance (tri-stated or powered down). A floating inverting input can result in:

- Op-amp instability or oscillations
- Increased noise sensitivity
- Unexpected voltage drift due to leakage currents

To evaluate whether the 10kΩ resistors are necessary, we analyze their voltage effect and impact on circuit stability for both the 3.3V and ±12V output stages.

8.1. Voltage Division & Leakage Current Analysis

If the DAC output enters high impedance mode (open circuit), the pulldown resistor determines the voltage at the op-amp's inverting input.

8.2. Calculation for the 3.3V Stage (OPA192)

- Op-amp: OPA192 (low-power, rail-to-rail, 5V single-supply)
- Pulldown resistor: $R_{PD} = 10k\Omega$
- DAC reference voltage: $V_{DAC_{max}} = 2.5V, V_{DAC_{min}} = 0V$
- Op-amp bias current (typical): $I_B = 1pA$
- Leakage current estimate $I_{leak} = 10nA$ (conservative assumption)

Voltage at the inverting input when DAC is in high-Z mode:

$$V_{IN-} = R_{PD} I_{leak} = 10k\Omega \cdot 10\text{nA} = 0.1\text{mV}$$

8.3. Calculation for the ±12V Stage (OPA197)

- Op-amp: OPA197 (precision, ±12V supply)
- Pulldown resistor: $R_{PD} = 100k\Omega$
- DAC reference voltage: $V_{DAC_{max}} = 2.5V, V_{DAC_{min}} = 0V$
- Op-amp bias current (typical): $I_B = 10pA$
- Leakage current estimate $I_{leak} = 20nA$

Voltage at the inverting input when DAC is in high-Z mode:

$$V_{IN-} = R_{PD} I_{leak} = 100k\Omega \cdot 20\text{nA} = 2\text{mV}$$

8.4 Impact on Stability & Frequency Response

The inverting input is highly sensitive. Without the pulldown resistor:

- Any residual charge on the PCB traces could cause voltage drift.
- Leakage currents from the DAC or op-amp could accumulate, shifting the voltage.
- Noise from adjacent signals could capacitively couple into the floating node, leading to oscillations.

Adding R_{PD} prevents floating and keeps the circuit deterministic even if the DAC is disabled.

8.5. Power Dissipation Analysis

For continuous operation, power consumption due to the pulldown resistors is:

$$P = \frac{V^2}{R}$$

The 3.3V Stage:

$$P = \frac{5V^2}{10k\Omega} = 2.5mW$$

The ±12V Stage:

$$P = \frac{12V^2}{100k\Omega} = 1.44mW$$