Analog Input Subsystem

1. Introduction

This document provides a detailed overview of the Analog Input (AI) subsystem of the DAQ system, focusing on signal acquisition, amplification, filtering, and communication with the ADC. It covers key components, signal flow, and considerations for optimal performance.

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2. System Overview

The Analog Input Subsystem consists of:

- 16 Differential Analog Inputs (AI)
- Programmable Gain Amplifiers (PGA) for signal conditioning
- Multiplexers for channel selection
- High-speed 14-bit ADC for conversion
- SPI communication for data transfer
- Power distribution and filtering

3. Analog Input (16 Channels)

The analog input section of the DAQ system is designed to provide high precision and flexibility, capable of acquiring signals from various sources.

3.1 Key Components

- External 14-bit ADC: ADS9234RIRHBR, a 14-bit, 3.5-MSPS dual SAR ADC with simultaneous sampling, internal reference, and enhanced SPI for high-speed acquisition.
- Multiplexers: 2 × DG409 for channel selection, enabling flexible signal routing to the ADC.
- Programmable Gain Amplifiers (PGA): ADA4254ACPZ for scalable input ranges, ensuring adaptability to different signal levels.

3.2 ADC Communication & Control

- SPI Interface:
    - SCLK (Clock Signal)
    - MOSI (Master Out Slave In)
    - MISO (Master In Slave Out)
    - CS (Chip Select)
- Control Signals:
    - ADC_RDY: Data ready indication
    - ADC_RST: Reset signal
    - MISO_SEL: Selects the correct SPI MISO line

3.3 Analog Input Switching Mechanism (Differential and Single-Ended Mode)

To maximize the flexibility of the system while maintaining accurate signal acquisition, a DG409 multiplexer is used to route the selected input signal to the ADA4254 programmable gain amplifier (PGA) before being fed into the ADS9234 ADC.

Each DG409 consists of four normally open SPST switches that can be controlled digitally. The AI+ signals are routed through the upper switch bank, while the corresponding AI- signals are routed through the lower switch bank. For differential measurements, both AI+ and AI- channels are selected. For single-ended measurements, either AI+ or AI- can be selected, while the unselected input is connected to ground.

3.4 Channel Selection Control (Differential and Single-Ended)

The DG409 multiplexer allows the selection of one of four differential input pairs or a single-ended configuration. The selection is made via two digital control inputs (A0, A1), which follow the logic below:

Differential Input Mode

A1	A0	Selected AI+ / AI- Pair
0	0	AI1+ / AI2-
0	1	AI3+ / AI4-
1	0	AI5+ / AI6-
1	1	AI7+ / AI8-

Single-Ended Input Mode

A1	A0	Selected Input	Other Input
0	0	AI1+ or AI2-	GND
0	1	AI3+ or AI4-	GND
1	0	AI5+ or AI6-	GND
1	1	AI7+ or AI8-	GND

By setting the control signals A0 and A1 correctly, any of the available differential or single-ended inputs can be connected to the PGA and ADC. The multiplexer transitions occur within 160ns, ensuring minimal signal delay.

3.5 Software Control of Channel Selection

In the software, the channel selection is managed by setting the GPIO pins connected to the DG409 control inputs (A0, A1). The selection process follows these steps:

1. Disable Data Acquisition: Before switching channels, the ADC sampling process is halted to prevent incorrect readings during transitions.
2. Set Multiplexer Control Lines: The microcontroller sets the GPIO pins corresponding to A0 and A1 based on the required channel.
3. Configure for Single-Ended or Differential Mode: If single-ended mode is selected, the corresponding AI- or AI+ input is connected to ground in software.
4. Delay for Settling Time: A short delay (~200ns) is introduced to allow the multiplexer switches to stabilize.
5. Enable Data Acquisition: Once the multiplexer output has stabilized, ADC sampling resumes.

This function allows dynamic switching between **differential and single-ended** configurations, with the ability to choose whether **AI+ or AI-** is used as the active signal.

3.6 PGA and ADC Interaction

Once a selected differential input signal is passed through the DG409 multiplexer, it is fed into the ADA4254 programmable gain amplifier (PGA). The gain of the PGA can be controlled dynamically based on system requirements to optimize signal-to-noise ratio before it is sent to the ADS9234 ADC for digitization.

3.7 Bandwidth for Each Gain Setting

The bandwidth is determined by the ADC's Nyquist limit and the PGA's frequency response. Lower gains maintain the ADC's full bandwidth, while higher gains are limited by the PGA.

Gain	Max Bandwidth (Hz)
1/16	1,750,000
1/8	1,750,000
1/4	1,750,000
1/2	1,750,000
1	1,750,000
2	1,750,000
4	1,750,000
8	1,250,000
16	625,000
32	312,500
64	156,250
128	78,125

3.8 Input Ranges for Different Gains

The input ranges are defined by the reference voltage (VREF = 2.5V), positive supply voltage (+12V), and negative supply voltage (-12V).

Gain	Differential Input Range (±V)	Positive Input Range (0 to V)	Negative Input Range (0 to -V)
1/16	±80.0	0 to 40.0	0 to -40.0
1/8	±40.0	0 to 20.0	0 to -20.0
1/4	±20.0	0 to 10.0	0 to -10.0
1/2	±10.0	0 to 5.0	0 to -5.0
1	±5.0	0 to 2.5	0 to -2.5
2	±2.5	0 to 1.25	0 to -1.25
4	±1.25	0 to 0.625	0 to -0.625
8	±0.625	0 to 0.3125	0 to -0.3125
16	±0.3125	0 to 0.15625	0 to -0.15625
32	±0.15625	0 to 0.078125	0 to -0.078125
64	±0.078125	0 to 0.0390625	0 to -0.0390625
128	±0.0390625	0 to 0.01953125	0 to -0.01953125

4. Power Subsystem for Analog Input

4.1 Power System Overview

The analog input subsystem requires multiple voltage levels to operate correctly. The ADC and SPI communication rely on a stable 3.3V power rail, while the PGA and analog input circuits need ±12V for proper operation. To generate these voltages, a combination of a boost converter and LDO regulators is used.

4.2 Boost Converter (5V to ±14V)

The TPS65131 is a dual-output DC-DC converter that efficiently converts a 5V input to ±14V, ensuring stable and isolated power for the high-performance analog circuits. The positive and negative voltage rails are generated using a single inductor topology, reducing PCB space and complexity. The output is stabilized using low-ESR capacitors (22µF and 10µF), ensuring minimal ripple.

4.3 LDO Regulation (±14V to ±12V)

The ±14V rails generated by the boost converter are further regulated using the TPS7A39, a precision low-noise LDO regulator. This step ensures that the analog circuits receive clean and low-ripple ±12V supplies. The regulator uses bulk 22µF capacitors for stable operation, with 100nF decoupling capacitors placed near the power pins of the PGA and ADC to prevent noise coupling.

4.4 Power Distribution Considerations

To ensure optimal performance, the power system is designed with:

- Separate ground planes for analog and digital sections to minimize interference.
- High-frequency decoupling capacitors near ICs to suppress transient noise.
- Low dropout regulators to improve power efficiency and thermal management.
- Current limiting and ESD protection at the power input to prevent damage from transient spikes or electrical surges.

5. Summary

This document focuses exclusively on the Analog Input Subsystem of the DAQ system, covering:

- 16 AI differential inputs with signal conditioning.
- PGA and multiplexer configurations for flexible input selection.
- SPI-based ADC communication and control logic.
- A well-structured power system, including boost conversion and LDO regulation.

This modular approach ensures seamless integration into the full DAQ system while maintaining signal integrity and accuracy.