ENERGIS 10IN Managed PDU

Main Board 1.1.0 PCB Layout Documentation

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This Technical File applies exclusively to ENERGIS 10IN Managed PDU, Hardware Revision 1.1.0, and corresponding firmware versions released for this hardware. Firmware versions are identified in the device user interface and are covered by this Technical File insofar as they do not change safety-relevant behavior. The Technical File is maintained in electronic

form by the manufacturer and can be made available without undue delay. All documents listed herein are retained for at least 10 years after the last product has been placed on the EU market.

Revision History

A revision is a new edition of the document and affects all sections of this document.

Version	Date	Responsible	Modification
1.0.0	12.12.2025	David Sipos	Initial creation of the document

Contents

1. Introduction

This document provides general technical information related to the printed circuit board (PCB) designs used within the ENERGIS 10-inch managed PDU system. It applies to all PCB layouts associated with the product, including but not limited to the main control board, display/interface board, and auxiliary adapter boards.

1.1 Purpose

The purpose of this document is to support technical documentation, compliance activities, and internal reference by describing the general characteristics, intended use, and design context of the PCB assemblies. It does not describe firmware behavior in detail and does not replace schematics, layout files, or test reports referenced elsewhere in the technical file.

This document is applicable to the PCB hardware revisions identified in the corresponding design documentation and manufacturing outputs. Any future hardware revisions may require an update or extension of this document where relevant.

2. General Information

The PCB assemblies covered by this document are designed for use as internal components of the ENERGIS 10-inch managed PDU and are not intended to be operated as standalone products. Each board fulfills a specific functional role within the overall system architecture and operates only when installed in the designated enclosure and used in accordance with the product documentation.

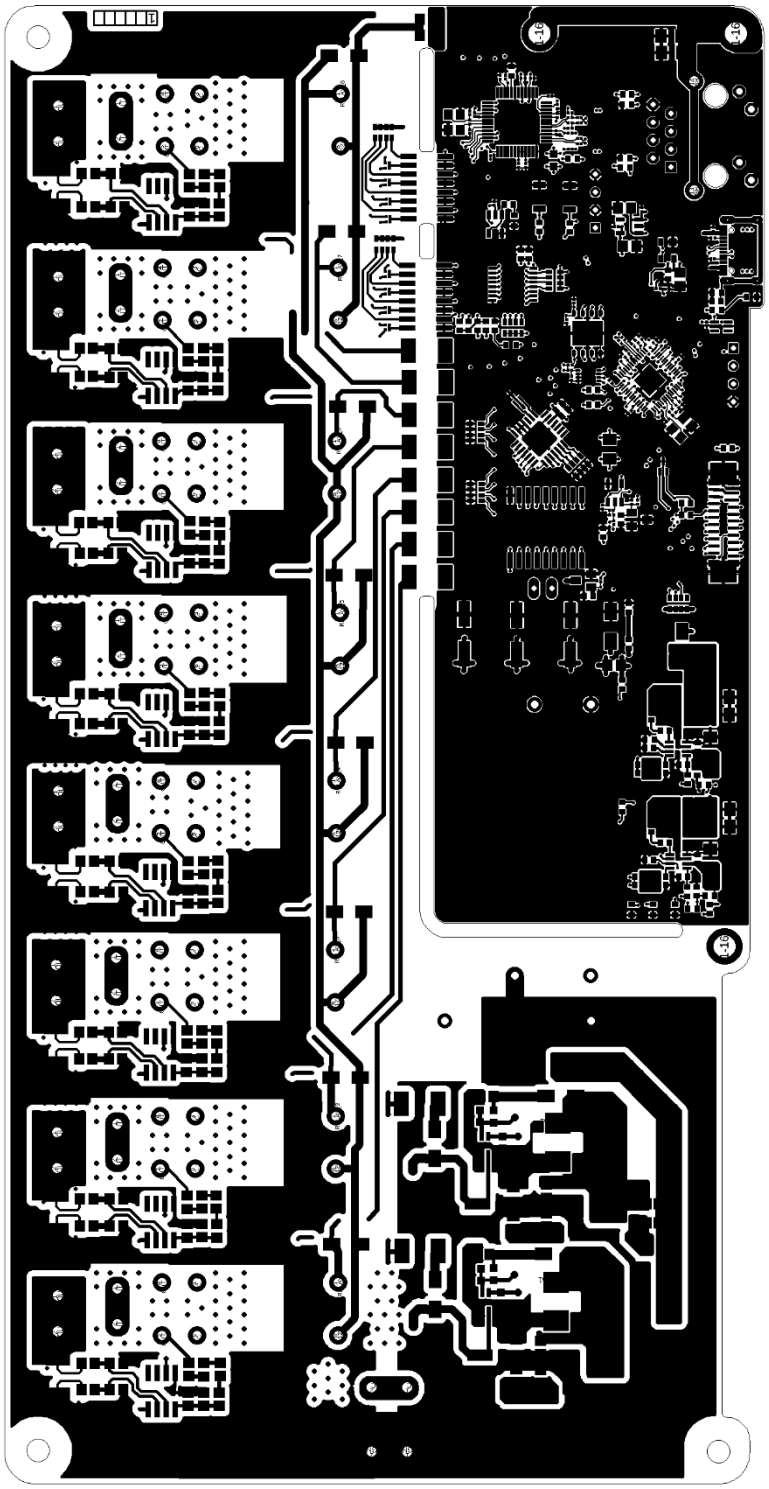
The PCB designs are developed using standard electronic design practices and manufactured using industry-standard PCB fabrication and assembly processes. Component selection is based on availability, electrical performance, and compliance with applicable regulatory requirements, including RoHS where applicable.

All PCB assemblies are intended for indoor use within controlled environmental conditions as specified in the product documentation. The boards do not include user-serviceable parts and are not designed for modification or repair by the end user.

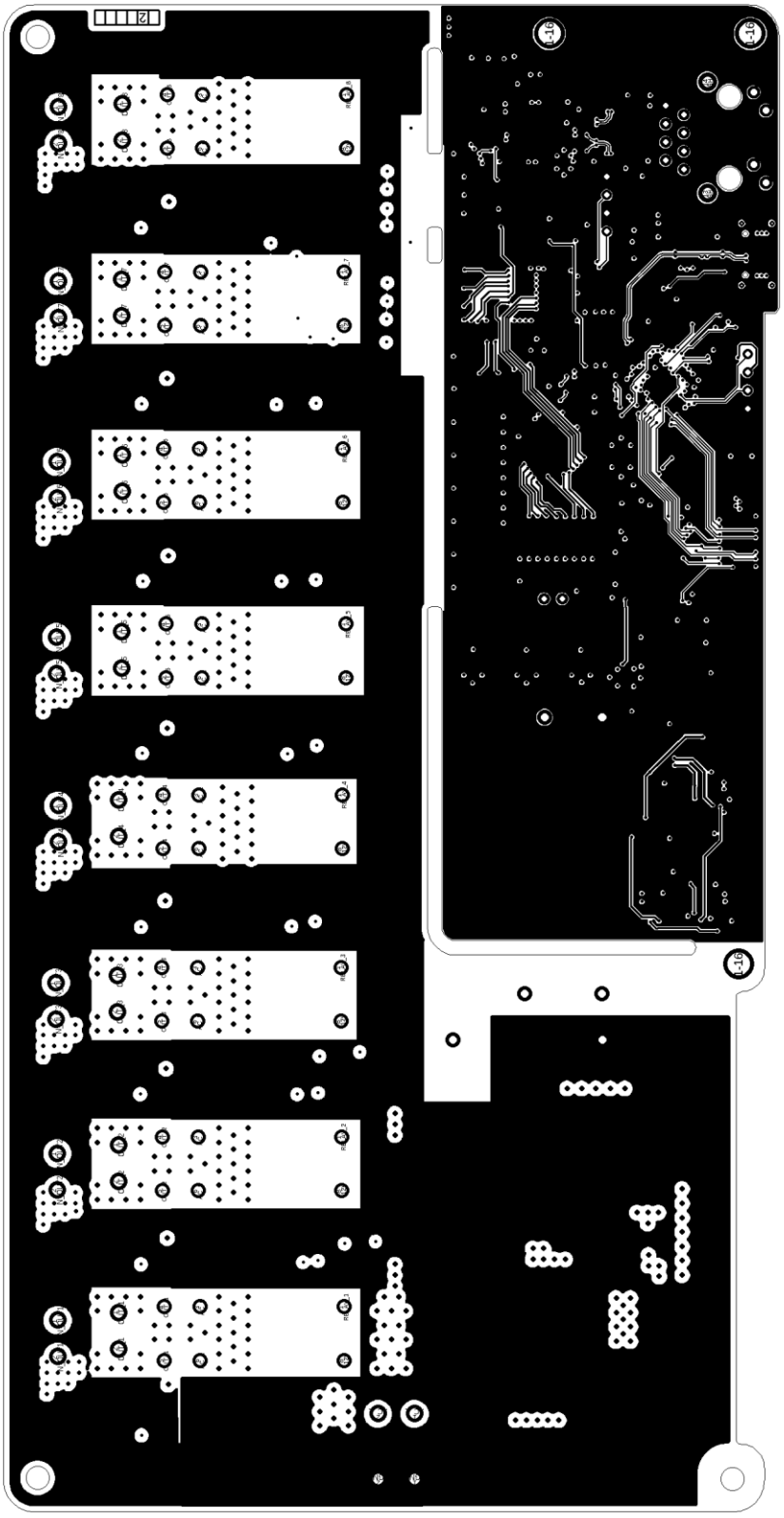
Detailed design data, including schematics, layout files, manufacturing data, and test results, are referenced in the Technical File Index and maintained as part of the overall technical documentation set.

3. ENERGIS_Rack-PDU_1.1.0 Layout

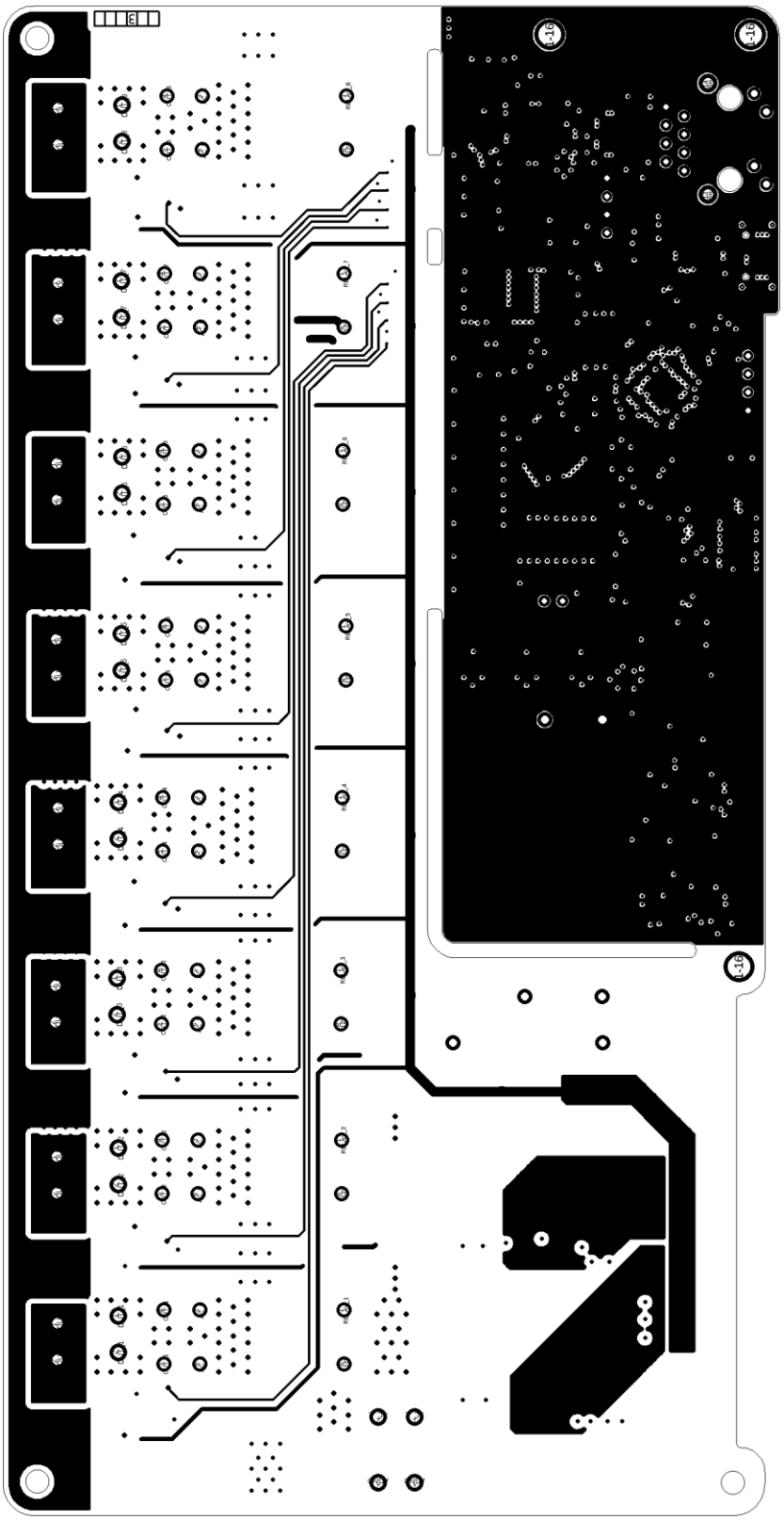
L1 Top layer



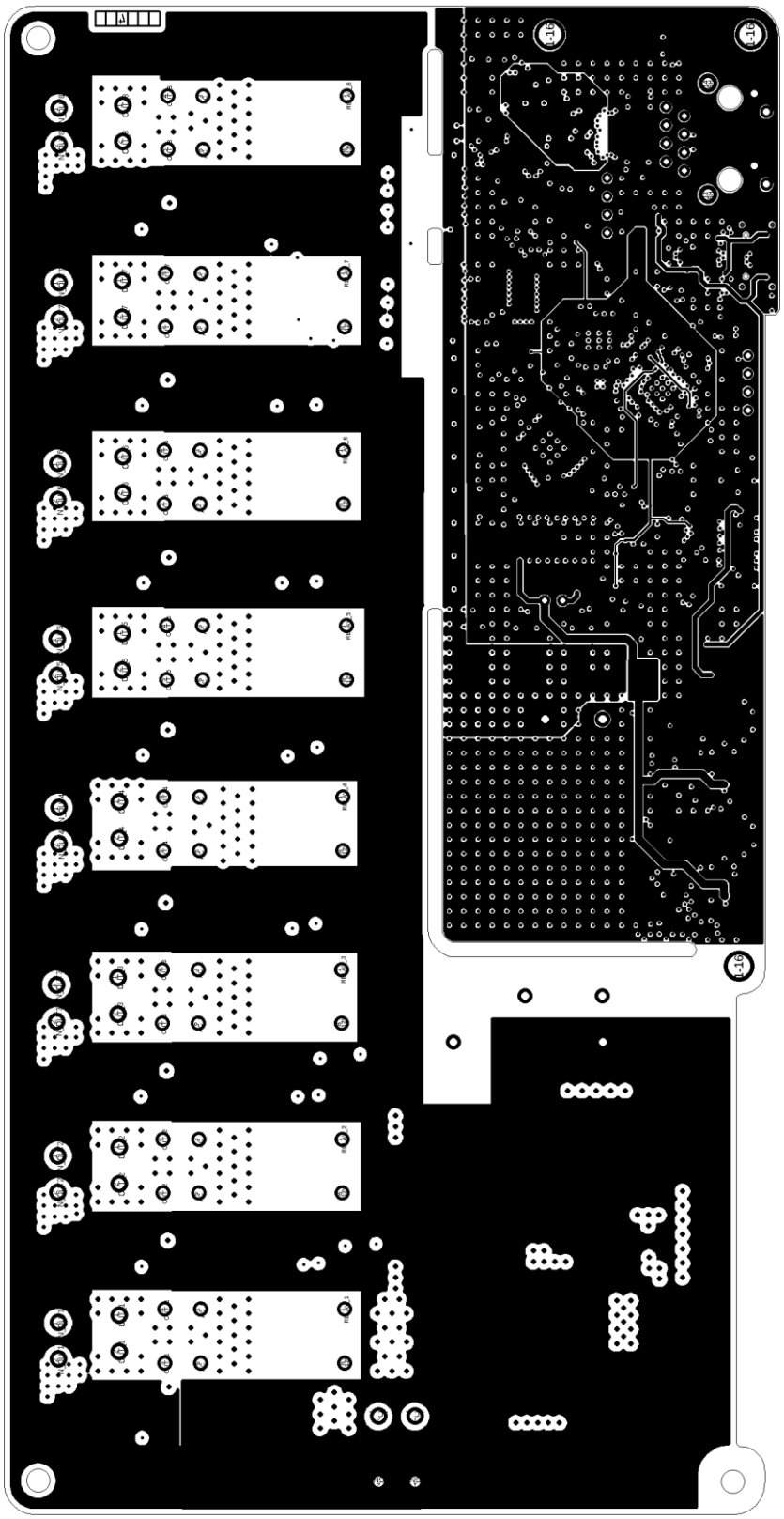
L2 Inner layer



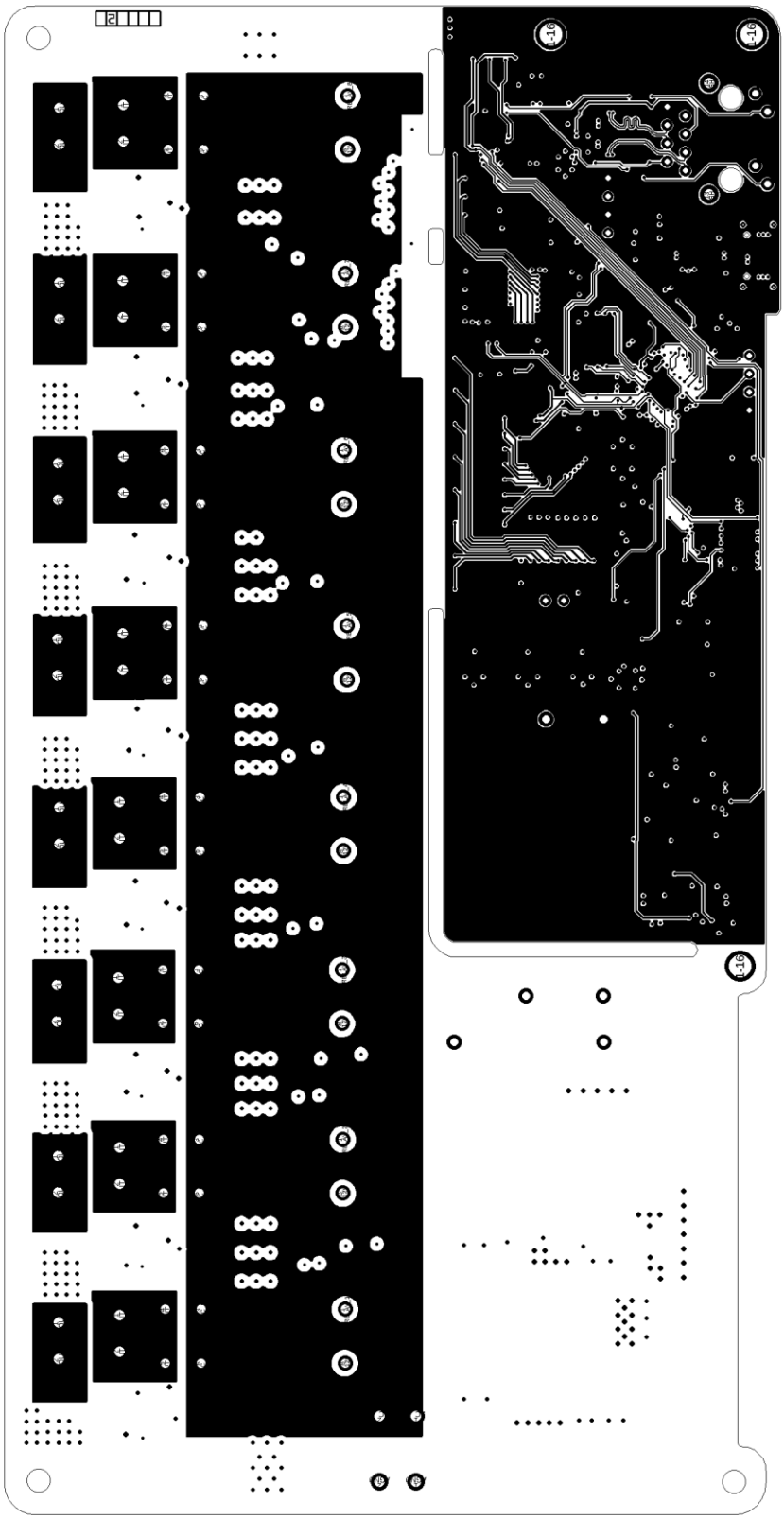
L3 Inner layer



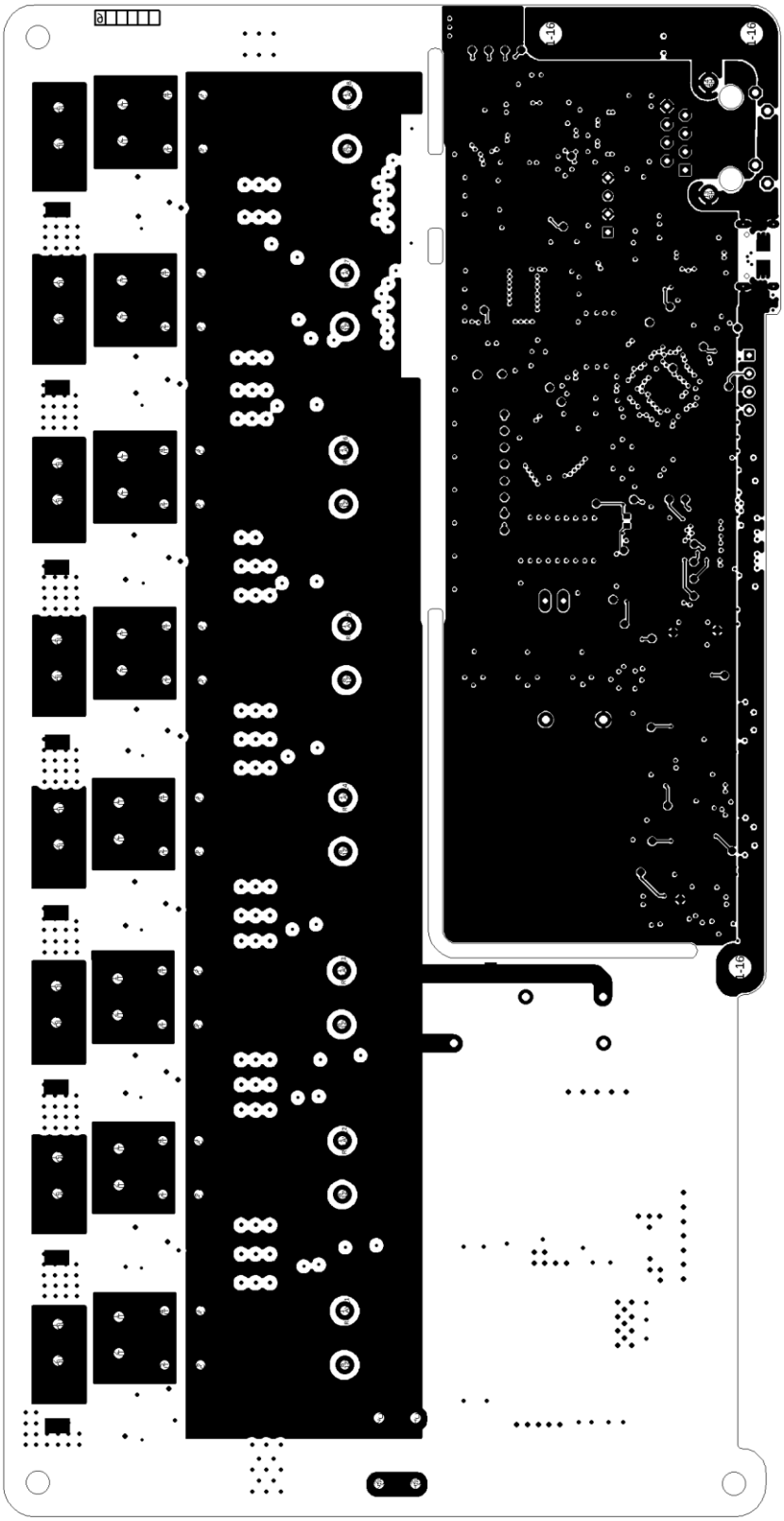
L4 Inner layer



L5 Inner layer



L6 Bottom layer



4. PCB Stackup and Controlled Impedance

4.1 PCB Stackup Overview

The printed circuit boards covered by this document are manufactured using standard multilayer FR4 materials and fabrication processes. Where applicable, a 6-layer PCB stackup is used to support signal integrity, power distribution, and electromagnetic compatibility requirements. For the 6-layer PCB designs, the following material specification and stackup configuration is applied.

PCB Material and Construction:

- **Material Type:** FR4
- **Laminate Specification:** JLC06161H-3313
- **Number of Layers:** 6
- **Finished Board Thickness:** approximately 1.54 mm (±10 %)
- **Outer Copper Weight:** 1 oz
- **Inner Copper Weight:** 0.5 oz
- **Manufacturing Standard:** JLCPCB standard multilayer process

4.2 Layer Stackup Details (6-Layer Configuration)

Layer	Description	Material / Copper Weight	Thickness (mm)
L1	Signal (Top)	Outer Copper, 1 oz	0.0350
	Prepreg	3313, RC57 %, 4.2 mil	0.0994
L2	Ground Plane	Inner Copper, 0.5 oz	0.0152
	Core	FR4 core (no copper)	0.5500
L3	Power Plane	Inner Copper, 0.5 oz	0.0152
	Prepreg	2116, RC54 %, 4.9 mil	0.1088
L4	Signal	Inner Copper, 0.5 oz	0.0152
	Core	FR4 core (no copper)	0.5500
L5	Ground Plane	Inner Copper, 0.5 oz	0.0152
	Prepreg	3313, RC57 %, 4.2 mil	0.0994
L6	Signal (Bottom)	Outer Copper, 1 oz	0.0350
	Total Thickness		**1.5384 mm**

This stackup is selected to provide:

- dedicated ground reference planes
- controlled impedance routing capability
- separation between power, signal, and reference layers
- mechanical robustness suitable for rack-mounted equipment

4.3 Controlled Impedance Routing

Selected signal nets on the PCB are routed using controlled impedance design rules to ensure reliable signal integrity, particularly for high-speed or noise-sensitive signals.

Controlled impedance parameters are defined within the PCB design tool and verified against the selected stackup. The impedance profiles include single-ended and differential configurations as required by the design.

Typical controlled impedance rules used include, but are not limited to:

- **Single-ended impedance:** approximately 50 Ω
- **Differential impedance:** approximately 90 Ω and 100 Ω (depending on interface requirements)

The controlled impedance parameters are defined by trace width, spacing, dielectric thickness, and reference plane configuration. An example of the controlled impedance rule definitions used in the design is shown in the associated design documentation and PCB rule configuration.

These impedance targets are achieved through a combination of:

- stackup selection
- copper thickness control
- dielectric material properties
- PCB manufacturer standard tolerances

Final impedance values are subject to normal manufacturing tolerances and are considered acceptable within the specified design margins.