ENERGIS 10IN Managed PDU

Display Board 1.1.0 PCB Layout Documentation

Author	David Sipos

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This Technical File applies exclusively to ENERGIS 10IN Managed PDU, Hardware Revision 1.1.0, and corresponding firmware versions released for this hardware. Firmware versions are identified in the device user interface and are covered by this Technical File insofar as they do not change safety-relevant behavior. The Technical File is maintained in electronic form by the manufacturer and can be made available without undue delay. All documents listed herein are retained for at least 10 years after the last product has been placed on the EU market.

Revision History

A revision is a new edition of the document and affects all sections of this document.

Version	Date	Responsible	Modification
1.0.0	12.12.2025	David Sipos	Initial creation of the document

Contents

1. Introduction

This document provides general technical information related to the printed circuit board (PCB) designs used within the ENERGIS 10-inch managed PDU system. It applies to all PCB layouts associated with the product, including but not limited to the main control board, display/interface board, and auxiliary adapter boards.

1.1 Purpose

The purpose of this document is to support technical documentation, compliance activities, and internal reference by describing the general characteristics, intended use, and design context of the PCB assemblies. It does not describe firmware behavior in detail and does not replace schematics, layout files, or test reports referenced elsewhere in the technical file.

This document is applicable to the PCB hardware revisions identified in the corresponding design documentation and manufacturing outputs. Any future hardware revisions may require an update or extension of this document where relevant.

2. General Information

The PCB assemblies covered by this document are designed for use as internal components of the ENERGIS 10-inch managed PDU and are not intended to be operated as standalone products. Each board fulfills a specific functional role within the overall system architecture and operates only when installed in the designated enclosure and used in accordance with the product documentation.

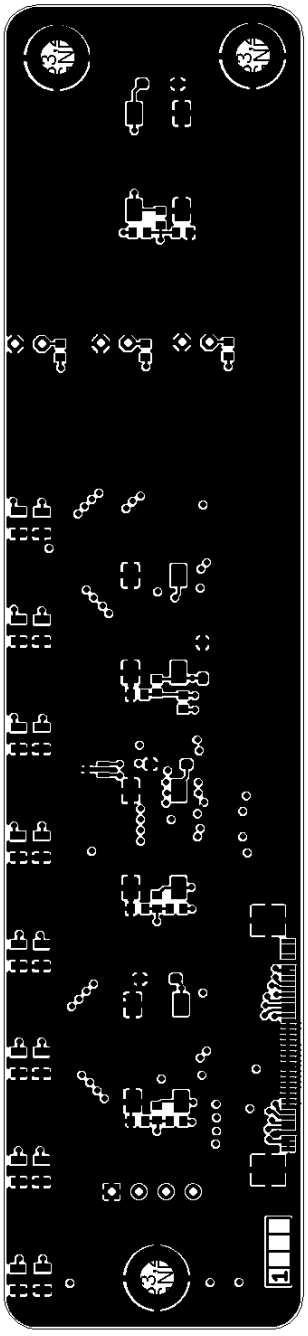
The PCB designs are developed using standard electronic design practices and manufactured using industry-standard PCB fabrication and assembly processes. Component selection is based on availability, electrical performance, and compliance with applicable regulatory requirements, including RoHS where applicable.

All PCB assemblies are intended for indoor use within controlled environmental conditions as specified in the product documentation. The boards do not include user-serviceable parts and are not designed for modification or repair by the end user.

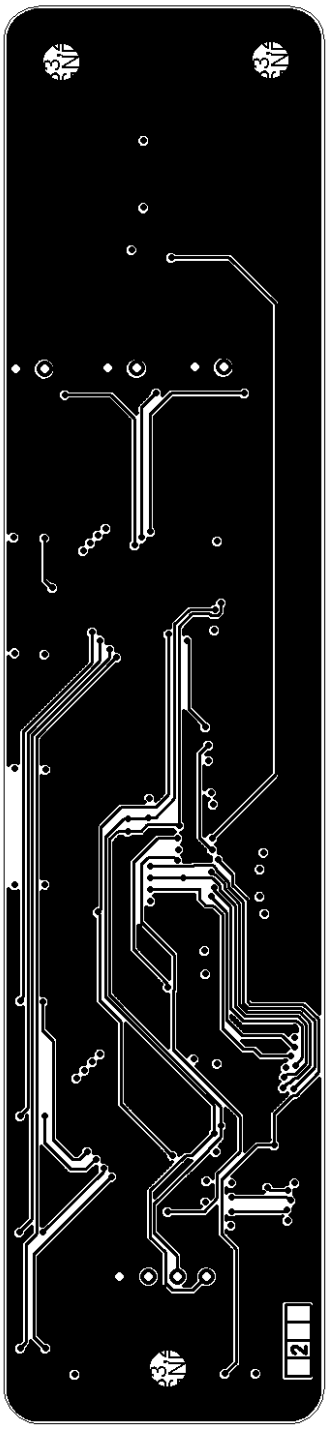
Detailed design data, including schematics, layout files, manufacturing data, and test results, are referenced in the Technical File Index and maintained as part of the overall technical documentation set.

3. ENERGIS_Display-Board_1.1.0 Layout

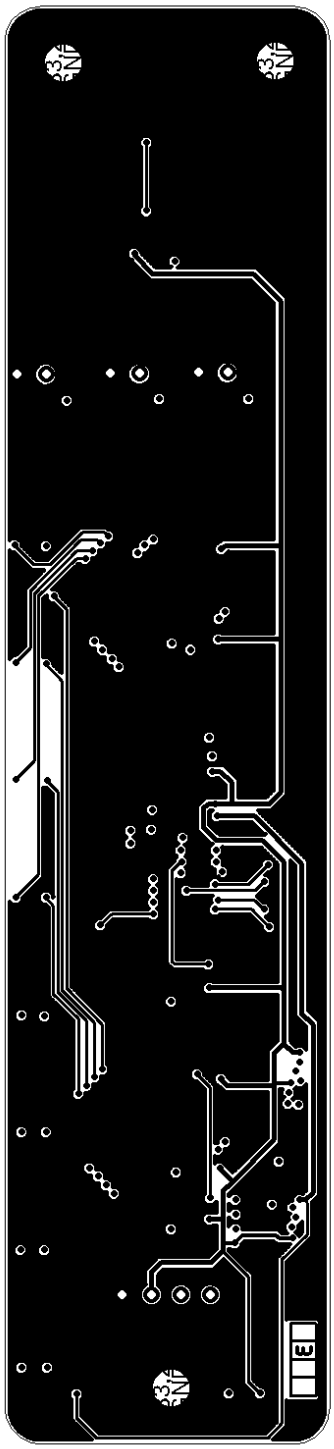
L1 Top layer



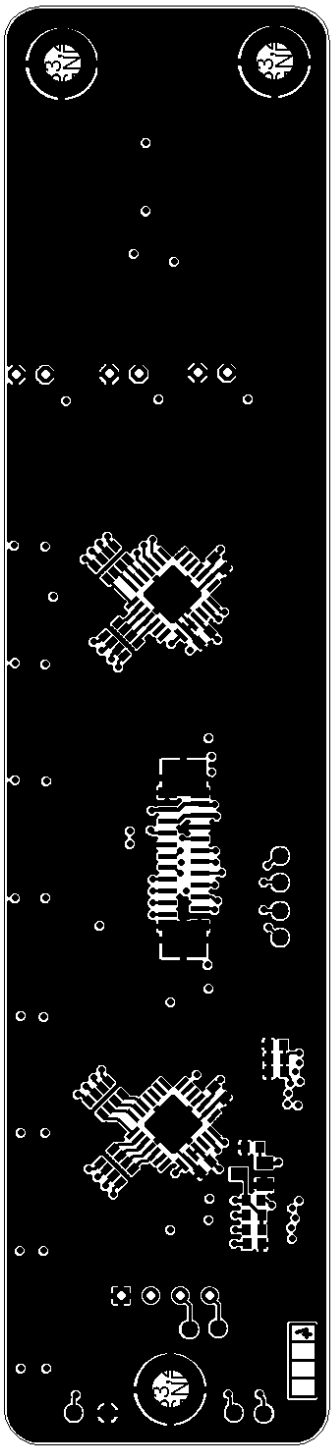
L2 Inner layer



L3 Inner layer



L4 Inner layer



4. PCB Stackup and Layer Usage

4.1 PCB Stackup Overview

The printed circuit board covered by this document is manufactured using a standard 4-layer FR4 stackup and is intended for use as an internal assembly within the ENERGIS system.

The stackup configuration is selected to provide low-impedance reference planes, robust power distribution, and predictable signal return paths for low- and medium-speed digital and analog signals. No controlled impedance routing is required for this PCB.

PCB Material and Construction:

- Material Type: FR4
- Laminate Specification: JLC04161H-3313
- Number of Layers: 4
- Finished Board Thickness: approximately 1.6 mm
- Outer Copper Weight: 1 oz
- Inner Copper Weight: 0.5 oz
- Manufacturing Standard: JLCPCB standard multilayer process

4.2 Layer Stackup Details (4-Layer Configuration)

Layer	Description	Material / Copper Weight	Thickness (mm)
L1	Ground Plane (Top)	Outer Copper, 1 oz	0.0350
	Prepreg	3313 ×1	0.0994
L2	Signal / Power Routing	Inner Copper, 0.5 oz	0.0152
	Core	FR4 core (with copper)	1.2650
L3	Signal / Power Routing	Inner Copper, 0.5 oz	0.0152
	Prepreg	3313 ×1	0.0994
L4	Ground Plane (Bottom)	Outer Copper, 1 oz	0.0350
	Total Thickness		**~1.6 mm**

This stackup is selected to provide:

- continuous ground reference planes on the outer layers
- low-inductance return paths for routed signals
- effective shielding between internal routing layers
- mechanical robustness suitable for rack-mounted equipment

4.3 Signal Routing and Reference Planes

All active signal routing is performed on the internal layers (L2 and L3). The outer layers (L1 and L4) are used primarily as continuous ground planes.

This configuration provides:

- stable reference planes for all routed signals
- reduced electromagnetic emissions
- improved immunity to external noise
- simplified return current paths

The use of internal routing layers combined with external ground planes supports predictable signal behavior without the need for controlled impedance constraints.

4.4 Notes on Manufacturing Tolerances

- Dielectric thicknesses and material properties are subject to standard PCB manufacturing tolerances.
- Copper thickness variations may affect resistance and current-carrying capability but do not impact functional operation within the intended use case.
- No impedance-controlled routing or post-manufacturing impedance validation is required for this PCB.