

The diagram illustrates the connection of the SWCLK and SWDIO pins for two debuggers, DBG2 and DBG1. For DBG2, the SWCLK pin is connected to the SWCLK pin of the target device, and the SWDIO pin is connected to the SWDIO pin of the target device. For DBG1, the SWCLK pin is connected to the UART0_RX/2TD pin of the target device, and the SWDIO pin is connected to the UART0_TX/2TD pin of the target device. Both debuggers have their SWCLK and SWDIO pins connected to GND.

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The diagram illustrates the RP2040 MCU with various components and their connections:

- Power and Reset:**
 - RESET:** Connected to a U-1000P-B pushbutton and a +3V3 supply through a 10K resistor (R50).
 - IOVDD:** Connected to +1V1.
 - DVDD:** Connected to +3V3.
 - AVDD:** Connected to +1V1.
 - TESTEN:** Connected to GND through a 57 ohm resistor.
- GPIOs and Peripherals:**
 - GPIO0-7:** Connected to UART0 RX/TX (7D) and a 4D03WVGJ0332T5E component.
 - GPIO8-15:** Connected to LCD DC2/6D, LCD BLU2/6D, LCD MISO/2/6D, LCD CS2/6D, LCD SCLK/2/6D, and LCD MOSI/2/6D.
 - GPIO16-18:** Connected to KEY 0/2/6D, KEY 1/2/6D, and KEY 2/2/6D.
 - GPIO19-23:** Connected to SPI0 MISO/2/3B, SPI0 CS/2/3B, SPI0 SCK/2/3B, SPI0 MOSI/2/3B, RST/2/3B, and INT/2/3B.
 - GPIO24-25:** Connected to MCP_DSP_RST/2/6D.
 - GPIO26-29:** Connected to V_USB, NC, and +12V_MEAS/2/7D.
 - GPIO30-33:** Connected to QSPI SD3, QSPI SCLK, QSPI SD0, QSPI SD2, QSPI SD1, and QSPI SS.
- Other Components:**
 - R21, R22:** 27 ohm resistors connected to DP_N and DP_P.
 - R38:** A network of resistors connected to +3V3 and various pins.
 - IC2:** A component connected to various GPIOs.

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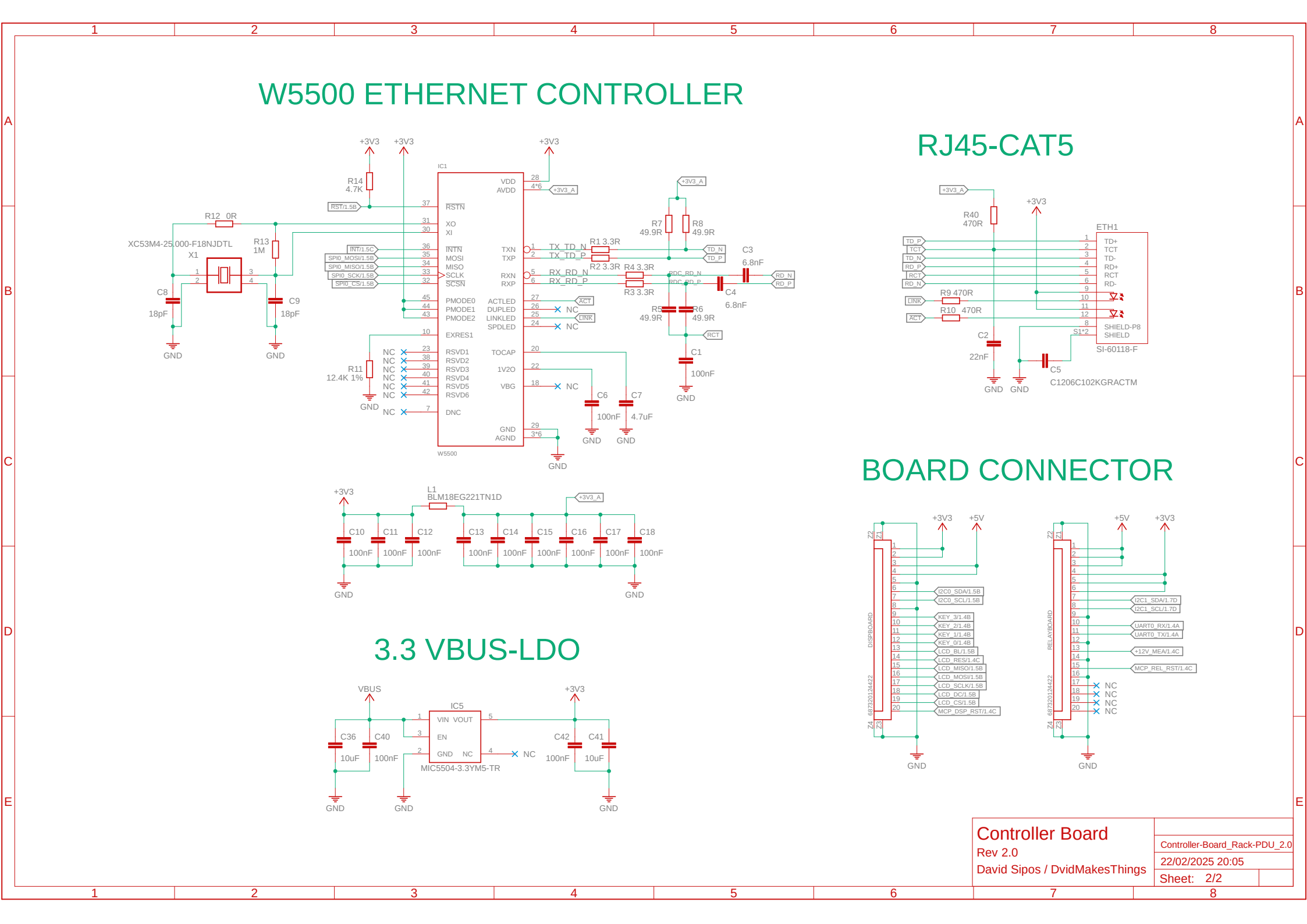
W5500 ETHERNET CONTROLLER

RJ45-CAT5

BOARD CONNECTOR

3.3 VBUS-LDO

Controller Board					
Rev 2.0					
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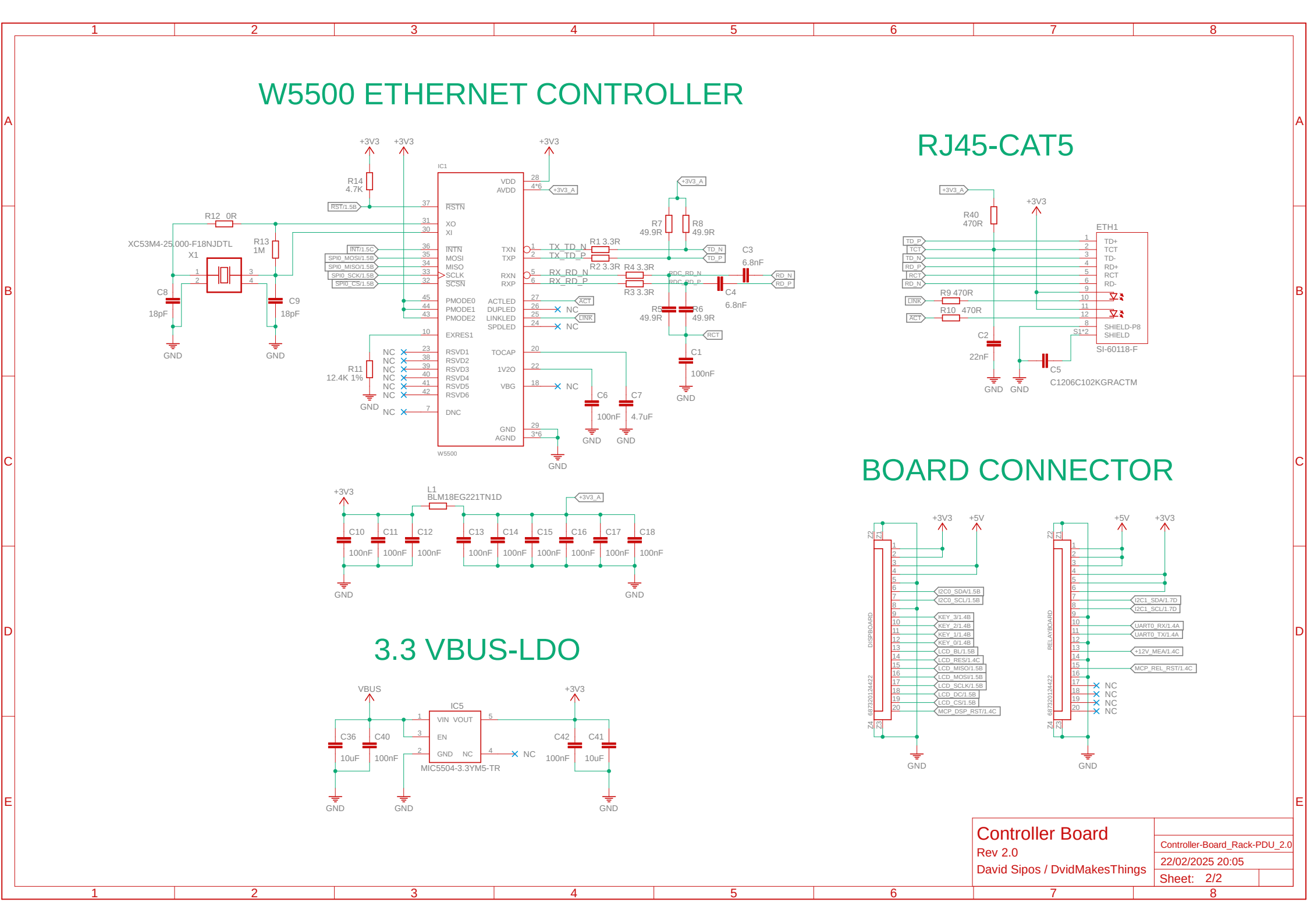
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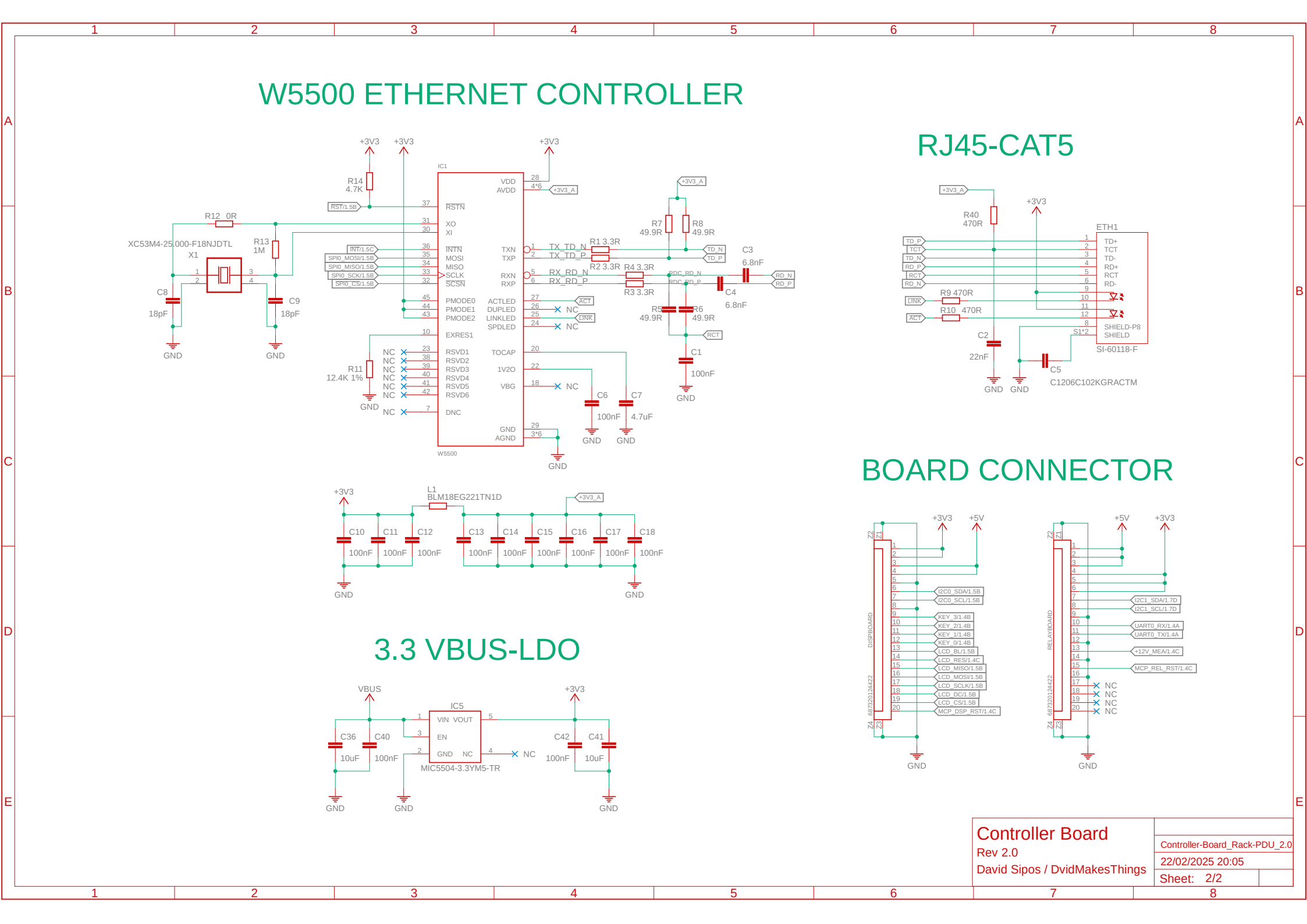
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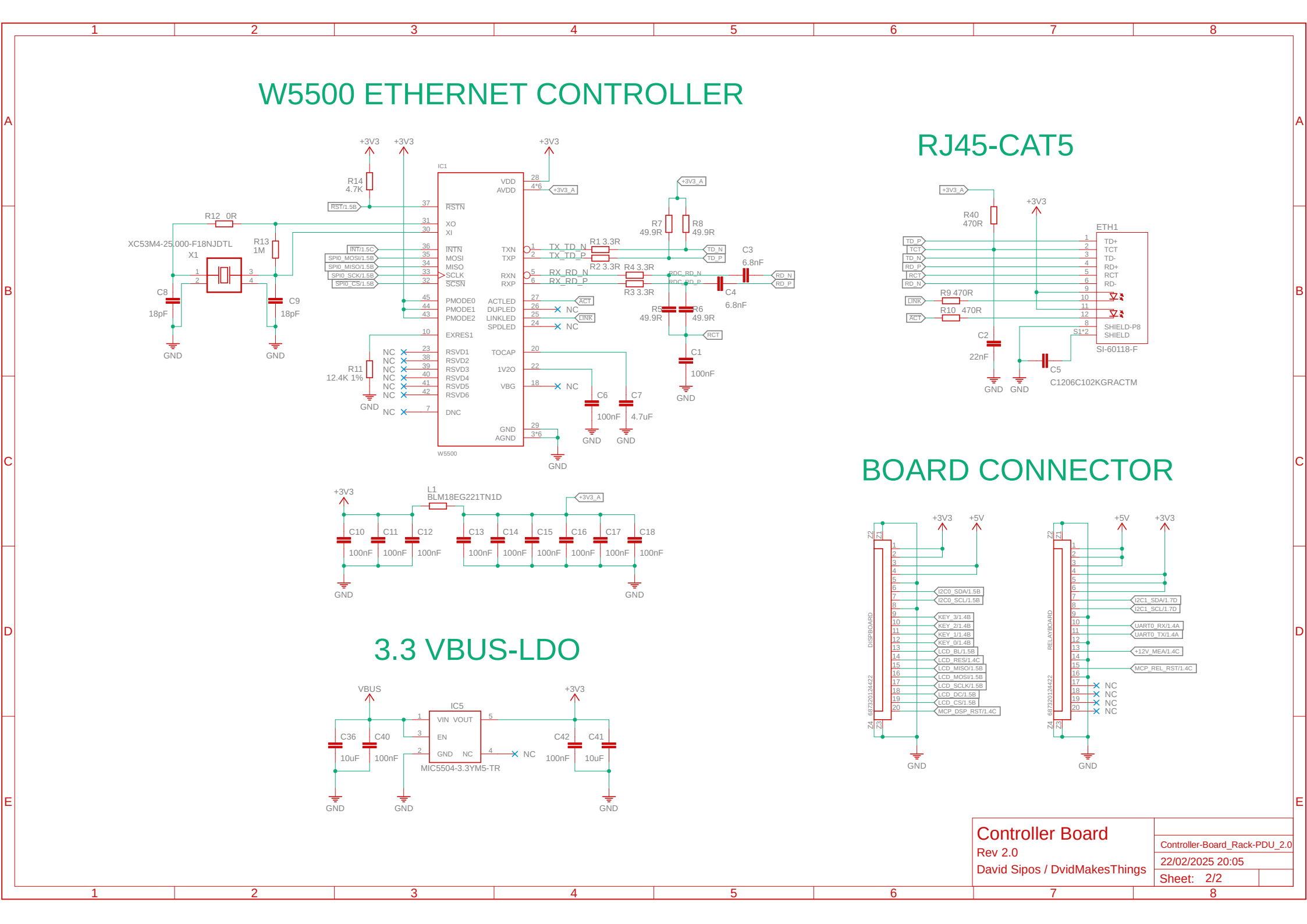
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