PDCard-4242 Schematic Documentation

# Project: PDNode-600 Board: PDCard-4242 Var: Pro

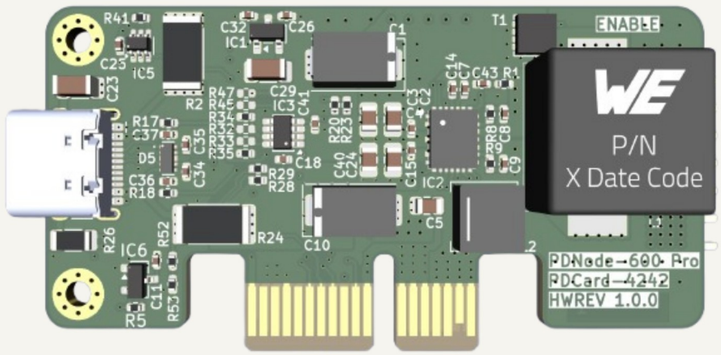
Rev 1.0.0 2026-02-25

## CONTENT

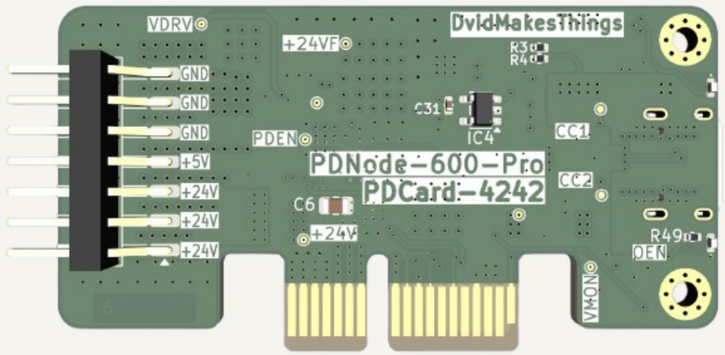


## PCB PREVIEW

### TOP VIEW




### BOTTOM VIEW




## COMMENT GUIDELINES

General comments are black, 50 mil size

Design notes and guidelines are blue, 50 mil size

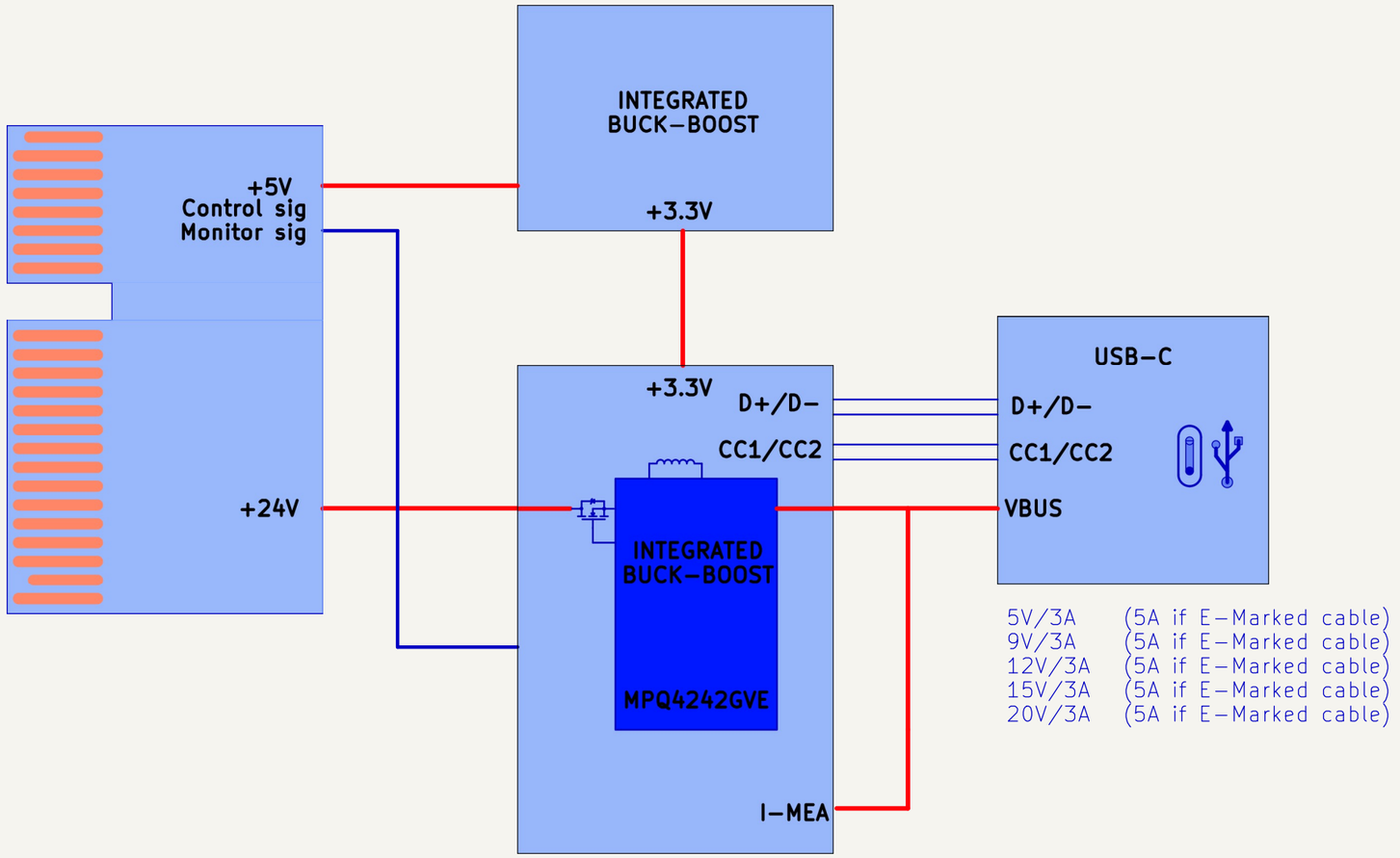
Layout instructions are red, 50 mil size

## NOTES

**Not fitted components are marked as X**

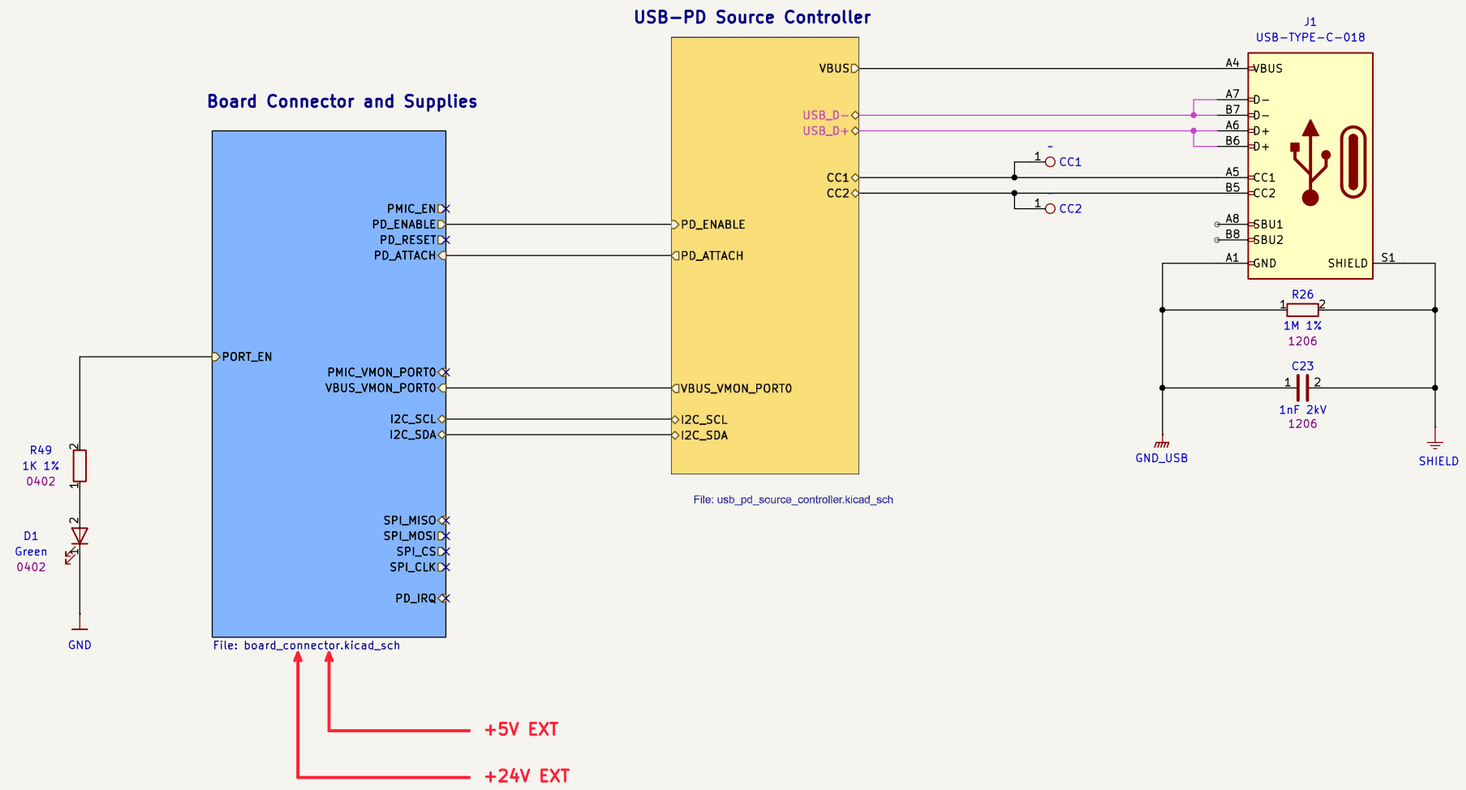
| | | | | |
|---|---|---|---|---|
| DMT<br>Date: 2025-01-12 | Board Name: PDNode-600 | | Project Name: PDCard-4242 | |
| | File Name: PDNode-PDCard-4242.kicad_sch | | Revision: 1.0.0 | Variant: Pro |
| Sheet Title: Root | Company: DvidMakesThings | Designer: David Sipos<br>Reviewer: | Size: A3 | Sheet: 1 of 7 |

# [2] Block Diagram




| | | | | |
|---|---|---|---|---|
| DMT<br>Date: 2026-01-31 | Board Name: **PDNode-600**<br>File Name: Block Diagram.kicad_sch | | Project Name: **PDCard-4242**<br>Revision: 1.0.0 | Variant: Pro |
| Sheet Title: Block Diagram | Company: **DvidMakesThings** | Designer: David Sipos<br>Reviewer: | Size: **A3** | Sheet: **2** of **7** |

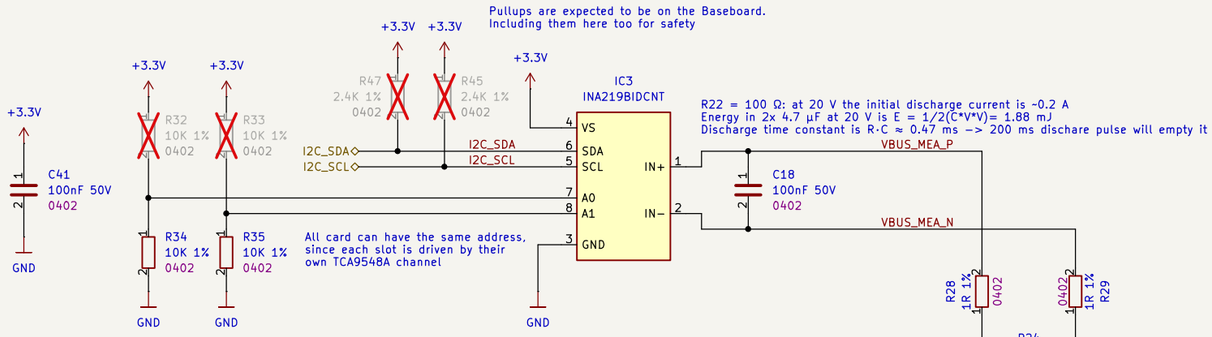
# Block Diagram




| | | | |
|---|---|---|---|
| DMT<br>Date: 2025-01-12 | Board Name: **PDNode-600**<br>File Name: Project Architecture.kicad_sch | | Project Name: **PDCard-4242**<br>Revision: 1.0.0 / Variant: Pro |
| Sheet Title: Project Architecture | Company: **DvidMakesThings** | Designer: David Sipos<br>Reviewer: | Size: **A3** / Sheet: **3** of **7** |

# USB-PD SOURCE CONTROLLER

## INA219BIDCNT CURRENT MEASUREMENT



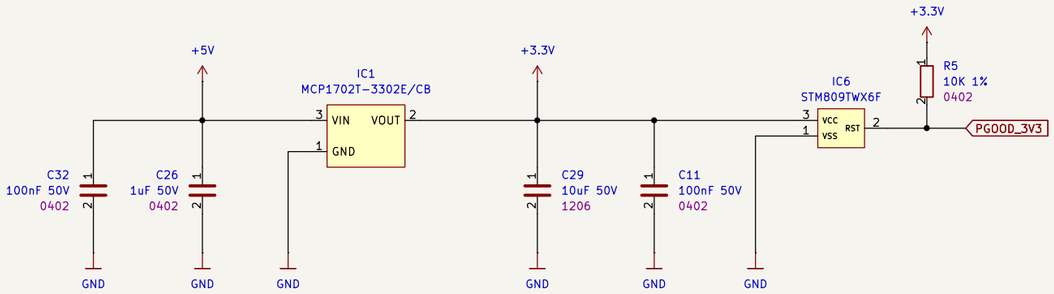

## MPQ4242 PD SOURCE CONTROLLER




| | | | |
|---|---|---|---|
| DMT<br>Date: 2025-01-12 | Board Name: **PDNode-600**<br>File Name: usb_pd_source_controller.kicad_sch | | Project Name: **PDCard-4242**<br>Revision: 1.0.0<br>Variant: Pro |
| Sheet Title: USB-PD Source Controller | Company: **DvidMakesThings** | Designer: David Sipos<br>Reviewer: | Size: **A3**<br>Sheet: **4** of **7** |

# BOARD CONNECTOR AND SUPPLIES

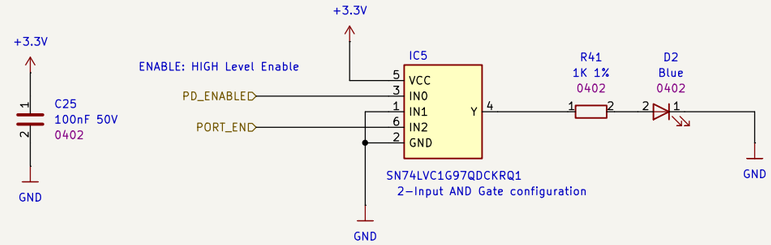
## +5V to 3.3V PMIC




3.3V setpoint (FB divider):
Datasheet "Setting the Output Voltage"
formula: Vout = Vfb * (1 + R1/R2), Vfb = 0.8V.

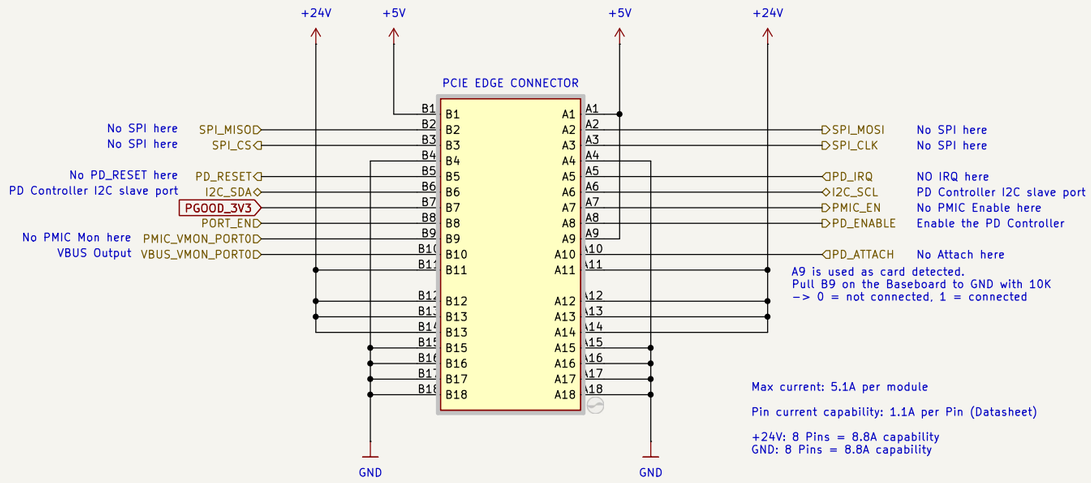
Chosen 1% values: R2 = 2.40k, R1 = 7.50k.
Result: Vout = 0.8 * (1 + 7.5/2.4) = 3.300V nominal.
R2 kept <= 4k to stay well under the datasheet's 4.99k guideline.

## ENABLE STATUS




## PCIE-X1 BOARD EDGE CONNECTOR

If +3.3V is selected, PMIC above is all DO NOT MOUNT except R37, since it would backfeed the carrier's 3.3V rail

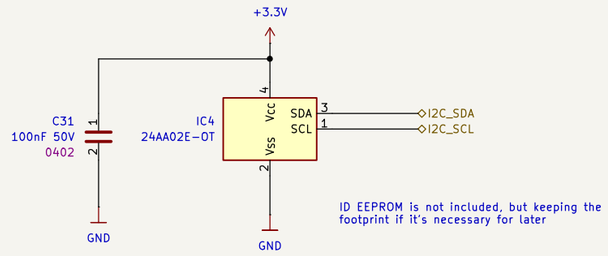



Max current: 5.1A per module

Pin current capability: 1.1A per Pin (Datasheet)

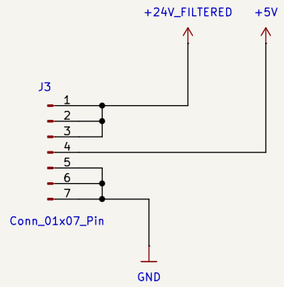
+24V: 8 Pins = 8.8A capability
GND: 8 Pins = 8.8A capability

## DEVICE ID EEPROM

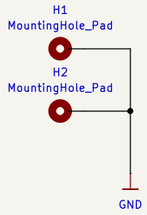



ID EEPROM is not included, but keeping the footprint if it's necessary for later

## DEBUG POWER CONNECTOR




## MOUNTING HOLES

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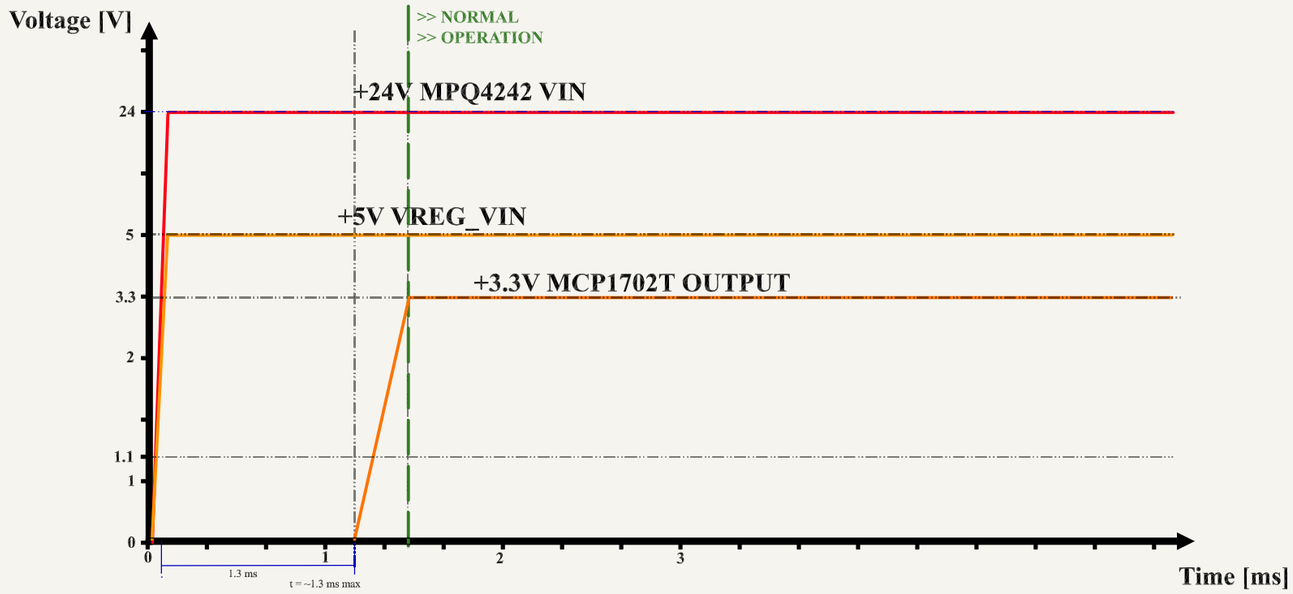
|---|---|---|---|
| DMT<br>Date: 2025-01-12 | Board Name: PDNode-600 | | Project Name: PDCard-4242 |
| | File Name: board_connector.kicad_sch | | Revision: 1.0.0 / Variant: Pro |
| Sheet Title: Board Connector and Supplies | Company: DvidMakesThings | Designer: David Sipos<br>Reviewer: | Size: A3 / Sheet: 5 of 7 |

# [6] Power - Sequencing




| | | | | |
|---|---|---|---|---|
| DMT<br>Date: 2025-01-12 | Board Name: **PDNode-600** | | Project Name: **PDCard-4242** | |
| | File Name: Power - Sequencing.kicad_sch | | Revision: 1.0.0 | Variant: Pro |
| Sheet Title: Power - Sequencing | Company: **DvidMakesThings** | Designer: David Sipos<br>Reviewer: | Size: **A3** | Sheet: **6** of **7** |

# Revision History

| DATE | REVISION | RESPONSIBLE | CHANGE |
|---|---|---|---|
| 25.02.2026 | 1.0.0 | DMT | INITIAL CREATION |
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DMT

Date: 2025-01-12

Board Name: **PDNode-600**

Project Name: **PDCard-4242**

File Name: Revision History.kicad_sch

Revision: 1.0.0

Variant: Pro

Sheet Title: Revision History

Company: **DvidMakesThings**

Designer: David Sipos

Reviewer:

Size: **A3**

Sheet: 7 of 7