

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications

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Device: CCG7D

About this document

Scope and purpose

This document provides an overview of hardware design guidelines for dual-port EZ-PD™ CCG7D USB Type-C power delivery (PD) and buck-boost controller in automotive charger applications.

Intended audience

Automotive rear seat charger (RSC), head-unit charger as well as rear seat entertainment (RSE) power electronics hardware designers using EZ-PD™ CCG7D USB Type-C PD and buck-boost controller.

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1 Introduction

These hardware design guidelines for EZ-PD™ CCG7D in automotive applications provide an overview of EZ-PD™ CCG7D's highly integrated dual-port USB Type-C PD solution with integrated buck-boost controllers and solution design guidelines for the CCG7D in automotive RSC applications. This solution is based on a peak current-controlled four-switch buck-boost converter (FSBBC) for automotive USB Type-C PD applications. Similar guidelines can be used for CCG7D in automotive head-unit charger applications and CCG7D in automotive RSE applications.

EZ-PD™ CCG7D is highly integrated dual-port USB Type-C PD solution with integrated buck-boost controllers. It complies with the latest USB Type-C and USB-PD specifications, and is targeted at automotive charger applications such as head-unit chargers and RSCs, as well as RSE. Integration offered by CCG7D not only reduces the bill of materials (BOM) but also provides a footprint-optimized solution for automotive charging needs.

CCG7D has integrated gate drivers for V_{BUS} NFET on the provider path. It also includes hardware-controlled protection features on the V_{BUS} . CCG7D supports a wide input voltage range (4 to 24 V with 40 V tolerance) and programmable switching frequency (150 to 600 kHz) in an integrated PD solution. CCG7D integrates monitoring, protection, and communication features needed to build a robust automotive USB-C charging system

CCG7D is the most programmable USB-PD solution with an on-chip 32-bit Arm® Cortex®-M0 processor, 128 kB Flash, 16 kB RAM and 32 kB ROM that leaves most Flash available for user application use. It also includes various analog and digital peripherals such as analog to digital converters (ADCs), pulse-width modulators (PWMs), I²C/SPI/UART interfaces and timers. The inclusion of a fully programmable MCU with analog and digital peripherals allows the implementation of custom system management functions such as power throttling, load sharing, temperature monitoring, and fault logging or “event data recording”.

2 EZ-PD™ CCG7D features and applications

2.1 Applications

- Head-unit charger
- RSC
- RSE

2.2 Features

2.2.1 USB-PD

- Supports two USB-PD ports
- Supports latest USB-PD 3.0 version 2.0 including programmable power supply (PPS) mode

2.2.2 Type-C

- Configurable Type-C pull-up termination resistors (R_P)
- V_{BUS} NFET gate driver
- Integrated 100 mW V_{CONN} power supply, control and protection

2.2.3 2x buck-boost controller

- 150 to 600 kHz switching frequency
- 5.5 to 24 V input, 40 V tolerance
- 3.3 to 21.5 V output
- 20 mV voltage and 50 mA current steps for PPS
- Supports pulse-skipping mode (PSM) for light-load efficiency
- Supports forced continuous current/conduction mode (FCCM) for minimum ripple
- Soft start to reduce inrush current
- Programmable spread spectrum frequency modulation for low EMI
- Switching synchronization with programmable phase shift across two ports to further reduce the EMI

2.2.4 2x legacy/proprietary charging blocks

- Supports USB-BC 1.2, QC 2.0/3.0, Apple charging 2.4 A/3.0 A and Samsung Adaptive Fast Charging (AFC)

2.2.5 Integrated voltage (V_{BUS}) regulation and current sense amplifier

- Supports current sensing (CS) for PPS current foldback operation
- Internal feedback network
- Supports external Type-II compensation network

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EZ-PD™ CCG7D features and applications

2.2.6 System-level fault protection

- On-chip V_{BUS_C} , overvoltage protection (OVP), overcurrent protection (OCP), undervoltage protection (UVP)
- V_{BUS_C} -to-CC short protection
- V_{BAT} -to-GND short protection FET gate driver
- Undervoltage lockout (UVLO)
- V_{CONN} OCP
- Supports overtemperature protection (OTP) through external and/or internal temperature sensor
- Supports connector and board temperature measurement using external thermistors

2.2.7 32-bit MCU subsystem

- 48-MHz Arm® Cortex®-M0 CPU
- 128 kB Flash
- 16 kB SRAM
- 32 kB ROM

2.2.8 Peripherals and GPIOs

- 19 GPIOs
- Two overvoltage-tolerant (OVT) GPIOs
- 3x 8-bit ADCs
- 4x 16-bit timers/counters/PWMs (TCPWMs)

2.2.9 Communication interfaces

- 4x SCBs (I²C/SPI/UART/LIN)

2.2.10 Clocks and oscillators

- Integrated oscillator, eliminating the need for an external clock

2.2.11 Power supply

- 4 to 24 V input (40 V tolerance)
- 3.3 to 21.0 V output
- Integrated LDO, capable of 5 V at 150 mA

2.2.12 Packages

- 68-pin 10 mm x 10 mm QFN, wettable flank, AEC-Q100
- Supports automotive temperature range (-40°C to +105°C)
- Max. 125°C operating junction temperature

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



EZ-PD™ CCG7D features and applications

2.3 CCG7D block diagram

Figure 1 shows a block diagram of the CCG7D architecture. For more details, see the CCG7D datasheet.

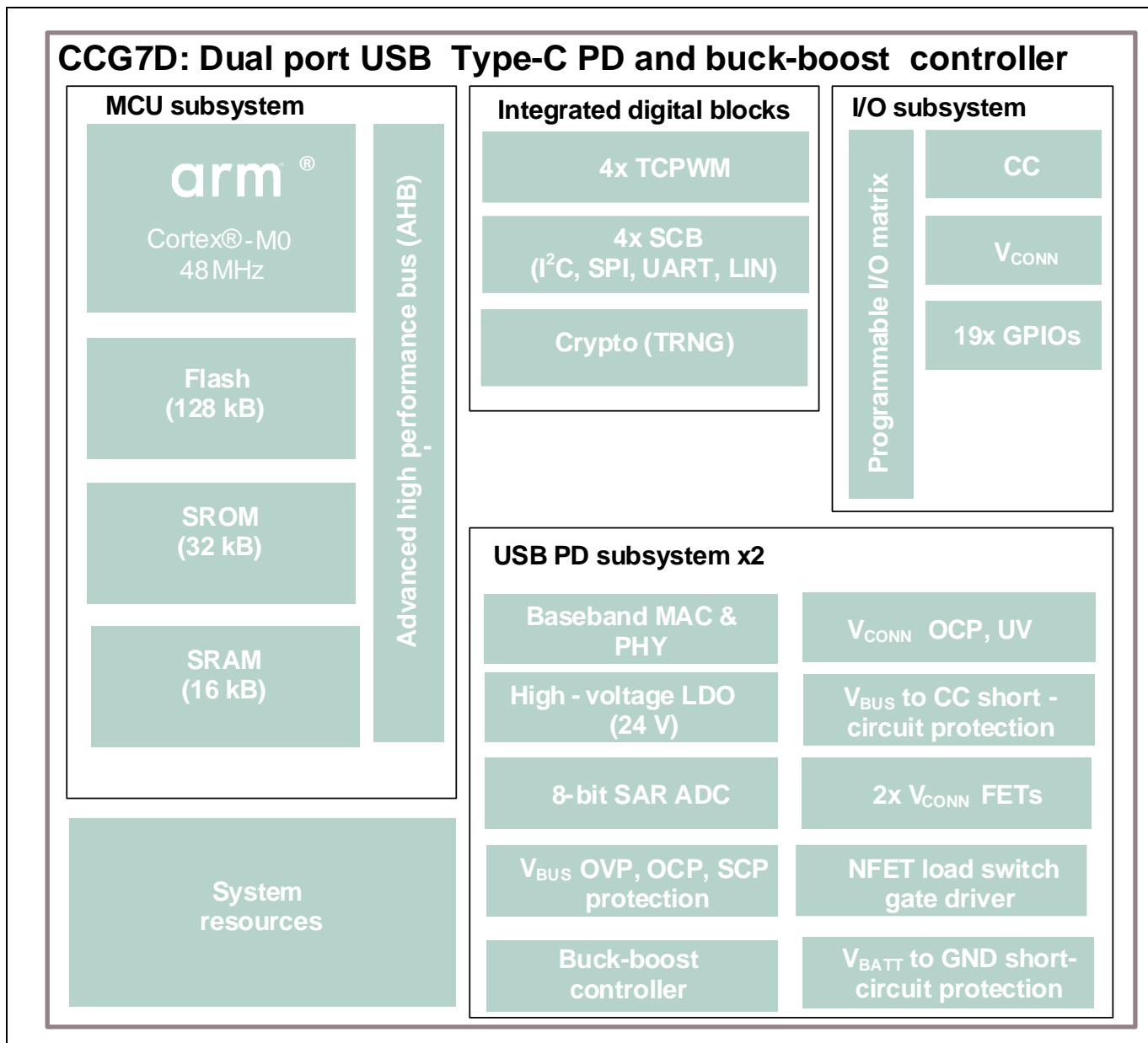


Figure 1 Logic block diagram

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



EZ-PD™ CCG7D features and applications

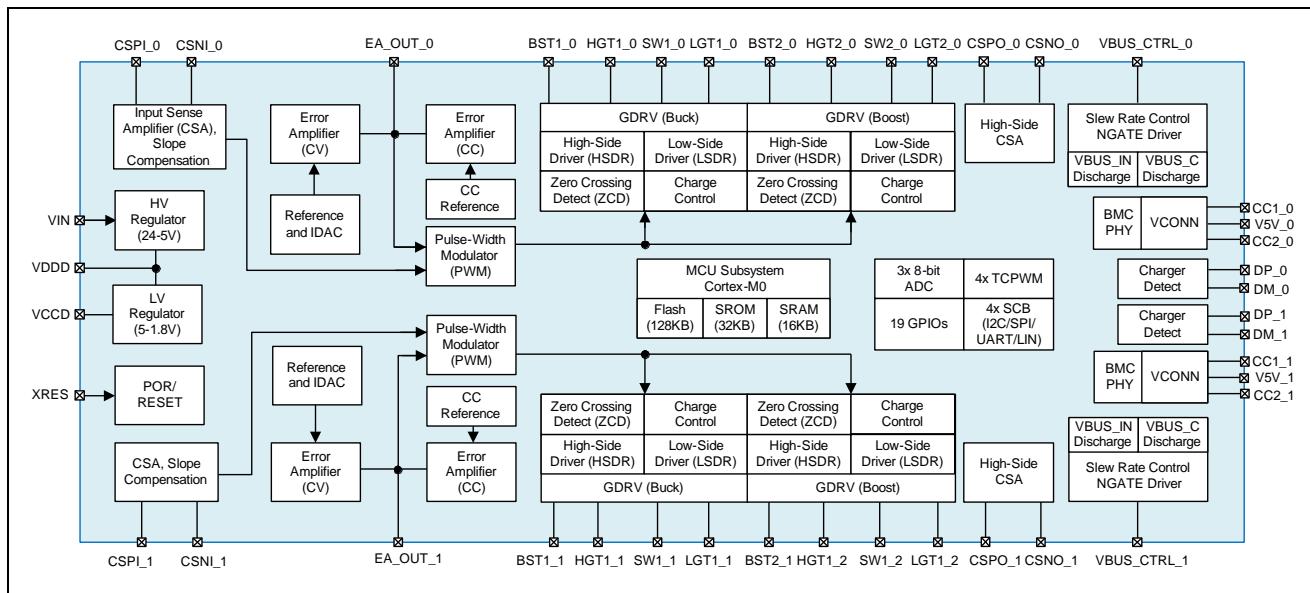


Figure 2 Functional block diagram

2.4 CCG7D in automotive head unit charger application

A head-unit charger (also known as a center stack) is located prominently in the center of the dashboard or console. These are powered by the car battery and are used primarily for charging the cell phone/tablet/laptop and for media transfer using USB data communications. In [Figure 3](#), CCG7D will always be in downstream-facing port (DFP) role supporting the charging of the device. It negotiates the power with the connected device and uses the integrated buck-boost controller to supply the required voltage and current.

The DP/DM lines of the Type-C receptacles are connected to the host processor/hub, for data connectivity to the head unit. These pins are also connected to CCG7D to support legacy charging protocol BC V1.2 CDP. The I²C interface is used to interface with the host processor/hub, to support host processor interface (HPI) commands, provide status to the head unit, and support firmware (FW) updates. Note that as per Battery Charging Specification 1.2, legacy charging protocols other than BC V1.2 CDP are not supported in conjunction with USB data communication.

CCG7D measures various temperatures using external negative temperature coefficient (NTC) thermistors. CCG7D throttles the output power based on temperature and/or shuts off the power under critical conditions. It also monitors the battery voltage and lowers the output power if the battery voltage is lower than the user-configured threshold. When no load is connected to the USB Type-C port, CCG7D remains in standby mode without switching on the buck-boost controller.

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EZ-PD™ CCG7D features and applications

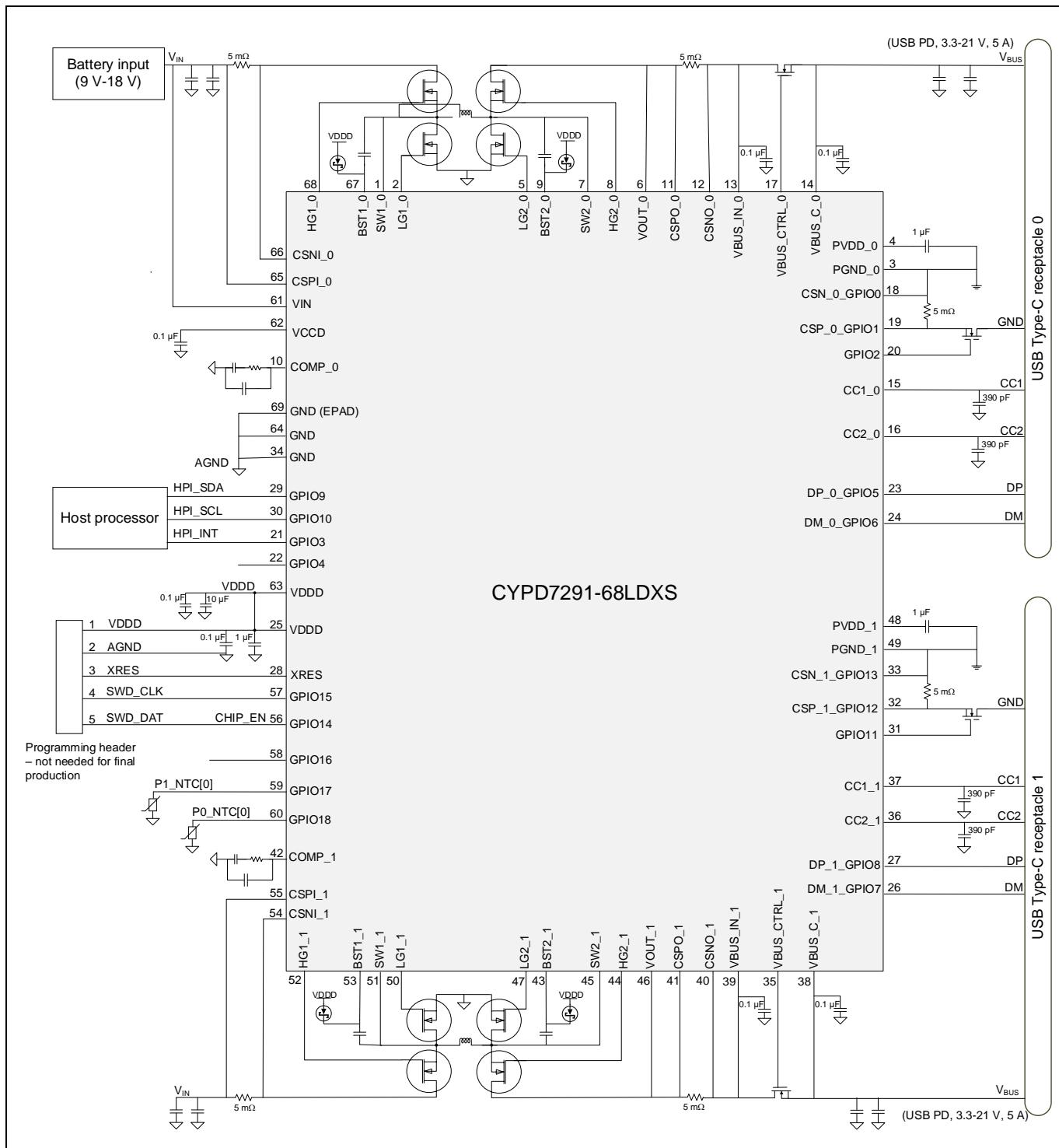


Figure 3 CCG7D head-unit charger application diagram

2.5 CCG7D in automotive RSC application

The USB-PD automotive RSC needs to deliver a wide range of configured positive output voltage and power from a 12 V nominal automotive battery. An FSBBC is the suitable topology, which can support variable input voltages and configurable output voltage applications such as USB-PD where high efficiency and power density are also required. The FSBBC configuration can act as buck, boost, or buck-boost converter to provide output voltage with the same polarity of the input voltage. Improved efficiency of the FSBBC is observed due to synchronous rectification (SR). In similar lines buck-only and boost-only operation can be achieved.

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EZ-PD™ CCG7D features and applications

Constant-frequency peak current-mode control (PCMC) is a popular control technique for switched-mode power converters. PCMC offers built-in OCP, robust dynamic responses, simplified voltage-loop compensator design, and rejection of input voltage disturbances.

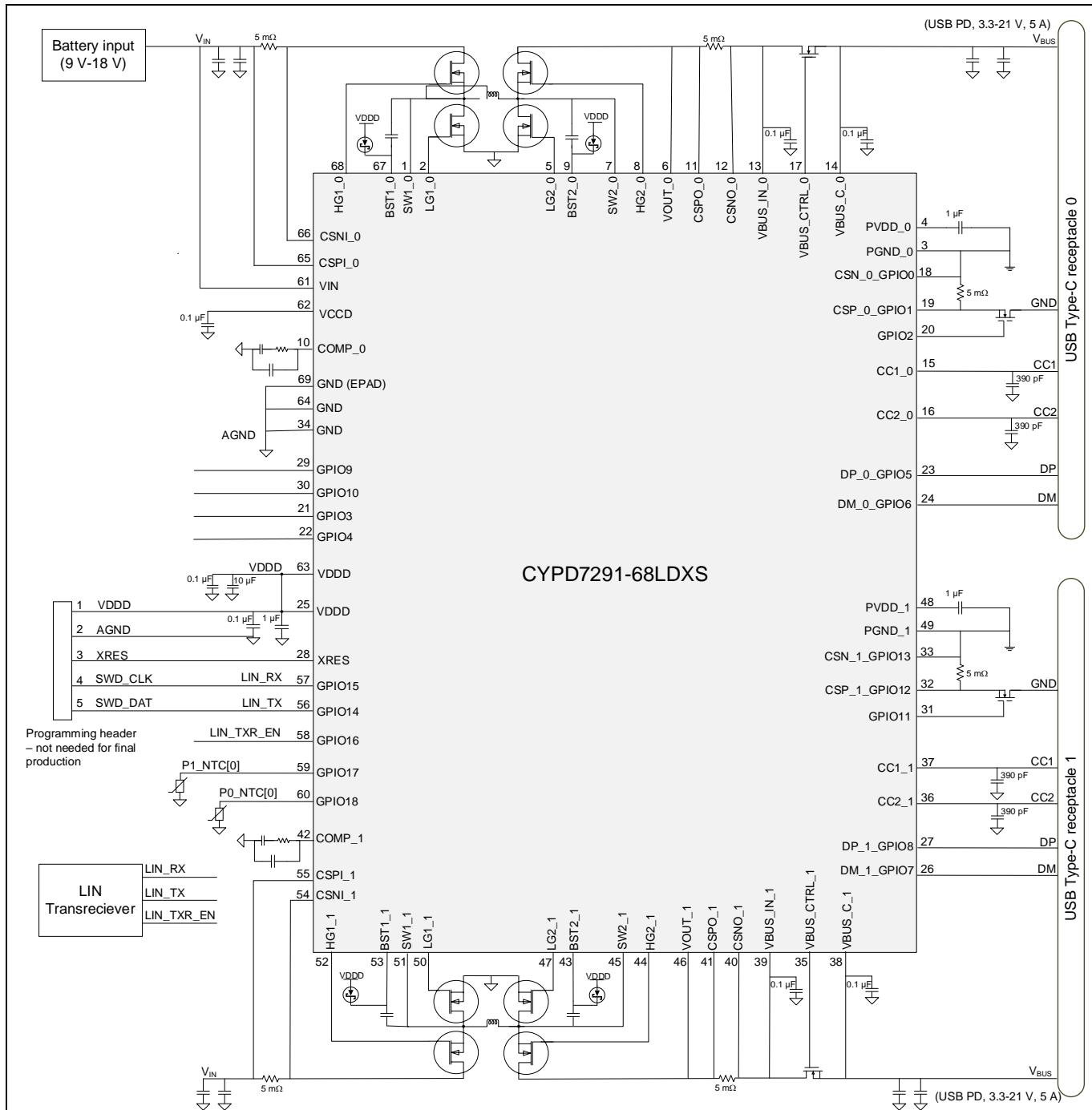


Figure 4 RSC application diagram

2.6 CCG7D in automotive RSE application

In the RSE application, one port is a dedicated charge-only port, and the second port is used for charging and streaming video content to the rear seat monitor, using a cell phone, PC or tablet. The implementation of the charging-only port is identical to the RSC application. CCG7D supports display port alternate mode sink in the

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EZ-PD™ CCG7D features and applications

port that supports video streaming and controls the external display port multiplexer over I²C. CCG7D also communicates with the system's system-on-chip (SoC) over I²C.

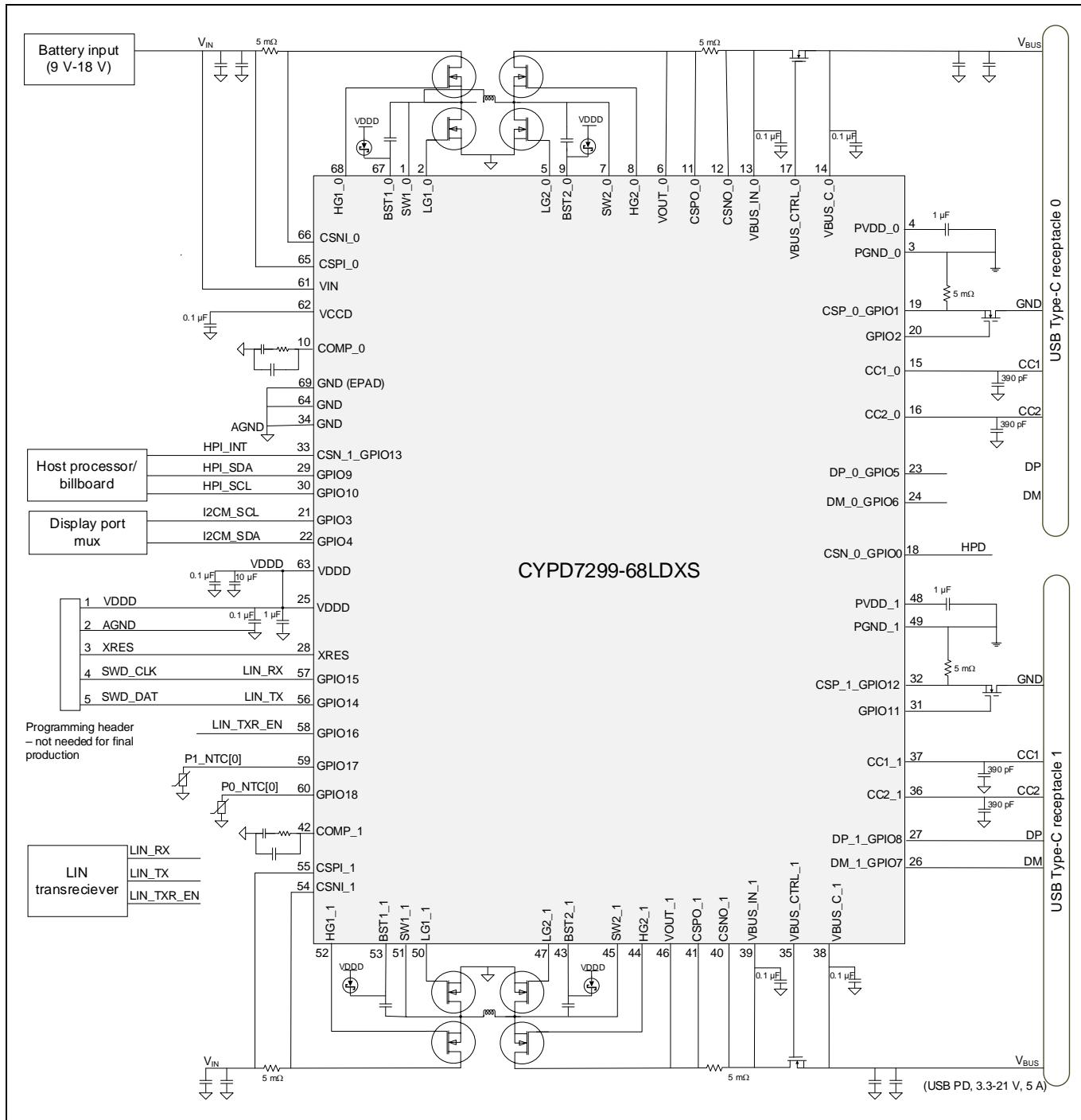


Figure 5 CCG7D RSE application diagram

3 RSC solution reference design kit requirements and features

In this hardware design user guide, the RSC solution reference design kit is taken as a use case to elaborate the design guidelines for CCG7D in automotive applications.

3.1 System description

The automotive RSC solution reference design kit exhibits the features of the CCG7D USB Type-C controller with PD and buck-boost controller. It is designed to operate from a nominal 12 V car battery and to output between 3.3 and 21 V at 3 A and a maximum of 60 W USB-PD power at each of its two source-only ports. These two ports support configurable load sharing.

3.2 Detailed feature list

- a. Highly integrated dual-port USB Type-C PD controller-based solution
- b. Two independent Type-C USB-PD charging ports controlled by a single controller
- c. Nominal switching frequency 400 kHz
- d. USB-PD source power delivery objects (PDOs)
 - i. Fixed PDOs: 5 V/3 A, 9 V/3 A, 15 V/3 A, 20 V/3 A
 - ii. PPS: 3.3 to 11 V, 3 A; 3.3 to 16 V, 3 A; 3.3 to 21 V, 3 A, with power limit
- e. Power output protections
 - i. Overvoltage protection (OVP)
 - ii. Undervoltage protection (UVP)
 - iii. Overcurrent protection (OCP)
 - iv. Short-circuit protection (SCP)
 - v. Overtemperature protection (OTP)
- f. Other power protections
 - i. V_{BUS} -to-CC short protection
 - ii. V_{BAT} -to-GND short protection
- g. Legacy charging support
 - i. USB BC 1.2
 - ii. 2.4 A Apple Charging
 - iii. Qualcomm QC 2.0, 3.0, 4.0
 - iv. Samsung AFC
- h. Programmable thermal throttling: Temperature thresholds and system responses configurable in EZ-PD™ Configuration Utility [7]
- i. Programmable input voltage throttling: Input voltage thresholds and system responses configurable in EZ-PD™ Configuration Utility [7]

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RSC solution reference design kit requirements and features

3.3 Operating conditions and characteristics

Table 1 Operating conditions and characteristics

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Units
Input voltage		V_{IN}	Full performance – meets all specs	9	12	18	V
			Full power output, with reduced performance (refer to Section 3.4.1)	5.5		11	
Output voltage range		V_{OUT}	Rated load = I_{OUT}	3.3		21.5	V
Output current range		I_{OUT}	Across all output voltages	0		3	A
Switching frequency		f_{SW}	Full load (with 15 percent spread spectrum)	340	400	460	kHz
Steady-state output voltage		V_{OUT}	Applies to DC accuracy, line regulation, load regulation, and output ripple	0.95 * V_{OUT}		1.05 * V_{OUT}	V
Output voltage during transient loads		V_{OUT}	Applies to DC accuracy, line regulation, load regulation, and output ripple Load current step 25 percent of maximum output current (I_{OUT})	0.95 * V_{OUT} - 0.1		1.05 * V_{OUT} + 0.1	V
Inrush current		I_{inrush}	V_{IN} : 0 to 12 V V_{IN} rise time: 10 ms			20	A
Port power output		P_{OUT}				60	W
System power output						120	W
Output OVP				1.15 * V_{OUT}		1.25 * V_{OUT}	V

3.4 Power throttling

Throttling refers to changing parameters or operating conditions to a predefined condition with respect to certain input parameters. Temperature and battery voltage (V_{IN}) are the parameters based on which power throttling shall be performed in this solution. We defined four operating conditions (OCs) or levels for the RSC solution, as summarized in the following table.

Table 2 Operating condition levels

Operating condition	Power per port (*PDP: PD power)
OC1	60 W
OC2	75 percent of PDP at OC1
OC3	50 percent of PDP at OC1
OC4	Shutdown

The OC2 and OC3 levels can be modified in the EZ-PD™ Configuration Utility [\[7\]](#).

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RSC solution reference design kit requirements and features

3.4.1 Power throttling based on input voltage

In V_{IN} -based power throttling, the power budget that is available to the source port depends on the V_{IN} voltage or car battery voltage level. The input voltage threshold settings for power throttling can be configured using the EZ-PD™ Configuration Utility [7]. The following table shows the operating conditions corresponding to the different voltage thresholds on the RSC solution demo board.

Table 3 Operating conditions for different voltage thresholds

Input voltage (V_{IN}) setpoint	Operating condition	Power per port	Voltage setpoint translation
$18 \text{ V} \geq V_{IN} \geq 11 \text{ V}$	OC1	60 W	The port will operate at 60 W for a voltage more than 11 V
$11 \text{ V} > V_{IN} \geq 9 \text{ V}$	OC2	75 percent of PDP at OC1	The port will operate at 75 percent of the PDP for a voltage more than 9 V and less than 11 V
$9 \text{ V} > V_{IN} \geq 5.5 \text{ V}$	OC3	50 percent of PDP at OC1	The port will operate at 50 percent of the PDP for a voltage more than 5.5 V and less than 9 V
$V_{IN} < 5.5 \text{ V}$	OC4	Shutdown	The port will shut down for a voltage less than 5.5 V

3.4.2 Power throttling based on temperature

In temperature-based power throttling, the power budget that is available to the source port depends on the measured temperature values. There is an option for adding up to four temperature sensors per port to the system. The sensors are placed in distinct locations and the values from all these sensors collectively determine the OC. There is one sensor per port on the RSC reference design.

The sensor's temperature settings for power throttling can be configured using the EZ-PD™ Configuration Utility [7]. The sensor can be enabled or disabled by setting the value of the sensor control parameter. Once the sensor is enabled, the required temperature thresholds can be set by changing the value against the OC threshold parameters in the EZ-PD™ Configuration Utility [7]. The following table shows the operating conditions for the sensor on the RSC solution demo board.

Table 4 Operating conditions for RSC solution demo board sensor

Temperature setpoint - thermistor	Operating condition	Power	Temperature setpoint translation
$-40 \leq T < 90$	OC1	60 W	The port will operate at 60 W for a temperature less than 90°C
	OC2	Skip	This condition will be skipped
$90 \leq T < 105$	OC3	50 percent of the PDP at OC1	The port will operate at 50 percent of the PDP for a temperature greater than or equal to 90°C and less than 105°C.
$T \geq 105$	OC4	Shutdown	The port will shut down for a temperature greater than or equal to 105°C.

4 Hardware design for the buck-boost converter

In the given range of input voltage, the choice of converter topology needs to provide stable output voltage. From the application specifications the input voltage can be either higher or lower than the required output voltage. The FSBBC topology provides step-up and step-down voltages seamlessly without inverting the polarity of the output voltage with respect to input voltage. The RSC solution board hardware components were chosen to meet the Type-C USB-PD standards.

4.1 Key specifications

- a. Input voltage range: +5.5 V DC to +18 V DC
- b. Output voltage range: +3.3 V DC to +21 V DC
- c. Topology: FSBBC
- d. Control method: PCMC
- e. Compensator: Type 2 compensator
- f. Support for USB-PD PPS current limit operation

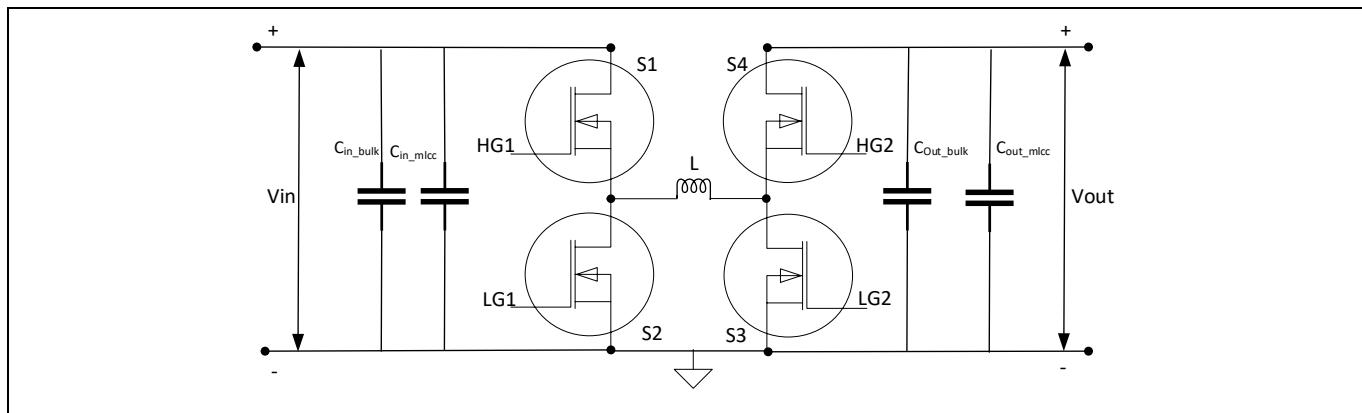


Figure 6 Simplified topology of FSBBC

4.2 Input capacitor selection

The function of input multilayer ceramic capacitors (MLCCs) is to reduce the ripple voltage amplitude on the input line, and this in turn reduces the rms ripple current handled by input bulk capacitors. Additionally, these reduce the switching noise on the input lines, thereby reducing conducted electromagnetic interference (EMI). The input capacitor's bank comprises a combination of ceramic and electrolytic capacitors. Ceramic capacitors are used to bring down the effective series resistance (ESR) of the capacitor bank, as ceramics will offer extremely low equivalent series resistance and limit the input voltage switching ripple. Bulk electrolytic capacitors are used to support the change in line current during load transient.

When the converter is operating in buck mode, the series switch (S1) [Figure 6](#) causes a pulsating ripple current with high di/dt at the input. In the absence of input filter capacitors, DC resistance of PCBs and parasitic inductance generates larger voltage ripple at the input. Input filter capacitors provide a shorter and lower-impedance path for ripple current, which in turn reduces conducted, radiated EMI and provides stability to the line voltage during input voltage fluctuations. Note that pulsating input current waves have high rms values, which cause significant heating and high harmonic content, resulting in EMI.

In an application, a good practice is to keep input voltage ripple lower than ± 5 percent to ± 10 percent of the input voltage. The input voltage peak-to-peak ripple produced by the input capacitor is equal to the input capacitor's ESR multiplied by the capacitor's rms current.

Hardware design for the buck-boost converter

The chosen input capacitor's current ratings should be equal to or greater than the rms capacitor current I_{Cin_rms} and its voltage rating is 40 to 50 percent higher than the maximum applied input voltage.

4.2.1 Input capacitor rms current – buck mode

The rms current of the input capacitor in buck mode is:

$$I_{Cin_rms} = \sqrt{\frac{1}{T} \int_0^T i_{Cin}^2 dt}$$

The input capacitor current, when switch S1 is on is ($I_{IN} - I_L$) and when switch S1 is off is I_{IN} , then I_{Cin_rms} can be written as

$$I_{Cin_rms} = \sqrt{\frac{1}{T} \left(\int_0^{DT} (I_{in} - I_L)^2 dt + \int_{DT}^T (I_{in})^2 dt \right)}$$

By neglecting the inductor ripple current (ΔI_L) in a buck converter ($I_L = I_{OUT}$) and using the relation ($I_{IN} = D * I_{OUT}$)
The rms current of the input capacitor in buck mode is:

$$I_{Cin_rms} = I_0 \sqrt{D(1 - D)}$$

Where:

I_L is the inductor current.

$$\text{The duty cycle of a buck converter } D = \frac{V_{out}}{V_{in} * \zeta}$$

ζ is the efficiency of the power converter.

4.2.2 Input ceramic capacitor selection – buck mode

The current flowing through the input capacitor (I_{CIN}) is the difference between input current (I_{IN}), inductor current (I_L) during the switch S1 on-state and only the input current (I_{IN}) during the switch S1 off-state. From this operation, during the switch S1 off-state, the input capacitors (C_{IN}) get charged with input current (I_{IN}) and during the switch S1 on-state, the input capacitor (C_{IN}) gets discharged. In steady-state the input capacitor charges added and removed are equal (i.e., capacitor amp-second balance). The input voltage ripple ΔV_{in_pk-pk} goes from its minimum to maximum value during the S1 off-state, that is, the charging period.

As we know:

$$I_{in} = C \frac{dV_{in}}{dt} = \frac{C \Delta V_{in}}{t_{off}}; \quad \text{in buck converter } I_{in} = DI_{out} \text{ and } t_{off} = (1 - D)T_{sw}$$

The MLCC value to meet the input voltage ripple requirement in buck mode is:

$$C_{in_mlcc} \gg = \frac{D (1 - D) I_{out_max}}{\Delta V_{in_pk-pk} * f_{sw}}$$

Where:

ΔV_{in_pk-pk} is allowed maximum peak-to-peak input voltage ripple

f_{sw} is operating/switching frequency of the converter

I_{out_max} is rated maximum output current

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Hardware design for the buck-boost converter

The loss due to the input capacitor's ESR is

$$P_{C_{in}} = I_{C_{in\ rms}}^2 * R_{C_{in\ mlcc}}$$

Where:

$R_{C_{in\ mlcc}}$ is the input MLCC network's total equivalent series resistance.

4.2.3 Input bulk capacitor selection – buck mode

The input supply lines are typically incapable of providing the required input current quickly enough for the converter to respond to a fast-transient load current. The input bulk capacitor provides the energy necessary to source current to the buck supply until the host supply can fill the demand. The choice of the input bulk capacitor should meet the allowable ripple current requirement and overshoot, undershoot specifications due to load transients.

The ESR of the input bulk capacitor ($R_{C_{in\ bulk}}$) and the capacitance ($C_{in\ bulk}$) need to meet the transient response requirement.

ESR of the input bulk capacitor is:

$$R_{C_{in\ bulk}} \ll 0.5 \left(\frac{V_{in_transient}}{I_{out_step} * D_{BUCK_{MAX}}} \right)$$

Where:

$V_{in_transient}$: Allowed input voltage transient undershoot or overshoot due to output load current transients

I_{out_step} : Allowed change in output load current

$D_{BUCK_{MAX}}$: Maximum duty cycle in buck mode

The capacitance of the input bulk capacitor to meet the output load transients is:

$$C_{in\ bulk} \gg \frac{D_{BUCK} * I_{out_step}}{2 * \pi * f_{bw_emi_filter} * V_{in_transient}}$$

Where:

$f_{bw_emi_filter}$: bandwidth of the input EMI LC filter

D_{BUCK} : Duty cycle in buck mode

Input voltage transient undershoot/overshoot due to load step is:

$$V_{in_transient} = \frac{I_{out_step} * D_{BUCK}}{2 * \pi * f_{bw_emi_filter} * (C_{in_bulk} + C_{in_mlcc})} + I_{out_step} * D_{BUCK} * (R_{C_{in\ bulk}})$$

Input voltage ripple is:

$$V_{in_ripple} = \frac{I_{out} * D_{BUCK} * (1 - D_{BUCK})}{f_{sw} * (C_{in_bulk} + C_{in_mlcc})} + I_{out_max} * D_{BUCK} * (R_{C_{in\ mlcc}})$$

4.2.4 Input capacitor rms current – boost mode

When the converter is operating in boost mode, the boost inductor (L) is always connected to the input, and it reduces the capacitance needed while greatly reducing the rms currents in the input capacitors.

The rms current (I_{Cin_rms}) of the input capacitor in boost mode is:

$$I_{Cin_rms} = \frac{\Delta I_L}{\sqrt{12}} \cong 0.3\Delta I_L$$

where ΔI_L is the power inductor peak-to-peak ripple current (continuous conduction mode).

4.2.5 Input bulk capacitor selection – boost mode

The capacitance of the input bulk capacitor to meet the output load transients is:

$$C_{in_bulk} \gg \frac{D_{BOOST} * I_{out_step}}{2 * \pi * f_{bw_emi_filter} * V_{in_transient}}$$

4.3 Power inductor selection

The chosen power inductor value must satisfy both buck and boost mode conditions. The lower the inductor value, the smaller the size, but this results in higher peak current.

4.3.1 Power inductor value – buck mode

The basic inductor current and voltage relation can be written as $V_L = L \frac{dI_L}{dt}$. In a buck converter the change in inductor current during the switch S1 on-time is equal to the change in current during the switch S1 off-time. The change in the inductor current (I_L) during the switch S1 on-time can be written as $\frac{\Delta I_L}{DT_{sw}}$.

$$L_{buck} = \frac{(V_{in_max} - V_{out}) * D_{Buck}}{\Delta I_L * f_{sw}}$$

ΔI_L can be fraction (0.2 to 0.4) of the I_{out_max}

Where:

V_{in_max} : maximum input voltage

4.3.2 Inductor peak current – buck mode

The maximum current passing through the power inductor in buck mode is:

$$I_{L_max_buck} = \frac{\Delta I_L}{2} + I_{out_max}$$

Switches S1 and S2 must withstand this peak current.

4.3.3 Inductor rms current – buck mode

The rms current passing through the power inductor in buck mode is:

$$I_{L_rms_buck} = \sqrt{(I_{out_max})^2 + \frac{(\Delta I_L)^2}{12}}$$

4.3.4 Power inductor value – boost mode

$$L_{boost} = \frac{V_{in_max} * D_{Boost}}{\Delta I_L * f_{sw}}$$

ΔI_L can be fraction (0.2 to 0.4) of the I_{out_max} multiplied by $\frac{V_{out}}{V_{in_min}}$

Note: In boost converter $I_{in} \approx I_L$

$$\Delta I_L = (0.2 \text{ to } 0.4) * I_{out_max} * \frac{V_{out}}{V_{in_min}}$$

Where:

$$\text{Boost converter duty cycle } D_{Boost} = 1 - \frac{(V_{in_max} * \zeta)}{V_{out}}$$

V_{in_min} : minimum input voltage

I_{in} is average input current

I_L is average inductor current

ζ is the efficiency of the converter

4.3.5 Inductor peak current – boost mode

In a boost converter the average input current I_{IN} and average inductor current I_L are equal. The peak-to-peak inductor ripple current is $\Delta I_L = D_{Boost} * \frac{V_{in}}{L * f_{sw}}$

Peak inductor current $I_{L_pk_boost}$ is the sum of the average value of the input current + one-half of the peak-to-peak inductor ripple current.

The peak current passing through the inductor is:

$$I_{L_pk_boost} = I_{in_avg} + \frac{\Delta I_L}{2} = \frac{I_{out_max}}{(1-D)} + \frac{\Delta I_L}{2}$$

The chosen switches S3, S4 should withstand this peak current.

Where:

I_{in_avg} : average input current

4.3.6 Inductor rms current – boost mode

The rms current passing through the inductor is:

$$I_{L_rms_boost} = \sqrt{(I_{in_max})^2 + \frac{(\Delta I_L)^2}{12}}$$

4.4 Power switches selection

The voltage rating of the selected power switches should be 1.5 to 2 times the maximum applied input voltage to the converter and continuous drain current rating to be greater than the computed switch peak current in a converter. The power losses of a converter depend on the chosen MOSFET characteristics such as drain-source on-state resistance (R_{ds_ON}), rise time (t_r), fall time (t_f), total gate charge (Q_g), MOSFET diode reverse recovery charge (Q_{rr}) and switching frequency (f_{sw}) of the converter. The efficiency of the converter depends on the chosen power MOSFETs, so a few basic empirical formulas are provided in the following section.

4.4.1 Power MOSFET selection – buck mode

When switch (S1) is turned on, the current passed through the switch I_{S1} is the current drawn from the input line. The switch rms current $I_{S1_rms_ON}$ is:

$$I_{S1_rms_ON} = \sqrt{\left(I_0^2 + \frac{\Delta I_L^2}{12}\right)(D_{BUCK})}$$

When switch (S2) is turned on the current passed through the switch rms current $I_{S2_rms_ON}$ is:

$$I_{S2_rms_ON} = \sqrt{\left(I_0^2 + \frac{\Delta I_L^2}{12}\right)(1 - D_{BUCK})}$$

4.4.2 Power MOSFET selection – boost mode

When switch (S3) is turned on, the current passed through the switch I_{S3} is the current drawn from the input line.

The switch rms current $I_{S3_rms_ON}$ is:

$$\begin{aligned} I_{S3_rms_ON} &= \sqrt{\frac{1}{T_{sw}} \int_0^{DT_{sw}} I_s^2 dt} = \sqrt{\frac{1}{T_{sw}} \int_0^{DT_{sw}} \left(\frac{I_0}{1 - D_{BOOST}}\right)^2 dt} = \frac{I_0}{1 - D_{BOOST}} \sqrt{\frac{1}{T_{sw}} \int_0^{DT_{sw}} dt} \\ &= \frac{I_0}{1 - D_{BOOST}} \sqrt{\frac{1}{T_{sw}} D_{BOOST} T_{sw}} \\ &= \sqrt{\left(\left(\frac{I_0}{1 - D_{BOOST}}\right)^2 + \frac{\Delta I_L^2}{12}\right)(D_{BOOST})} \end{aligned}$$

When switch (S4) is turned on, the current passed through the switch rms current $I_{S4_rms_ON}$ is:

$$I_{S4_rms_ON} = \sqrt{\left(\left(\frac{I_0}{1 - D_{BOOST}}\right)^2 + \frac{\Delta I_L^2}{12}\right)(1 - D_{BOOST})}$$

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Hardware design for the buck-boost converter

4.4.3 Power MOSFET losses – buck mode

In a synchronous buck converter, power MOSFET losses can be conduction losses, switching losses, body diode reverse recovery losses, dead time losses and gate charge losses. The empirical formulas for each of the losses are given for S1 and S2 separately.

Conduction losses in switch (S1): $(I_{S1_rms_ON})^2 * R_{ds_ON}$

Switching losses in switch (S1):

$$V_{in} * \left(I_0 - \frac{\Delta I_L}{2} \right) * 0.5 * (t_{r,s1}) * f_{sw} + V_{in} * (I_0 + \frac{\Delta I_L}{2}) * 0.5 * (t_{f,s1}) * f_{sw}$$

Diode reverse recovery losses ($t_{f,s1}$) = $V_{in} * Q_{rr} * f_{sw}$

Conduction losses in switch (S2): $(I_{S2_rms_ON})^2 * R_{ds_ON}$

Switching losses in switch (S2):

$$V_{IN} * (I_0 - \frac{\Delta I_L}{2}) * 0.5 * (t_{f,s2}) * f_{sw}$$

Dead time losses and gate charge losses are for both the S1 and S2.

Dead time losses = $2 * V_{S2Diode} * (I_0) * (t_{deadtime}) * f_{sw}$

MOSFET gate charge losses = $2 * Q_g * f_{sw} * V_{gd}$

Where:

$t_{deadtime}$: Dead time between S1 and S2

$t_{r,s1}$: Rise time of the S1

$t_{f,s1}$: Fall time of the S1

$t_{r,s2}$: Rise time of the S2

$t_{f,s2}$: Fall time of the S2

Q_{rr} : Reverse recovery charge of the switch

R_{ds_ON} : MOSFET drain-source on-state resistance – datasheet parameter

V_{gd} : Gate driving voltage

Q_g : Gate charge

4.4.4 Power MOSFET losses – boost mode

In a synchronous boost converter power MOSFET losses can be conduction losses, switching losses, body diode reverse recovery losses, dead time losses and gate charge losses. The empirical formulas for each of the losses are given for S3 and S4 separately.

Conduction losses in switch (S3): $(I_{S3_rms_ON})^2 * R_{ds_ON}(T)$

Switching losses in switch (S3):

$$V_o * \left(\frac{I_0}{(1 - D_{BOOST})} - \frac{\Delta I_L}{2} \right) * 0.5 * (t_{f,s3}) * f_{sw} + V_o * \left(\frac{I_0}{(1 - D_{BOOST})} + \frac{\Delta I_L}{2} \right) * 0.5 * (t_{r,s3}) * f_{sw}$$

Conduction losses in switch (S4): $(I_{S4_rms_ON})^2 * R_{ds_ON}$

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Switching losses in switch (S4):

$$V_{out} * \left(\frac{I_0}{(1 - D_{BOOST})} - \frac{\Delta I_L}{2} \right) * 0.5 * (t_{r,S4}) * f_{sw}$$

Diode reverse recovery losses (S4) = $V_o * f_{sw} * Q_{rr,S4}$

Dead time losses and gate charge losses are for both the S3 and S4.

Dead time losses = $2 * V_{S4\text{Diode}} * I_0 * T_{deadtime} * f_{sw}$

MOSFET gate charge losses = $2 * Q_g * f_{sw} * V_{gd}$

Here:

$t_{r,S3}$: S3 MOSFET rise time – datasheet parameter

$t_{f,S3}$: S3 MOSFET fall time – datasheet parameter

$t_{r,S4}$: S4 MOSFET rise time – datasheet parameter

$t_{f,S4}$: S4 MOSFET fall time – datasheet parameter

$Q_{rr,S4}$: MOSFET diode reverse recovery charge – datasheet parameter

Q_g : MOSFET gate charge total – datasheet parameter

V_{gd} : MOSFET gate drive voltage – specified in the controller datasheet

$R_{ds,ON}$: Drain-source on-state resistance – datasheet parameter

$t_{deadtime}$: Dead time between S3 and S4

$V_{S4\text{Diode}}$: High-side switch inverse diode forward voltage

4.5 Output capacitors selection

When there is a change in the load current (load transient), the converter's output feedback control loop senses the change and adjusts the duty cycle of the converter. Typically, in an application the rate of change in load current is faster than the loop response. Hence, to support the load transients bulk capacitors at the output need to be added and for output ripple to be in the specified limits high-frequency bypass capacitors (MLCCs) need to be added in parallel to the output bulk capacitors.

4.5.1 Output capacitor selection – buck mode

An output capacitor is required to maintain a regulated output voltage while the switch (S1) is off, and must be able to respond to change in load current. It is necessary to minimize the amount of ripple on the output voltage. The output capacitor's maximum ESR can be computed using the specified maximum output voltage ripple, $\Delta V_{out,pk-pk}$ and the maximum load current $I_{out,max}$. The maximum ESR of the output capacitors must be lower than the computed $R_{Cout,max}$ to have an output voltage ripple below the specification value.

$$R_{Cout,max} = 0.5 * \left(\frac{\Delta V_{out,pk-pk}}{I_{out,max}} \right)$$

Here,

$\Delta V_{out,pk-pk}$ is allowed output voltage ripple; typically it will be 3 to 5 percent of V_{out} .

The output capacitor value in a buck converter to meet the specified ripple requirement is:

$$C_{out,mlcc} \gg \frac{\Delta I_L}{8 * f_{sw} * \Delta V_{out,pk-pk}}$$

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Hardware design for the buck-boost converter

The output capacitor must be able to handle output current transient requirements.

$$C_{out_Bulk} = \frac{I_{out_Step}}{\Delta V_{out_transient}} * \frac{1}{2 * \pi * f_{BW_Buck}}$$

The output voltage ripple equation can be written as:

$$\Delta V_{out_pk-pk} = \frac{\Delta I_L}{8 * f_{sw} * C_{out_mlcc}} + \Delta I_L * R_{Cout_max}$$

4.5.2 Output capacitor rms current – buck mode

Ripple current flowing through the output capacitor in buck mode is:

$$I_{Cout_rms} = \sqrt{I_{L_max_buck}^2 - I_{out_max}^2}$$

or

rms current in the output capacitor in buck mode is:

$$I_{Cout_rms} = \frac{\Delta I_L}{\sqrt{12}} \cong 0.3\Delta I_L$$

Where,

ΔI_L is the power inductor peak-to-peak ripple current (continuous conduction mode).

4.5.3 Output capacitor selection – boost mode

Output voltage ripple is contributed by capacitor ESR and charging/discharging of the output capacitor. When the power switch S3 is on, the output capacitor supports the required load demand and when the power switch (S3) turns off, I_{Lmax_boost} flows into the output capacitor causing change in output voltage $\Delta V_{out} = I_{Lmax_boost} * R_{Cout_max}$.

The output capacitor in a boost converter can be computed by using:

$$C_{out_mlcc} = \frac{I_{out_max} * D_{max_Boost}}{f_{sw} * \Delta V_{out}}$$

The maximum ESR of the output capacitors must be lower than the computed R_{Cout_max} to have an output voltage ripple below the specification value.

$$R_{Cout_max} \ll \frac{\Delta V_{out}}{\frac{I_{out_max}}{1 - D_{max_boost}} + \frac{\Delta I_L}{2}}$$

Boost converters will have a right-half plane (RHP) zero in the control to output transfer function and due to this the total loop bandwidth is limited to one-fifth of the RHP zero frequency (f_{RHP_Zero}).

$$f_{RHP_zero} = \frac{R_o}{2\pi L_{BOOST}} * \left(\frac{V_{in}}{V_o}\right)^2 = \frac{V_o}{I_o * 2\pi L} * \left(\frac{V_{in}}{V_o}\right)^2$$

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Hardware design for the buck-boost converter

Now the choice of output bulk capacitor to meet the load transient requirement is:

$$C_{out_bulk} = \frac{I_{out_Step}}{\Delta V_{out_transient}} * \frac{1}{2 * \pi * f_{BW_Boost}}$$

Here:

I_{out_step} is the step change of the output load

$\Delta V_{out_transient}$ output voltage variation due to step change of output load

Output voltage ripple ΔV_{out_ripple} is:

$$\Delta V_{out_ripple} = \frac{I_{out_max} * D_{max_boost}}{f_{sw} * C_{out_bulk}} + (I_{out_max} * R_{Cout_max})$$

4.5.4 Output capacitor rms current – boost mode

The output capacitor ripple current in boost mode is:

$$I_{Cout_rms} = \sqrt{(I_{in} - I_0)^2 * (1 - D_{BOOST}) + I_0^2 * D_{BOOST}}$$

$$I_{Cout_rms} = I_0 \sqrt{\frac{D_{BOOST}}{(1 - D_{BOOST})}}$$

4.6 EMI filter selection

EMI is the disruption of correct operation of an electronic device, caused by an electromagnetic field generated by a different device. To prevent electronics from interfering with the operation of other devices, device EMI is regulated by the government or regulatory bodies where the electronic device is being sold.

EMI is difficult to accurately predict, so the best thing is to minimize the known causes of EMI when planning PCB layout and design. Note that EMI performance can be affected by board design, filters, MOSFET slew rates, inductor shielding and bypass capacitor placement.

Compliance with EMI standards frequently offers a significant challenge to many automotive designers and engineers. Automotive EMI standards are more stringent than industrial and communication standards. The RSC solution board is designed to meet the CISPR 25 class 5 specifications.

Typically, the low-pass filter (LPF) provides greater attenuation for the higher-order harmonics of the switching frequency, and the corner frequency ($f_{bw_emi_filter}$) of the LPF can be one-tenth of the switching frequency.

One of the design criteria is that the impedance of the EMI filter (Z_{filter}) must be much smaller than the converter input (Z_{in_smps}) impedance.

$$Z_{in_smps} = \frac{V_{in}^2 * \zeta}{V_{out} * I_{out}}$$

$$Z_{filter} \ll \frac{Z_{in_smps}}{10}$$

$$f_{bw_emi_filter} \approx \frac{f_{sw}}{10}$$

The filter capacitor (C_{filter}) value can be computed with:

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$$C_{\text{filter}} = \frac{1}{2\pi * f_{\text{bw_emi_filter}} * Z_{\text{filter}}}$$

From Z_{filter} and C_{filter} , the filter inductor (L_{filter}) value can be computed:

$$L_{\text{filter}} = Z_{\text{filter}}^2 * C_{\text{filter}}$$

The front-end EMI filter ($L_{\text{filter}}, C_{\text{filter}}$) leads to a modified control to output transfer function, which may cause instability. A capacitor (C_{damping}) much larger than C_{filter} is required for the ($L_{\text{filter}}, C_{\text{filter}}$) filter to detect R_{damping} at the middle frequency; $C_{\text{damping}} \gg 4C_{\text{filter}}$ may be an acceptable value.

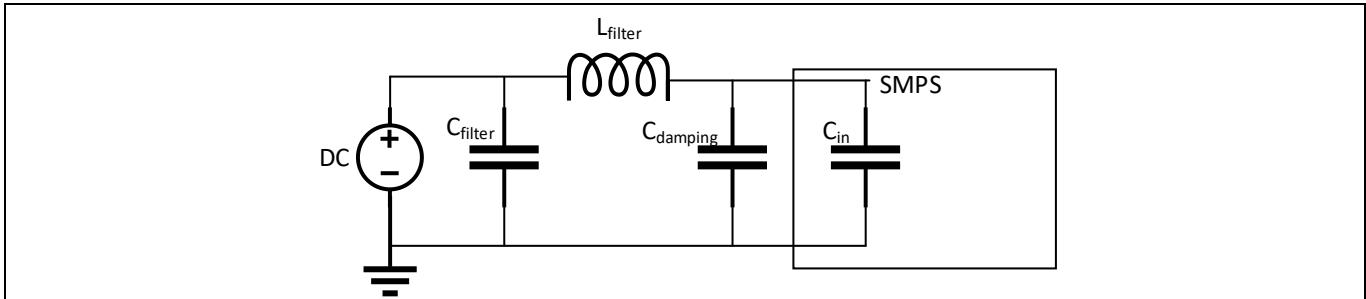


Figure 7 SMPS with input EMI LC filter

4.6.1 Second-stage EMI filter

The impedance of the inductor decreases at the FM frequency band (76 to 108 MHz). As such, it is recommended to add another filter stage with a ferrite bead, as it has a higher resonant frequency.

A ferrite bead filters high-frequency noise energy over a broad frequency range, offers resistance over its intended frequency range and dissipates noise energy in the form of heat. Capacitors on either side of the ferrite bead form a LPF network, further reducing the high-frequency power supply noise.

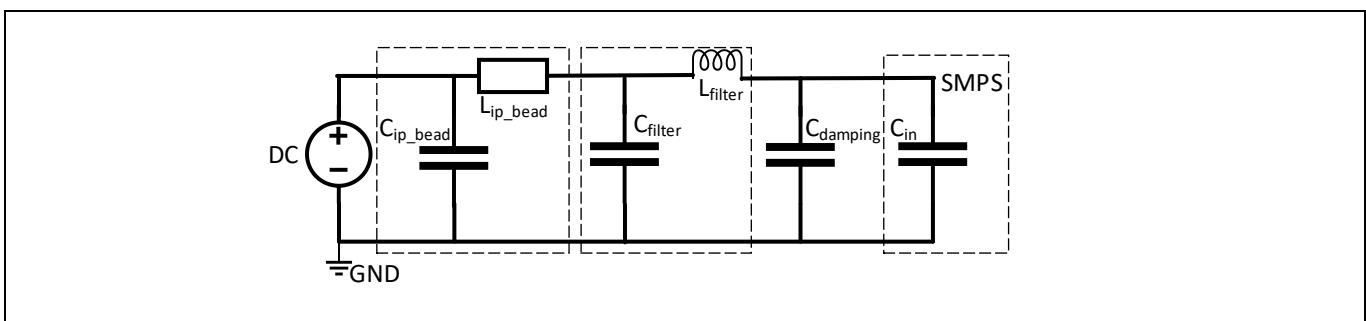


Figure 8 Two-stage EMI filter

Choose a ferrite bead which offers highest impedance at around the FM frequency band ($f_{L-\text{ip_bead}}$). Compute inductance of the ferrite bead using:

$$L_{\text{ip_bead}} = \frac{X_{L,\text{ip_bead}}}{2 * \pi * f_{L-\text{ip_bead}}}$$

Here:

Impedance $Z = X_{L,\text{ip_bead}}$

A ferrite bead-based filter capacitor can be computed using: $f_{\text{FM_band}} = \frac{1}{2\pi\sqrt{L_{\text{ip_bead}} * C_{\text{ip_bead}}}}$

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Hardware design for the buck-boost converter

4.6.2 Ferrite bead filter – output

When the converter is operating in boost mode, ferrite beads at the output side will be effective. The frequency vs. impedance characteristics are critical when choosing the ferrite beads; ensure that the resistive impedance (R) is much higher than the reactive impedance (X) in the noise frequency range.

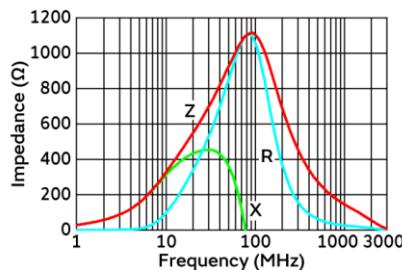


Figure 9 Impedance-frequency characteristics of BLM21SP102SH1 – Murata

4.7 Current sense resistor (R_i) selection

CCG7D internal high-side CS amplifiers (CSAs) measure the peak current (I_{IN}) sensing through an external CS resistor (R_i) placed in the V_{IN} path. The drop across R_i is applied between the CCG7D terminal CSPI and CSNI. The choice of external CS resistor (R_i) is critical to the control of FSBBC; a smaller value of R_i will provide lower power loss, and at the same time, it should support the dynamic range required for the measurement.

A minimum 5 mΩ CS resistor is required to have a good signal-to-noise ratio in the feedback path and to accurately measure the input current. CCG7D has the programmable CSA gain to amplify the feedback signal. Make sure the product of CSA gain and V_{IN} ($I_{IN} * R_i$) is not more than 1.60 V. A CSA gain setting of 9 is recommended for better signal fidelity.

4.8 Bootstrap circuit design

A bootstrap circuit is used in half-bridge configurations to supply bias to the high-side MOSFET (S1), as it requires a voltage supply referenced at the source of the high-side MOSFET. The basic circuit elements are C_{Boot} , D_{Boot} and these are to be designed to reliably drive the high-side MOSFET.

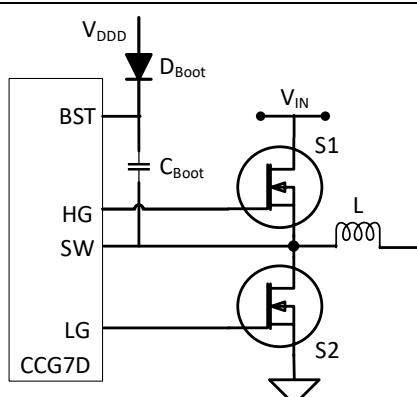


Figure 10 Bootstrap circuit

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Hardware design for the buck-boost converter

4.8.1 Bootstrap capacitor (C_{Boot}) design

The minimum charge needs to be supplied by the bootstrap capacitor $Q_{bs} = 2 * Q_g$.

The bootstrap capacitor must be able to supply this charge and retain its full voltage. If that does not happen, there will be a significant amount of ripple on the V_{bs} voltage (Voltage across the C_{Boot}).

$$C_g = \frac{Q_g}{(V_{DD-} - V_{fbootdiode})}$$

$$C_{Boot} \gg 20 * C_g$$

Where:

V_{DDD} : Supply voltage

$V_{fbootdiode}$: Forward voltage drop across the bootstrap diode

Q_g : Gate charge of high-side FET

The chosen bootstrap capacitor (C_{Boot}) should be able to withstand a minimum of switch node voltage (SW) + V_{DDD} .

4.8.2 Bootstrap diode (D_{Boot}) design

The bootstrap diode (D_{Boot}) needs to be able to block the full power rail voltage, which is seen when the high-side MOSFET (S1) is switched on. It must be a fast recovery diode to minimize the amount of charge fed back from the bootstrap capacitor (C_{Boot}) into the V_{DDD} supply, and similarly the high temperature reverse leakage current will be important if the capacitor must store charge for long periods of time. The current rating of the bootstrap diode is the product of the gate charge of the MOSFET and the switching frequency (f_{sw}).

$$i_{DBoot} = Q_g * f_{sw}$$

4.9 Provider FET design

The provider FET or series switch is connected between the FSBBC output and USB Type-C connector. The maximum differential voltage is the expected maximum output voltage (V_{BUS_OUT}) and the drain current is the maximum output current of the output port. The chosen MOSFET should have lower $R_{DS(on)}$ as this switch is only to connect or disconnect with the load/sink. The high-side MOSFET gate drive is provided by CCG7D pin V_{BUS_CTRL} and the chosen FET gate threshold voltage should be lower than the V_{DDD} of the silicon (5 V).

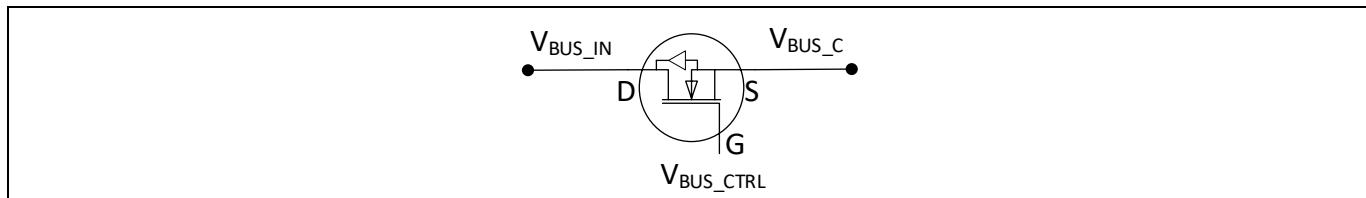


Figure 11 Provider FET

4.10 Bypass capacitor selection

The choice of bypass capacitors at V_{DDD} , V_{CCD} , P_{VDD} should meet the values recommended in the CCG7D datasheet and the typical values shown in [Figure 12](#). The chosen capacitors should have low ESR to bypass the AC signal present in the DC voltage, and typically it is a combination of high-value and low-value capacitors.

The high-value capacitors, typically in the range of 4.7 to 10 μ F, suppress the low-frequency noise and the high-frequency noise is suppressed by low-value capacitors typically in the range of 0.01 to 0.1 μ F.

To absorb the dynamic change of voltages at V_{BUS_IN} , V_{BUS_C} and V_{IN} , it is recommended to place capacitor value in the order of 0.1 μ F.

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Hardware design for the buck-boost converter

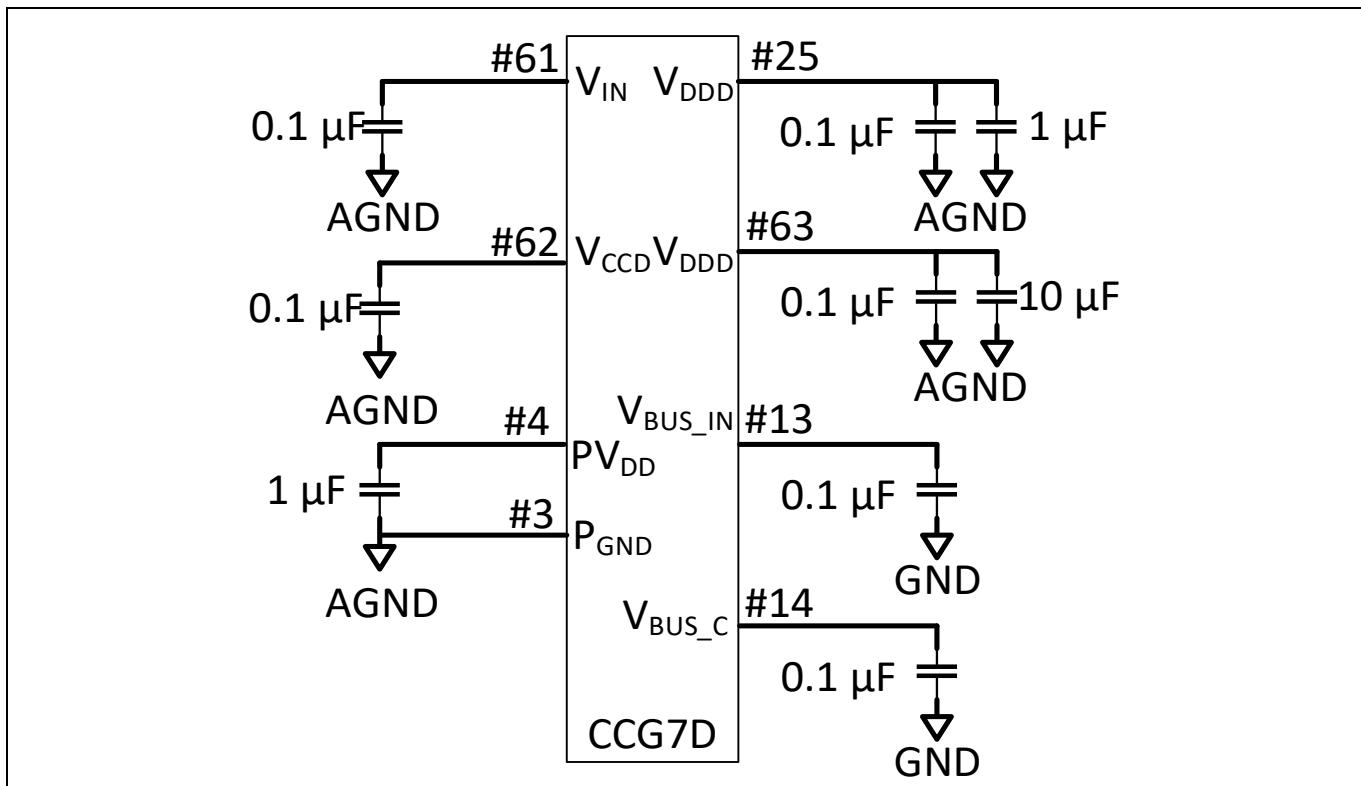


Figure 12 Bypass capacitors

4.11 Cable voltage drop compensation

In an ideal PD connection, voltage seen at the sink port must be same as the contracted voltage. Though the source supplies requested voltage, voltage at the sink end may be less due to the external cable voltage drop. The external cable voltage drop depends on two parameters: cable resistance and requested sink current. By considering the external cable resistance as a constant, which is a fixed value for a captive design and typical value for a receptacle design, the source shall supply an extra voltage in addition to the contracted voltage to compensate the external cable drop for the changing load current or sink current.

The USB cable resistance can go up to ~500 mΩ, considering the use case of more than 3-meter-long cable connected between the car dashboard and the rear charging port. The USB cable resistance can be configured through EZ-PD™ Configuration Utility [7].

4.12 V_{BUS} discharge

CCG7D supports V_{BUS} discharge capability on both V_{BUS_IN} and V_{BUS_C} ends (before and after the provider FET respectively). V_{BUS_IN} discharge is via #13, while V_{BUS_C} discharge is via #14 of CCG7D for port #0 and V_{BUS_IN} discharge is via #39, while V_{BUS_C} discharge is via #38 of CCG7D for port #1. The discharge FET and resistors are internal to CCG7D and no external components are needed for either of discharge paths.

V_{BUS_IN} and V_{BUS_C} discharge are enabled upon disconnecting the USB cable and during the output voltage transitions from higher voltage to lower voltage. The default discharge resistor values are set to 500 Ω on V_{BUS_IN} and 2 kΩ on V_{BUS_C}. Maximum and minimum discharge strength values are software-configurable pre-processor switches. The discharge drive strength can be configured through EZ-PD™ Configuration Utility [7].

4.13 CC and DP/DM terminations

CCG7D supports termination needed on the CC line for Type-C PD. The only external component needed is a 390 pF capacitor on each of the CC lines (CC1 and CC2).

CCG7D also has the required termination on the D+/D- lines to support legacy charging protocols such as BC1.2, Samsung AFC, Apple Charging and Qualcomm Charging. CCG7D supports two pairs of D+/D- lines, which can be useful in dual-port charging systems.

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Constant current and constant voltage regulation

5 Constant current and constant voltage regulation

The CCG7D is targeted toward charging of sink devices such as cell phones, battery banks and laptops in the automotive environment. The sink device broadcasts its state of battery charging to the source device, the CCG7D built-in constant current (CC) loop, and a constant voltage (CV) loop, which transition automatically from CC to CV mode and vice versa based on the connected sink device battery status. In CC mode, CCG7D modulates the feedback to keep the load current constant and in CV mode, the output voltage is constant.

The CC/CV feedback loops are implemented by means of two transconductance amplifiers and an external compensator network sets the frequency response of the CC and CV feedback loops.

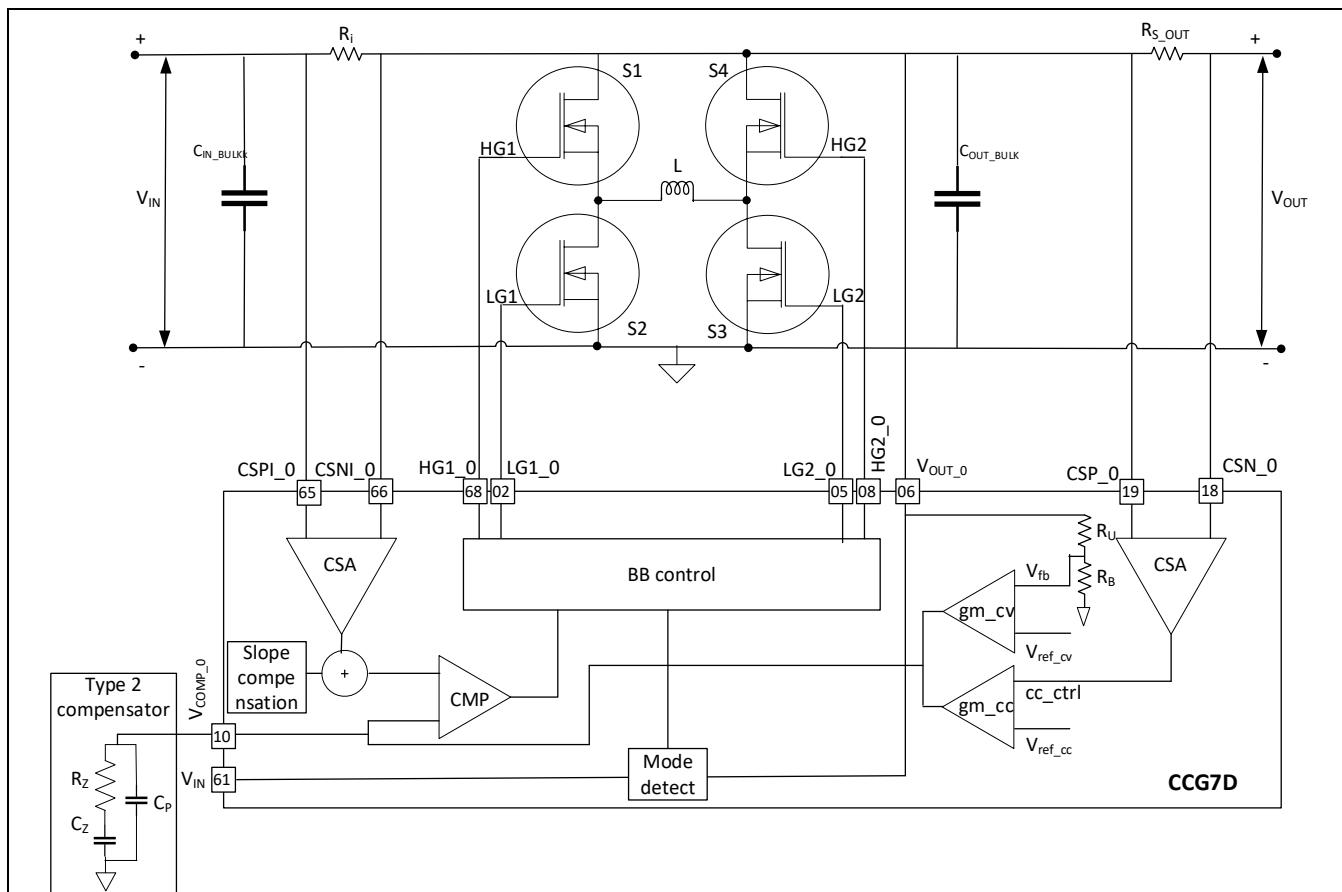


Figure 13 Control loop architecture

The error amplifier block regulates output voltage (V_{BUS_C}) or output current (I_{OUT}) during CV or CC mode, respectively. The port #0 control loop architecture is shown in [Figure 13](#).

CCG7D is designed to regulate constant output voltage (V_{BUS_C}) in the 3.3 V to 21 or 21.5 V range, with a 20 mV step size as needed by the PPS specification. Default 5 V output voltage (V_{BUS_C}) is dictated by the reference voltage V_{ref_cv} and the internal resistor divider of R_U 200 k Ω and R_B 34.5 k Ω . CC operation can be achieved based on the V_{ref_cc} setting and gain of the amplifier (CSA_{OUTPUT}).

The CCG7D silicon family supports V_{BUS_C} current (I_{OUT}) measurement and control using an external sense resistor R_{S_OUT} (5 m Ω) in series with the V_{BUS_C} path. The voltage drop across the external sense resistor, R_{S_OUT} , measures the average output current (I_{OUT}). R_{S_OUT} also controls the output current in the PPS current foldback mode of operation.

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Constant current and constant voltage regulation

The CV and CC loops are independent of each other, sharing the same external compensation network. The compensation network must be designed based on the choice of the power converter operating mode and chosen power stage component values.

6 Control system design

The choice of the type 2 external compensator component (R_Z , C_Z and C_P) values are based on the desired loop crossover frequency (f_c), chosen power component values and transconductance amplifier gain (g_{m_cv}).

6.1 Type 2 compensator component selection

The compensator resistor R_Z can be computed by choosing the required crossover frequency. As a rule of thumb, in a buck converter the crossover frequency can be about one-tenth of the switching frequency.

In a boost converter the crossover frequency can be about one-tenth of the switching frequency and about one-fifth of the RHP zero frequency, whichever is lower.

$$R_Z = \frac{2\pi(R_U + R_B) * R_i * C_{out} * f_c}{R_B * g_{m_cv}} \text{ - for buck converter}$$

$$R_Z = \frac{\pi(R_U + R_B) * R_i * C_{out} * f_c}{R_B * g_{m_cv} * (1-D)} \text{ - for boost converter}$$

CCG7D has the internal resistive divider from the output to error amplifier. $R_B = 34.5 \text{ k}\Omega$ $R_U = 200 \text{ k}\Omega$. R_i is the input CS resistor multiplied by input CSA gain (G_{CSA}).

The compensator zero (f_{zcomp}) is placed at the dominant pole (f_{pplant}) of the power converter, simplifying the equation to get C_Z :

$$C_Z = \frac{R_{out} * C_{out}}{R_Z} \text{ - for buck converter}$$

$$C_Z = \frac{R_{out} * C_{out}}{2 * R_Z} \text{ - for boost converter}$$

The compensator pole (f_{pcomp}) is placed at ESR zero (f_{zplant}) of the power converter, simplifying the equation to get C_P :

$$C_P = \frac{R_{Cout} * C_{out}}{R_Z}$$

7 Fault protections

The CCG7D offers integrated fault protection features such as input OVP/UVP, output (V_{BUS_C}) OVP/UVP, V_{BUS_C} OCP and SCP, V_{BUS} -to-CC short protection, and internal temperature protection. The CCG7D also provides gate drive signal for the V_{BAT} -to-GND protection FET and supports board temperature measurement using external thermistors. This user guide also discusses a few external system-level fault protections.

7.1 Input under/overvoltage protection

CCG7D supports input UVP/OVP when input voltage is below or above reliable threshold levels. It guarantees predictable behavior when the CCG7D is up and running. The input UV/OV fault thresholds are configurable using EZ-PD™ Configuration Utility [7].

7.2 Output (V_{BUS}) under/overvoltage protection

CCG7D supports monitoring of output (V_{BUS_C}) UV/OV faults using internal V_{BUS_IN} / V_{BUS_C} resistor dividers. The fault thresholds and response times are configurable using EZ-PD™ Configuration Utility [7].

7.3 V_{BUS} overcurrent protection and short-circuit protection

CCG7D supports monitoring of output (V_{BUS_C}) faults using internal comparators. Short circuit is at a higher threshold as compared to overcurrent threshold. Response times for short circuit protection are much faster compared to OC. External filters on the current sensing path will increase the response time to over current and short circuit current protections. The OCP and SCP thresholds and response times are configurable using EZ-PD™ Configuration Utility [7].

7.4 V_{BUS} -to-CC short protection

CCG7D CC pins have integrated protection from accidental shorts to HV V_{BUS_C} and V_{BAT} . CCG7D silicon can handle up to 24 V external voltage on its CC pins without damage.

7.5 Built-in overtemperature protection

CCG7D supports OTP through an integrated ADC circuit and internal temperature sensor. The overtemperature cutoff value, restart value and debounce period (ms) are configurable using EZ-PD™ Configuration Utility [7].

7.6 V_{CONN} switches and protection

CCG7D's internal LDO voltage regulator is capable of powering a 100 mW V_{CONN} supply for electronically marked cable assemblies (EMCAs), V_{CONN} -powered devices (VPDs) and V_{CONN} -powered accessories as defined in the USBC Specification [6]. All circuitry including V_{CONN} switches and OCP is integrated in the device.

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Fault protections

7.7 V_{BAT}-to-GND protection

The CCG7D silicon can protect against high currents through the Type-C return (ground) path. An NFET and a CS resistor are placed in series with the ground return path from the Type-C connector, as shown in [Figure 14](#). This resistor senses the current, and if it exceeds the FW-configured threshold, the NFET is turned off to interrupt the current. This protects against OC conditions caused by external faults (e.g., if the Type-C connector ground is accidentally connected to the car's battery). The CS can be implemented with either a single-ended connection (referenced to internal ground, CSN_0_GPIO0 is optional in [Figure 14](#)) or with a true differential connection (CSN_0_GPIO0 connection in [Figure 14](#)). The differential connection provides better current measurement accuracy but uses an extra GPIO.

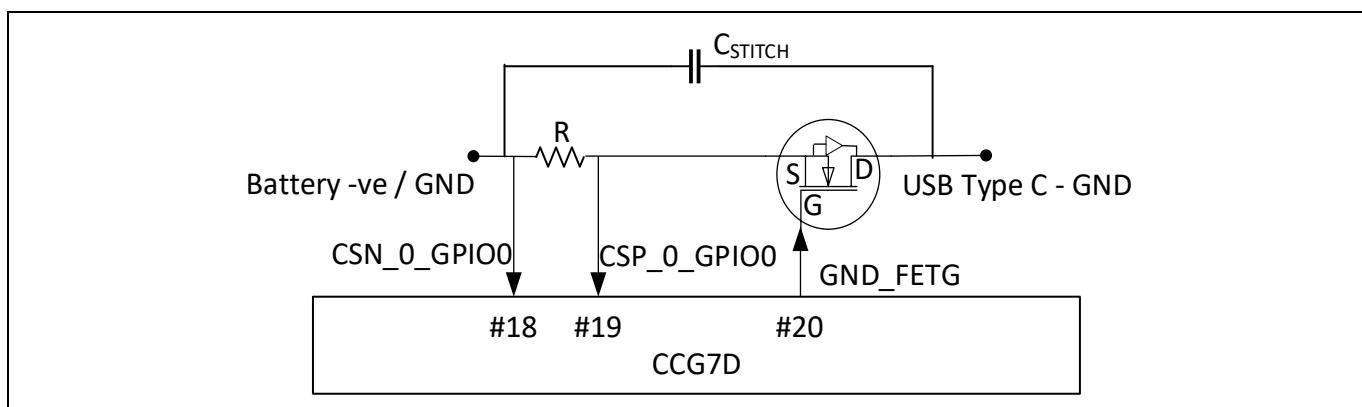


Figure 14 V_{BAT}-to-ground SCP

7.8 Battery reverse polarity protection

A battery reverse polarity protection circuit is inevitable in the automotive environment. During maintenance there may be a possibility of reversing the battery polarity and this can damage the electronics connected to it.

ISO 16750-2 Road vehicles – Environmental conditions and testing for electrical and electronic equipment – Part 2: Electrical loads “4.7 Reversed voltage” checks the ability of a device under test (DUT) to withstand the connection of a reversed battery while using an auxiliary starting device. The nominal voltage of 12 V battery-driven systems should withstand a test reverse voltage of 14 V for at least 60 s ± 6 s.

System-level battery reverse polarity protection can be achieved with an N-channel MOSFET, which will offer lower power losses than a Schottky diode, and the N-channel MOSFET requires a gate driver circuit. The maximum drain-to-source voltage must be high enough to withstand the highest differential voltage seen in the application, and for this application it is recommended to use a MOSFET with voltage rating of 60 V. The continuous drain current rating of the MOSFET should be higher than the maximum continuous input current.

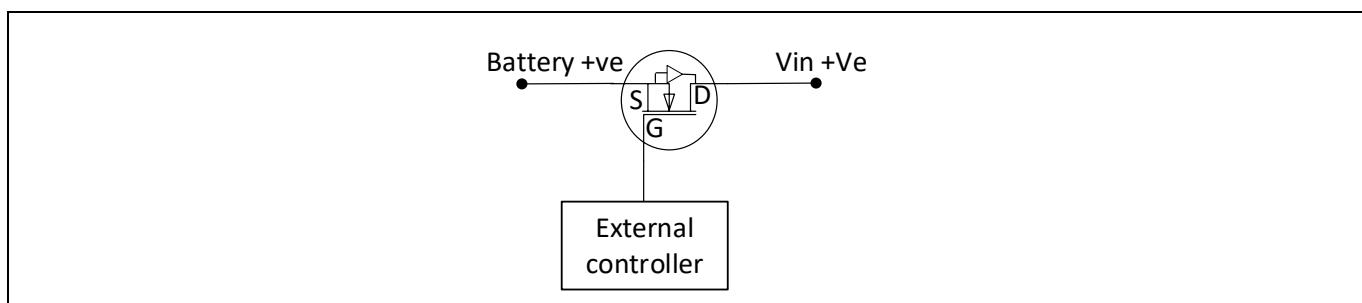


Figure 15 Battery reverse polarity protection circuit

Note: An N-channel MOSFET in the low-side circuit/return path eliminates the need for a charge pump and also introduces a ground shift that is not acceptable for automotive applications.

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Fault protections

7.9 TVS diode selection

The transient voltage suppression (TVS) diode at the input of a system protects the downstream electronic circuits and equipment during a transient overvoltage to immediately conduct and shunt current to ground, keeping the system voltage exposure to a safe, low level. However, during normal operation, the TVS diode has no impact. Choose a diode which has a breakdown voltage (V_{BR}) higher than the normal operating voltage. Ensure that the nominal voltage (V_{IN}) stays below reverse standoff/reverse working maximum voltage, V_{RWM} , rather than breakdown voltage V_{BR} , to assure very low system leakage.

It is recommended to choose discrete single-line transient voltage suppressor (TVS) diodes which has low junction capacitance, low dynamic resistance, and ESD withstanding capacity based on the regulatory / IEC standard to be met.

The International Electrotechnical Commission (IEC) has developed transient immunity standards which have become minimum requirements for original equipment manufacturers. For automotive applications, the typical standard is ISO 10605: Road vehicles – Test methods for electrical disturbances from electrostatic discharge (ESD) [11]. It is recommended to place TVS diodes on the USB Type-C receptacle pins VBUS, CC lines and DP, DM, as shown in [Figure 16](#).

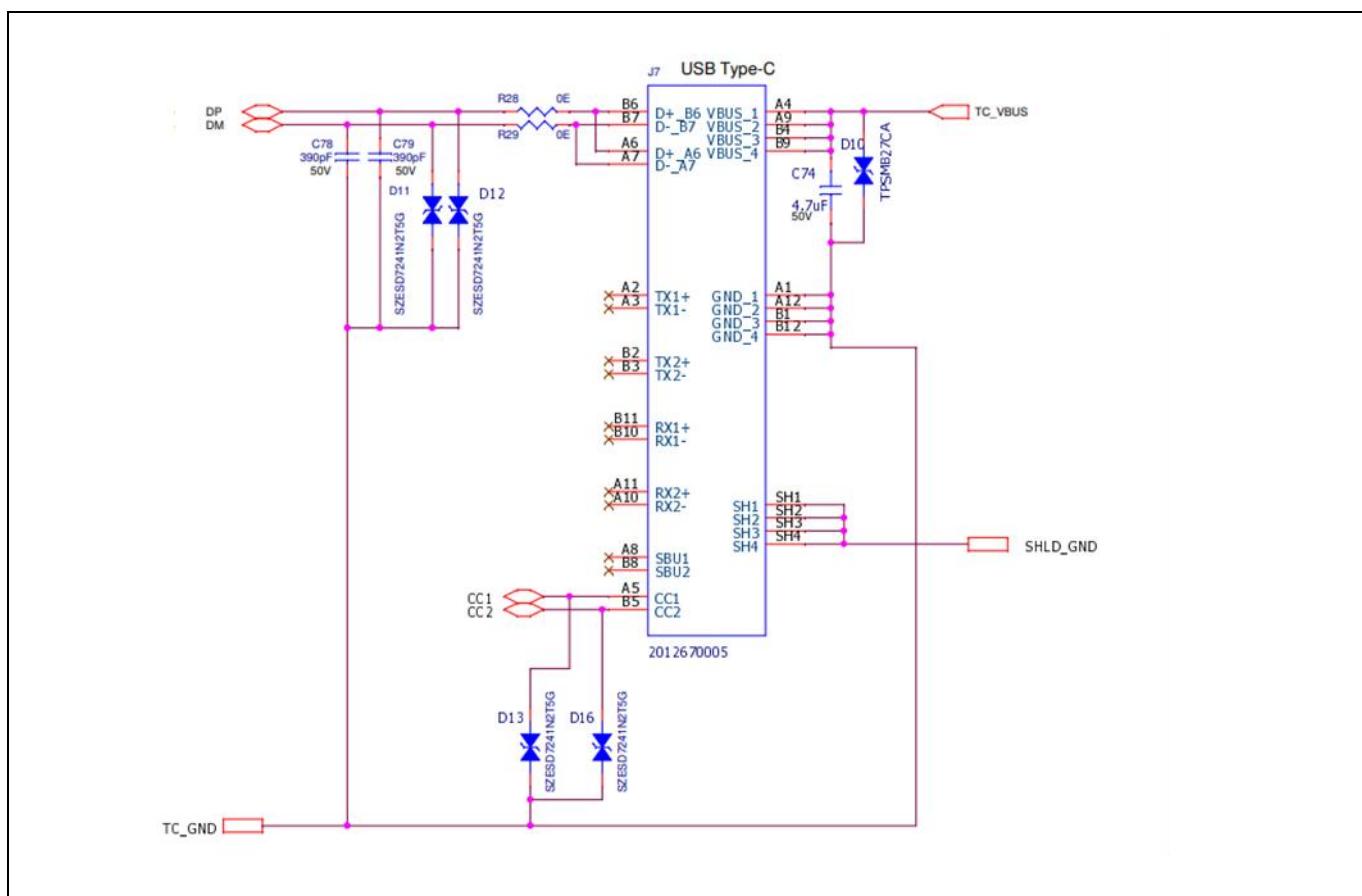


Figure 16 Electrostatic discharge diodes on the USB Type-C connector

7.10 DP and DM lines protection

The USB 2.0 D+ and D- lines are connected to CCG7D to support legacy charging. These lines do not have internal protection against HV faults. Thus, these NFETs are included to provide this function.

Under normal conditions, the voltages on the D+ and D- lines are under 3.3 V. The NFET source and drain are connected to the CCG7D side and the USB Type-C connector side of these lines, respectively. These NFETs are rated for 30 V V_{DS} . These will turn off and protect the CCG7D part if a V_{BAT} or V_{BUS} short to D+ and D- were to occur.

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Fault protections

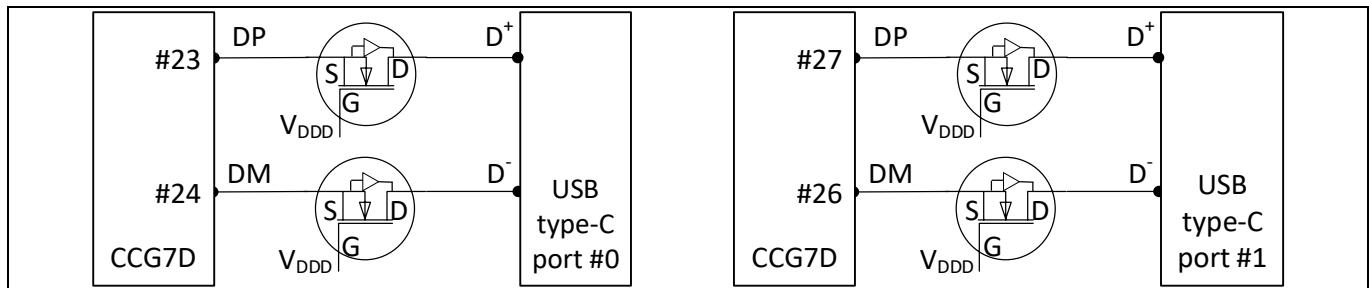


Figure 17 DP and DM lines protection circuit

7.11 External thermistor overtemperature protection

The temperature of power circuit components in the vicinity is measured with an NTC thermistor. In an NTC thermistor the resistance falls as the temperature increases and the voltage drop across the thermistor is measured to protect the circuit by turning off the PWM to the power switching MOSFETs. Temperature thresholds can be adjusted by the choice of a series resistor connected to the NTC thermistor and these characteristics can be obtained from the NTC datasheets. Select an NTC thermistor and resistor (R) value such that the voltage is linear in the desired temperature region.

The port #0 NTC RT1 is terminated to silicon pin #60 and the port #1 NTC RT2 is terminated to silicon pin #59 to sense the temperature of the NTC-placed locations.

The port #0 NTC sensor controls the power throttling based on temperature and the port #1 NTC sensor controls the power throttling based on the operating temperature conditions specified in the EZ-PD™ Configuration Utility [7] (refer to [Section 3.4.2](#)), and if the measured temperature exceeds the operating condition -3, the DUT enters OTP mode.

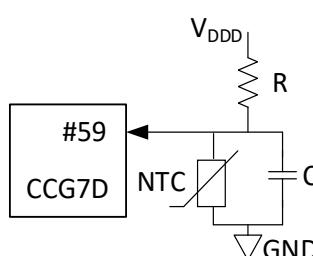


Figure 18 NTC thermistor

Fault protections

7.12 Protection diodes

In a highly noisy environment, you need to ensure that signals are clamped to within the power rails specified in the EZ-PD™ CCG7D automotive datasheet table, “pin-based absolute maximum ratings”. Adding an external clamp diode prevents the device from exceeding operating conditions, which in turn enhances the lifespan and also corrects the functionality. Choose the clamping diode in such a way that its diode drop falls within the absolute maximum ratings. The diode connectivity is shown in [Figure 19](#).

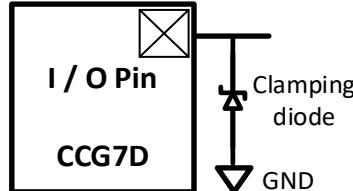


Figure 19 External clamping diodes

8 Hardware configuration for buck only converter

In the buck-only converter configuration, the CCG7D controller's unused pins (boost converter application silicon/controller pins) are to be terminated as recommended:

- SW2 – terminate this silicon/controller pin to power ground/battery negative terminal
- BST2 – terminate this silicon/controller pin to V_{DDD}
- HG2 – floating
- LG2 – floating

9 Application example – four-switch buck boost converter

9.1 Key specifications

- Input voltage range: +5.0 to +18 V DC
- Output voltage range: +3.3 to +21 V DC
- Output current range: 0.0 to 3.0 A

Note: Design calculations are shown separately for buck converter and boost converter. If the power converter is a non-inverting output FSBC, choose the best components from the buck and boost converter calculations.

9.2 Power components selection – buck converter

Buck converter design example calculations made considering the following inputs.

- V_{IN} : 12 V DC, V_{OUT} : 5 V DC, I_{OUT} : 3 A, f_{sw} : 400 kHz; loop bandwidth (f_{C_Buck}): 10 kHz

Table 5 Buck converter power components calculation

Parameter	Formula	Calculated value	Remarks
Input bulk capacitor	$\frac{D_{BUCK} * I_{tran_max}}{2 * \pi * f_{bw_emi_filter} * V_{in_transient}}$	11.05 μF	Considered load transient (I_{tran_max}) 1A EMI filter bandwidth ($f_{bw_emi_filter}$) 10 kHz Allowed input voltage transient ($V_{in_transient}$) 5 percent of V_{IN}
Input MLCC	$\frac{D_{BUCK} (1 - D_{BUCK}) I_{out_max}}{\Delta V_{in_pk-pk} * f_{sw}}$	5.06 μF	Considered 3 percent of V_{IN} as (ΔV_{in_pk-pk}) peak-to-peak ripple
EMI filter inductor [at $V_{IN} = 13.5$ V, $V_{Bus_C} = 12$ V, $I_{OUT} = 3$ A]	$Z_{filter}^2 * C_{filter}$	1.27 μH	$Z_{filter} = (R_{OUT}/D^2)/10$ $C_{filter} = (D*(1-D) * (I_{OUT}))/(f_{sw}*V_{IN_RIPPLE})$ – here V_{IN_RIPPLE} considered as 150 mV $R_{OUT} = V_{OUT}/I_{OUT}$
Power inductor	$\frac{(V_{in_max} - V_0) * D_{BUCK}}{\Delta I_L * f_{sw}}$	8.1 μH	Considered 30 percent of I_{OUT} as inductor ripple (ΔI_L) – I_{tran_max} considered as 1.0 A
Output bulk capacitor	$\frac{I_{tran_max}}{2 * \pi * f_{C_Buck} * V_{out_transient}}$	106 μF	Considered 3 percent transient on output voltage ($V_{out_transient}$)
Output MLCC	$\frac{\Delta I_L}{8 * f_{sw} * \Delta V_{out_pk-pk}}$	5.6 μF	Considered 1 percent of output voltage as output voltage ripple (ΔV_{out_pk-pk}) $\Delta I_L = \frac{(V_{in} - V_{out}) * D_{BUCK}}{L * f_{sw}}$

9.3 Plant transfer function – buck converter

The plant transfer function for the buck converter is:

$$G_{vc}(s) = \frac{kR_0(1 + sR_{cout}C_{out})F_n(s)}{R_i(1 + kR_0C_{out}s)}$$

The above component values are considered for the following frequency analysis.

Table 6 Buck converter plant calculations

Parameter	Formula	Calculated value	Remarks
Plant pole – 1 $f_{p_{plant}}$	$\frac{1}{2\pi R_0 C_{out}}$	1.1 kHz	C_{OUT} is sum of output bulk and MLCCs $R_{OUT} = V_{OUT}/I_{OUT}$
Plant zero $f_{z_{plant}}$	$\frac{1}{2\pi R_{cout}C_{out}}$	92 kHz	Considered ESR as 20 mΩ. The actual ESR value should be noted from the selected output capacitor.
Plant pole – 2 $F_n(s)$	$\frac{1}{1 + \left(\frac{s}{\omega_n}\right)^2 + \frac{s}{\omega_n Q}}$	1256 kHz	$\omega_n = \pi f_{sw}$
Plant DC gain	$k = \frac{k * R_0}{R_i}$ $k = \frac{1}{\left(1 + \frac{T_s R_0}{L} (m_c D' - 0.5)\right)}$	28 dB	$m_c = 1 + \frac{S_e}{S_n}$, where S_e is the external slope added (50 to 100 percent of (V_{OUT}/L)) S_n is the input slope of inductor current (V_{IN}/L) $D' = (1-D)$ $T_s = 1/f_{sw}$
Feedback network gain $G_{div}(s)$	$\frac{R_B}{R_U + R_B}$	0.147 p.u.	$R_B = 34.5 \text{ k}\Omega$ $R_U = 200 \text{ k}\Omega$

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Application example – four-switch buck boost converter

9.4 Compensator transfer function – buck converter

The compensator transfer function is:

$$G_{cv}(s) = \frac{(1 + sR_ZC_Z)}{sC_Z(1 + sR_ZC_P)}$$

Table 7 Buck converter type 2 compensator calculations

Parameter	Formula	Calculated value	Remarks
R _Z	$\frac{2\pi * (R_U + R_B) * R_i * C_{out} * f_{C_Buck}}{R_B * g_{m_cv}}$	1.28 kΩ	R _i = R _s x CSA _{IN} g _{m_cv} = 1.20 millisiemens CSA _{IN} = 9 R _s = 5 mΩ f _{C_Buck} = 10 kHz
C _Z	$\frac{R_O * C_{out}}{R_Z}$	104 nF	
C _P	$\frac{R_{Cout} * C_{out}}{R_Z}$	1.25 nF	Considered ESR as 20 mΩ
Compensator pole f _{PComp}	$\frac{1}{2\pi R_Z C_P}$	99.5 kHz	Locate the pole to cancel the plant zero
Compensator zero f _{ZComp}	$\frac{1}{2\pi R_Z C_Z}$	1.19 kHz	Locate the zero to cancel the plant pole
Compensator DC gain	$20 \log(\frac{g_{m_cv}}{C_Z})$	82 dB	

9.5 Loop transfer functions – buck converter

Table 8 Buck converter loop transfer function calculations

Parameter	Formula	Calculated value	Remarks
Loop gain G _{LTF} (s)	$\frac{R_B}{R_U + R_B} * \frac{g_{m_cv}}{2\pi f_x} * \frac{1}{R_i * C_{out} * R_Z}$	1.09 dB	f _x = f _{C_Buck} ; loop gain will be “1”
Crossover frequency f _{C_Buck}	$\frac{R_B}{R_U + R_B} * \frac{g_{m_cv}}{2\pi} * \frac{1}{R_i * C_{out} * R_Z}$	10.9 kHz	Calculated crossover frequency is close to designed crossover frequency

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Application example – four-switch buck boost converter

Parameter	Formula	Calculated value	Remarks
Loop phase	$90 + \tan^{-1}\left(\frac{f_{C_Buck}}{f_{ZComp}}\right) - \tan^{-1}\left(\frac{f_{C_Buck}}{f_{PPlant}}\right) + \tan^{-1}\left(\frac{f_{C_Buck}}{f_{ZPlant}}\right) - \tan^{-1}\left(\frac{f_{C_Buck}}{f_{PComp}}\right)$	90.04 degrees	

9.6 Power components selection – boost converter

Boost converter design example calculations are made considering the following inputs.

- V_{IN} : 12 V DC, V_{OUT} : 20 V DC, I_{OUT} : 3 A, f_{sw} : 400 kHz; f_{C_Boost} : 10 kHz

Table 9 Boost converter power components calculation

Parameter	Formula	Calculated value	Remarks
Input bulk capacitor	$\frac{I_{tran_max}/(1 - D_{BOOST})}{2 * \pi * f_{bw_emi_filter} * V_{in_transient}}$	44 μF	Considered, load transient (I_{tran_max}) 1A EMI filter bandwidth ($f_{bw_emi_filter}$) 10 kHz Allowed input voltage transient ($V_{in_transient}$) 5 percent of V_{IN}
Input MLCC	$\frac{\Delta I_L}{8 * f_{sw} * \Delta V_{in_pk-pk}}$	5.2 μF	Considered 1 percent of V_{IN} as (ΔV_{in_pk-pk}) peak to peak ripple $\Delta I_L = (0.2 \text{ to } 0.4) * I_{out_max} * \frac{V_{out}}{V_{in_min}}$
Power inductor	$\frac{V_{in_max} * D_{BOOST}}{\Delta I_L * f_{sw}}$	6.0 μH	
Output bulk capacitor	$\frac{I_{tran_max}}{2 * \pi * f_{C_Boost} * V_{out_transient}}$	27.0 μF	Considered 3 percent transient on output voltage. F_{RHP} zero = 47.7 kHz. Make sure f_{C_Boost} is less than (F_{RHP} zero/5)

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Application example – four-switch buck boost converter

Parameter	Formula	Calculated value	Remarks
Output MLCC	$\frac{I_o * D_{BOOST}}{f_{sw} * \Delta V_{out_pk-pk}}$	15.0 μF	Considered 1 percent output voltage ripple

9.7 Plant transfer function – boost converter

$$\text{Plant transfer function } G_{vc}(s) = \frac{\hat{v}_{out}(s)}{\hat{v}_c(s)} = \frac{kR_{out}D' \left(1 - \frac{s}{\left(R_O D' / L \right)} \right) \left(1 + \frac{s}{(1/R_{Cout}C_{out})} \right) F_n(s)}{R_i \left(1 + \frac{s}{(2/R_O C_{out})} \right)}$$

Table 10 Boost converter plant calculations

Parameter	Formula	Calculated value	Remarks
Plant pole – 1 f_{pplant}	$2/(2\pi R_O C_{out})$	1.13 kHz	Total C_{out} is considered
Plant zero f_{zplant}	$1/(2\pi R_{Cout}C_{out})$	192 kHz	Considered ESR as 20 m Ω . The actual ESR value should be noted from the selected output capacitor.
RHP zero ($F_{RHPzero}$)	$R_O(1 - D_{BOOST})^2 / (2\pi L_{boost})$	47.74 kHz	
Plant DC gain	$20\log(\frac{R_o}{R_i} * (1 - D_{BOOST}))$	39 dB	$R_i = R_s * \text{CSA gain} = 5 \text{ m}\Omega * 9 = 45 \text{ m}\Omega$
Plant phase	$Tan^{-1}\left(\frac{f_{cp}}{f_{zplant}}\right) - Tan^{-1}\left(\frac{f_{cp}}{f_{pplant}}\right)$	-61 degrees	Plant crossover frequency (fcp) is $f_{pplant} * 10^{DCgain/20}$
Feedback network gain $G_{div}(s)$	$\frac{R_B}{R_U + R_B}$	0.147 p.u.	$R_B = 34.5 \text{ k}\Omega$ $R_U = 200 \text{ k}\Omega$

9.8 Compensator transfer function – boost converter

$$\text{Type 2 compensator transfer function: } G_{ea}(s) = \frac{(1+sR_ZC_Z)}{sC_Z(1+sR_ZC_P)}$$

Table 11 Boost converter type 2 compensator calculations

Parameter	Formula	Calculated value	Remarks
R_Z	$\frac{\pi * (R_U + R_B) * R_i * C_{out} * f_{C_Boost}}{R_B * g_{m_cv} * (1 - D_{BOOST})}$	560 Ω	$g_{m_cv} = 1.20 \text{ ms}$
C_Z	$\frac{R_O * C_{out}}{2 * R_Z}$	250 nF	
C_P	$\frac{R_{Cout} * C_{out}}{R_Z}$	1.5 nF	

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Application example – four-switch buck boost converter

Parameter	Formula	Calculated value	Remarks
Compensator pole $f_{P\text{Comp}}$	$\frac{1}{2\pi R_Z C_P}$	189 kHz	
Compensator zero $f_{Z\text{Comp}}$	$\frac{1}{2\pi R_Z C_Z}$	1.13 kHz	
Compensator DC gain	$20 \log \left(\frac{g_{m_cv}}{C_Z} \right)$	73.6 dB	

9.9 Loop transfer functions – boost converter

Table 12 Boost converter loop transfer function calculations

Parameter	Formula	Calculated value	Remarks
Loop gain $G_{LTF}(s)$	$\frac{(1 - D_{BOOST})}{R_i} * \frac{R_B}{R_U + R_B} * g_{m_cv} * \frac{1}{\pi f_{\text{Boost}}} * \frac{R_Z}{C_{out}}$	0.510 dB	$F_x = f_{c_Boost}$; loop gain will be “1”
Crossover frequency f_{c_Boost}	$\frac{(1 - D_{BOOST})}{R_i} * \frac{R_B}{R_U + R_B} * g_{m_cv} * \frac{1}{\pi} * \frac{R_Z}{C_{out}}$	5 kHz	
Loop phase	$90 + (\text{ATAN}(2\pi f_c R_Z C_Z) * \frac{180}{\pi}) - (\text{ATAN}(\pi f_c R_O C_{out}) * \frac{180}{\pi})$	89.9 degrees	

10 PCB layout guidelines – best practices

The PCB layout plays an important role in achieving the system's functional, EMC and thermal goals. The following guidelines should help to reduce the design cycle time and cost to achieve the electrical performance and to meet automotive regulatory standards. Acceptable performance can also be obtained with alternate layout schemes.

The following best practices are intended as guidelines.

Note: *The silicon pin numbers referenced in this are w.r.t reference the CCG7D 68-pin QFN package.*

a. PCB layers stack – multilayer board:

A multilayer PCB helps achieve the highest level of signal integrity.

Below is an example of layer stacking for a single-sided component placement PCB design.

- Top layer: Switching power components and power traces
- Second layer: GND plane; it is common practice to almost completely fill with ground; this is the layer immediately below the power components/traces layer
- Third layer: Switching signals and GND plane. Ensure that signals in the third layer do not overlap with signals or power traces in the bottom layer
- Bottom layer: DC and low-frequency signals, GND plane, and DC power traces

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



PCB layout guidelines – best practices

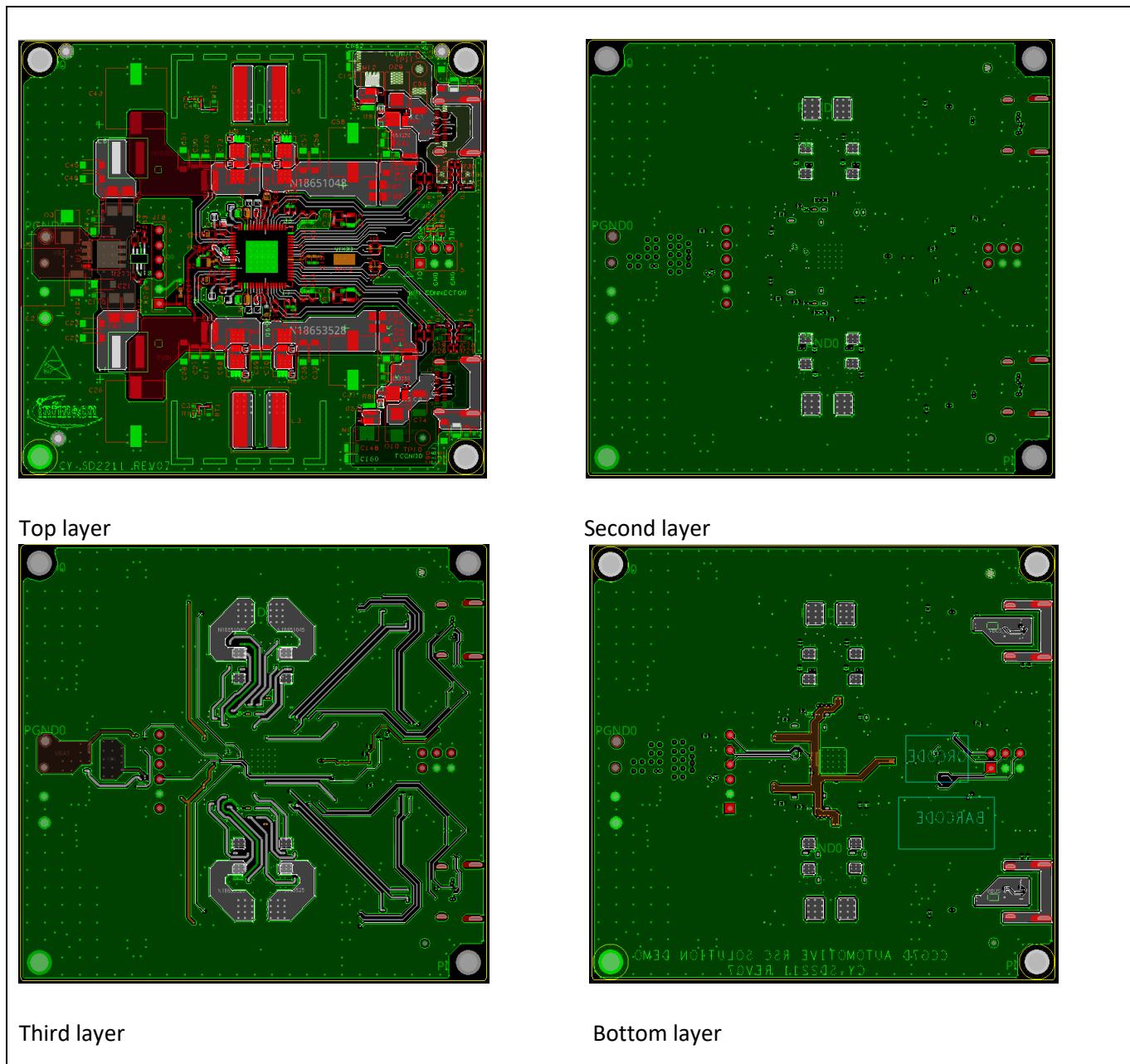


Figure 20 PCB layers – top, second, third, and bottom layers

- b. CCG7D mounting:** Connect the silicon exposed pad (EPAD) to the GND plane and connect this to the battery/board input (V_{IN}) negative terminal via a low-impedance path. The exposed EPAD helps to dissipate the heat into the PCB and, for better transfer of heat, through-hole vias can be made over the EPAD area.

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



PCB layout guidelines – best practices

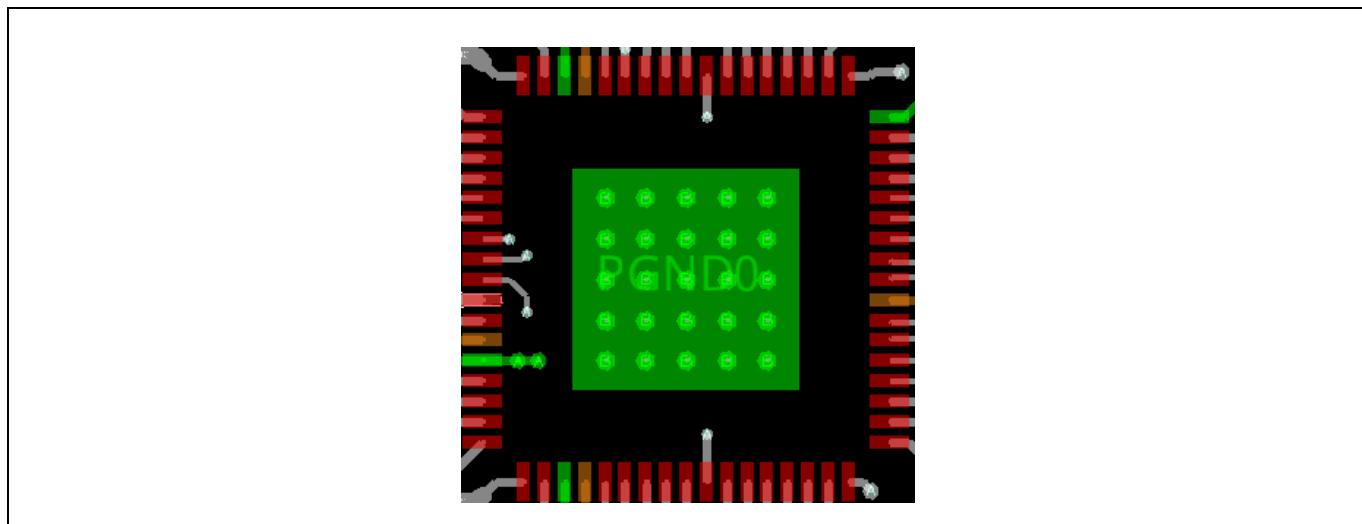


Figure 21 CCG7D EPAD through-hole vias

- c. **SW1 and PGND traces:** Connect the CCG7D SW1 and PGND pins to the drain and source of the power MOSFET (controlled by CCG7D LG1 pin, port #0 pin #2 is LG1_0 and port #1 pin #50 is LG1_1) using dedicated low-impedance traces. SW1 and PGND should be differentially routed with no other switching or noise supply traces next to them. A good option is to provide ground-guarding traces on either side. For port #0, pin #1 is SW1_0, pin #3 is PGND_0, and for port #1, pin #51 is SW1_1 and pin #49 is PGND_1.



Figure 22 SW1 and P_{GND} traces of port #0 and port #1

- d. **SW2 and V_{OUT} traces:** Connect the CCG7D SW2 and V_{OUT} pins to the source and drain of the power MOSFET (controlled by the CCG7D HG2 pin, port #0 pin #8 is HG2_0 and port #44 pin #50 is HG2_1) using dedicated low-impedance traces. SW2 and V_{OUT} should be differentially routed with no other switching or noise supply traces next to them. A good option is to provide ground-guarding traces on either side. For port #0, pin #7 is SW2_0, pin #6 is V_{OUT}_0 and for port #1, pin #45 is SW2_1, pin #46 is V_{OUT}_1.

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



PCB layout guidelines – best practices

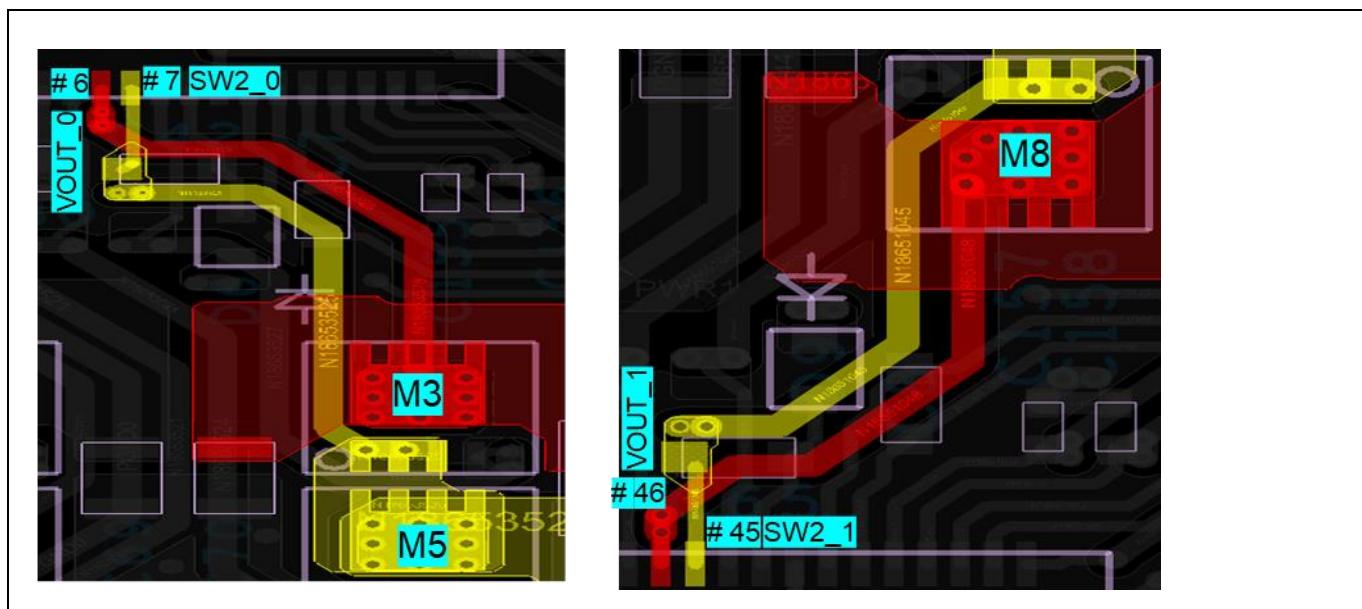


Figure 23 SW2 and V_{OUT} traces of port #0 and port #1

- e. **CSPI and CSNI pin traces:** Connect the port #0 peak input CS resistor (R12) positive terminal to the CCG7D pin #65 CSPI_0 and negative terminal to pin #66 CSNI_0 using a dedicated Kelvin connection. Connect the port #1 peak input CS resistor (R21) positive terminal to the CCG7D pin #55 CSPI_1 and negative terminal to pin #54 CSNI_1 using a dedicated Kelvin connection. CSPI and CSNI should be differentially routed with no other switching or noise supply traces next to them; a good option is to provide ground-guarding traces on either side.

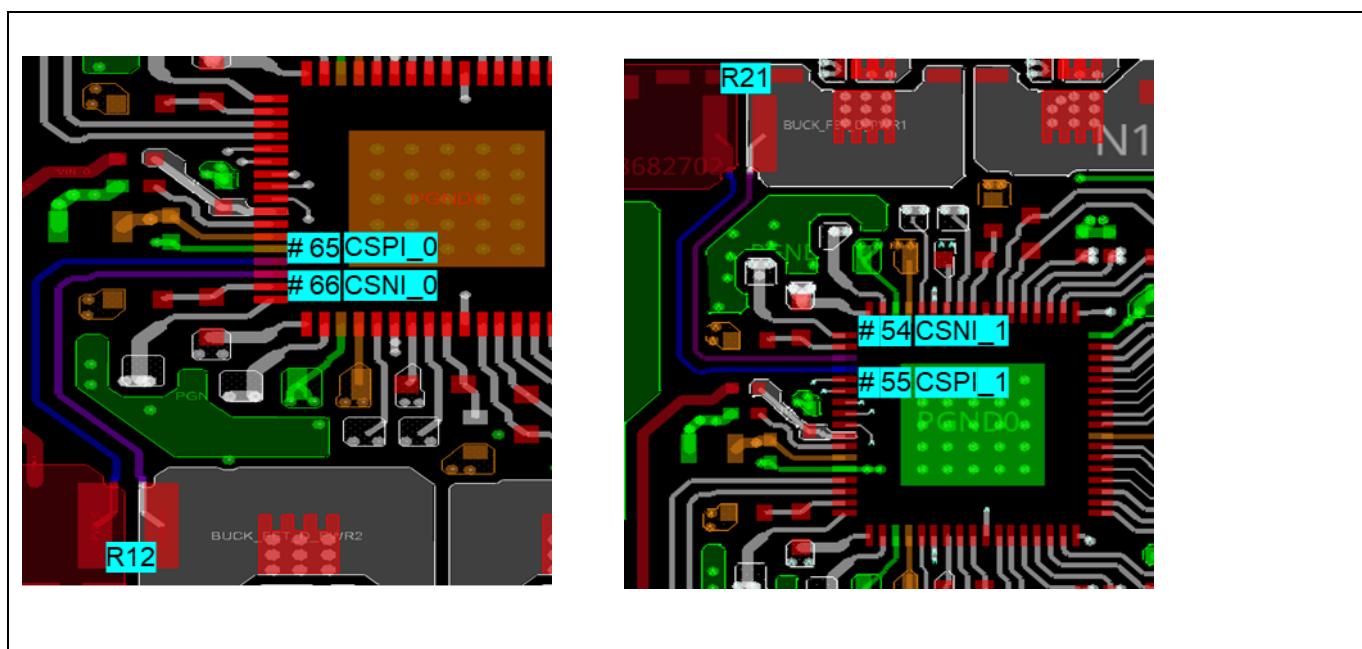


Figure 24 Port #0 and port #1 peak input CS resistor traces connection to the CCG7D

- f. **CSPO and CSNO pin traces:** Connect the port #0 output CS resistor (R13) positive terminal to the CCG7D pin #11 CSPO_0 and negative terminal to pin #12 CSNO_0 using a dedicated Kelvin connection. Connect the port #1 input CS resistor (R22) positive terminal to CCG7D pin #41 CSPO_1 and negative terminal to pin #40

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



PCB layout guidelines – best practices

CSNO_1 using a dedicated Kelvin connection. CSPO and CSNO should be differentially routed with no other switching or noise supply traces next to them. A good option is to provide ground-guarding traces on either side. Provide an option to place a decoupling capacitor between CSPO and CSNO to suppress noise, if any.

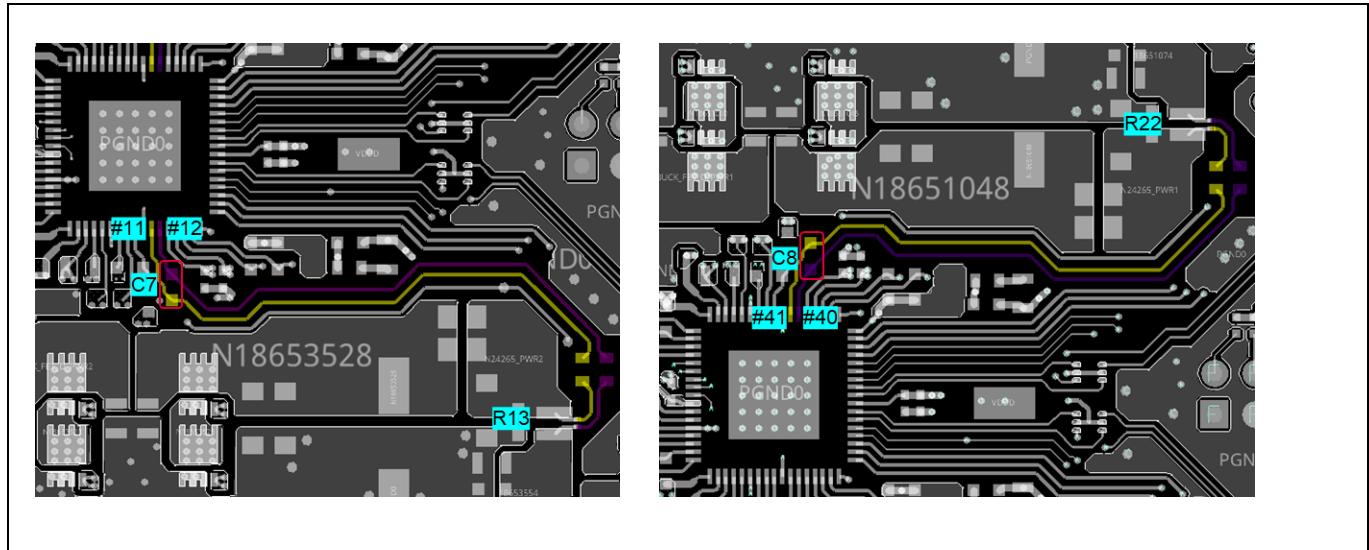


Figure 25 Port #0 and port #1 output CS resistor traces connection to the CCG7D

g. Bootstrap capacitor placement: Both the buck and boost converter bootstrap capacitors should be kept as close as possible to the CCG7D pins. Place the port #0 buck converter circuit bootstrap capacitor C_{Boot} close to pin #1 (SW1_0) and pin #67 (BST1_0), port #0 boost converter circuit bootstrap capacitor C_{Boot} close to pin #7 (SW2_0) and pin #9 (BST2_0). Place the port #1 buck converter circuit bootstrap capacitor C_{Boot} close to pin #51 (SW1_1) and pin #53 (BST1_1), port #1 boost converter circuit bootstrap capacitor C_{Boot} close to the pin #45 (SW2_1) and pin #43 (BST2_1).

Similarly place the port #0 buck converter bootstrap diode D_{Boot} close to pin #67 (BST1_0), port #0 boost converter bootstrap diode D_{Boot} close to pin #53 (BST1_1) and place the port #1 buck converter bootstrap diode D_{Boot} close to pin #9 (BST2_0), port #1 boost converter bootstrap diode D_{Boot} close to pin #43 (BST2_1).

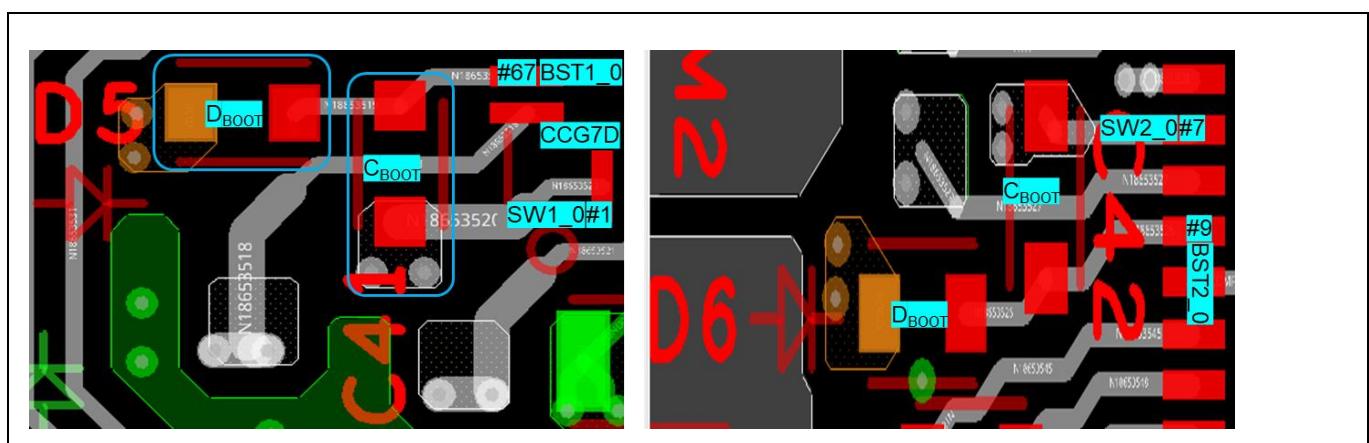


Figure 26 Buck and boost converter bootstrap capacitor and diode placement of port #0

h. Error amplifier traces (COMP): Place the type 2 compensator network components (R_z , C_z , C_p) near the CCG7D COMP pin and the silicon ground. Ensure that traces do not pass through noisy areas, such as switch nodes. Port #0 and port #1 error amplifier output pin #10 is connected to the type 2 compensator network

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PCB layout guidelines – best practices

R7, C11 and C10, and port #1 error amplifier output pin #42 is connected to the type 2 compensator network R8, C12 and C9.

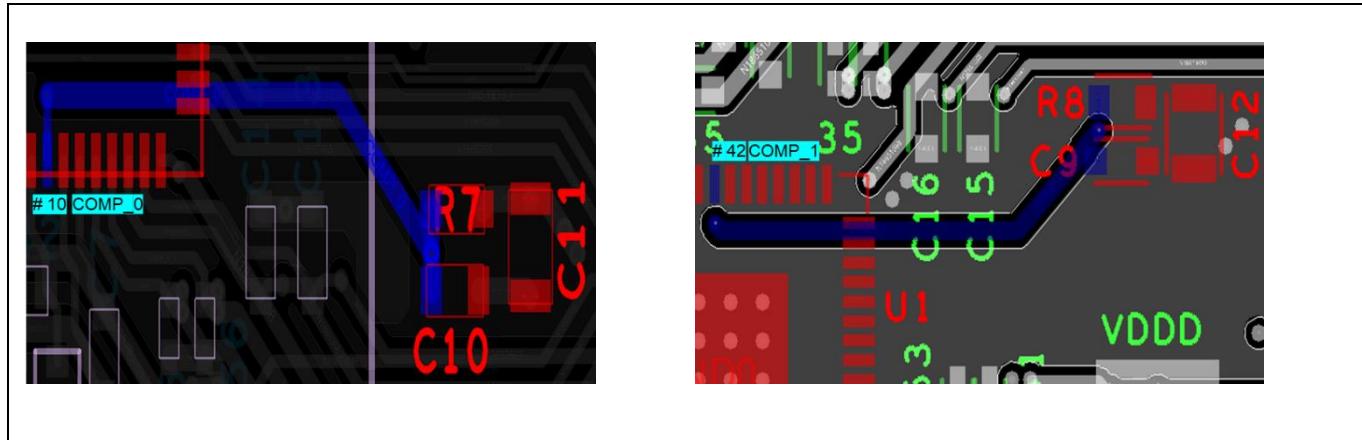


Figure 27 Error amplifier traces (COMP) port #0 and port #1

- i. **Bypass or decoupling capacitors to ground plane:** Bypass or decoupling capacitors to the ground plane can reduce the return current path, which reduces the size of the loop and hence radiation. Make sure not to connect a bypass capacitor between a power plane and an unrelated ground plane, which can cause capacitive coupling. The capacitor value is selected based on the impedance vs. frequency graph. The bypass capacitor should be placed as close as possible to the silicon pins and silicon ground via the low-impedance path.

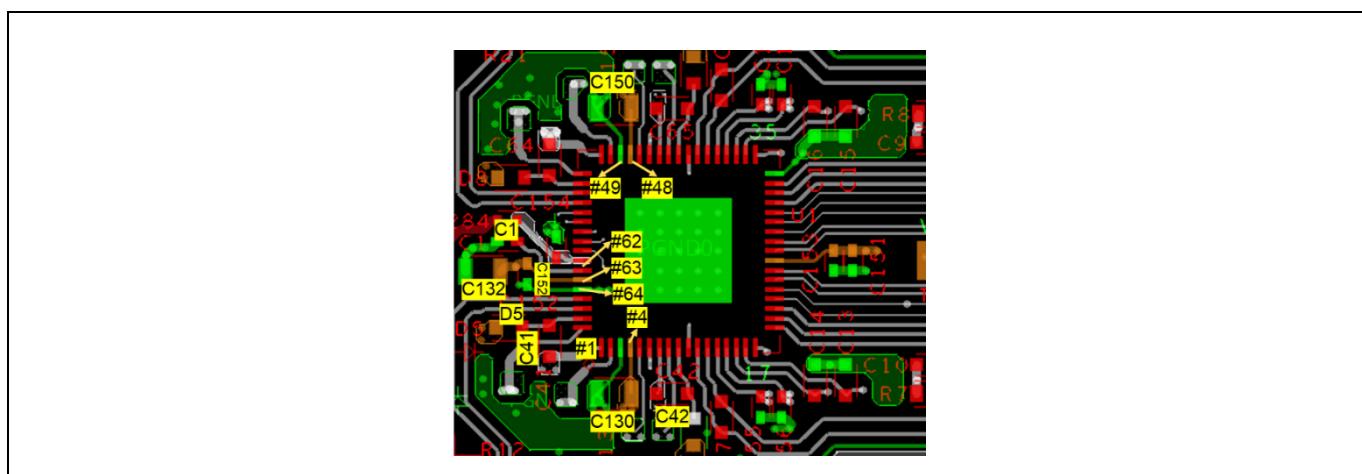


Figure 28 MLCC placement

- j. **MOSFET gate drive traces:** The FSBBC gate drive loops must be as small as possible to improve the switch turn-on/-off performance and to reduce EMI. The gate drive trace length should be short with wide trace to minimize the gate path impedance. Ensure that there is a solid ground plane in the layer adjacent to any layer with the gate drive signals.

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PCB layout guidelines – best practices



Figure 29 Gate drive traces port #0 and port #1

- k. **Shorter return paths:** Keep return current paths as short as possible and route them along paths of least resistance. Return paths should be about the same length as transmit traces or shorter.

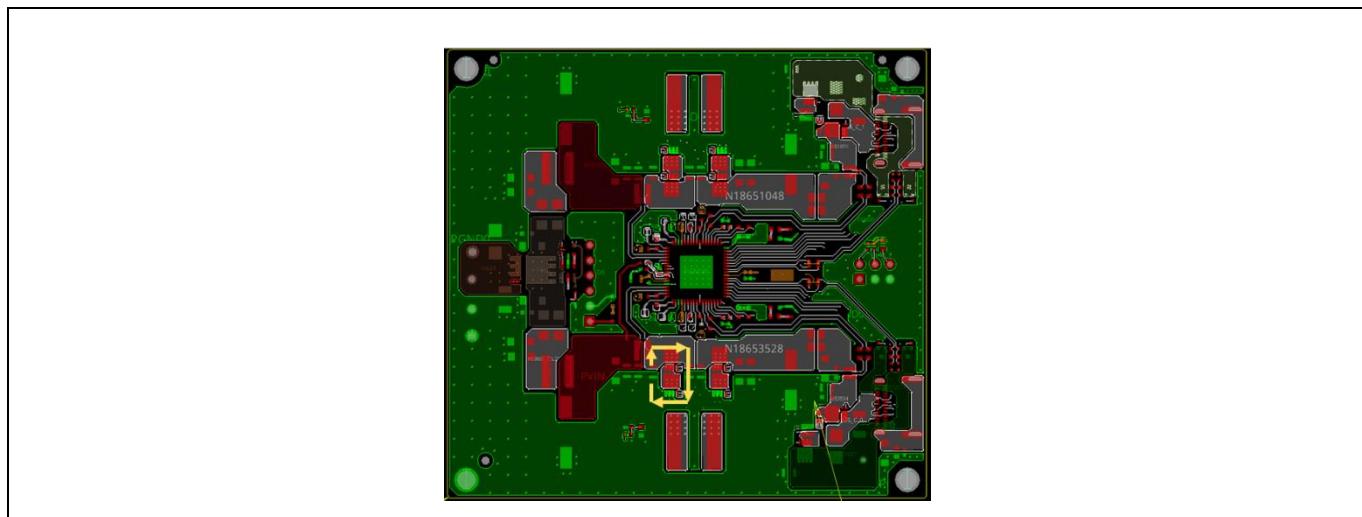


Figure 30 Shorter return paths

- l. **High-frequency capacitors:** The high (di/dt) pulsating currents radiate magnetic fields, and generate high-voltage ringing and spikes across MOSFETs, and PCB traces. The high-frequency decoupling capacitors (C_{HF}) should be placed as close as possible to the half-bridge MOSFETs to mitigate artifacts of high di/dt .

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PCB layout guidelines – best practices

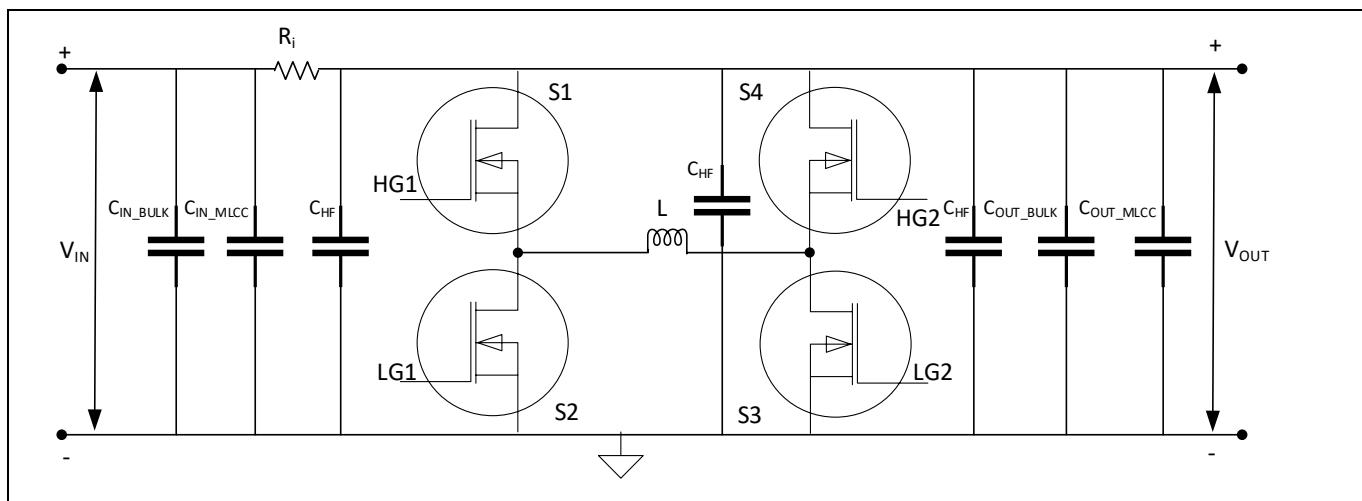


Figure 31 High-frequency capacitors (C_{HF}) in the circuit schematics

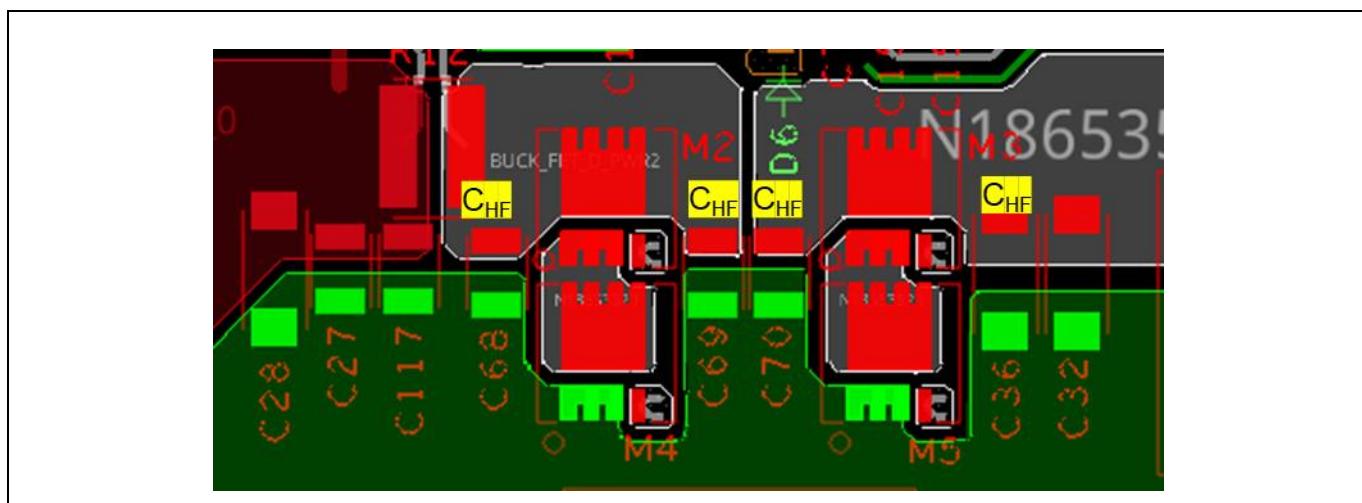


Figure 32 High-frequency capacitors (C_{HF}) placement on the PCB layout

m. Minimize switch node area: In buck mode, the high dV/dT switch node voltage SW1 swings between V_{IN} and GND and in boost mode the high dV/dT switch node voltage SW2 swings between V_{OUT} and GND, and this causes high-frequency switching noise, which is a strong source of EMI noise. The switch node copper area should be minimal to have the least coupling capacitance between the switch node and other noise-sensitive traces. However, to have an allowable temperature rise of power MOSFETs, provide a solid copper area in the immediate PCB layer.

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PCB layout guidelines – best practices

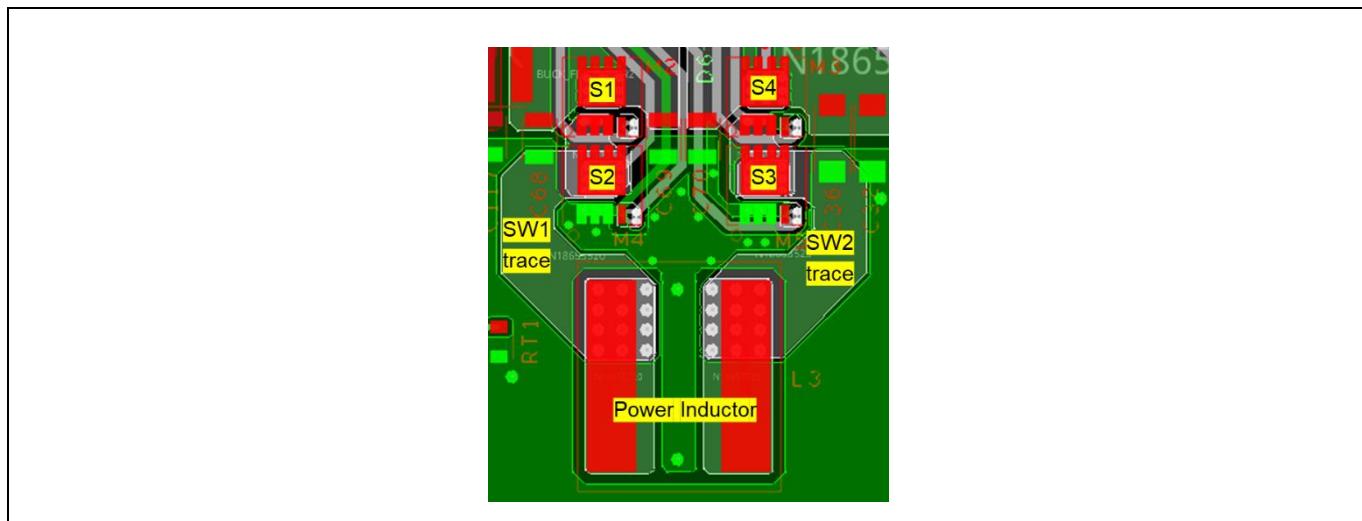


Figure 33 Switch node traces

- n. **EMI shield:** Shield the noise-producing components/circuits with a Faraday cage; that is, an enclosure made of conductive materials with sufficient thickness to block RF waves. Ensure that the EMI filter components are outside the EMI shield.

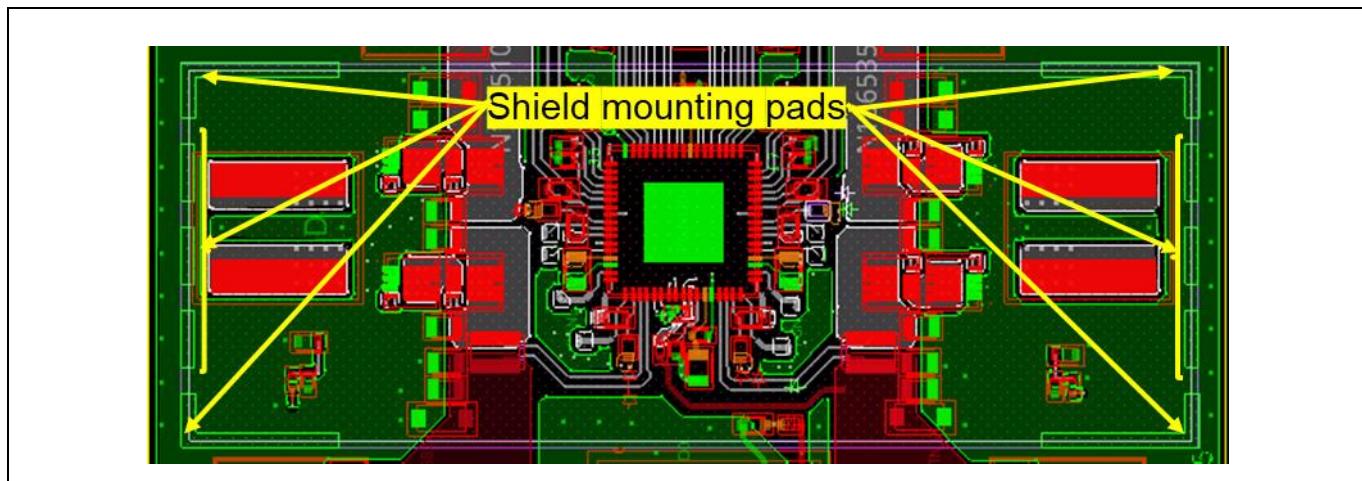


Figure 34 EMI shield mounting pads

- o. **Unused area:** In all layers, fill unused areas with copper to reduce the temperature of power components. Connect the copper areas to either V_{IN} , V_{BUS_C} or GND (preferably to GND).
- p. **Ground connection:** When routing the circuitry around the IC, the analog small-signal ground and the power ground (used for the compensation networks) for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum. This helps keep the analog ground quiet.
- q. **Ground plane:** Larger solid ground planes provide lower impedance, and signals can disperse more easily with more area, reducing emissions, cross-talk and noise. Ensure there is a good reason to use a split ground plane and ensure that they are only connected at a single point (some of the applications may demand separate analog and digital grounds to avoid noise coupling). Multiple ground connections in a split-ground PCB can create loops, resulting in an antenna that radiates EMI. The ground plane layer should be as close as possible to the layer with power MOSFETs.

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PCB layout guidelines – best practices

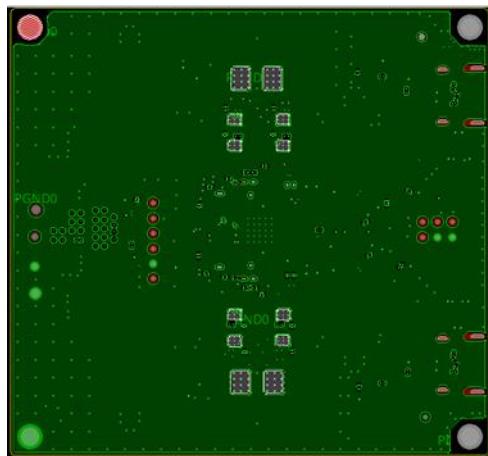


Figure 35 PCB layer 2

- r. **Ground vias:** Place several ground-connecting vias close to the component grounds directly to the dedicated ground plane. Do not keep the ground plane isolated. Stitch it to internal layers with vias for better EMI/EMC. A few are marked in [Figure 36](#).

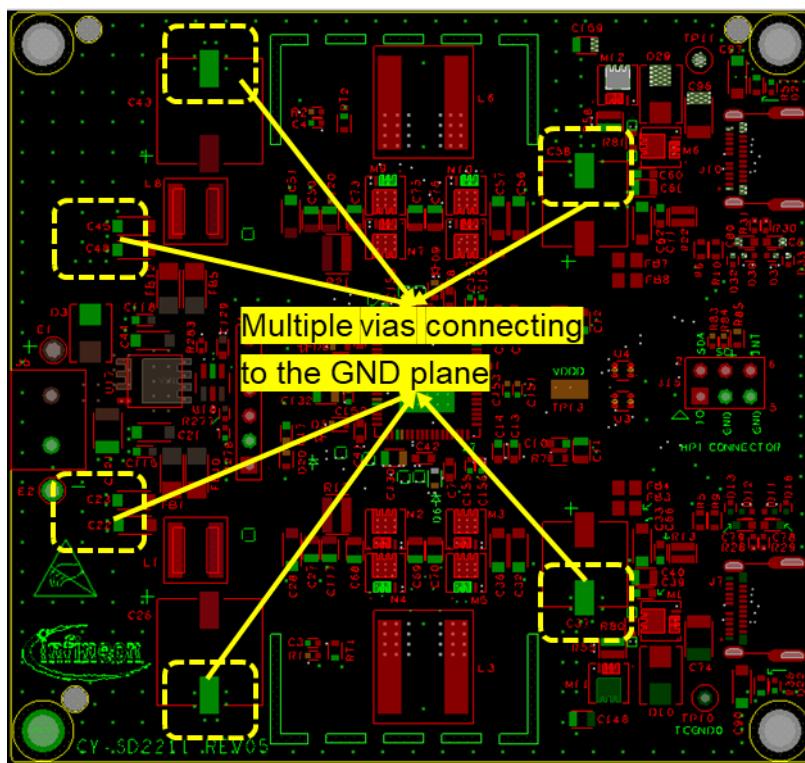


Figure 36 Multiple vias connecting to the GND plane

- s. **Avoid sharp right-angle bends:** Sharp right-angle bends cause changes in the characteristic impedance and reflections. This can be mitigated by rounding right angle bends to help reduce the radiated EMI.

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



PCB layout guidelines – best practices

- t. **High dV/dT signals:** Keep the high dV/dT nodes such as SW1, SW2, BST1, BST2, HG1 and HG2 away from sensitive small-signal nodes.
- u. **Separate high- and low-speed signals:** Keep high-speed signals such as PWM separate from low-speed signals such as compensation networks, and analog signals separate from digital signals.
- v. **Control signals trace width:** To minimize the trace impedance control signal traces should be at least 10 to 20 mil wide.
- w. **High current-carrying power-path traces:** High current-carrying power-path traces should be as short as possible and should be sized to carry twice the rated current.
- x. **ESD immunity:** To improve ESD immunity, connect MLCCs close to the USB type-C connector GND and V_{bus} terminals through the low-impedance paths.
- y. **CC lines:** Keep trace lengths to a minimum from the type-C receptacle to the CC lines and the external ESD diodes.

Thermal considerations

11 Thermal considerations

In automotive applications, the USB Type-C PD solutions are concealed within the auto body without air cooling, and without external heatsink. Typically, components such as power MOSFETs and inductors are surface mounted; hence placement of power components and trace width, and size of copper area are critical to limit thermal stress.

The power components should be placed in such a way that minimizes the length of the high-current flow paths through power MOSFETs, inductors, CS resistors, and input and output capacitors, which results in lower conduction losses. Low impedance traces and solid low impedance power component land patterns minimize the thermal stress.

In a dual-output USB Type-C PD, make sure to have a symmetrical layout for each port to avoid hotspots.

Refer to [PCB layout guidelines – best practices](#) for details of best practices to follow.

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Circuit schematic and PCB layout review checklist

12 Circuit schematic and PCB layout review checklist

Table 13 is a checklist for the key circuit schematic component choices and **Table 14** is a checklist for the PCB layout guidelines. Please provide an answer for each checklist item to find out the extent to which your hardware design meets these guidelines.

Table 13 Circuit schematic checklist

No.	Checklist item	Answer (Yes/No/NA)
1	Are the components chosen for the automotive application solution compliant with the AEC-Q standards?	
2	Are the current measurement resistors chosen with a minimum of 5 mΩ resistance value and is tolerance better than 1 percent?	
3	Is the bypass capacitor connected between V _{BUS_IN} and GND 0.1 μF at maximum operating output voltage?	
4	Is the bypass capacitor connected between P _{VDD} and P _{GND} 1.0 μF at an operating voltage of 5.0 V?	
5	Is the capacitor connected at V _{CCD} 0.1 μF at an operating voltage of 1.8 V?	
6	Is the bootstrap capacitor connected at the buck side SW node and BST 0.1 μF at the maximum input voltage?	
7	Is the bootstrap capacitor connected at the boost side SW node and BST 0.1 μF at the maximum output voltage?	
8	Confirm that the chosen bootstrap diode forward voltage is small to ensure lower conduction losses?	
9	Confirm that the chosen bootstrap diode reverse recovery time is very small, to achieve a reduction in reverse recovery losses?	
10	Confirm that a 1.0 μF capacitor is connected in parallel with 0.1 μF connected at V _{DDD} pin #25 and this capacitor offers the specified capacitance at the operating voltage of 5.0 V?	
11	Confirm that a 10.0 μF capacitor is connected in parallel with 0.1 μF connected at V _{DDD} pin #63 and this capacitor offers the specified capacitance at the operating voltage of 5.0 V?	
12	Confirm that a 0.1 μF ceramic bypass capacitor is connected at V _{IN} pin #61 and the capacitor offers the specified capacitance at the maximum operating input voltage?	
13	Confirm that a 0.1 μF ceramic bypass capacitor is connected at V _{BUS_IN} pin #13 to ground, pin #39 to ground and the capacitor offers the specified capacitance at the maximum operating output voltage?	
14	Confirm that a 0.1 μF ceramic bypass capacitor is connected at V _{BUS_C} pin #14 to ground, pin #38 to ground and the capacitor offers the specified capacitance at the maximum operating output voltage?	
15	Confirm that provision is given for a ceramic capacitor between the silicon pins CSPO and CSNO?	
16	Is the 390 pF capacitor terminated between CC1, CC2 and ground, respectively?	
17	Confirm that the chosen bulk capacitors can carry the computed ripple current?	

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Circuit schematic and PCB layout review checklist

18	Confirm that the calculated maximum temperature of the bulk capacitors is within the temperature range offered by the chosen capacitor?	
19	Confirm that the chosen bulk capacitor's ESR can result in lower than the specification ripple limits?	
20	Do the chosen type 2 compensator resistor and capacitors have lower tolerance across the operating conditions?	
21	Confirm that the chosen buck-boost switches are of N-channel logic-level MOSFETs?	
22	Ensure that the chosen N-channel buck-boost MOSFET gate threshold voltage is much lower than 5.0 V?	
23	Confirm that the chosen MOSFETs are N-channel?	
24	Ensure that the chosen N-channel MOSFETs' maximum gate source voltage is more than DUT rated output voltage?	
25	Ensure that the selected input TVS diode's reverse working maximum voltage (V_{RWM}) is higher than maximum operating voltage?	
26	Ensure that the TVS diode breakdown voltage (V_{BR}) is significantly lower than the maximum allowable voltage rating of the silicon, specified in the silicon datasheet table "Electrical Specifications: Absolute Maximum Ratings and Pin Based Absolute Maximum Ratings" at V_{IN} , V_{BUS_C} , DP, DM, CC1, and CC2?	
27	Ensure that reverse current of the TVS diode (I_R) is low in nominal operating voltage?	
28	Confirm that the chosen inductors are magnetically shielded to minimize EMI?	
29	Confirm that the chosen inductor has lower DCR value to ensure better efficiency?	
30	Is the chosen inductor's inductance variation less than 20 percent?	
31	Is the chosen inductor's saturation current much higher than the inductor peak operating current (minimum 2 times)?	
32	Are the selected power inductor SRFs much higher (at least 10 times) than operating switching frequency?	
33	Is the selected NTC thermistor's operating range between -40°C and 125°C and lower than the maximum operating conditions of the DUT?	
34	Is the resistor connected in series with the NTC chip thermistor, and does nominal resistance value meet the maximum operating temperature specifications?	
35	Is a capacitor connected across the (~1000 pF) NTC thermistor to roll off high-frequency noises?	
36	Is there a provision to assemble 10 to 20 μ F capacitors across the V_{BAT} -to-GND protection MOSFET and its sense resistor? Note: this provision is not required where a V_{BAT} -to-GND protection circuit is not used.	

Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Circuit schematic and PCB layout review checklist

Table 14 PCB layout guidelines checklist

No.	Checklist item	Answer (Yes/No/NA)
1	Is the CCG7D exposed pad (EPAD) connected to ground using vias?	
2	Are the CCG7D SW1 and PGND pins routed differentially to the respective silicon pins with dedicated low-impedance trace?	
3	Are the CCG7D SW1 and PGND traces provided with ground guarding on either side?	
4	Are the CCG7D SW2 and V _{OUT} pins routed differentially to the respective silicon pins with dedicated low-impedance trace?	
5	Are the CCG7D SW2 and V _{OUT} traces provided with ground guarding on either side?	
6	Are the CCG7D CSPI and CSNI pins connected to the input CS resistor using dedicated Kelvin connections and with the shortest trace length?	
7	Are the CCG7D CSPI and CSNI pins routed differentially with no other switching or noisy trace next to them?	
8	Are the CCG7D CSPI and CSNI traces provided with ground guarding on either side?	
9	Are the CCG7D CSPO and CSNO pins connected to the output CS resistor using dedicated Kelvin connections and with the shortest trace length?	
10	Are the CCG7D CSPO and CSNO pins routed differentially with no other switching or noisy trace next to them?	
11	Are the CCG7D CSPO and CSNO traces provided with ground guarding on either side?	
12	Are bootstrap capacitors and diodes placed close to the CCG7D pins?	
13	Are compensator network elements (R _Z , C _Z , C _P) placed near the CCG7D COMP pin and the silicon ground? Is it ensured that corresponding traces avoid noisy nodes and traces?	
14	Are the decoupling capacitors placed closed to the silicon pin and silicon ground with minimum trace length?	
15	Is it ensured that the MOSFET gate driver traces are short and wide?	
16	Is it ensured that the solid ground plane is placed in layers adjacent to MOSFET gate driver signal traces?	
17	Is it ensured that the return current path is as short as possible?	
18	Are the high-frequency capacitors placed as close as possible to the half-bridges to ensure that high di/dt current loop area is reduced significantly?	
19	Is it ensured that the SW node area is optimized?	
20	Is it ensured that any unused area is filled with copper and connected to GND?	
21	Are analog small-signal ground and power ground kept separated and connected at a point where switching activities are less?	
22	Is it ensured that a large solid ground plane is provided without any unnecessary split?	
23	Is it ensured that sufficient ground vias are placed near to the component ground to the dedicated ground layer?	
24	Is it ensured that sharp right-angle bends are avoided?	
25	Is it ensured that high dV/dT nodes are kept away from sensitive small-signal nodes?	
26	Is it ensured that high-frequency and low-frequency signal traces are kept separate?	

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Hardware design guidelines for EZ-PD™ CCG7D in automotive applications



Revision history

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**	2021-06-08	Initial release
V 1.1	2023-02-10	Added section 7.12 and chapter 8; minor edits to the document

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