High-Speed Differential Pair Routing Guidelines

Interface	Type	Signal Names	Pair Matching Tolerance	Inter-Pair Matching Tolerance	Additional Notes
USB 2.0	Differential	DP_N, DP_P	±150 mil	Not required	Keep traces short, avoid vias
USB 3.0	Differential	SSRX_N, SSRX_P / SSTX_N, SSTX_P	±2 mil	±5 mil	Avoid stubs, tightly controlled impedance
USB 3.1/3.2	Differential	SSRX_N, SSRX_P / SSTX_N, SSTX_P	±2 mil	±5 mil	Minimize vias, length matching critical
USB4 / Thunderbolt 3	Differential	HSRX_N, HSRX_P / HSTX_N, HSTX_P	±1 mil	±3 mil	Use well-matched controlled impedance stackup
Ethernet 100BASE-TX	Differential	TD_N, TD_P / RD_N, RD_P	±50 mil	±100 mil	Terminate properly, avoid large trace gaps
Ethernet 1000BASE-T	Differential	TX1_N, TX1_P / TX2_N, TX2_P / TX3_N, TX3_P / TX4_N, TX4_P	±5 mil	±10 mil	All pairs must be matched for delay skew
Ethernet 10GBASE-T	Differential	TXA_N, TXA_P / TXB_N, TXB_P / TXC_N, TXC_P / TXD_N, TXD_P	±2 mil	±5 mil	Use high-quality PCB material
HDMI 1.4	Differential	TMDS0_N, TMDS0_P / TMDS1_N, TMDS1_P / TMDS2_N, TMDS2_P / TMDS_CK_N, TMDS_CK_P	±5 mil	±20 mil	Keep CLK pair shorter than data pairs
HDMI 2.0	Differential	TMDS0_N, TMDS0_P / TMDS1_N, TMDS1_P / TMDS2_N, TMDS2_P /	±2 mil	±10 mil	All lanes must be length-matched

		TMDS_CK_N, TMDS_CK_P			
DisplayPort 1.2	Differential	ML0_N, ML0_P / ML1_N, ML1_P / AUX_N, AUX_P	±3 mil	±10 mil	Minimize skew between lanes
DisplayPort 2.0	Differential	ML0_N, ML0_P / ML1_N, ML1_P / AUX_N, AUX_P	±2 mil	±5 mil	Very strict inter-pair matching
PCIe Gen1/2	Differential	PCIE_RX_N, PCIE_RX_P / PCIE_TX_N, PCIE_TX_P	±5 mil	±20 mil	Avoid impedance discontinuities
PCIe Gen3	Differential	PCIE_RX_N, PCIE_RX_P / PCIE_TX_N, PCIE_TX_P	±2 mil	±10 mil	Tighter matching than Gen1/2
PCIe Gen4	Differential	PCIE_RX_N, PCIE_RX_P / PCIE_TX_N, PCIE_TX_P	±1 mil	±5 mil	Low-loss PCB materials recommended
PCIe Gen5	Differential	PCIE_RX_N, PCIE_RX_P / PCIE_TX_N, PCIE_TX_P	±0.5 mil	±2 mil	Extremely tight tolerance, use high-speed stackup
SATA 3.0	Differential	SATA_TX_N, SATA_TX_P / SATA_RX_N, SATA_RX_P	±5 mil	±20 mil	Shortest possible path, avoid vias
SAS 12G	Differential	SAS_TX_N, SAS_TX_P / SAS_RX_N, SAS_RX_P	±2 mil	±5 mil	Keep differential impedance strict
MIPI DSI/CSI	Differential	DSID0_N, DSID0_P / DSID1_N, DSID1_P / DSID2_N, DSID2_P / DSID3_N, DSID3_P / DSIC_N, DSIC_P	±2 mil	±10 mil	Use matched trace routing for high-speed
LVDS	Differential	LVDS0_N, LVDS0_P / LVDS1_N, LVDS1_P	±5 mil	±20 mil	Terminate correctly at receiver

General Routing Guidelines:

1. **Use an impedance calculator** (based on your stackup) to determine trace width & spacing.
2. **Keep differential pairs tightly coupled** (avoid large gaps between P/N).
3. **Minimize vias**—every via adds impedance discontinuity.
4. **Match each pair within tolerance** to ensure proper signal integrity.
5. **Inter-pair matching is critical** for multi-lane interfaces (Ethernet, HDMI, PCIe, DP).
6. **Avoid stubs**—use direct traces whenever possible.