Single-layer MoS_2 Transistor

Dwaipayan Paul
Roll no:- 1811064
School of Physical Sciences
National Institute of Science Education and Research

I. Introduction and fabrication

Due to their relative ease of fabrication, two-dimensional materials are appealing for application in next-generation nanoelectronic devices. Begining with the discussions of 2D nanomaterials, we need to talk about graphene. Graphene nanoribbons were one of the first and most studied 2D material. Graphene has unusually high mobility (Hall effect mobility in suspended graphene can exceed $2 \times 10^5\ cm^2V^1s^{-1}$ at low temperature). It also offers rich physics owing to its unique electronic structure. However, the bandgap, which is necessary for many applications including transistors, in pristine graphene is absent. Creating a graphene bandgap introduces other difficulties like lowering of mobilities(200 $cm^2V^{-1}s^{-1}$ for a 150 meV bandgap) to those of strained silicon sheets, or necessitates high voltages (creating a bandgap of 250 meV requires 100V or more).
MoS_2 was the step towards graphene analogue materials. This type of materials are classified as metal dichalcogenides. They have advantages like wide direct band gap, good transport properties and flexible. People are interested in single layer MoS_2 more because of its direct band gap of 1.89 eV, whereas the bulk has indirect bandgap of 1.2 eV. MoS2 monolayer transistors generally display n-type behaviour, with carrier mobilities (approximately 350cm$^2V^{-1}$S^{-1}). It does not show dangling bond and its thermal stability is up to 1000 C.
As for the fabrication, MoS_2 monolayers are made by micro-mechanically exfoliating MoS_2 using scotch tape. These monolayers are then transferred to a degenerately doped Si substrate with 270 nm thick SiO_2 layer. The electrodes are made using electron beam lithography with deposition of 50 nm thick gold electrodes. The device is then annealed at 200 C to remove resist residue and decrease contact resistance. To boost its room temperture mobility, dielectric HfO_2 (30nm, deposited using Atomic Layer Deposition) is used due to its high dielectric constant.

II. Characteristics and applications

The characterization of this device is performed with a semiconductor parameter analyzer and probe station. The sample had a channel thickness of 6.5 nm, a channel length of 1.5 μm, and channel width of 4 μm. First, we do bottom gate characterization by setting $V_{tg} = 0$. With the dielectric constant of SiO_2 as 3.9, we calculated specific capacitance $1.3 \times 10^{-4} Fm^{-2}$ and mobility from the bottom gate as 217 $cm^2V^{-1}s^{-1}$. Similarly, top-gate characterization was performed with $V_{bg} = 0$. Due to the dielectric, we get specific conductance as $7.4 \times 10^{-3} Fm^{-2}$ and mobility of 406 $cm^2V^{-1}s^{-1}$ at $V_{ds} = 500mV$. In both of the characterizations, we find linear V_{ds} vs I_{ds} plots suggesting Ohmic behavior of metal contacts. We can also observe typical V_{gs} vs I_{ds} curves in both of the cases. Moreover, it was found that through the bottom gate we achieve $I_{on}/I_{off} = 10^6$ where through the top gate it is 10^8. In top gate characterization, the subthreshold swing is found to be $72mVdec^{-1}$, which makes it usable for interband tunnel FETs. We can attribute the difference between the two types of gate characterization to the suppression of coulomb scattering and modification of phonon dispersion relation due to high k-dielectric. The values of mobility make it comparable to graphene nanoribbons and strained Si films, but with a higher bandgap.
Some of its future applications could be: precise control over phase, layer numbers, domain size, morphology and twist angle, large area (wafer-scale)growth , site-specific design , in-situ characterization and carrier doping , high reproducibility and low-temperature growth.