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PRACTICAL – 7

AIM: To study and design bus system for four register using multiplexer.

THEORY:

A typical digital computer has many registers, and paths must be provided to transfer in formation form one register to another. The number of wires will be excessive if separate lines are used between each register and all other registers in the system. A more efficient scheme for transferring information between registers in a multiple-register configuration is a common bus system. A bus structure consists of a set of common lines, one for each bit of a register, through which binary information is transferred one at a time. Control signals determine which register is selected by the bus during each particular register transfer.

One way of constructing a common bus system is with multiplexers. The multiplexers select the source register whose binary information is then placed on the bus. The construction of a bus system for four registers is shown is Fig. Each register has four bits, numbered 0 through 3. The bus consists of four 4×1 multiplexers each having four data inputs, 0 through 3, and two selection inputs, S_1 and S_0. In order not to complicate the diagram with 16 lines crossing each other, we use labels to show the connections from the outputs of the registers to the inputs of the multiplexers. For example, output 1 of register A is connected to input 0 of MUX 1 because this input is labeled A_1. The diagram shows that the bits in the same significant position in each register are connected to the data inputs of one multiplexer to form one line of the bus. Thus MUX 0 multiplexes the four 0 bits of the registers, MUX 1

multiplexes the four 1 bits of the registers, and similarly for the other two bits.
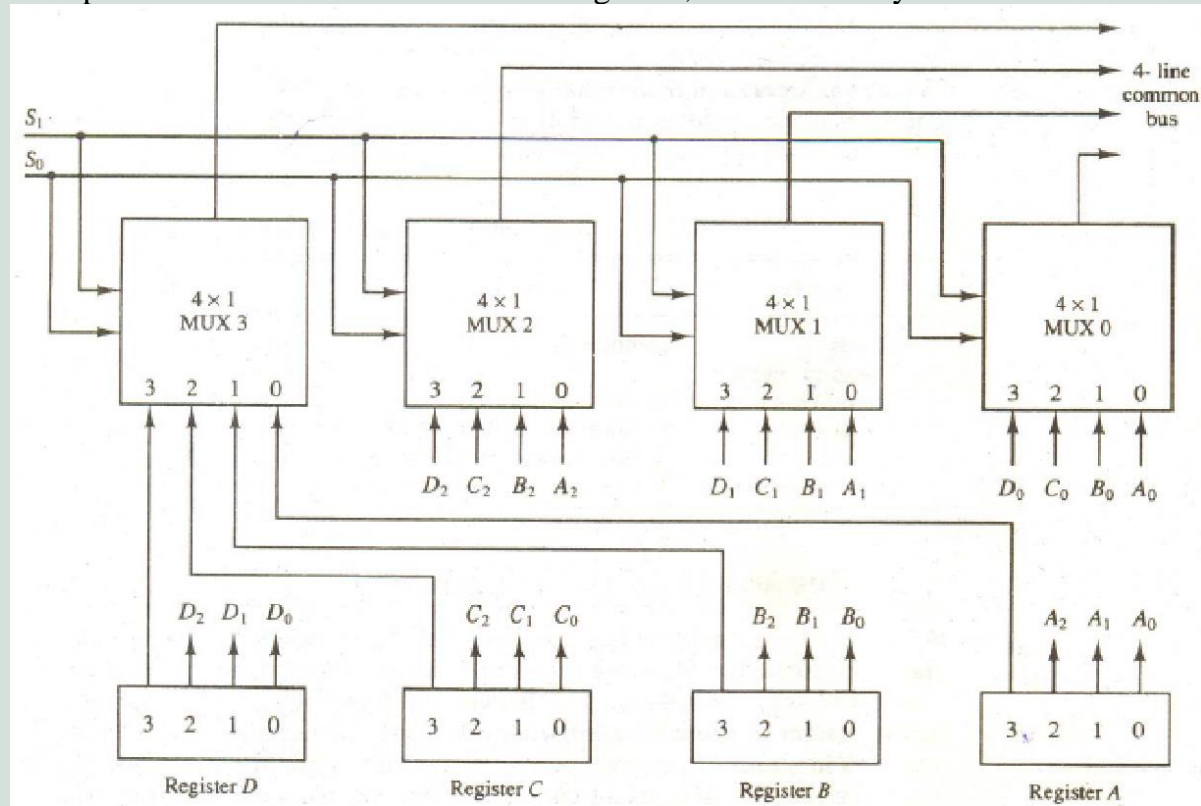
Function Table for BUS

S_1	S_0	Register selected
0	0	A
0	1	B
1	0	C
1	1	D

The two selection lines S_1 and S_0 are connected to the selection inputs of all four multiplexers. The selection lines choose the four bits of one register and transfer them into the four line common bus. When $S_1 S_0 = 00$, the 0 data inputs of all four multiplexers are selected and applied to the outputs that form the bus. This causes the bus lines to receive the content of register A since the outputs of this register are connected to the 0data inputs of the multiplexers. Similarly, register B is selected if $S_1 S_0 = 01$, and so on. Table shows the register that is selected by the bus for each of the four possible binary value of the selection lines.
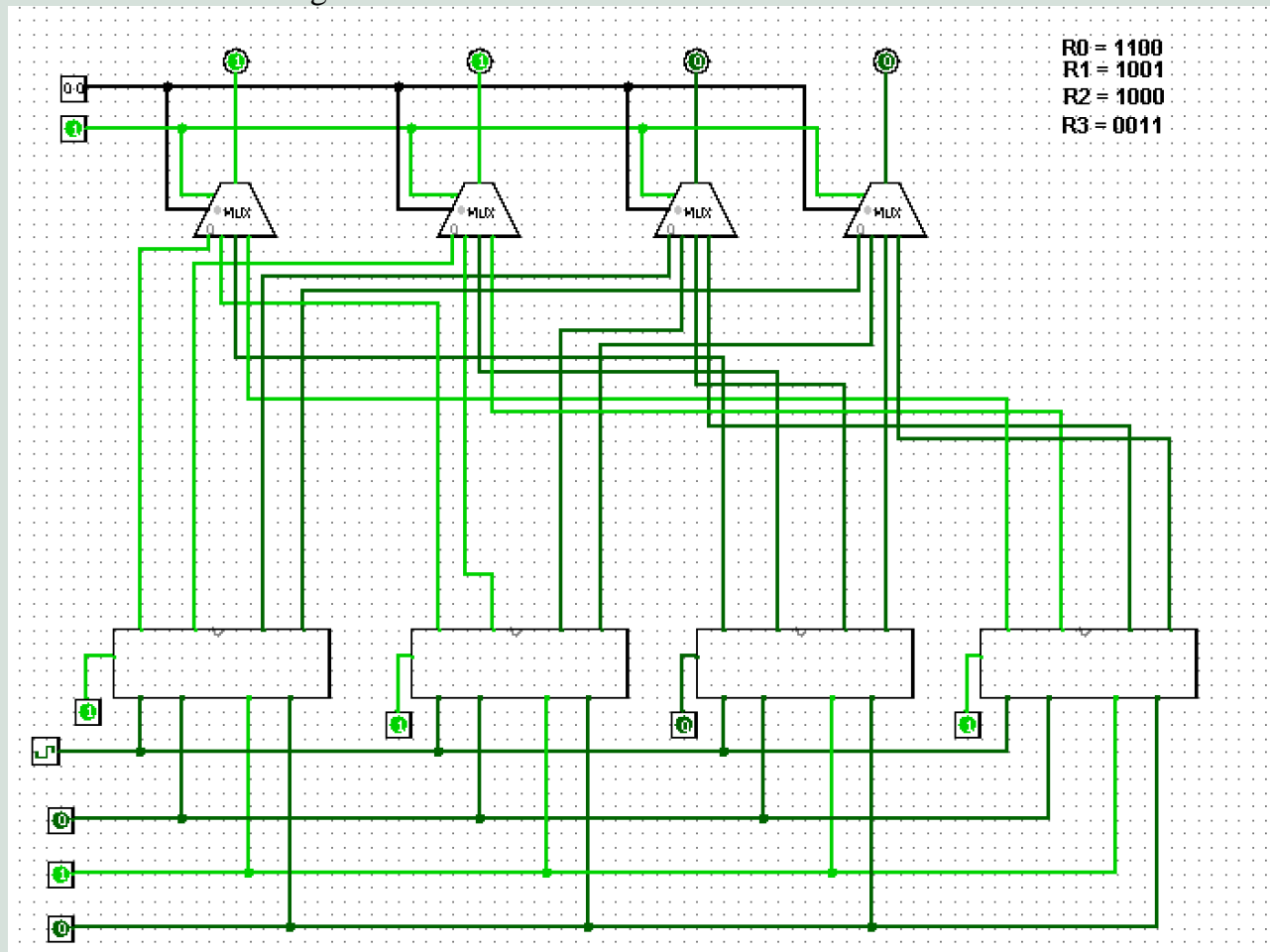
In general, a bus system will multiples k registers of n bits each to produce an n-line common bus. The number of multiplexers needed to construct the bus is equal to n, the number of bits in each register. The size of each multiplexer must be k ×1 since it multiplexes k data lines. For example, a common bus for eight registers of 16 bits each requires 16 multiplexers, one

for each line in the bus. Each multiplexer must have eight data input lines and three selection lines to multiplex one significant bit in the eight registers.
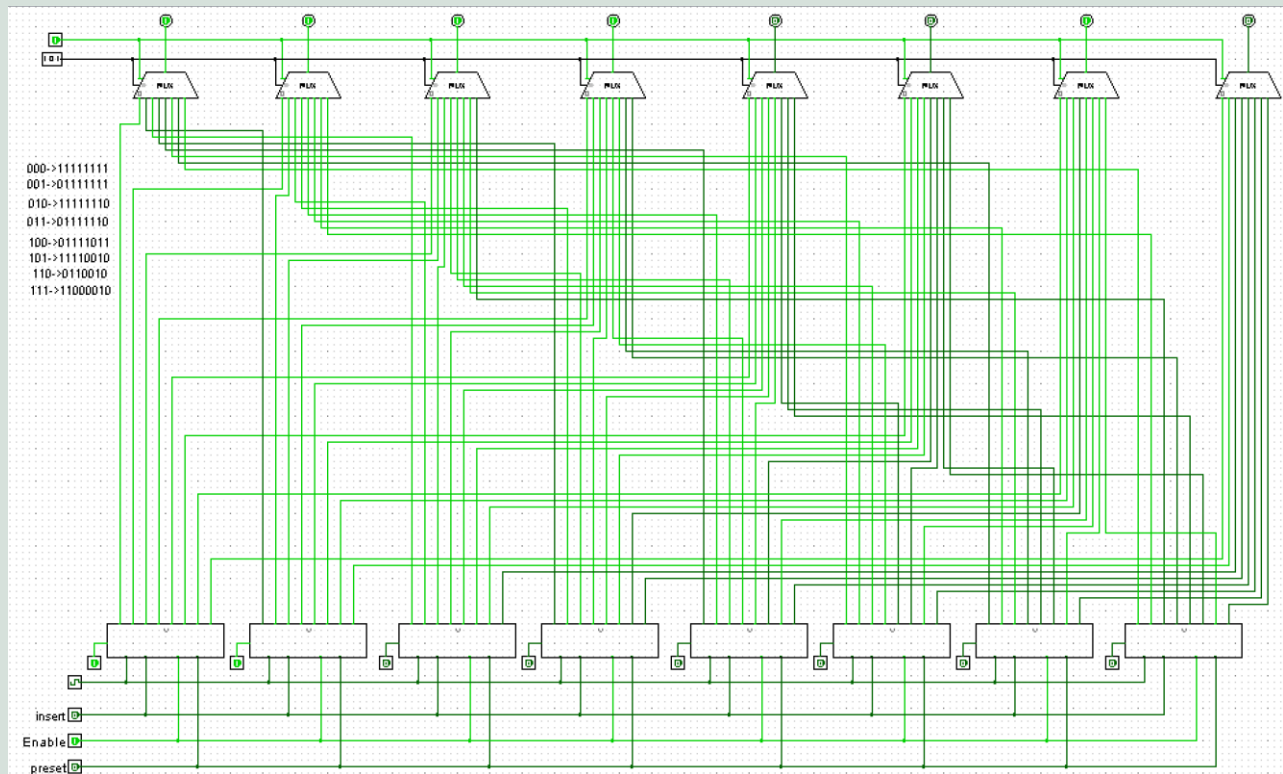
The transfer of information from a bus into one of many destination registers can be accomplished by connecting the bus lines to the inputs of all destination registers and activating the load control of the particular destination register selected.

Components:

1. 4-bit Registers

2. 4×1 multiplexers

000->11111111
001->01111111
010->11111110
011->01111110
100->01111011
101->11110010
110->0110010
111->11000010

insert
Enable
preset

Result: Explain working

LABWORK: add extra page

1. bus system for four register

CONCLUSION:
A common bus system in digital computers uses multiplexers to efficiently transfer binary information between registers, reducing the number of required wires. Selection lines control which register's data is placed on the bus. The bus connects to all registers, allowing easy transfer of data to a selected destination register.