PRACTICAL - 3

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AIM: To design Ripple Carry Subtractor.

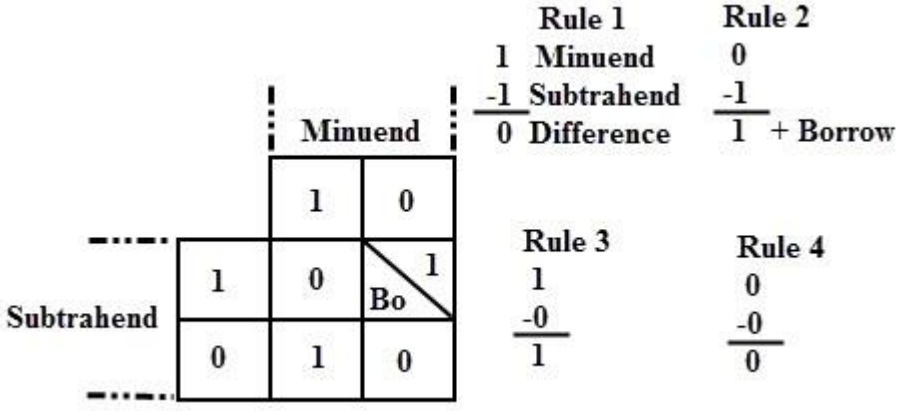
THEORY:

The Binary Subtractor is another type of combinational arithmetic circuit that is the opposite of the Binary Adder we looked at in a previous practical. As their name implies, a Binary Subtractor is a decision making circuit that subtracts two binary numbers from each other, for example, X – Y to find the resulting difference between the two numbers.

Unlike the Binary Adder which produces a SUM and a CARRY bit when two binary numbers are added together, the binary subtractor produces a DIFFERENCE, D by using a BORROW bit, B from the previous column. Then obviously, the operation of subtraction is the opposite to that of addition.

Binary Subtraction Circuits

Subtraction is a mathematical operation in which one integer number is deducted from another to obtain the equivalent quantity. The number from which other number is to be deducted is called as minuend and the number subtracted from the minuend is called subtrahend. Similar to the binary addition, binary subtraction is also has four possible alternative operations.

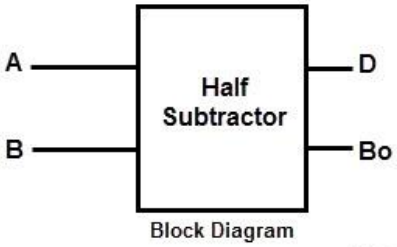


The above figure shows the four possible rules or elementary operations of the binary subtractions. In all the operations, each subtrahend bit is deducted from the minuend bit.

But in the second rule, minuend bit is smaller than the subtrahend bit, hence 1 is borrowed to perform the subtraction. Similar to the adder circuits, subtraction circuits are also classified as half subtractors, full subtractors and parallel subtractors.

Half Subtractor

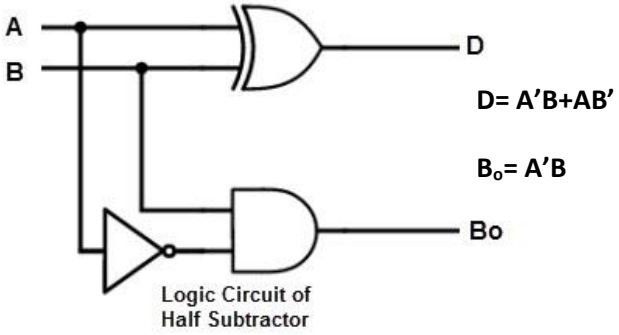
A half subtractor is a multiple output combinational logic network that does the subtraction of two bits of binary data. It has input variables and two output variables. Two inputs are corresponding to two input bits and two output variables corresponds to the difference bit and borrow bit. The binary subtraction is also performed by the Ex-OR gate with additional circuitry to perform the borrow operation. Thus, a half subtractor is designed by an Ex-OR gate including AND gate with A input complemented before fed to the gate.



Block Diagram

A	B	D	B_o
0	0	**0**	**0**
0	1	**1**	**1**
1	0	**1**	**0**
1	1	**0**	**0**

Truth Table



D= A'B+AB'

B_o= A'B

Logic Circuit of Half Subtractor

This circuit is similar to the half adder with only difference in input A i.e., minuend which is complemented before applied at the AND gate to implement the borrow output.

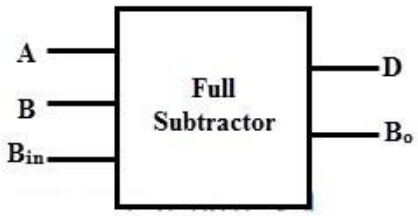
In case of multi-digit subtraction, subtraction between the two digits must be performed along with borrow of the previous digit subtraction, and hence a subtractor needs to have three inputs. Therefore, a half subtractor has limited applications and strictly it is not used in practice.

Full Subtractor

A combinational logic circuit performs a subtraction between the two binary bits by considering borrow of the lower significant stage is called as the full subtractor. In this,

subtraction of the two digits is performed by taking into consideration whether a 1 has already borrowed by the previous adjacent lower minuend bit or not.

It has three input terminals in which two terminals corresponds to the two bits to be subtracted (minuend A and subtrahend B), and a borrow bit Bi corresponds to the borrow operation. There are two outputs, one corresponds to the difference D output and other borrow output Bo as shown in figure along with truth table

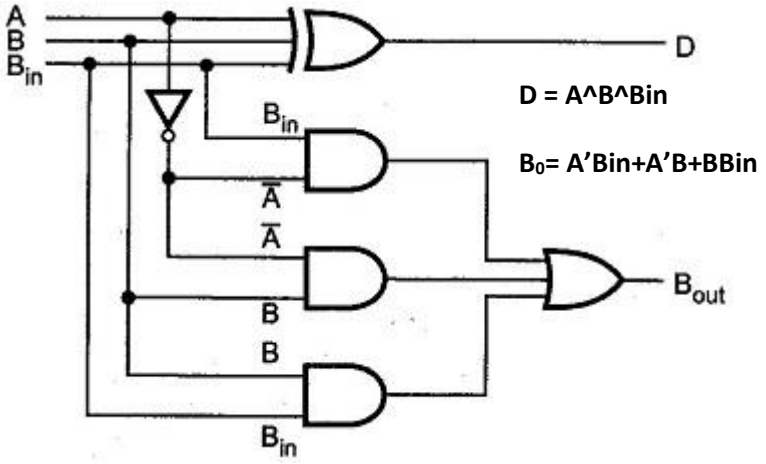


Block Diagram of Full Subtractor

A	B	B_{in}	D	B_o
0	0	0	**0**	**0**
0	0	1	**1**	**1**
0	1	0	**1**	**1**
0	1	1	**0**	**1**
1	0	0	**1**	**0**
1	0	1	**0**	**0**
1	1	0	**0**	**0**
1	1	1	**1**	**1**

Truth Table

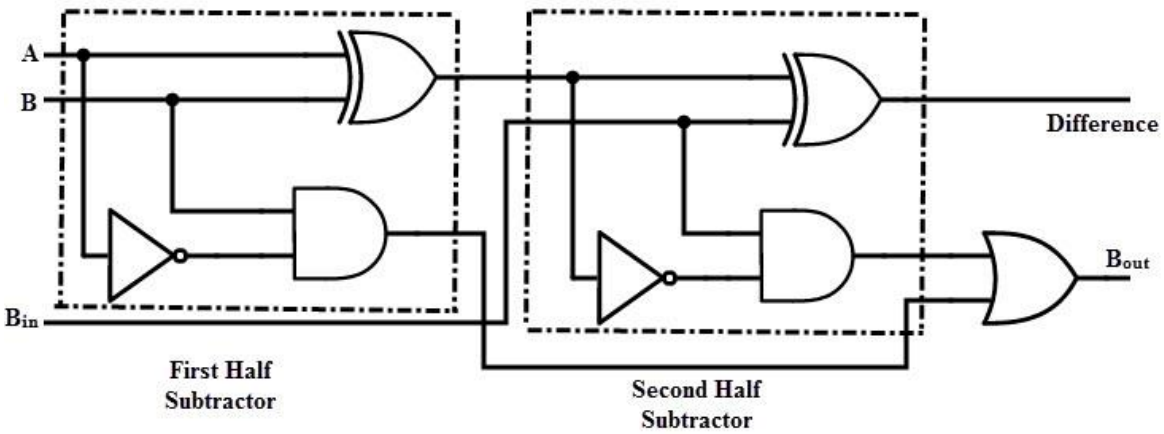
By deriving the Boolean expression for the full subtractor from above truth table, we get the expression that tells that a full subtractor can be implemented (a) directly and with (b) half subtractors with OR gate as shown in figure below.



D = A^B^Bin

B_0= A'Bin+A'B+BBin

(a)



(b)

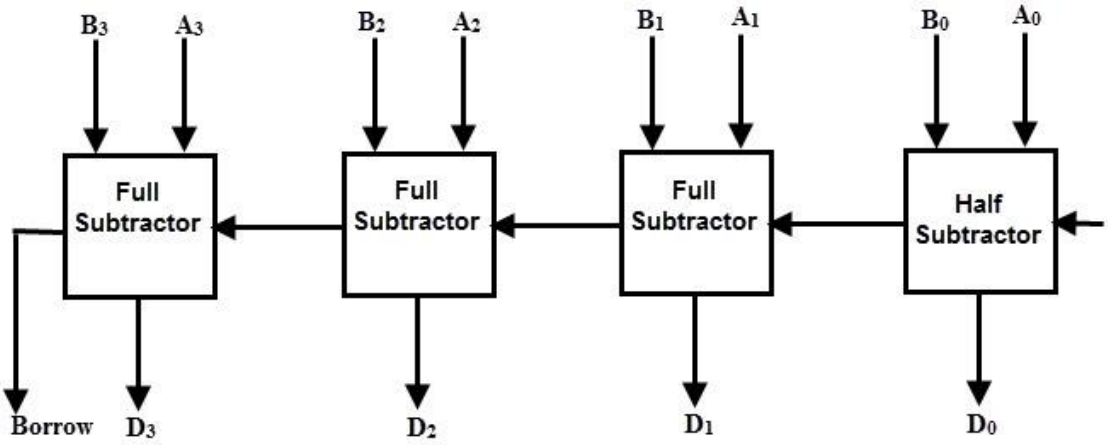
By comparing the adder and subtractor circuits or truth tables, one can observe that the output D in the full subtractor is exactly same as the output S of the full adder. And the only difference is that input variable A is complemented in the full subtractor. Therefore, it is possible to convert the full adder circuit into full subtractor by simply complementing the input A before it is applied to the gates to produce the final borrow bit output Bo.

Parallel Binary Subtractors

To perform the subtraction of binary numbers with more than one bit is performed through the parallel subtractors. This parallel subtractor can be designed in several ways, including combination of half and full subtractors, all full subtractors, all full adders with subtrahend complement input, etc.

The below figure shows a 4 bit parallel binary subtractor formed by connecting one half subtractor and three full subtractors.

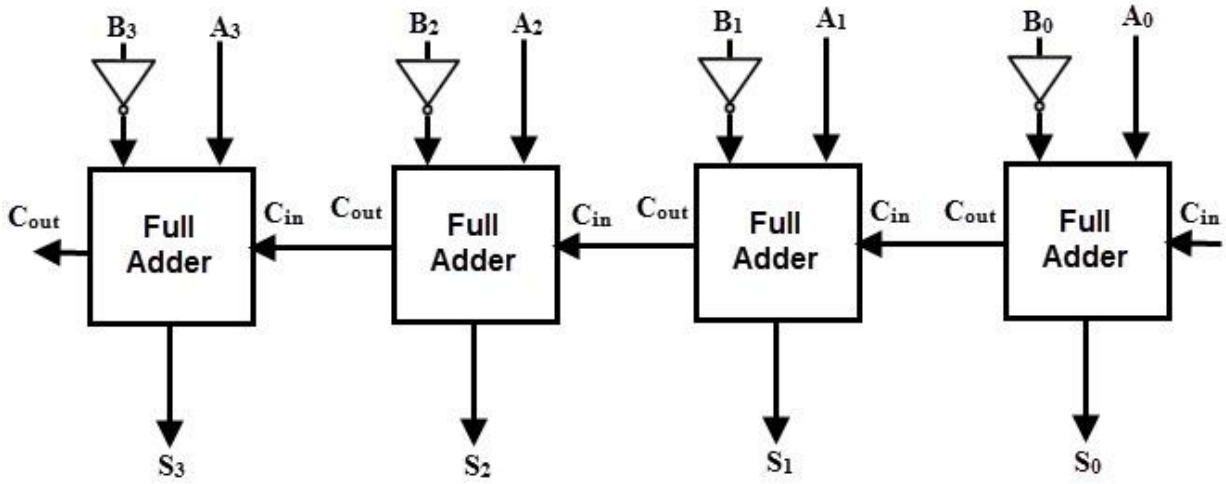
In this subtractor, 4 bit minuend A3A2A1A0 is subtracted by 4 bit subtrahend B3B2B1B0 and gives the difference output D3D2D1D0. The borrow output of each subtractor is connected as the borrow input to the next preceding subtractor.



It is also possible to design a 4 bit parallel subtractor 4 full adders as shown in the below figure. This circuit performs the subtraction operation by considering the principle that the addition of minuend and the complement of the subtrahend is equivalent to the subtraction process.

We know that the subtraction of A by B is obtained by taking 2's complement of B and adding it to A. The 2's complement of B is obtained by taking 1's complement and adding 1 to the least significant pair of bits.

Hence, in this circuit 1's complement of B is obtained with the inverters (NOT gate) and a 1 can be added to the sum through the input carry.

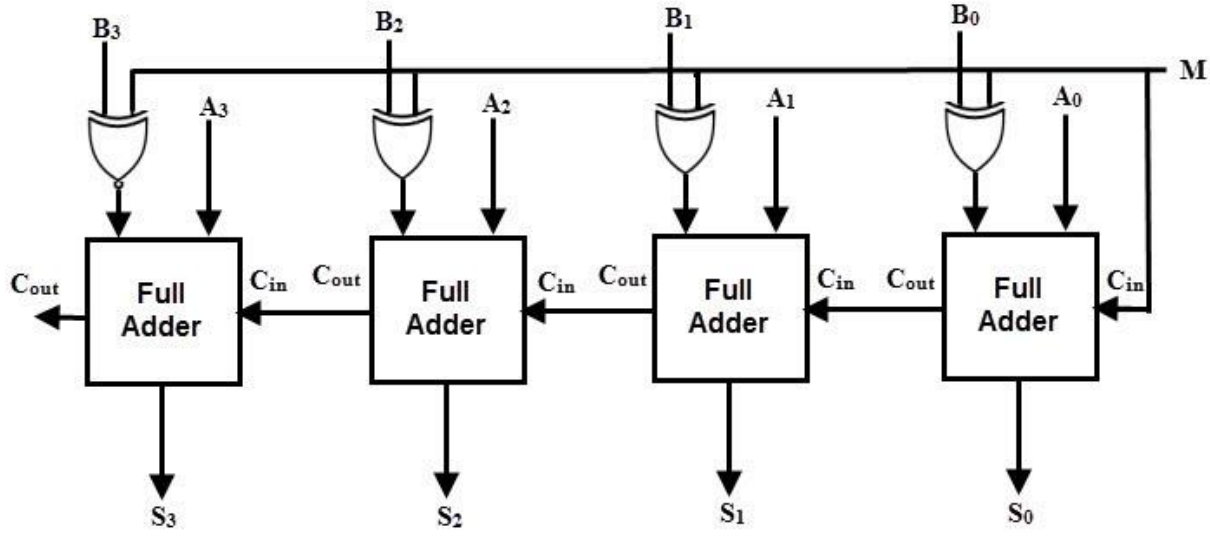


Parallel Adder / Subtractor

The operations of both addition and subtraction can be performed by a one common binary adder. Such binary circuit can be designed by adding an Ex-OR gate with each full adder as shown in below figure. The figure below shows the 4 bit parallel binary adder/subtractor which has two 4 bit inputs as A3A2A1A0 and B3B2B1B0.

The mode input control line M is connected with carry input of the least significant bit of the full adder. This control line decides the type of operation, whether addition or subtraction.

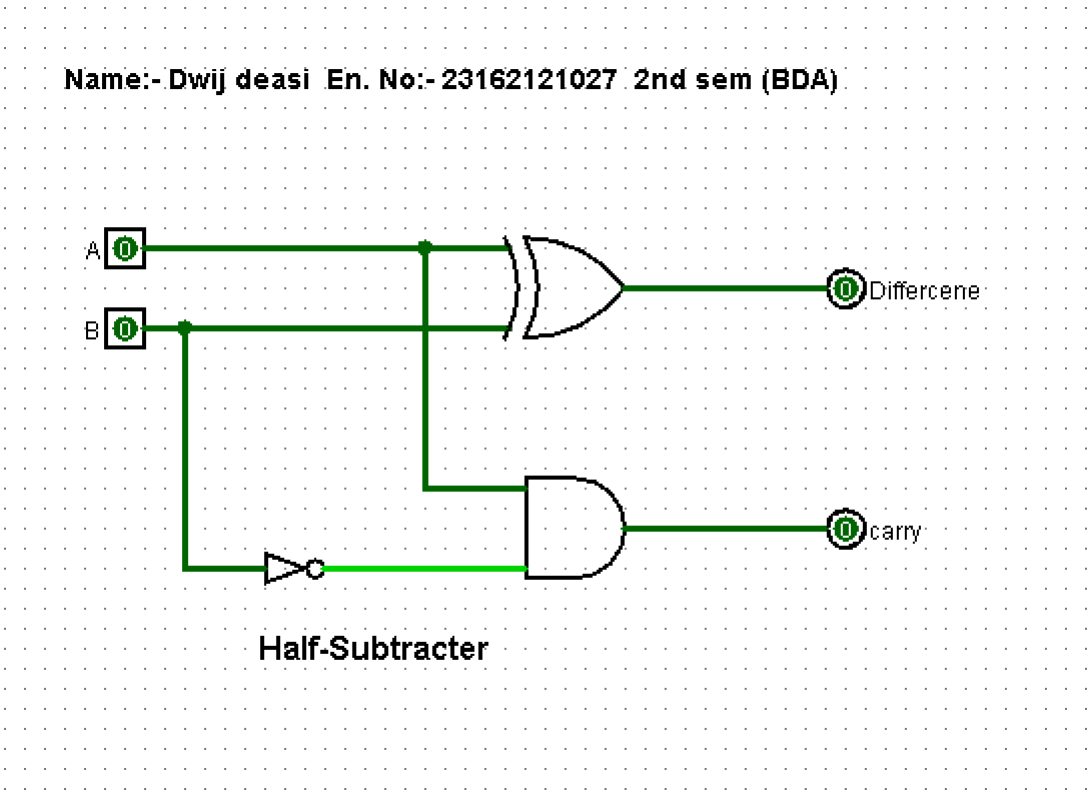
When M= 1, the circuit is a subtractor and when M=0, the circuit becomes adder. The Ex-OR gate consists of two inputs to which one is connected to the B and other to input M. When M = 0, B Ex-OR of 0 produce B. Then full adders add the B with A with carry input zero and hence an addition operation is performed.



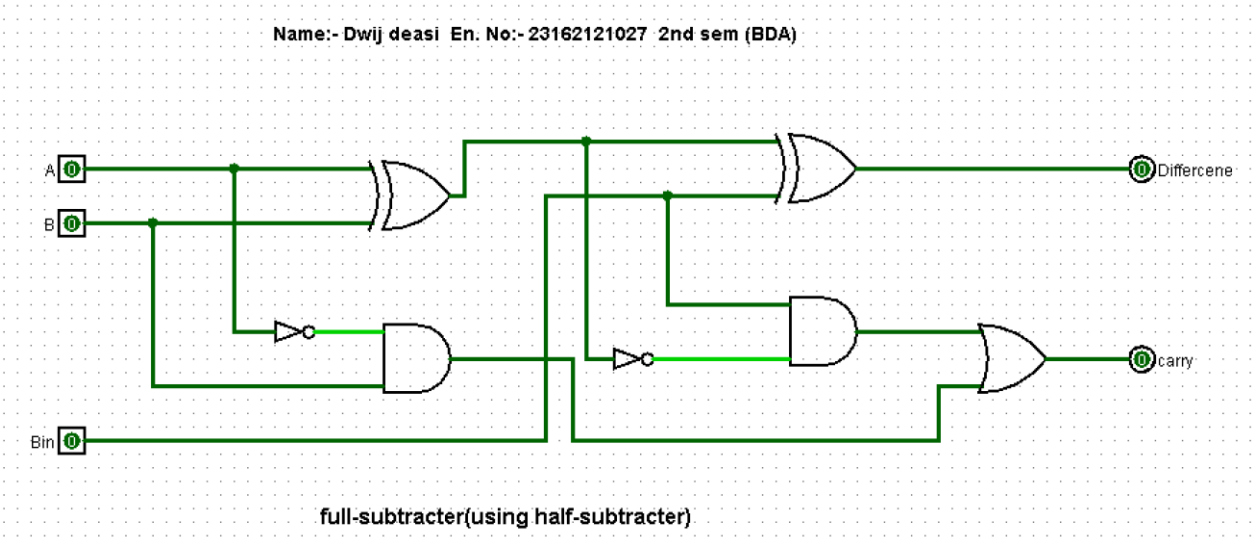
When M = 1, B Ex-OR of 0 produce B complement and also carry input is 1. Hence the complemented B inputs are added to A and 1 is added through the input carry, nothing but a 2's complement operation. Therefore, the subtraction operation is performed.

LABWORK: add extra pages

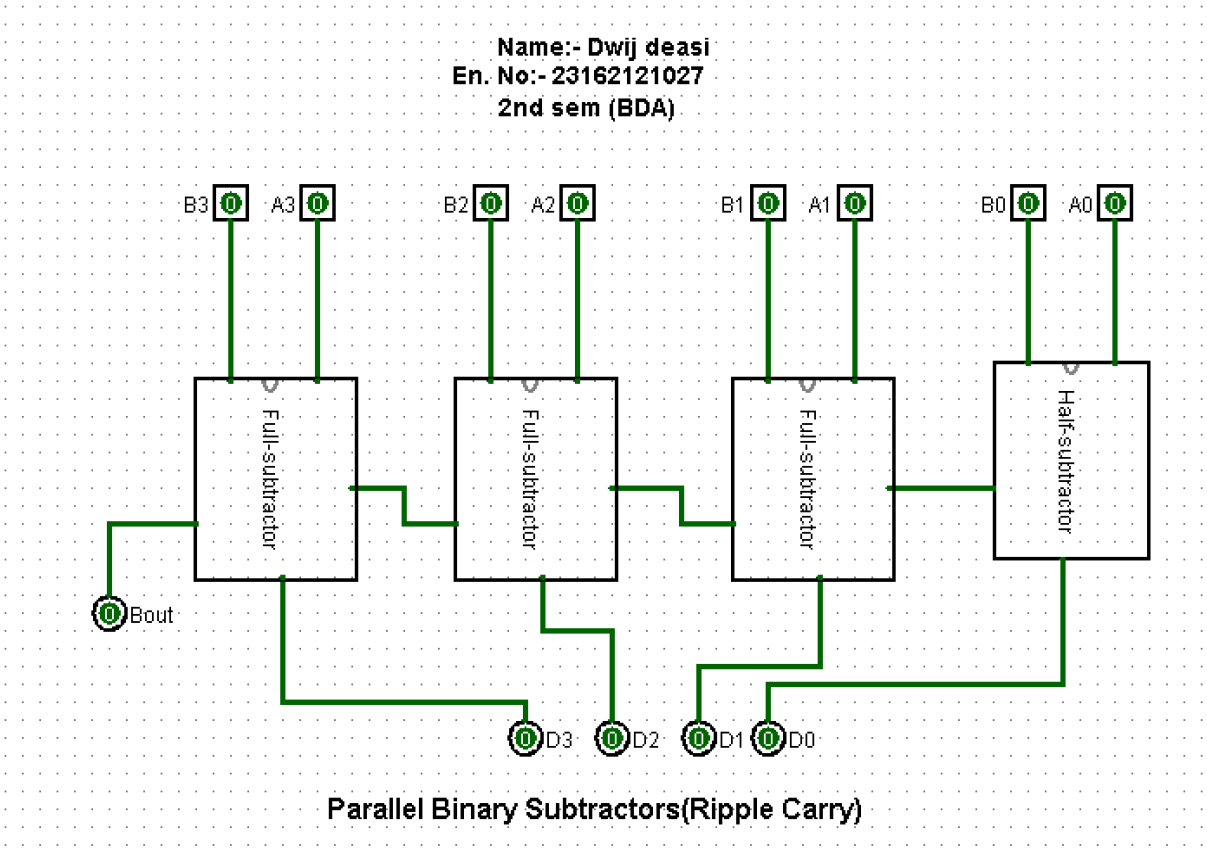
1. **Half Subtractor**



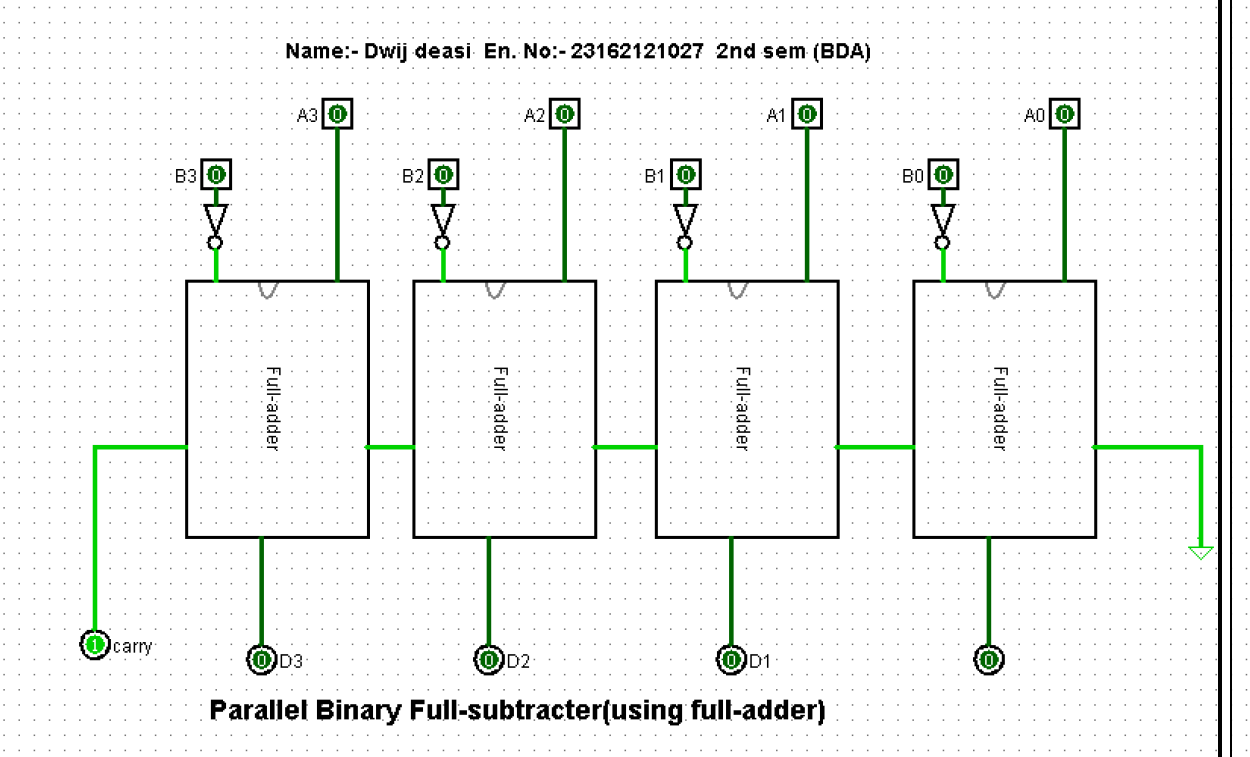
2. **Full-subtracter(using half-subtracter)**



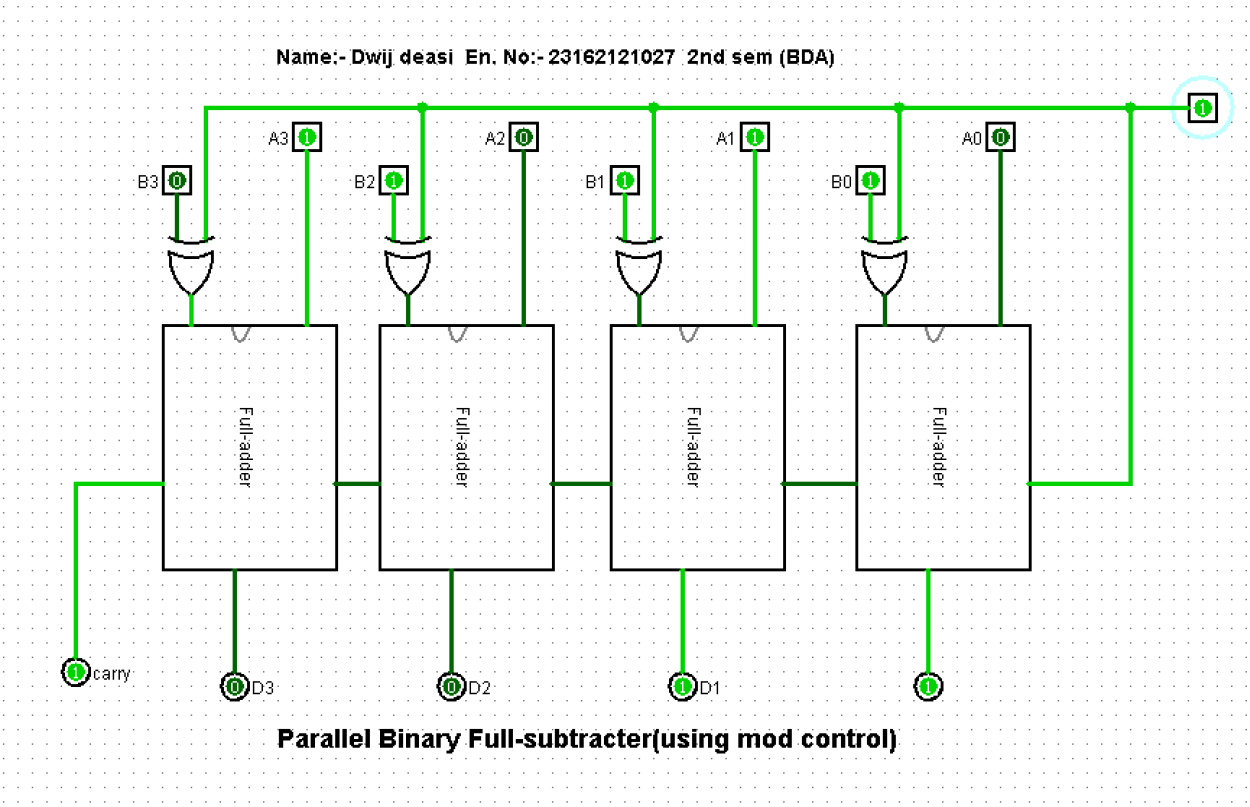
3. **Parallel Binary Subtractors(Ripple Carry)**



4. Parallel Binary Full-subtracter(using full-adder)



5. Parallel Binary Full-subtracter(using mod control)



CONCLUSION:

The Binary Subtractor circuit, including the Half Subtractor, Full Subtractor, and Parallel Binary Subtractors, provides the functionality to subtract binary numbers efficiently. These circuits utilize various logic gates and principles, such as 2's complement and borrow, to perform subtraction accurately. Additionally, the design of a Parallel Adder/Subtractor demonstrates the versatility of binary circuits to perform both addition and subtraction operations based on a control input, showcasing the flexibility of digital logic design.