

Ganpat University
Faculty of Engineering & Technology
Computer Science & Engineering
2CSE205: Computer Organization

Name:- Dwij Vatsal Desai

Sem:- 2

Sub: - CO

Enrollment No.:- 23162121027

Prac:- 9

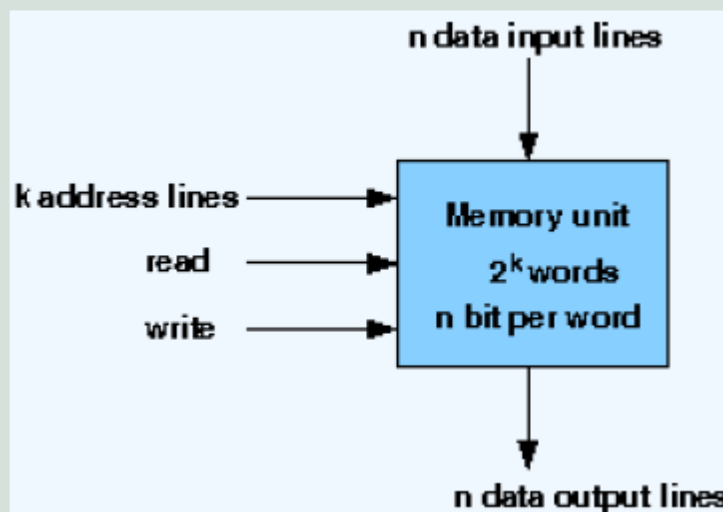
PRACTICAL - 9

AIM: To study and design 1 bit and 16-bit memory cell.

THEORY:

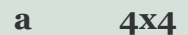
A memory unit is a collection of storage cells together with associated circuits needed to transform information in and out of the device. Memory cells which can be accessed for information transfer to or from any desired random location is called random access memory(RAM). The block diagram of a memory unit-

4096x16

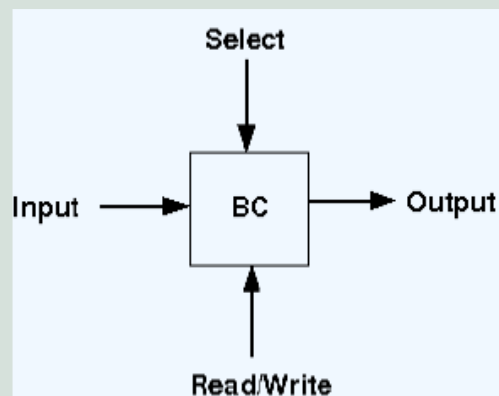


The internal construction of a random-access memory of m words with n bits per word consists of $m \times n$ binary storage cells and associated decoding circuits for selecting individual words. The binary cell is the basic building block of a memory unit.

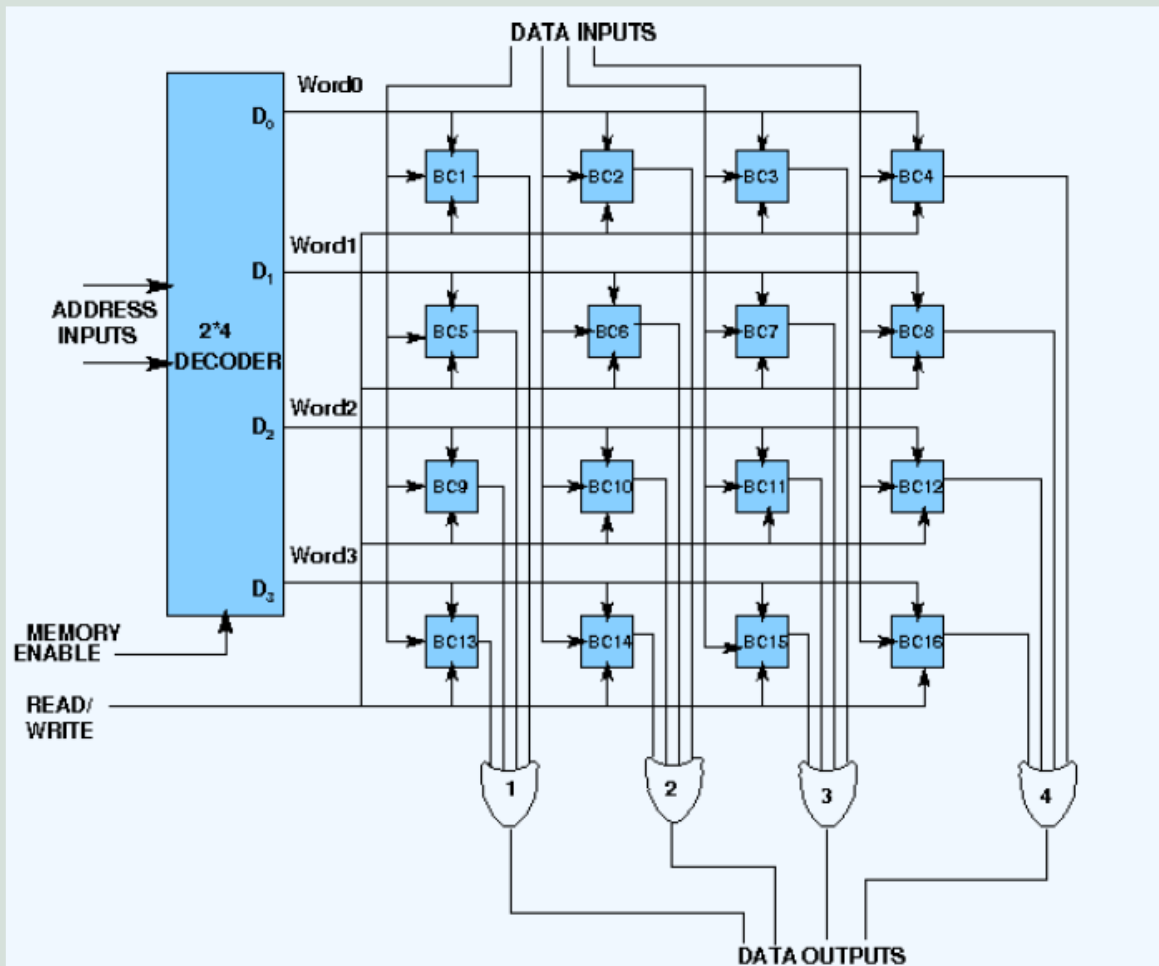
The binary cell has three inputs and one output. The select input enables the cell for reading or writing and the read/write input determines the cell operation when it is selected. A 1 in the read/write input provides the read operation by forming a path from the flip-flop to the output terminal. A 0 in the read/write input provides the write operation by forming a path from the input terminal to the flip-flop. The logic diagram is-



The logical construction of a small RAM 4X4 is shown below. It consists of 4 words of 4 bits each and has a total of 16 binary cells. Each block labeled BC represents the binary cell with its 3 inputs and 1 output. The block diagram of a binary cell-



A memory with 4 words needs two address lines. The two address inputs go through a 2×4 decoder to select one of the four words. The decoder is enabled with the memory enable input. When the memory enable is 1, all outputs of the decoder are 0 and none of the memory words are selected. With the memory enable at 0, one of the four words is selected, dictated by the value in the two address lines. Once a word has been selected, the read/write input determines the operation. The logic diagram is-



Components:

1. SR Flip Flop
2. 2×4 Decoder
3. OR, AND and NOT gate

Result:

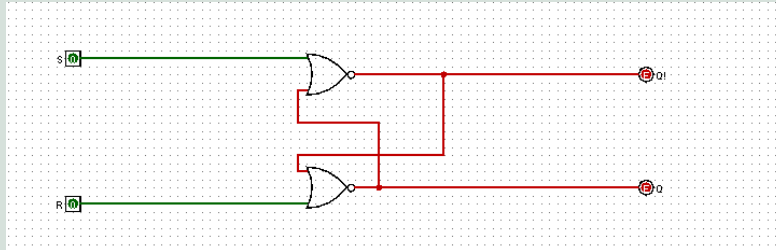
Examining the write behavior:

Examining the Read behavior:

LABWORK: add extra pages

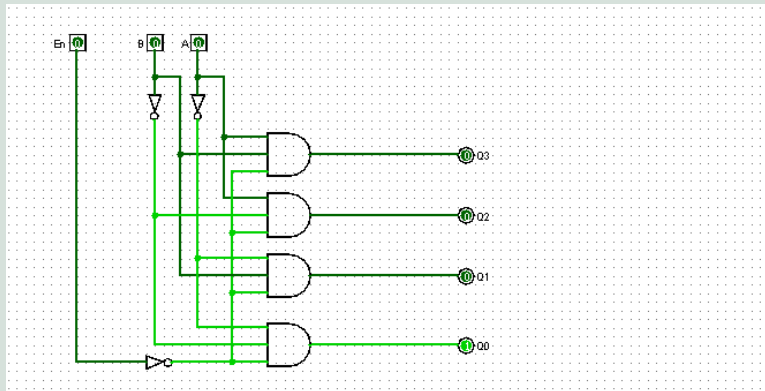
1. SR Flip Flop

Screenshot:-



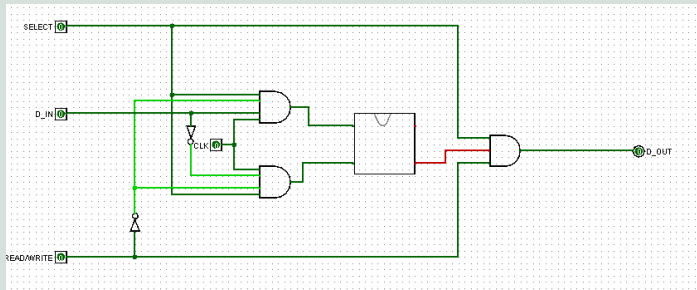
2. 2*4 Decoder

Screenshot:-



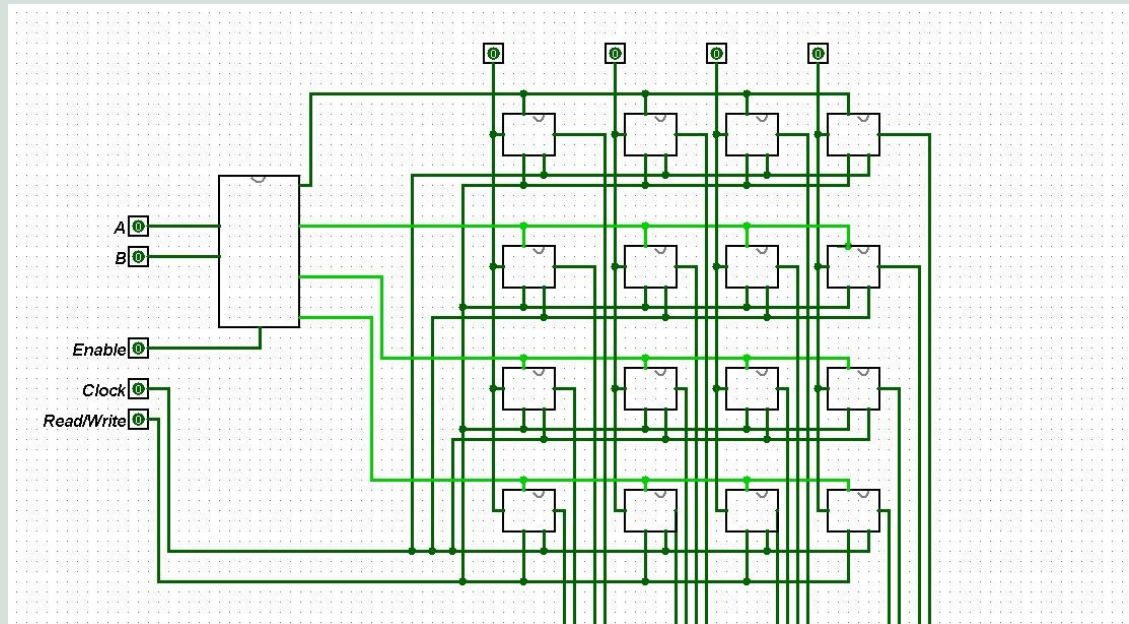
3. 1 bit Memory Cell

Screenshot:-



4. 16 bit Memory Cell

Screenshot:-



CONCLUSION:

We Got To Know About Memory Cell