

GNU-ICT CO (2023-2025)

Assignment - 2

Name :- Dwij Vatsal Desai

En. no :- 23162121027

Sem. :- 2nd (BDA)

Date :- 07/05/2024

Q-1 (7.1) What is the difference between a microprocessor and a microprogram? Is it possible to design a microprocessor without a microprogram? Are all microprogrammed computers also microprocessors?

Ans A microprocessor is a small size CPU (computer on a chip). Microprogram is a program for a sequence of microoperations. The control unit of a microprocessor can be hardwired or microprogrammed, depending on the specific design. A microprogrammed computer does not have to be a microprocessor.

Q-2 (7.3) Define the following :

(a) microoperation

Ans An elementary digital computer operation.

(b) Microinstruction

Ans An instruction stored in control memory.

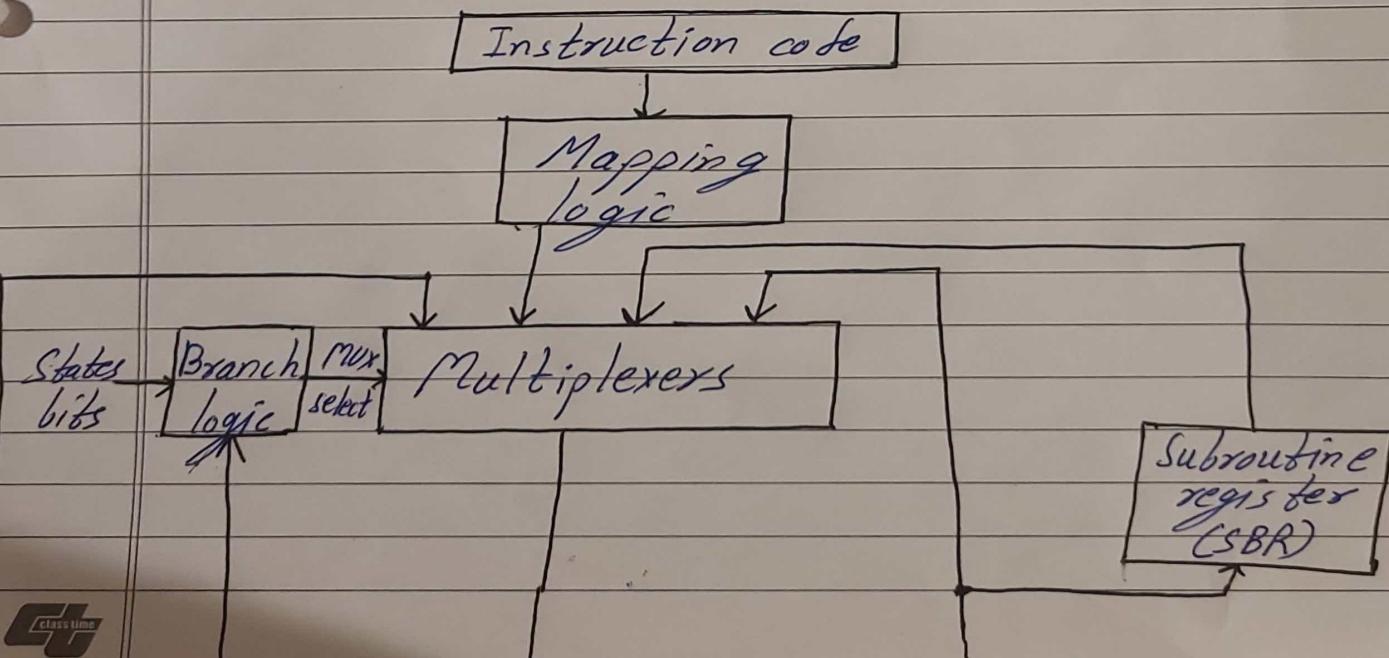
(c) Microprogram

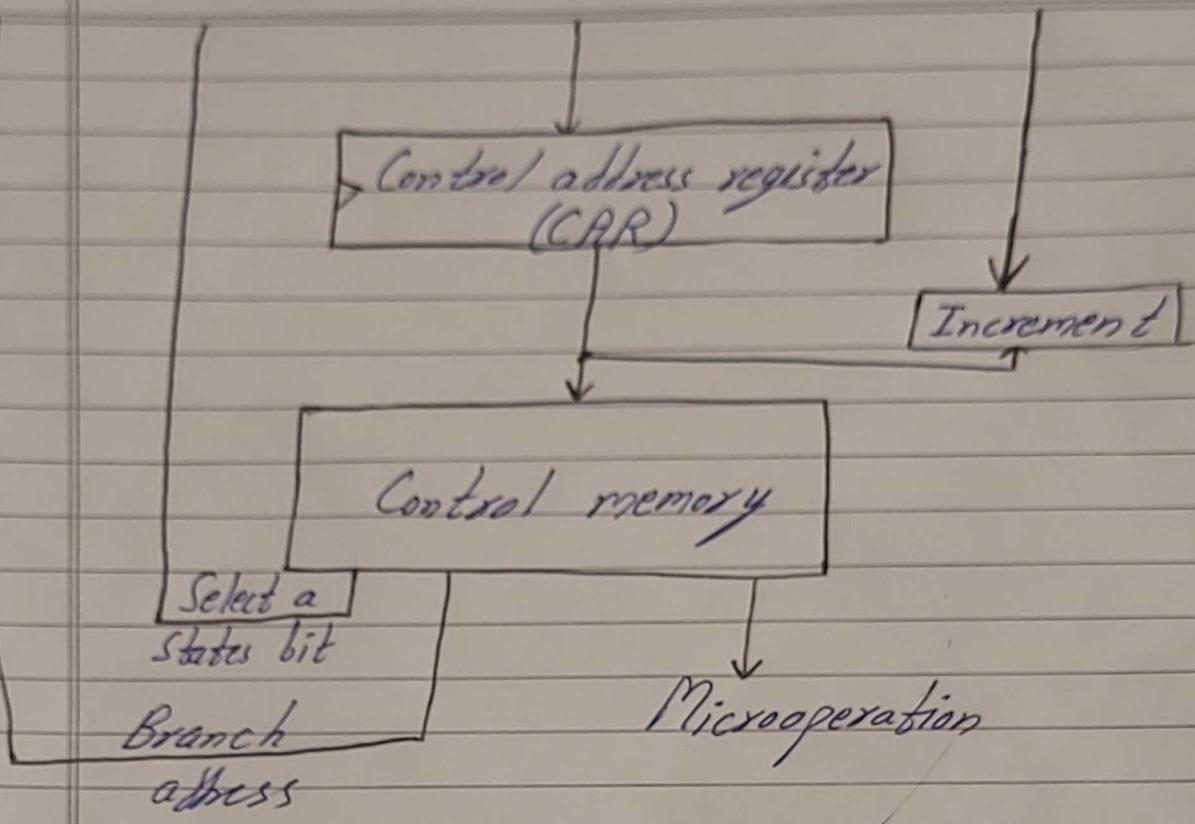
Ans A sequence of microinstructions.

(d) Microcode

Ans Same as microprogram.

Q-3 (7.5) The system shown in Figure below uses a control memory of 1024 words of 32 bits each. The microinstruction has three fields as shown in the diagram. The microoperations field has 16 bits.





- (a) How many bits are there in the branch address field and the select field?

Ans Control memory = $2^{10} \times 32$

6	10	16
Select	Address	Micro operation

= 32 bits

- (b) If there are 16 status bits in the system, how many bits of the branch logic are used to select a status bit?

Ans 4 bits.

(c) How many bits are left to select an input for the multiplexers?

Ans 2 bits

Q-4 (7.11) Given the 9-bit microoperations to register transfer statements and to binary.

a. $AC \leftarrow AC + I, DR \leftarrow DR + I$

b. $PC \leftarrow PC + I, DR \leftarrow M[AR]$

c. $DR \leftarrow AC, AC \leftarrow DR$

Ans F1 F2 F3

(a)	011	110	000	INCAC	INCDR	NOP
(b)	000	100	101	NOP	READ	INCPC
(c)	100	101	000	DRTAC	ACTDR	NOP

Q-5 (7.12) Convert the following symbolic microoperations to register transfer statements and to binary.

- a. READ, INCPC
- b. ACTDR, DRTAC
- c. ARTPC, DRTAC, WRITE.

Ans (a) Binary
READ $DR \leftarrow M[AR]$ $F2 = 100$
DRTAC $AC \leftarrow DR$ $F3 = 101$ 001 100 101

(b) ACTDR $DR \leftarrow AC$ $F2 = 101$ 000 100 101
DRTAC $AC \leftarrow DR$ $F1 = 100$

(c) ARTPC $PC \leftarrow AR$ $F3 = 110$
DRTAC $AC \leftarrow DR$ $F1 = 100 \rightarrow$ Impossible
WRITE $M[AR] \leftarrow DR$ $F1 = 111 \rightarrow$ Both use FI.

Q-6 (7.14) The following is a symbolic microprogram for an instruction in the computer defined.

NOP	S	JMP	FETCH
NOP	Z	JMP	FETCH
NOP	I	CALL	INDRCT
ARTPC	U	JMP	FETCH

Ans (a) (a) Specify the operation performed when the instruction is executed.

Ans Branch if $S=0$ and $Z=0$ (positive and non-zero AC).

(1) Convert the four microinstructions into their equivalent binary form.

40	:	000	000	000	10 00	10000000
41	:	000	000	000	11 00	10000000
42	:	000	000	000	01 01	1000011
43	:	000	000	100	00 00	10000000

Q-7 (7.2) Explain the difference between hardware control and microprogrammed control. Is it possible to have a hardwired control associated with a control memory?

Ans Hardwired Control :-

- Hardwired control unit generates the control signal needed for the processor using logic circuit.
- Hardwired control unit faster when compared to micro-programmed control unit as the required control signals are generated with help of hardware.
- Hardwired used in computers that makes use of reduced instruction set computers (RISC).

⇒ Micro-programmed Control :-

- Micro-programmed control unit generates the control signal with the help of micro-instructions stored in control memory.
- This is slower than the other as micro-instruction are used for generating signals.
- Micro-programmed control units used in computer

that makes use of complex instruction's set computers (CISC).

Q-8 (8.1) A bus-organized CPU similar to Tiger has 16 registers with 32 bits in each, an ALU, and a destination decoder.

a. How many selection multiplexers are there in the A bus, and what is the size of each multiplexer?

Ans Number of bit equal to number of multiplexer, so 36 multiplexer are there in CL bus and size of multiplexer is 16×1 (32 multiplexer in use & 4 multiplexer in ground).

b. How many selection inputs are needed for MUX A and MUX B?

Ans 4-inputs each, to select one of 16 registers.

c. How many inputs and outputs are there in the decoder?

Ans 4-to-16 lines of decoder.

d. How many inputs and outputs are there in the ALU for data, including input and output carries?

Ans $32 + 32 + 1 = 65$ data input lines

- e. Formulate a control word for the system assuming that the ALU has 35 operations.

Ans

4 4 4 6 = 18 bits

SEL A	SEL B	SEL D	OPR
-------	-------	-------	-----

Q-9 (8.3) Convert the following arithmetic expressions from infix to reverse Polish notation.

a. $A * B + C * D + E * F$

Ans $AB * CD * EF * ++$

b. $A * B + A * (B * D + C * E)$

Ans $AB * ABD * CE * + * +$

c. $A + B * [C * D + E * (F + G)]$

Ans $FG + E * CD * + B * A +$

d. $A * [B + C * (D + E)] / F * (G + H)$

Ans $ABCDE + * + * FGH + */$

Q-10 (8.9) Convert the following numerical arithmetic expression into reverse Polish notation and show the stack operations for evaluating the numerical result.

$$(3+4)[10(2+6)+8]$$

Ans $(3+4)[10(2+6)+8]$

Convert it in to RPN

$$34 + 10 26 + * 8 + *$$

- let evaluate RPN expression using stack push 3 and 4 on to stack, Apply addition operator,

$$3+4=7$$

- Put 10, 2 and 6 on to stack
- ↓ ↓ ↓
 Multiplication → addition

$$\begin{aligned} 2+6 &= 8 \\ 8 * 10 &= 80 \end{aligned}$$

Push 8 on to stack, Apply addition operation with 80,

$$80+8 = 88.$$

Push 88 on stack.

Apply multiplication operator on 88×7

$$\therefore 88 * 7 = 616$$

(a)

$$(B+4)[10(2+6)+8] = 616$$

Q-11 (8.18) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is

(a) direct.

Ans Effective address is the address field value which is 400.

(b) immediate.

Ans Effective address is the address field itself which is 301.

(c) Relative.

Ans Effective address is the sum of the address field value and the current program counter $301 + 400 = 701$.

(d) Register indirect :-

Ans Value stored in the register RI which is 200.

(e) Index with RI as the index register :-

Ans Effective address is the sum of the address field value and the content of register

$$RI (400 + 200 = 600)$$

Q-12 (8.25) An 8-bit computer has a register R. Determine the value of status bits C, S, Z and V after each of the following instructions. The initial value of register R in each case is hexadecimal 72. The numbers below are also in hexadecimal.

a. Add immediate operand C6 to R.

Ans

$$\begin{array}{r} 01110010 \rightarrow 72 \\ 11000110 \rightarrow C6 \\ \hline 00111000 \rightarrow 138 \end{array}$$

$$\therefore C=1, S=0, Z=0 \text{ & } V=1$$

b. Add immediate operand IE to R.

Ans

$$\begin{array}{r}
 01110010 \rightarrow 72 \\
 00011110 \rightarrow \underline{IE} \\
 \hline
 10010000 \rightarrow 70
 \end{array}$$

$C=0, S=1, Z=0, V=1$

c. Subtract immediate operand IA from R.

Ans

$$\begin{array}{r}
 10011010 \rightarrow 9A \\
 01100110 \stackrel{2^5 \text{ comp.}}{\rightarrow} \\
 01110010 \rightarrow \underline{72} \\
 \hline
 11011000 \rightarrow \underline{D8}
 \end{array}$$

$C=0, S=1, Z=0 \text{ & } V=1$

(Borrow = 1)

d. AND immediate operand SD to R.

Ans

$$\begin{array}{r}
 01110010 \rightarrow 72 \quad C=0, S=0, Z=1, V=0 \\
 10001100 \rightarrow 8D \\
 \hline
 00000000 \rightarrow \underline{00}
 \end{array}$$

e. Exclusive-OR R with R.

Ans

$C=0, S=0, Z=1, V=0$

Q-B (Q37) Three computers use register windows with the following characteristics. Determine the window size and the total number of register in each computer.

Ans $A \geq B$ implies that $A - B \geq 0$ (positive or zero)

Sign $S=0$ if no over flow (positive)

or $S=1$ if over flow (sign reversal)

Boolean expression : $S'V' + SV = 1$ or $(S \oplus V) = 0$

$A < B$ is the complement of $A \geq B$ ($A - B$ negative)

then, $S=1$ if $V=0$

or, $S=0$ if $V=1$ $(S \oplus V)=1$

$A > B$ Implies $A \geq B$ but not $A=B$

$(S \oplus V)=0$ and $Z=0$

$A \leq B$ Implies $A < B$ or $A=B$

$S \oplus V=1$ or $Z=1$.

Q-14 (9.2) Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.

Ans

Segment 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13

1	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8				
2		T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8			
3			T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8		
4				T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	
5					T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8
6						T_1	T_2	T_3	T_4	T_5	T_6	T_7

$$(K+n-1)t_p = 6+8-1 = 13 \text{ cycle}$$

Q-15 (9.4) A nonpipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?

Ans $t_n = 50\text{ns}$ $k=6$ $t_p = 10\text{ns}$ $n=100$

$$S = \frac{n t_n}{(k+n-1) t_p} = \frac{100 \times 50}{(6-1) \times 10} = 4.76$$

$$S_{\max} = \frac{t_n}{t_p} = \frac{50}{10} = 5$$

Q-16 (9.5) The pipeline of figer has the following propagation times : 40ns for the operands to be read from memory into registers R1 and R2, 45ns for the signal to propagate through the multiplier, 5ns for the transfer into R3, and 15ns to add the two number into R5.

- a. What is the minimum clock cycle time that can be used?

Ane $t_p = 45 + 5 , \approx k = 3$

$$= \underline{\underline{50\text{ns}}}$$

- b. How many segments are there in the pipeline?

Ane $t_n = 40 + 45 + 15$

$$= \underline{\underline{100\text{ns}}}$$

c. Calculate the speedup of the pipeline for 10 tasks and again for 100 tasks.

Ans

$$S = \frac{n t_n}{(K+n-1) t_p} = \frac{10 \times 100}{(3+99)50} = \underline{\underline{1.67}}$$

$$= \frac{100 \times 100}{(2+99)50} = \underline{\underline{1.96}}$$

~~$$S_{max} = \frac{t_n}{t_p} = \frac{100}{50} = 2$$~~

d. What is the maximum speedup that can be achieved?

Ans

$$S_{max} = \frac{t_n}{t_p} = \frac{100}{50} = 2$$

O-17 (9.7) The time delay of the four segments in the pipeline are as follows:

$$t_1 = 50\text{ns}, t_2 = 30\text{ns}, t_3 = 95\text{ns} \text{ and } t_4 = 45\text{ns}.$$

The interface registers delay time $t_r = 5\text{ns}$.

a. How long would it take to add 100 pair of numbers in the pipeline?

Ans

$$\text{Clock cycle} = 95 + 5 = 100\text{ns} \text{ (Time for segment 3)}$$

for $n=100$, $k=4$, $t_p = 100\text{ns}$.

$$\begin{aligned}\text{Time to add 100 numbers} &= (k+n-1)t_p \\ &= (4+99)100 \\ &= 10,300\text{ns} = \underline{\underline{10.3\mu s}}\end{aligned}$$

(b) How can we reduce the total time to about one-half to of the time calculated in part (a)?

Ans Divide segment 3 into two segments of $50+5 = 55$

and $45+5=50\text{ns}$. This makes $t_p = 55\text{ns}$.

$$\begin{aligned}K=5 \quad (k+n-1)t_p &= (5+99)55 \\ &= 5720\text{ns} = \underline{\underline{5.72\mu s}}\end{aligned}$$

—X—X—X—X—X—X—