

Ganpat University  
Faculty of Engineering & Technology  
Computer Science & Engineering  
2CSE205: Computer Organization

**Name:- Dwij Vatsal Desai**

**Sem:- 2**

**Sub: - CO**

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**Prac:- 6**

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<b>PRACTICAL - 6</b>
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**AIM:** To study and design Combinational Multiplier.

**THEORY:**

Combinational Multipliers do multiplication of two unsigned binary numbers. Each bit of the multiplier is multiplied against the multiplicand, the product is aligned according to the position of the bit within the multiplier, and the resulting products are then summed to form the final result. Main advantage of binary multiplication is that the generation of intermediate products are simple: if the multiplier bit is a 1, the product is an appropriately shifted copy of the multiplicand; if the multiplier bit is a 0, the product is simply 0.

The design of a combinational multiplier to multiply two 4-bit binary number is illustrated below:

			<b>A<sub>3</sub></b>	<b>A<sub>2</sub></b>	<b>A<sub>1</sub></b>	<b>A<sub>0</sub></b>
			<b>B<sub>3</sub></b>	<b>B<sub>2</sub></b>	<b>B<sub>1</sub></b>	<b>B<sub>0</sub></b>
			<hr/>			
			<b>A<sub>3</sub> . B<sub>0</sub></b>	<b>A<sub>2</sub> . B<sub>0</sub></b>	<b>A<sub>1</sub> . B<sub>0</sub></b>	<b>A<sub>0</sub> . B<sub>0</sub></b>
		<b>A<sub>3</sub> . B<sub>1</sub></b>	<b>A<sub>2</sub> . B<sub>1</sub></b>	<b>A<sub>1</sub> . B<sub>1</sub></b>	<b>A<sub>0</sub> . B<sub>1</sub></b>	
	<b>A<sub>3</sub> . B<sub>2</sub></b>	<b>A<sub>2</sub> . B<sub>2</sub></b>	<b>A<sub>1</sub> . B<sub>2</sub></b>	<b>A<sub>0</sub> . B<sub>2</sub></b>		
<b>A<sub>3</sub> . B<sub>3</sub></b>	<b>A<sub>2</sub> . B<sub>3</sub></b>	<b>A<sub>1</sub> . B<sub>3</sub></b>	<b>A<sub>0</sub> . B<sub>3</sub></b>			
			<hr/>			
<b>S<sub>6</sub></b>	<b>S<sub>5</sub></b>	<b>S<sub>4</sub></b>	<b>S<sub>3</sub></b>	<b>S<sub>2</sub></b>	<b>S<sub>1</sub></b>	<b>S<sub>0</sub></b>

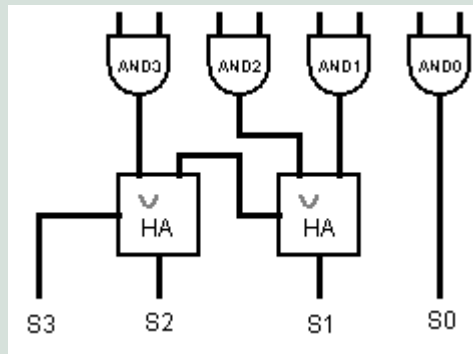
If two n-bit numbers are multiplied then the output will be less than or equals to 2n bits.

Features of the multiplication scheme:

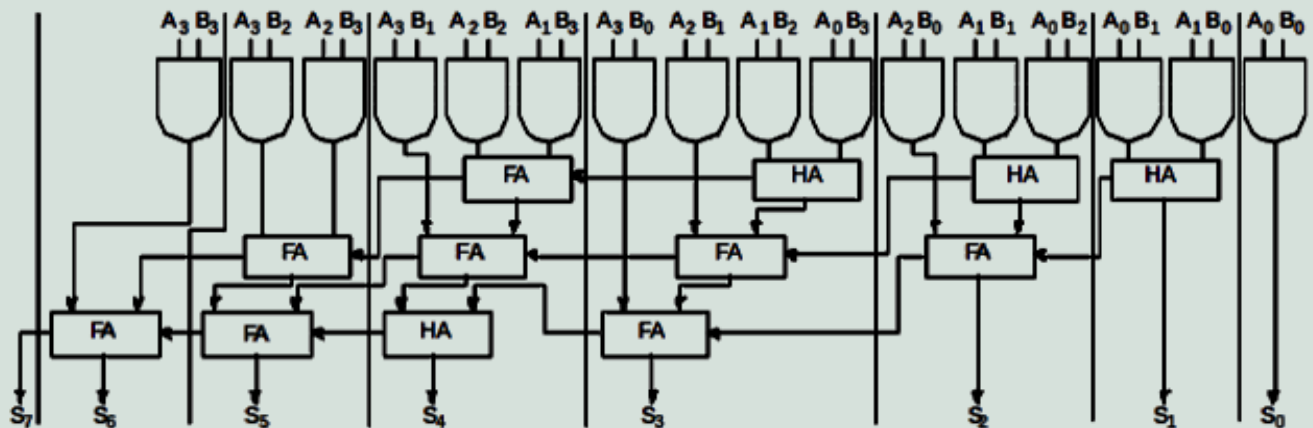
- It can be designed by unrolling the multiplier loop.
- Instead of handling the carry out of partial product summation bit, the carry out can be sent to the next bit of the next step.
- This scheme of handling the carry is called carry save addition.
- This scheme is more regular and modular.

### Circuit Diagram:

**Case 1:** multiplication of two 2-bit numbers



**Case 2:** multiplication of two 4-bit numbers



### Components:

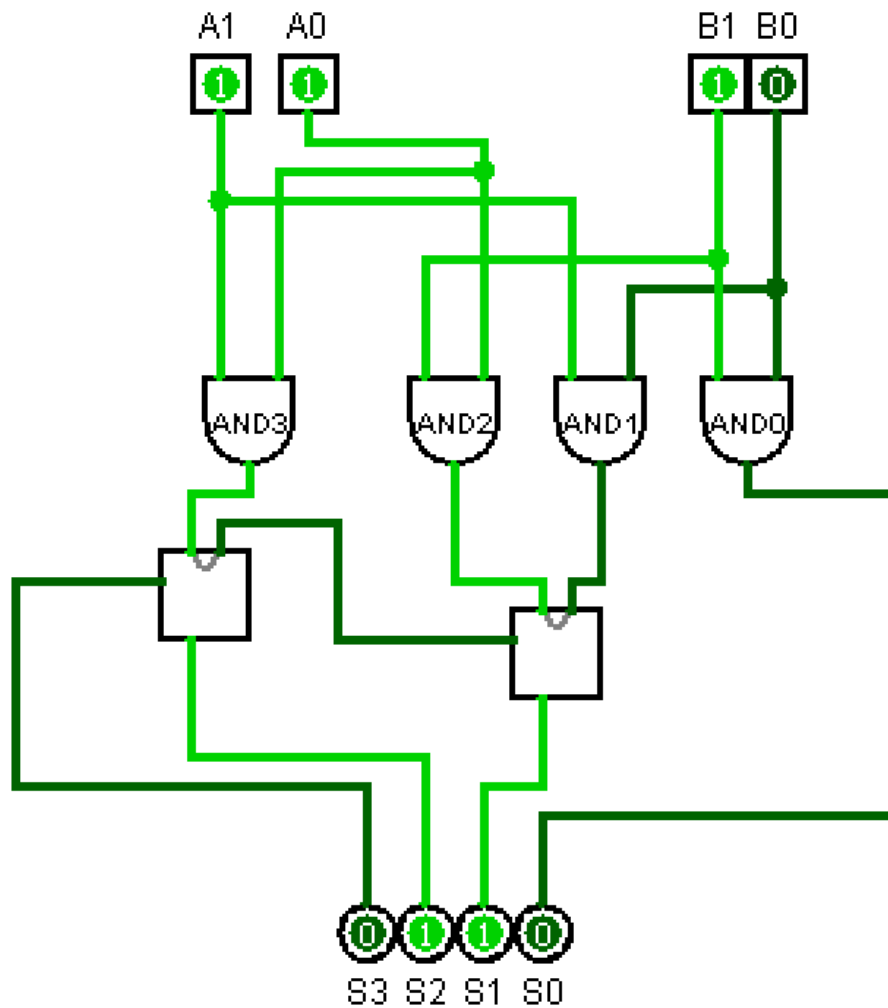
1. AND gate

2. Half Adder
3. Full Adder

**Result:** show steps for each case.

**LABWORK:** add extra pages

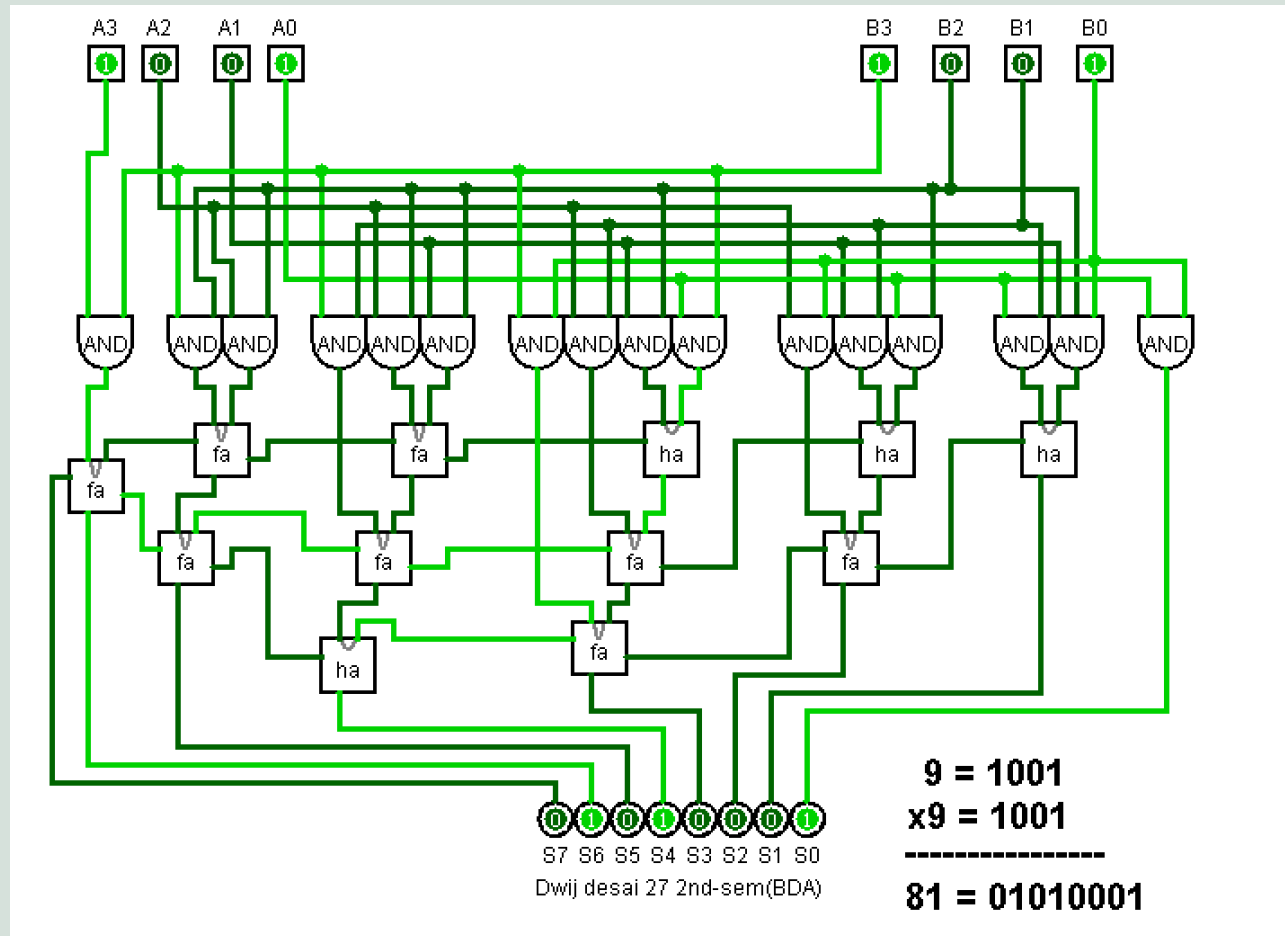
1. multiplication of two 2-bit numbers



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$$3 * 2 = 6$$

## 2. multiplication of two 4-bit numbers



### CONCLUSION:

In conclusion, combinational multipliers provide a fundamental understanding of how binary multiplication can be implemented in digital circuits. Their simplicity makes them valuable for educational purposes and small-scale applications. However, for larger scale and performance-critical applications, exploring alternative multiplier architectures is often necessary.