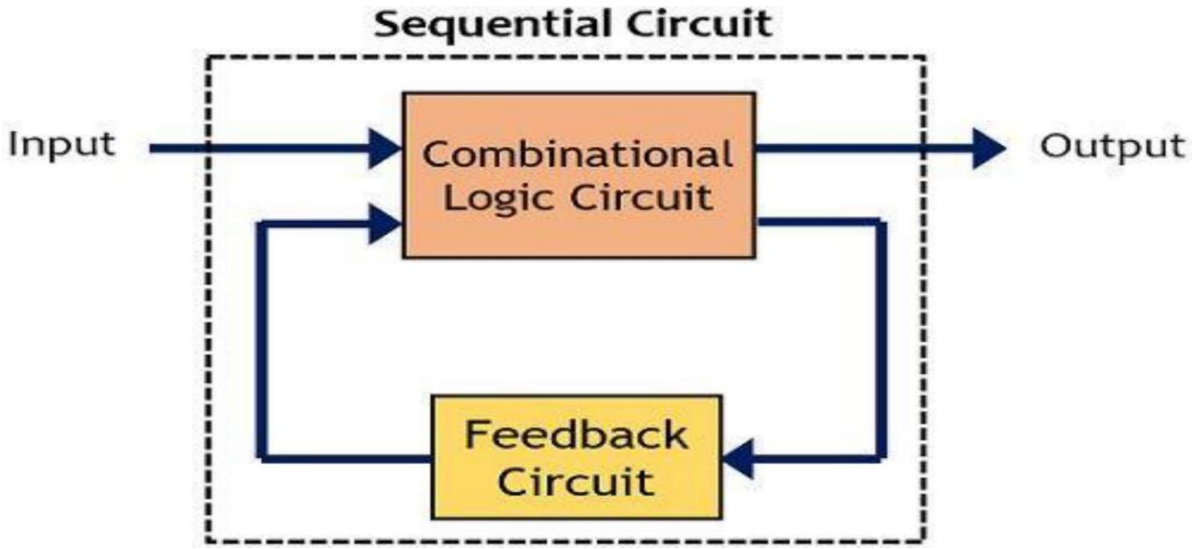
EXPERIMENT NO:-10

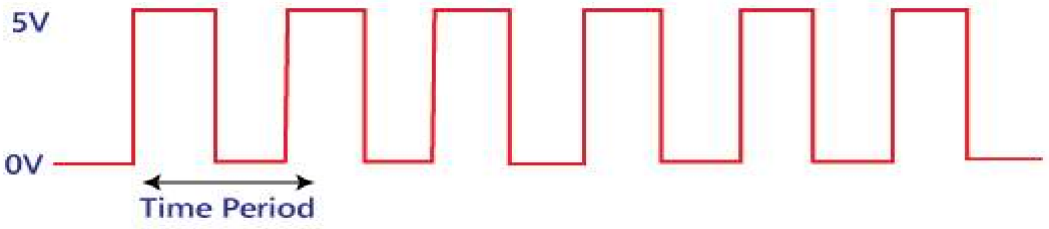
- **AIM:** To study and test Flip-Flop circuits.(SR, D, T , JK FFs)
- **APPARATUS :** Multisim/ Logisim software, Trainer kits

The sequential circuit is a special type of circuit that has a series of inputs and outputs. The outputs of the sequential circuits depend on both the combination of present inputs and previous outputs. The previous output is treated as the present state. So, the sequential circuit contains the combinational circuit and its memory storage elements.



Clock signal

A clock signal is a periodic signal in which ON time and OFF time need not be the same. When ON time and OFF time of the clock signal are the same, a square wave is used to represent the clock signal. Below is a diagram which represents the clock signal:

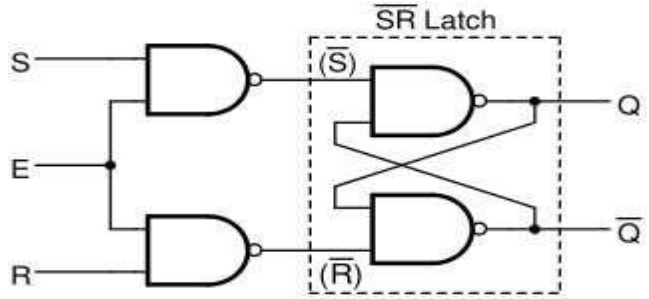


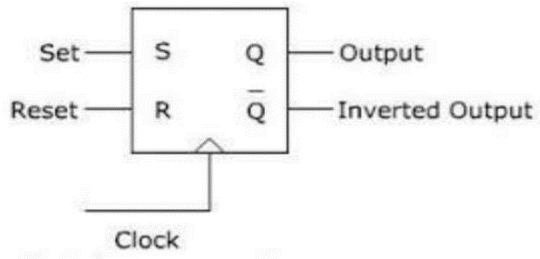
Basics of Flip Flop

A circuit that has two stable states is treated as a flip flop. These stable states are used to store binary data that can be changed by applying varying inputs. The flip flops are the fundamental building blocks of the digital system. Flip flops and latches are examples of data storage elements. In the sequential logical circuit, the flip flop is the basic storage element. The latches and flip flops are the basic storage elements but different in working.

SR flip flop:

The SR flip flop is a 1-bit memory bistable device having two inputs, i.e., SET and RESET. The SET input 'S' set the device or produce the output 1, and the RESET input 'R' reset the device or produce the output 0. The SET and RESET inputs are labeled as **S** and **R**, respectively. The SR flip flop stands for "Set-Reset" flip flop. The reset input is used to get back the flip flop to its original state from the current state with an output 'Q'. This output depends on the set and reset conditions, which is either at the logic level "0" or "1".

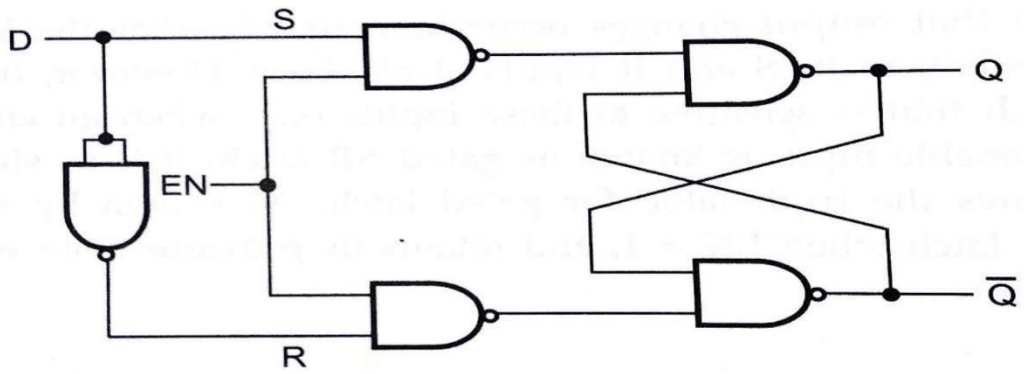




Serial No.	clock	S	R	Q(n-1)	$\overline{Q}$(n-1)	Q	$\overline{Q}$	Remark
1	0	0	0	X	X	0	1	No Change
2	1	0	0	0	1	0	1	No change
3	1	1	0	0	1	1	0	set
4	1	0	1	1	0	0	1	Reset
5	1	1	1	0	1	0	0	INVALID

D- FF:

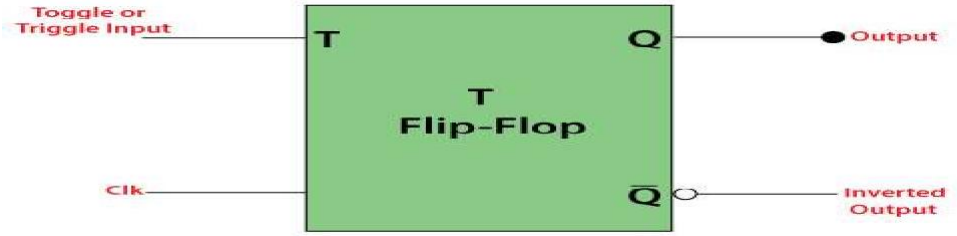
D flip flop is an electronic devices that is known as "delay flip flop" or "data flip flop" which is used to store single bit of data. D flip flops are synchronous or asynchronous. The clock single required for the synchronous version of D flip flops but not for the asynchronous one. The D flip flop has two inputs, data and clock input which controls the flip flop. When clock input is high, the data is transferred to the output of the flip flop and when the clock input is low, the output of the flip flop is held in its previous state.

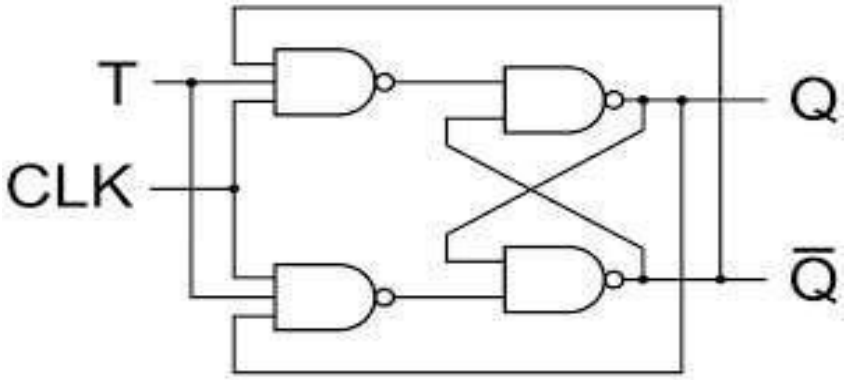


Serial No.	clock	D	Q(n-1)	Q'(n-1)	Q	Q'	Remark
1	0	0	X	X	0	1	No Change
2	0	1	0	1	0	1	No change
3	1	0	0	1	0	1	Reset
4	1	1	0	1	1	0	set

T-Flip Flop:

In T flip flop, "T" defines the term "Toggle". In SR Flip Flop, we provide only a single input called "Toggle" or "Trigger" input to avoid an intermediate state occurrence. Now, this flip-flop work as a Toggle switch. The next output state is changed with the complement of the present state output. This process is known as "Toggling"'. We can construct the "T Flip Flop" by making changes in the "JK Flip Flop". The "T Flip Flop" has only one input, which is constructed by connecting the input of JK flip flop. This single input is called T. In simple words, we can construct the "T Flip Flop" by converting a "JK Flip Flop". Sometimes the "T Flip Flop" is referred to as single input "JK Flip Flop".





Serial No.	Clock	T	Q_{n-1}	$\bar{Q}_{n-1}$	Q	$\bar{Q}$	Remarks
1	0	0	X	X	0	1	No Change
2	1	0	0	1	0	1	No change
3	0	1	0	1	0	1	No Change
4	1	1	0	1	1	0	Toggle

J-K Flip Flop:

The SR Flip Flop or Set-Reset flip flop has lots of advantages. But, it has the following switching problems:

When Set 'S' and Reset 'R' inputs are set to 0, this condition is always avoided.

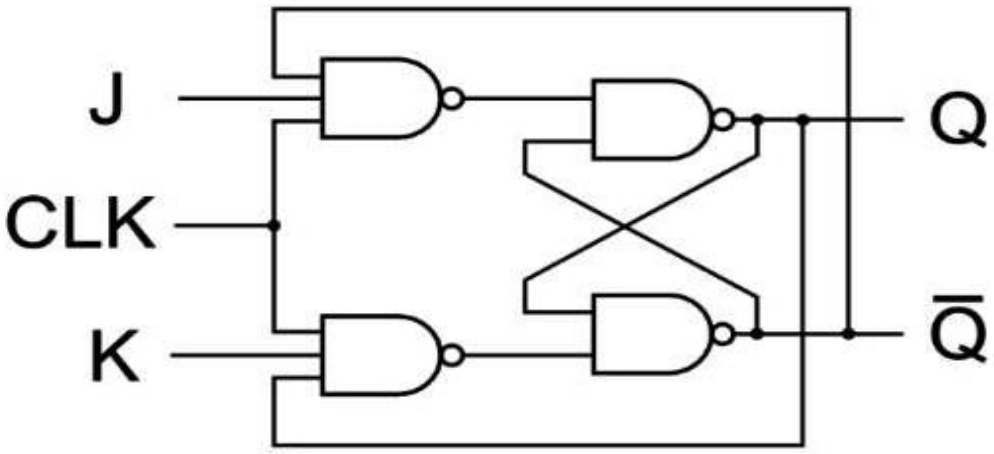
When the Set or Reset input changes their state while the enable input is 1, the incorrect latching action occurs.

The JK Flip Flop removes these two drawbacks of SR Flip Flop.

The JK flip flop is one of the most used flip flops in digital circuits. The JK flip flop is a universal flip flop having two inputs 'J' and 'K'. In SR flip flop, the 'S' and 'R' are the shortened abbreviated letters for Set and Reset, but J and K are not. The J and K are themselves autonomous letters which are chosen to distinguish the flip flop design from other types.

The JK flip flop work in the same way as the SR flip flop work. The JK flip flop has 'J' and 'K' flip flop instead of 'S' and 'R'. The only difference between JK flip flop and SR flip flop is that when both inputs of SR flip flop is set to 1, the circuit produces the invalid states as outputs, but in case of JK flip flop, there are no invalid states even if both 'J' and 'K' flip flops are set to 1.

J-K Type



Serial No.	clock	J	K	Q(n-1)	$\bar{Q}$(n-1)	Q	$\bar{Q}$	Remark
1	0	0	0	X	X	0	1	No Change
2	1	0	0	0	1	0	1	No change
3	1	0	1	0	1	0	1	Reset
4	1	1	0	0	1	1	0	set
5	1	1	1	1	0	0	1	toggle

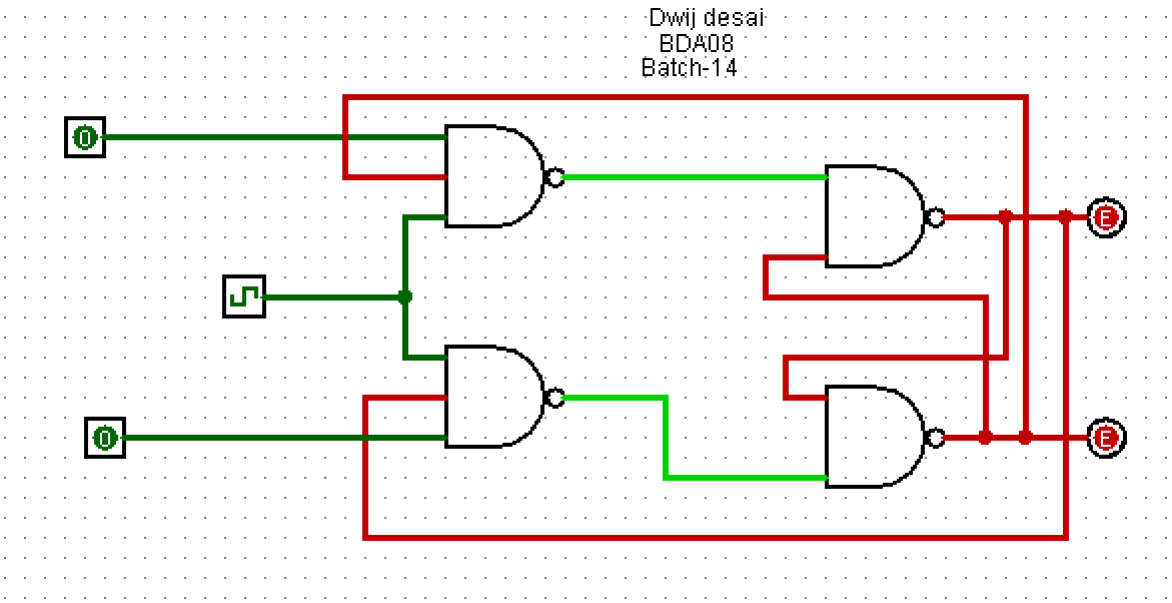
- **PROCEDURE:**

1. Connect the circuit on the bread board using ICs or if there is a kit ready, then connect the circuit as per the given instructions in kit's manual.
2. Switch ON the power supply.
3. Test the truth table of each flip-flop circuit and verify it.

- **CONCLUSION: Designing for flip flop circuit is crusial part of DE to understand Clock ‘s And RAM { How to store information }**

- **Exercise:**

Q. Design and show function of J-K master slave FF using NAND only gates.

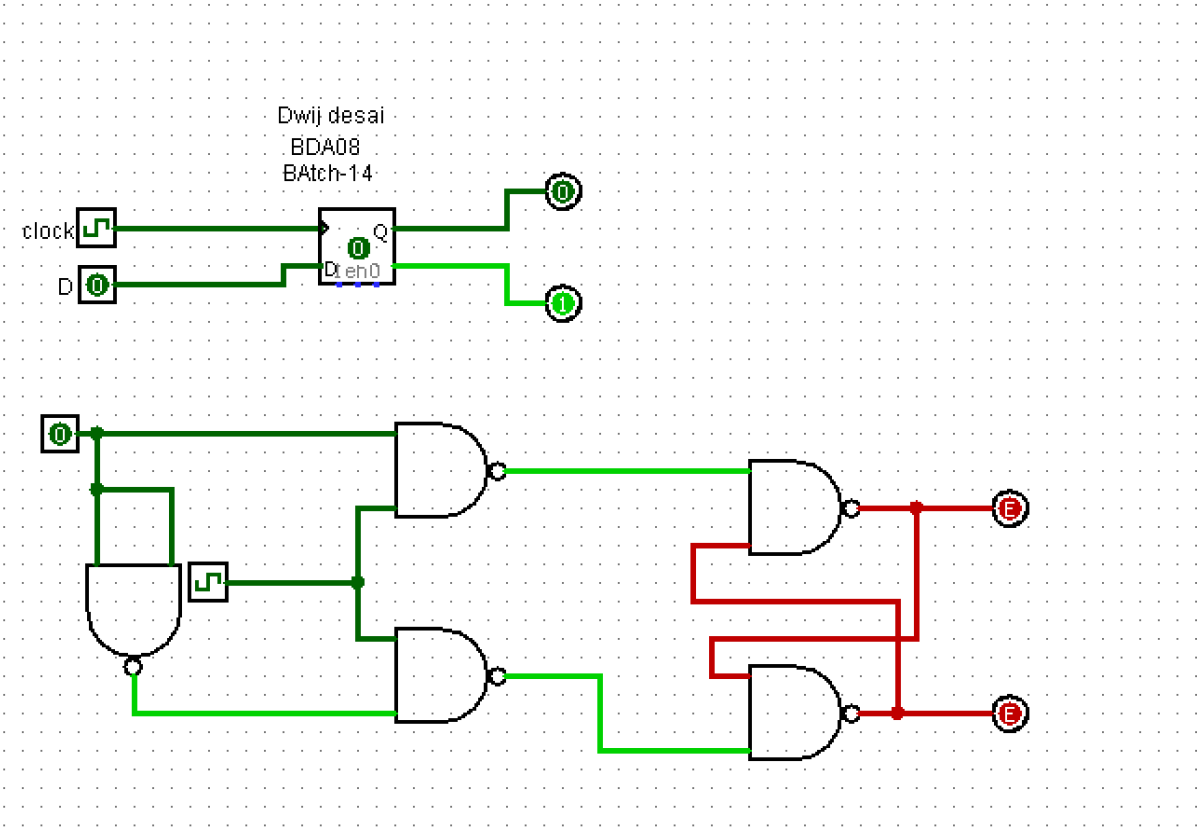


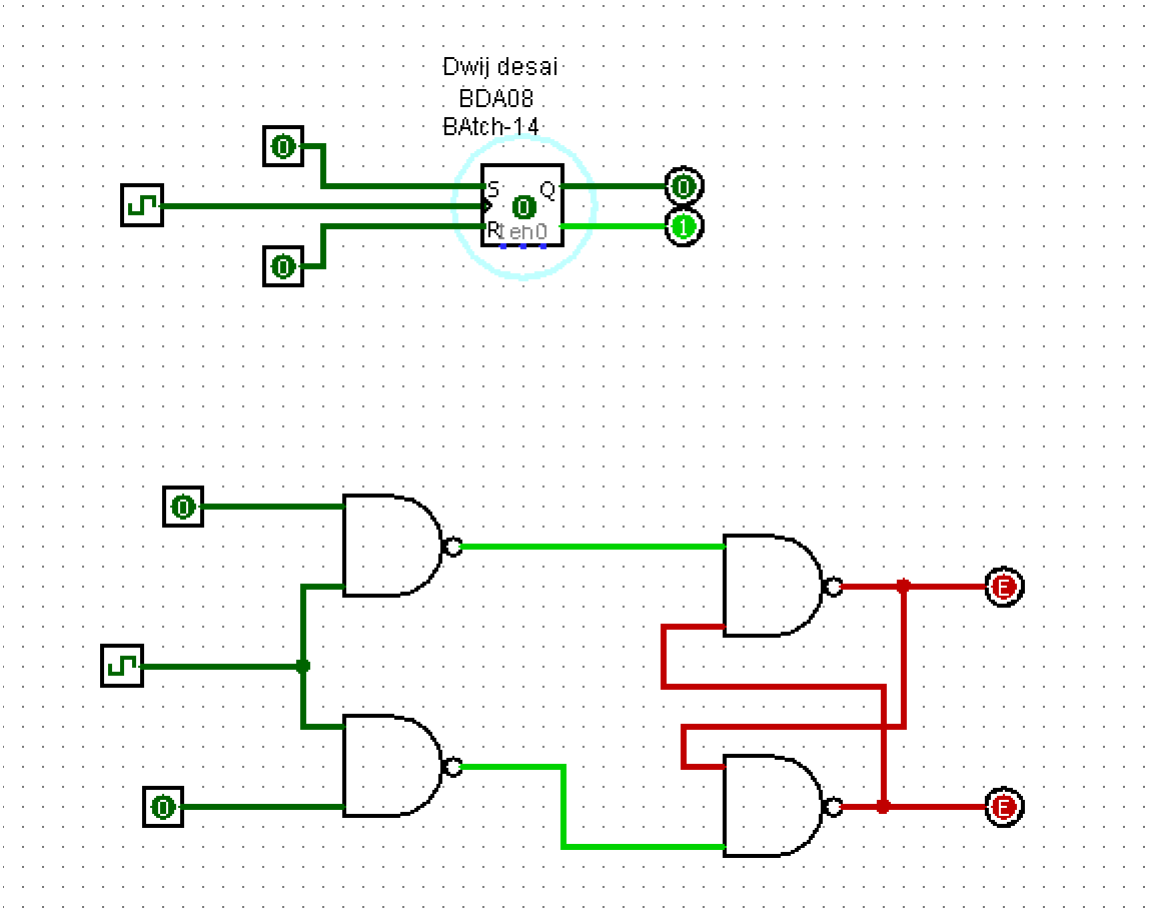
Q. Why we use J-K master-slave?

To avoid the problem of race around condition in JK flip flop, we use the JK flip flop in the Master and Slave Mode. Hence, the JK flip flop is called Master-Slave Flip Flop.

Race Around Condition In JK Flip-flop – For J-K flip-flop, if J=K=1, and if clk=1 for a long period of time, then Q output will toggle as long as CLK is high, which makes the output of the flip-flop unstable or uncertain. This problem is called race around condition in J-K flip-flop.

Q. Make D FF using SR FF.

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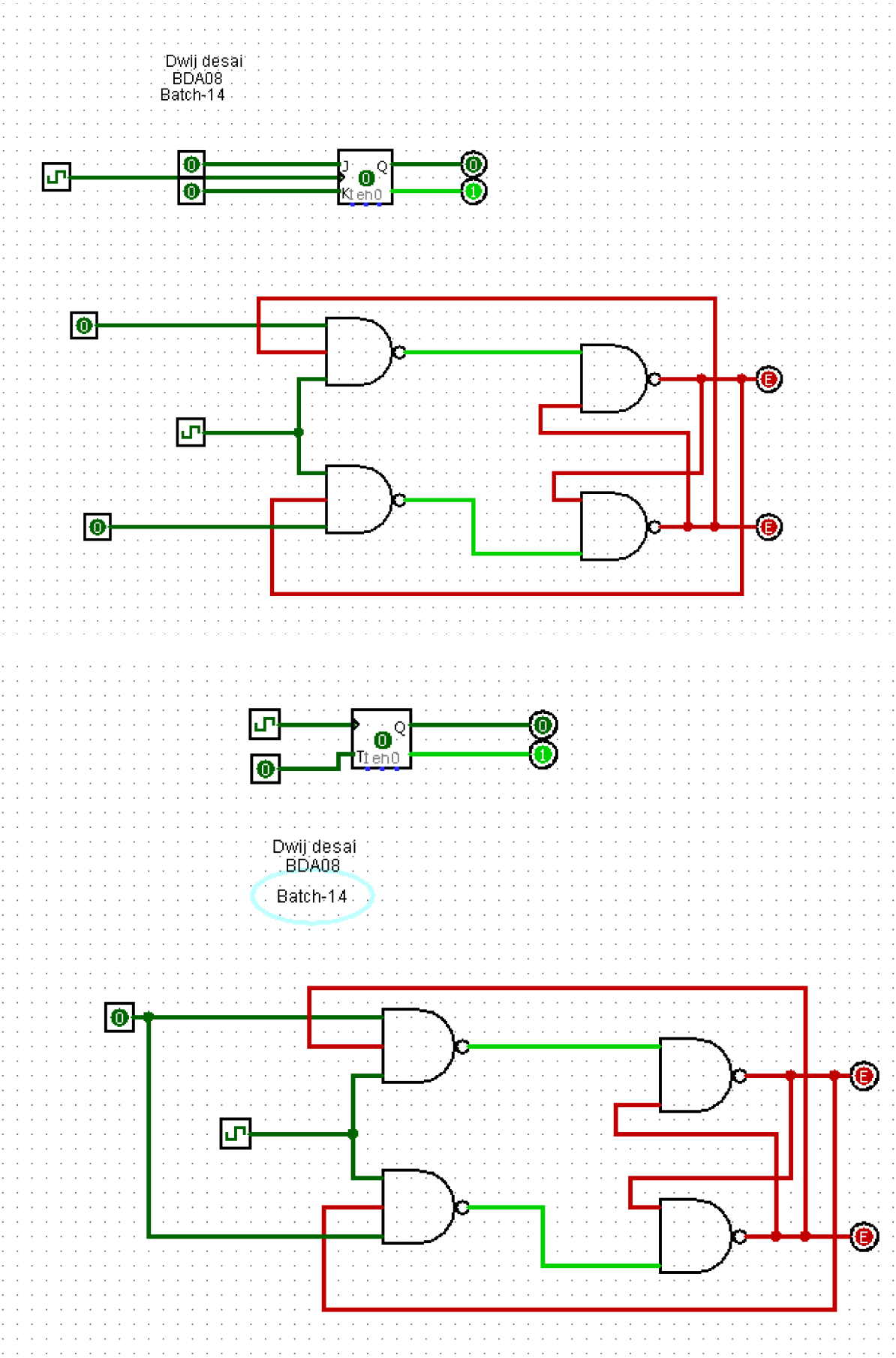
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