EXPERIMENT NO:-4

➢ **AIM:** To design and test Half / Full adder and Subtractor circuits.

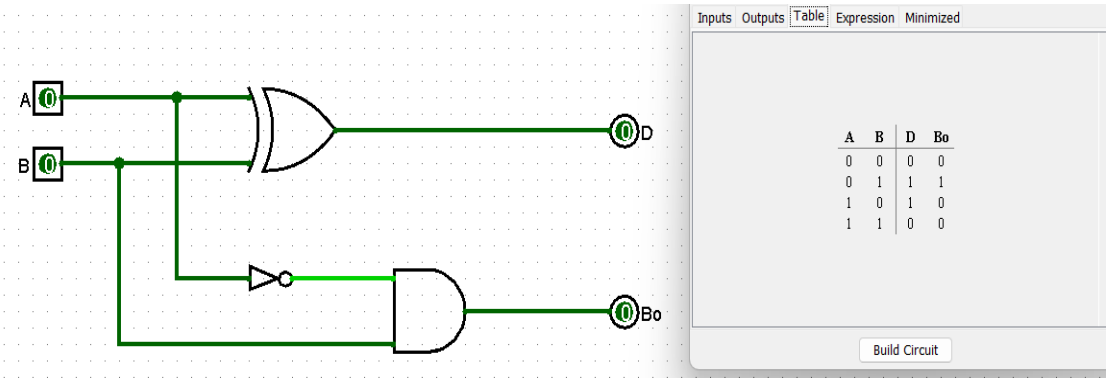
➢ **APPARATUS**: Logisim simulator.

➢ **THEORY:**

Digital computers perform variety of information processing task. Among the basic functions encountered are the various types of arithmetic operations. Here we will see how these operations can be performed using digital hardware.

➢ **(1)Half subtractor:** This Subtractor subtracts one bit from another but ignores any borrow from the previous stage. The outputs of the half adder are DIFFERENCE and BORROW. Truth table and expression for difference and borrow are given below.

CIRCUIT DIAGRAM FOR HALF SUBSTRACTOR:



TRUTH TABLE:

HALF SUBSTRACTOR

A	B	D	Bo
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

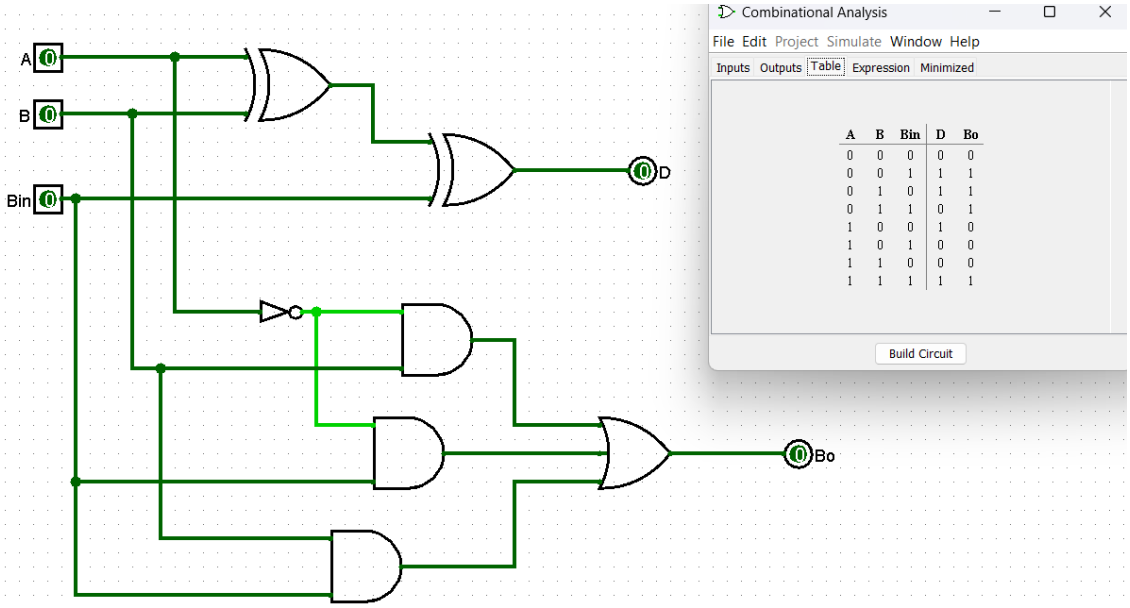
Expression for Difference and Borrow Out:

$D = A(+)B$

Bo = A`.B

➢ **(2)Full Subtractor:** This Subtractor subtracts binary digits along with borrow from the previous stage. The outputs of the Subtractor are difference and borrow out.

CRCUIT DIAGRAM OF FULL SUBTRACTOR:



Expression for Difference and Borrow Out:

D = [A(+)B](+)Bin

Bo = A`.Bin + B.Bin + A`.B

TRUTH TABLE:

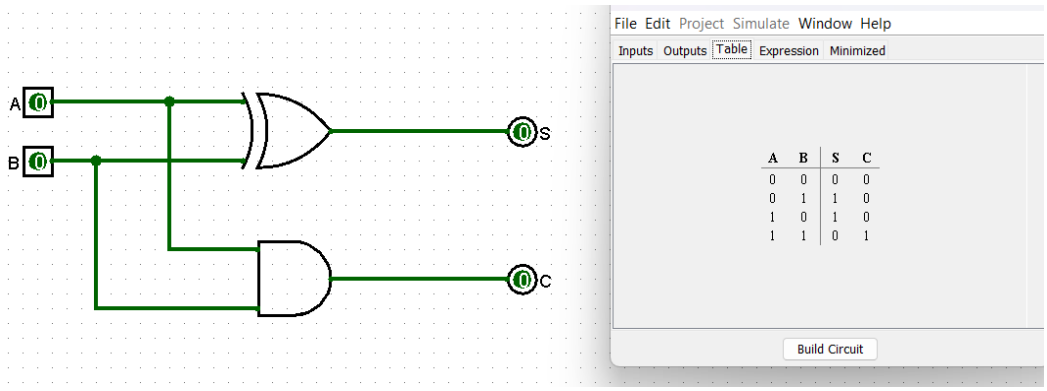
FULL SUTRACTOR

A	B	Bin	D	Bo
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0

1	1	0	0	0
1	1	1	1	1

➢ **(3)Half adder:** The adder adds only two bits and carries from the previous stage will not be added. The outputs of the adder and are SUM and CARRY. Truth table of half adder is given below.

CIRCUIT DIAGRAM OF HALF ADDER:



TRUTH TABLE:

HALF ADDER

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

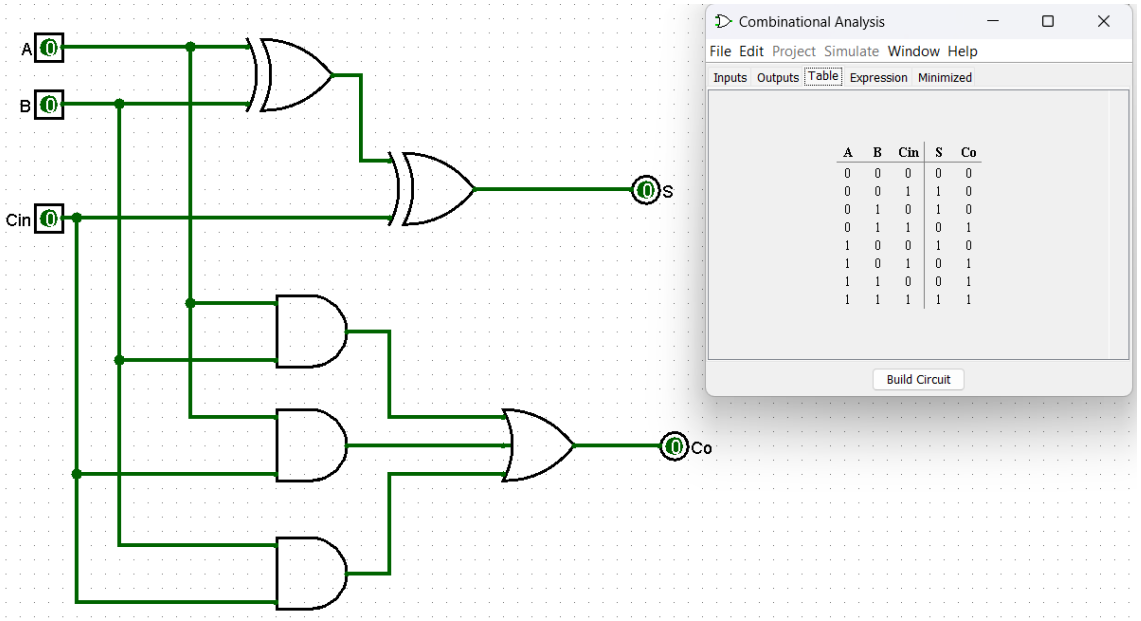
Expression for Sum and Carry Out:

S = A(+)B

C = AB

➢ **(4)Full adder:** This adder adds two bits and carries from the previous stage. The outputs of the adder are SUM and CARRY. Truth table and simplified expression for sum and carry are given below.

CIRCUIT DIAGRAM OF FULL ADDER:



Expression for Sum and Carry Out:

S = [A(+)B](+)Cin

Cout = A.B + A.Cin + B.Cin

TRUTH TABLE:

FULL ADDER

A	B	Cin	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1