Page 881 Exercises 4.1, 4.3, 4.4, 4.7

4.1 Consider the following instruction:

Instruction: and rd, rsl, rs2 Interpretation: Reg[rd] = Reg[rs1] AND Reg[rs2]

4.1.1 [5] <§4.3> What are the values of control signals generated by the control in Figure 4.10 for this instruction?

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RegWrite = 1
MemRead , ALUMux, MemWrite, Branch = 0
ALUOp = Add
RegMux = 1
```

4.1.2 [5] <§4.3> Which resources (blocks) perform a useful function for this instruction?

```
All resources performed a useful function except branch add,

and data memory.
```

4.1.3 [10] <§4.3> Which resources (blocks) produce no output for this instruction? Which resources produce output that is not used?

```
Branch, Add output is not used.
Data Memory has no output.
```

4.3 Consider the following instruction mix:

4.3.1 [5] <§4.4> What fraction of all instructions use data memory?

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35%
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4.3.2 [5] <§4.4> What fraction of all instructions use instruction memory?

24%+28% = 52%

4.3.3 [5] <§4.4> What fraction of all instructions use the sign extend?

-- I-type + load + store + branch jump
= 28% + 25% +10% + 11% + 2%

= 76%

4.3.4 [5] <§4.4> What is the sign extend doing during cycles in which its output is not needed ?

the sign extend is computed every cycle for the aforementioned 76% of the instructions.

4.4 When silicon chips are fabricated, defects in materials (e.g., silicon) and manufacturing errors can result in defective circuits. A very common defect is for one signal wire to get "broken" and always register a logical 0. This is often called a "stuck-at-0" fault.

4.4.1 [5] <§4.4> Which instructions fail to operate correctly if the MemToReg wire is stuck at 0?

Load and Store instructions.

4.4.2 [5] <§4.4> Which instructions fail to operate correctly if the ALUSrc wire is stuck at 0?

add and subtract instructions.

4.7 Problems in this exercise assume that the logic blocks used to implement a processor's data path have the following latencies:

I-Mem / D-Mem	Register File	Mux	ALU	Adder	Singlegate	Register Read	Register Setup	Sign extend	Control
250ps	150ps	25ps	200ps	150ps	5ps	30ps	20ps	50ps	50ps

"Register read" is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only. "Register setup" is the amount of time a register's data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.

4.7.1 [5] <§4.4> What is the latency of an R-type instruction (i.e.,ho w long must the clock period be to ensure that this instruction works correctly)?

Latency of R-type instruction = 30+250+150+25+200+25+20= 700

4.7.2 [10] <§4.4> What is the latency of lw? (Check your answer carefully. Many students place extra muxes on the critical path.)

30+ 250+ 150+ 25+ 200+ 250+ 25+ 20 = 950

4.7.3 [10] <§4.4> What is the latency of sw? (Check your answer carefully. Many students place extra muxes on the critical path.)

30+ 250+ 150+ 200+ 25+ 250 = 905

4.7.4 [5] <§4.4> What is the latency of beq?

30+ 250+ 150+ 25+ 200+ 5+ 25+ 20 = 705

4.7.5 [5] <§4.4> What is the latency of an arithmetic, logical, or shift I-type (non-load) instruction?

30+ 250+ 150+ 25+ 200+ 25+ 20 = 700

4.7.6 [5] <§4.4> What is the minimum clock period for this CPU?

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