Design Rule Verification Report

Date:	3/13/2022		
Time:	11:49:31 PM	**Warnings:**	0
Elapsed Time:	00:00:01	**Rule Violations:**	0
Filename:	W:\ECE295\ECE295Repo\ECE295\M2\D2.PcbDoc		

Summary

Warnings	**Count**
Total	**0**

Rule Violations	**Count**
Clearance Constraint (Gap=10mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=10mil) (Max=200mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4) (All)	0
Hole Size Constraint (Min=12mil) (Max=900mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=1mil) (All),(All)	0
Silk To Solder Mask (Clearance=1mil) (IsPad),(All)	0
Silk to Silk (Clearance=0mil) (All),(All)	0
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0

Total 0