# 2Gb D-die Mobile DDR SDRAM

## 8x13, 90FBGA, 64M x32
## VDD / VDDQ = 1.8V / 1.8V

datasheet

# Revision History

| Revision No. | History | Draft Date | Remark | Editor |
|---|---|---|---|---|
| 0.0 | - First version for target specification. | Sep. 20, 2011 | Target | J.Y.Bae |
| 0.5 | - Preliminary datasheet. | Dec. 15, 2011 | Preliminary | J.Y.Bae |
| 0.9 | - | Dec. 25, 2011 | Preliminary | J.Y.Bae |
| 1.0 | - Final datasheet.<br>- Revised DC characteristics.<br>1. IDD0 : 70 -> 60 [mA]<br>2. IDD2N : 8 -> 6 [mA]<br>3. IDD3N : 15 -> 12 [mA]<br>4. IDD4R : 100 -> 85 [mA]<br>5. IDD4W : 80 -> 65 [mA]<br>6. IDD5 : 160 -> 150 [mA] | Jan. 31, 2012 | Final | J.Y.Bae |

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## 2Gb D-die Mobile DDR SDRAM

***64Mx32 Mobile DDR SDRAM in 90FBGA 8x13***

# 1.0 FEATURES

• VDD/VDDQ = 1.8V/1.8V
• Double-data-rate architecture; two data transfers per clock cycle.
• Bidirectional data strobe (DQS).
• Four banks operation.
• Differential clock inputs (CK and $\overline{CK}$).
• MRS cycle with address key programs.
  - CAS Latency (2, 3)
  - Burst Length (2, 4, 8, 16)
  - Burst Type (Sequential & Interleave)
• EMRS cycle with address key programs.
  - Partial Array Self Refresh (Full, 1/2, 1/4 Array)
  - Output Driver Strength Control (Full, 1/2, 1/4, 1/8, 3/4, 3/8, 5/8, 7/8)
• Internal Temperature Compensated Self Refresh.
• All inputs except data & DM are sampled at the positive going edge of the system clock (CK).
• Data I/O transactions on both edges of data strobe, DM for masking.
• Edge aligned data output, center aligned data input.
• No DLL; CK to DQS is not synchronized.
• DM for write masking only.
• Auto refresh duty cycle.
  - 7.8us for -25 to 85 °C
• Clock stop capability.

# 2.0 OPERATING FREQUENCY

| | DDR400 |
|---|---|
| Speed @ CL2 1) | 83Mhz |
| Speed @ CL3 1) | 200Mhz |

**NOTE:**
1) CAS Latency

# 3.0 ADDRESS CONFIGURATION

| Organization | Bank Address | Row Address | Column Address |
|---|---|---|---|
| 64M x 32 | BA0, BA1 | A0 - A13 | A0 - A9 |

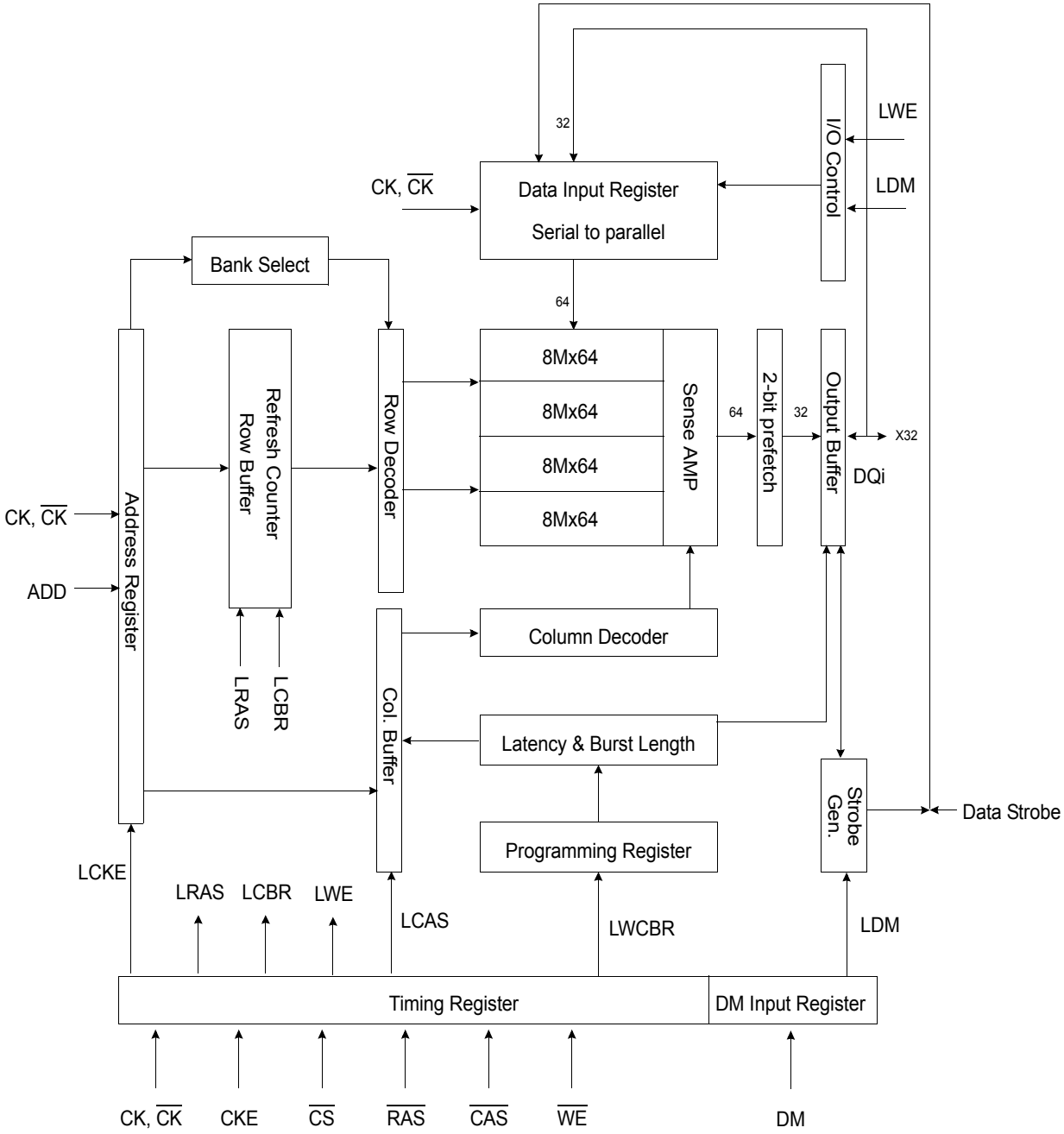
- DM is internally loaded to match DQ and DQS identically.

# 4.0 ORDERING INFORMATION

| Part No. | Max Freq. | Interface | Package |
|---|---|---|---|
| K4X2G323PD-8GD8 | 200MHz(CL=3,$t_{RCD}$=3,$t_{RP}$=3),83MHz(CL=2) | LVCMOS | 90FBGA 8x13 |

- K4X2G323PD-**8***GD8 : 90FBGA (Pb Free, Halogen Free)
- K4X2G323PD-8**G***D8 : Low Power, Extended Temperature (-25 °C ~ 85 °C)
- K4X2G323PD-8G**D8*** : 200MHz (CL=3)

# 5.0 FUNCTIONAL BLOCK DIAGRAM



# 6.0 PACKAGE INFORMATION

## 6.1 Package Ballout

| 90Ball(6x15) FBGA | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| A | VSS | DQ31 | VSSQ | | | | VDDQ | DQ16 | VDD |
| B | VDDQ | DQ29 | DQ30 | | | | DQ17 | DQ18 | VSSQ |
| C | VSSQ | DQ27 | DQ28 | | | | DQ19 | DQ20 | VDDQ |
| D | VDDQ | DQ25 | DQ26 | | | | DQ21 | DQ22 | VSSQ |
| E | VSSQ | DQS3 | DQ24 | | | | DQ23 | DQS2 | VDDQ |
| F | VDD | DM3 | NC | | | | A13 | DM2 | VSS |
| G | CKE | CK | $\overline{CK}$ | | | | $\overline{WE}$ | $\overline{CAS}$ | $\overline{RAS}$ |
| H | A9 | A11 | A12 | | | | $\overline{CS}$ | BA0 | BA1 |
| J | A6 | A7 | A8 | | | | A10 | A0 | A1 |
| K | A4 | DM1 | A5 | | | | A2 | DM0 | A3 |
| L | VSSQ | DQS1 | DQ8 | | | | DQ7 | DQS0 | VDDQ |
| M | VDDQ | DQ9 | DQ10 | | | | DQ5 | DQ6 | VSSQ |
| N | VSSQ | DQ11 | DQ12 | | | | DQ3 | DQ4 | VDDQ |
| P | VDDQ | DQ13 | DQ14 | | | | DQ1 | DQ2 | VSSQ |
| R | VSS | DQ15 | VSSQ | | | | VDDQ | DQ0 | VDD |

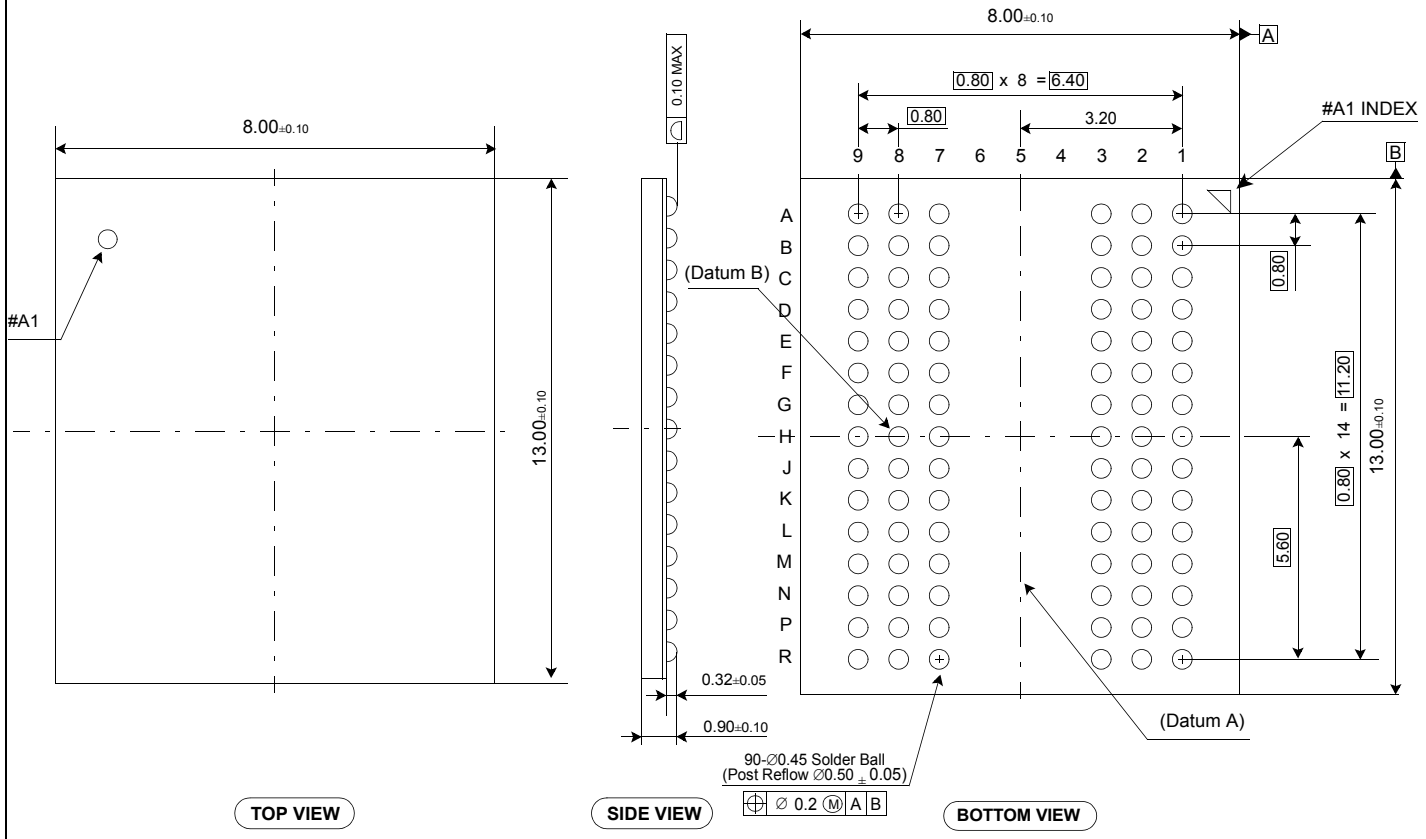
**[Top View]**

| | |
|---|---|
| | Power |
| | Ground |
| | NC |

# 6.2 Package Dimension

**90-Ball Fine pitch Ball Grid Array Package (measured in millimeters)**

Units:millimeters



## 6.3 Input/Output Function Description

| Symbol | Type | Description |
|---|---|---|
| CK, $\overline{CK}$ | Input | Clock : CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Internal clock signals are derived from CK / $\overline{CK}$. |
| CKE | Input | Clock Enable : CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER-DOWN (row ACTIVE in any banks). CKE is synchronous for all functions except for disabling outputs, which is achieved asynchronously. Input buffers, excluding CK, $\overline{CK}$ and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption. |
| $\overline{CS}$ | Input | Chip Select : $\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder.<br>All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code. |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Input | Command Inputs : $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered. |
| DM0,DM1,<br>DM2,DM3 | Input | Input Data Mask : DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. DM pins include dummy loading internally, to match the DQ and DQS loading. For the x32, DM0 corresponds to the data on DQ0-DQ7; DM1 corresponds to the data on DQ8-DQ15, DM2 corresponds to the data on DQ16-DQ23, DM3 corresponds to the data on DQ24-DQ31 |
| BA0, BA1 | Input | Bank Address Inputs : BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. |
| A [n : 0] | Input | Address Inputs : Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the opcode during a MODE REGISTER SET command. BA0 and BA1 determines which mode register (mode register or extended mode register) is loaded during the MODE REGISTER SET command. |
| DQ | I/O | Data Inputs/Outputs : Data bus |
| DQS0,DQS1,<br>DQS2,DQS3 | I/O | Data Strobes : Output with read data, input with write data. Edge-aligned with read data, centered in write data. it is used to fetch write data. For the x32, DQS0 corresponds to the data on DQ0-DQ7; DQS1 corresponds to the data on DQ8-DQ15,DQS2 corresponds to the data on DQ16-DQ23, DQS3 corresponds to the data on DQ24-DQ31 |
| NC | - | No Connect : No internal electrical connection is present. |
| VDDQ | Supply | DQ Power Supply : 1.7V to 1.95V |
| VSSQ | Supply | DQ Ground. |
| VDD | Supply | Power Supply : 1.7V to 1.95V |
| VSS | Supply | Ground. |

# 7.0 FUNCTIONAL DESCRIPTION

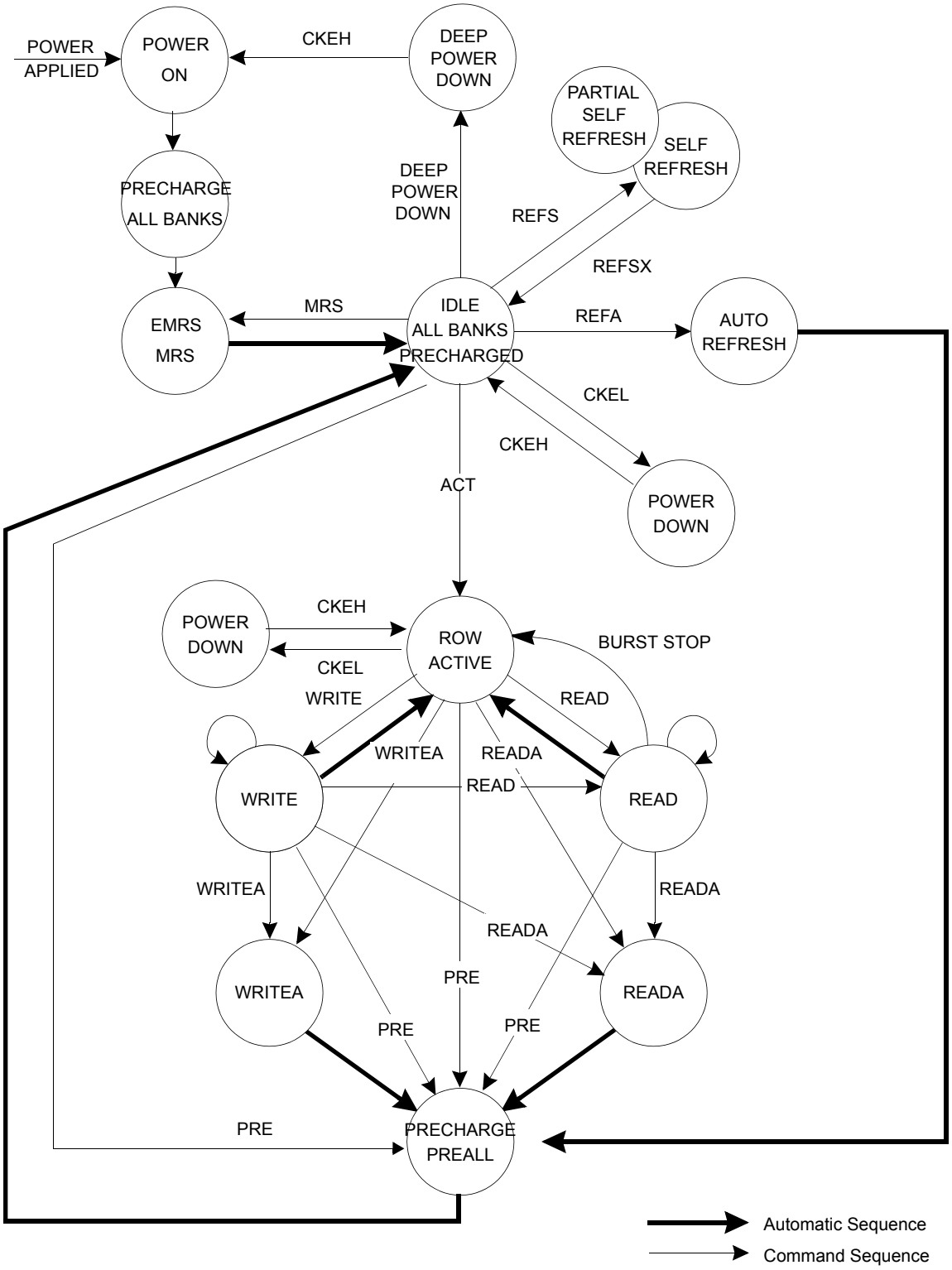
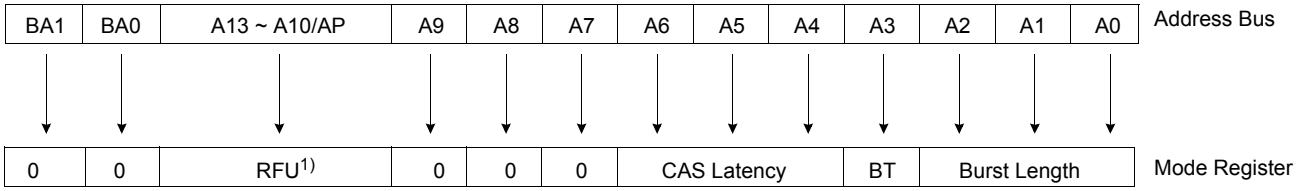



**Figure 1. State diagram**

# 8.0 MODE REGISTER DEFINITION

## 8.1 Mode Register Set (MRS)

The mode register is designed to support the various operating modes of Mobile DDR SDRAM. It includes Cas latency, addressing mode, burst length, test mode and vendor specific options to make Mobile DDR SDRAM useful for variety of applications. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The Mobile DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The states of address pins A0 ~ A13 and BA0, BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low are written in the mode register. Two clock cycles are required to complete the write operation in the mode register. Even if the power-up sequence is finished and some read or write operation is executed afterward, the mode register contents can be changed with the same command and two clock cycles. This command must be issued only when all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0 ~ A2, addressing mode uses A3, Cas latency (read latency from column address) uses A4 ~ A6, A7 ~ A13 is used for test mode. BA0 and BA1 must be set to low for proper MRS operation.




| $A_3$ | Burst Type |
|---|---|
| 0 | Sequential |
| 1 | Interleave |

| A6 | A5 | A4 | CAS Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

| $A_2$ | $A_1$ | $A_0$ | Burst Type |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | 2 |
| 0 | 1 | 0 | 4 |
| 0 | 1 | 1 | 8 |
| 1 | 0 | 0 | 16 |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

**Figure 2. Mode Register Set**

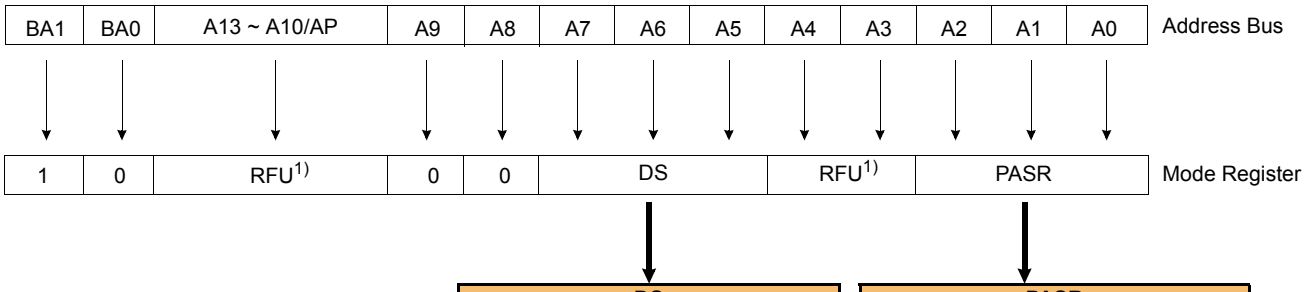
**NOTE** :
1) RFU (Reserved for future use) should stay "0" during MRS cycle

**[Table 1] Burst address ordering for burst length**

| Burst Length | Starting Address (A3, A2, A1, A0) | Sequential Mode | Interleave Mode |
|---|---|---|---|
| 2 | xxx0 | 0, 1 | 0, 1 |
| | xxx1 | 1, 0 | 1, 0 |
| 4 | xx00 | 0, 1, 2, 3 | 0, 1, 2, 3 |
| | xx01 | 1, 2, 3, 0 | 1, 0, 3, 2 |
| | xx10 | 2, 3, 0, 1 | 2, 3, 0, 1 |
| | xx11 | 3, 0, 1, 2 | 3, 2, 1, 0 |
| 8 | x000 | 0, 1, 2, 3, 4, 5, 6, 7 | 0, 1, 2, 3, 4, 5, 6, 7 |
| | x001 | 1, 2, 3, 4, 5, 6, 7, 0 | 1, 0, 3, 2, 5, 4, 7, 6 |
| | x010 | 2, 3, 4, 5, 6, 7, 0, 1 | 2, 3, 0, 1, 6, 7, 4, 5 |
| | x011 | 3, 4, 5, 6, 7, 0, 1, 2 | 3, 2, 1, 0, 7, 6, 5, 4 |
| | x100 | 4, 5, 6, 7, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3 |
| | x101 | 5, 6, 7, 0, 1, 2, 3, 4 | 5, 4, 7, 6, 1, 0, 3, 2 |
| | x110 | 6, 7, 0, 1, 2, 3, 4, 5 | 6, 7, 4, 5, 2, 3, 0, 1 |
| | x111 | 7, 0, 1, 2, 3, 4, 5, 6 | 7, 6, 5, 4, 3, 2, 1, 0 |
| 16 | 0000 | 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15 | 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15 |
| | 0001 | 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0 | 1, 0, 3, 2, 5, 4, 7, 6, 9, 8, 11,10,13,12,15,14 |
| | 0010 | 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1 | 2, 3, 0, 1, 6, 7, 4, 5,10,11, 8, 9, 14,15,12,13 |
| | 0011 | 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2 | 3, 2, 1, 0, 7, 6, 5, 4,11,10, 9, 8, 15,14,13,12 |
| | 0100 | 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3 | 4, 5, 6, 7, 0, 1, 2, 3,12,13,14,15, 8, 9, 10,11 |
| | 0101 | 5, 6, 7,8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4 | 5, 4, 7, 6, 1, 0, 3, 2,13,12,15,14, 9, 8,11,10 |
| | 0110 | 6, 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5 | 6, 7, 4, 5, 2, 3, 0, 1,14,15,12,13,10,11, 8, 9 |
| | 0111 | 7, 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5, 6 | 7, 6, 5, 4, 3, 2, 1, 0, 15,14,13,12,11,10, 9, 8 |
| | 1000 | 8, 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5, 6, 7 | 8, 9,10,11,12,13,14,15, 0, 1, 2, 3, 4, 5, 6, 7 |
| | 1001 | 9, 10, 11, 12, 13, 14,15, 0, 1, 2, 3, 4, 5, 6, 7, 8 | 9, 8, 11,10,13,12,15,14,1, 0, 3, 2, 5, 4, 7, 6 |
| | 1010 | 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9 | 10,11, 8, 9, 14,15,12,13, 2, 3, 0, 1, 6, 7, 4, 5 |
| | 1011 | 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 | 11,10, 9, 8, 15,14,13,12, 3, 2, 1, 0, 7, 6, 5, 4 |
| | 1100 | 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 | 12,13,14,15, 8, 9, 10,11, 4, 5, 6, 7, 0, 1, 2, 3 |
| | 1101 | 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11,12 | 13,12,15,14, 9, 8,11,10, 5, 4, 7, 6, 1, 0, 3, 2 |
| | 1110 | 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13 | 14,15,12,13,10,11, 8, 9, 6, 7, 4, 5, 2, 3, 0, 1 |
| | 1111 | 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14 | 15,14,13,12,11,10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0 |

## 8.2 Extended Mode Register Set (EMRS)

The extended mode register is designed to support for the desired operating modes of DDR SDRAM. The extended mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and high on BA1, low on BA0(The Mobile DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0 ~ A13 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the extended mode register. Two clock cycles are required to complete the write operation in the extended mode register. Even if the power-up sequence is finished and some read or write operations is executed afterward, the mode register contents can be changed with the same command and two clock cycles. But this command must be issued only when all banks are in the idle state. A0 - A2 are used for partial array self refresh and A5 - A7 are used for driver strength control. "High" on BA1 and "Low" on BA0 are used for EMRS. All the other address pins except A0,A1,A2,A5,A6,A7, BA1, BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.




| DS | | | |
|---|---|---|---|
| $A_7$ | $A_6$ | $A_5$ | Driver Strength |
| 0 | 0 | 0 | Full |
| 0 | 0 | 1 | 1/2 |
| 0 | 1 | 0 | 1/4 |
| 0 | 1 | 1 | 1/8 |
| 1 | 0 | 0 | 3/4 |
| 1 | 0 | 1 | 3/8 |
| 1 | 1 | 0 | 5/8 |
| 1 | 1 | 1 | 7/8 |

| PASR | | | |
|---|---|---|---|
| $A_2$ | $A_1$ | $A_0$ | Refreshed Area |
| 0 | 0 | 0 | Full Array |
| 0 | 0 | 1 | 1/2 Array |
| 0 | 1 | 0 | 1/4 Array |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

**Figure 3. Extended Mode Register Set**

**NOTE :**
1) RFU (Reserved for future use) should stay "0" during EMRS cycle

## 8.3 Internal Temperature Compensated Self Refresh (TCSR)

1. In order to save power consumption, this Mobile DRAM includes the internal temperature sensor and control units to control the self refresh cycle automatically according to the real device temperature.

2. TCSR ranges for IDD6 shown in the table are only examples.

3. If the EMRS for external TCSR is issued by the controller, this EMRS code for TCSR is ignored.

| Temperature Range | Self Refresh Current (IDD6) | | | Unit |
|---|---|---|---|---|
| | Full Array | 1/2 Array | 1/4 Array | |
| 85 °C | 1700 | 1400 | 1200 | uA |
| 45 °C | 400 | 270 | 200 | |

**NOTE :**
1) IDD6 85°C is guaranteed, IDD6 45°C is typical value.

## 8.4 Partial Array Self Refresh (PASR)

1. In order to save power consumption, Mobile DDR SDRAM includes PASR option.
2. Mobile DDR SDRAM supports three kinds of PASR in self refresh mode; Full array, 1/2 Array, 1/4 Array.

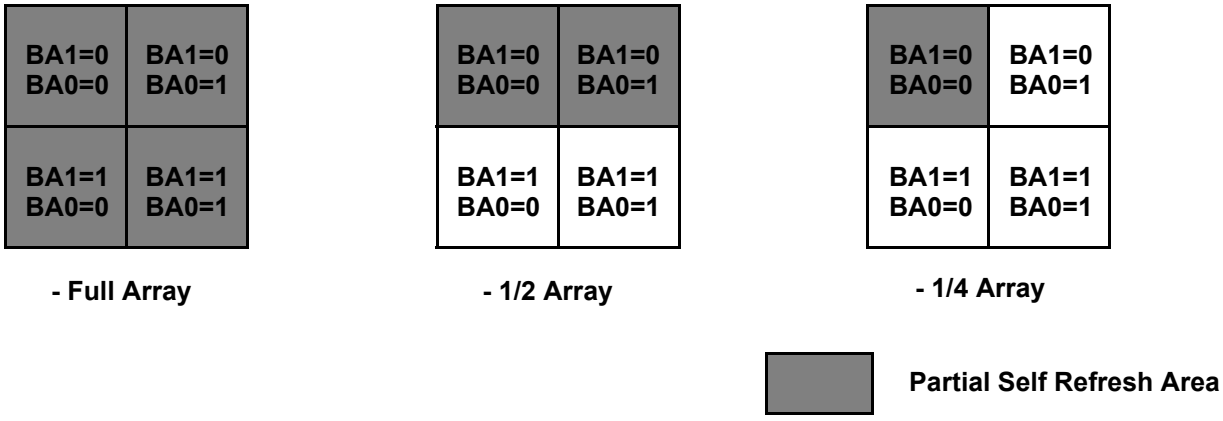



**Figure 4. EMRS code and TCSR, PASR**

# 9.0 ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to VSS | $V_{IN}$, $V_{OUT}$ | - 0.5 ~ 2.7 | V |
| Voltage on VDD supply relative to VSS | VDD | - 0.5 ~ 2.7 | V |
| Voltage on VDDQ supply relative to VSS | VDDQ | - 0.5 ~ 2.7 | V |
| Storage temperature | $T_{STG}$ | - 55 ~ + 150 | °C |
| Power dissipation | $P_D$ | 1.0 | W |
| Short circuit current | $I_{OS}$ | 50 | mA |

**NOTE :**
1) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
2) Functional operation should be restricted to recommend operation condition.
3) Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

# 10.0 DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to VSS=0V, $T_C$ = -25°C to 85°C)

| Parameter | | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage (for device with a nominal VDD of 1.8V) | | VDD | 1.7 | 1.95 | V | 1 |
| I/O Supply voltage | | VDDQ | 1.7 | 1.95 | V | 1 |
| Input logic high voltage | Address | $V_{IH}$(DC) | 0.8 x VDDQ | VDDQ + 0.3 | V | 2 |
| | Data | | 0.7 x VDDQ | VDDQ + 0.3 | V | |
| Input logic low voltage | Address | $V_{IL}$(DC) | -0.3 | 0.2 x VDDQ | V | 2 |
| | Data | | -0.3 | 0.3 x VDDQ | V | |
| Output logic high voltage | | $V_{OH}$(DC) | 0.9 x VDDQ | - | V | $I_{OH}$ = - 0.1mA |
| Output logic low voltage | | $V_{OL}$(DC) | - | 0.1 x VDDQ | V | $I_{OL}$ = 0.1mA |
| Input leakage current | | $I_I$ | -2 | 2 | uA | 3 |
| Output leakage current | | $I_{OZ}$ | -5 | 5 | uA | |

**NOTE :**
1) Under all conditions, VDDQ must be less than or equal to VDD.
2) These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.
3) Any input 0V ≤ VIN ≤ VDDQ.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with tri-state outputs.

# 11.0 DC CHARACTERISTICS

Recommended operating conditions (Voltage referenced to $V_{SS}$ = 0V, Tc = -25 to 85°C)

| Parameter | Symbol | Test Condition | DDR400 | Unit | Note |
|---|---|---|---|---|---|
| Operating Current (One Bank Active) | IDD0 | tRC=tRCmin; tCK=tCKmin; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE | 60 | mA | |
| Precharge Standby Current in power-down mode | IDD2P | all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE | 1.0 | mA | |
| | IDD2PS | all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE | 1.0 | | |
| Precharge Standby Current in non power-down mode | IDD2N | all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE | 6 | mA | |
| | IDD2NS | all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE | 4 | | |
| Active Standby Current in power-down mode | IDD3P | one bank active, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE | 6 | mA | |
| | IDD3PS | one bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE | 5 | | |
| Active Standby Current in non power-down mode (One Bank Active) | IDD3N | one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE | 12 | mA | |
| | IDD3NS | one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE | 10 | | |
| Operating Current (Burst Mode) | IDD4R | one bank active; BL=4; CL=3; tCK = tCKmin; continuous read bursts; $I_{OUT}$ =0 mA address inputs are SWITCHING; 50% data change each burst transfer | 85 | mA | |
| | IDD4W | one bank active; BL = 4; tCK = tCKmin; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer | 65 | | |
| Refresh Current | IDD5 | tRC ≥ tRFC; tCK = tCKmin; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE | 150 | mA | 1 |
| Self Refresh Current | IDD6 | CKE is LOW; t CK = t CKmin; Extended Mode Register set to all 0's; address and control inputs are STABLE; data bus inputs are STABLE | **TCSR Range** | **Values** | | 5 |
| | | | **Full Array** 85°C | 1700 | uA | |
| | | | **Full Array** 45°C | 400 | uA | |
| | | | **1/2 Array** 85°C | 1400 | uA | |
| | | | **1/2 Array** 45°C | 270 | uA | |
| | | | **1/4 Array** 85°C | 1200 | uA | |
| | | | **1/4 Array** 45°C | 200 | uA | |
| Deep Power Down Current | IDD8 | Deep Power Down Mode Current | 85°C | 100 | uA | 6,7 |
| | | | 45°C | 10 | | |

**NOTE :**

1) IDD5 is measured in the below test condition.

| Density | 128Mb | 256Mb | 512Mb | 1Gb | 2Gb | Unit |
|---|---|---|---|---|---|---|
| $t_{RFC}$ | 80 | 80 | 110 | 140 | 140 | ns |

2) The IDD values need to be measured after devices are properly initialized following all sequences including MRS and EMRS in "Power Up Sequence" section in the specification.

3) Input slew rate is 1V/ns.

4) Definitions for IDD: LOW is defined as $V_{IN} \leq 0.1 * VDDQ$;
HIGH is defined as $V_{IN} \geq 0.9 * VDDQ$;
STABLE is defined as inputs stable at a HIGH or LOW level;
SWITCHING is defined as: - address and command: inputs changing between HIGH and LOW once per two clock cycles;
- data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.

5) IDD6 85°C is guaranteed, IDD6 45°C is typical value.

6) IDD8 85°C is guaranteed, IDD8 45°C is typical value.

7) DPD (Deep Power Down) function is an optional feature, and it will be enabled upon request.
Please contact Samsung for more information.

# 12.0 AC OPERATING CONDITIONS & TIMMING SPECIFICATION

| Parameter/Condition | Symbol | Min | Max | Unit | Note |
|---|---|---|---|---|---|
| Input High (Logic 1) Voltage, all inputs | $V_{IH}$ (AC) | 0.8 x VDDQ | VDDQ + 0.3 | V | 1 |
| Input Low (Logic 0) Voltage, all inputs | $V_{IL}$ (AC) | -0.3 | 0.2 x VDDQ | V | 1 |
| Input Crossing Point Voltage, CK and $\overline{CK}$ inputs | $V_{IX}$ (AC) | 0.4 x VDDQ | 0.6 x VDDQ | V | 2 |

**NOTE :**
1) These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.
2) The value of $V_{IX}$ is expected to equal 0.5*VDDQ of the transmitting device and must track variations in the DC level of the same.

# 13.0 AC TIMMING PARAMETERS & SPECIFICATIONS

| Parameter | | Symbol | DDR400 | | Unit | Note |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Clock cycle time | CL=2 | $t_{CK}$ | 12.0 | | ns | 1,2 |
| | CL=3 | | 5 | | | |
| Row cycle time | | $t_{RC}$ | 55 | | ns | |
| Row active time | | $t_{RAS}$ | 40 | 70,000 | ns | |
| RAS to CAS delay | | $t_{RCD}$ | 15 | | ns | |
| Row precharge time | | $t_{RP}$ | 15 | | ns | |
| Row active to Row active delay | | $t_{RRD}$ | 10 | | ns | |
| Write recovery time | | $t_{WR}$ | 12 | | ns | |
| Last data in to Active delay | | $t_{DAL}$ | - | | - | 3 |
| Last data in to Read command | | $t_{CDLR}$ | 2 | | tCK | |
| Col. address to Col. address delay | | $t_{CCD}$ | 1 | | tCK | |
| Clock high level width | | $t_{CH}$ | 0.45 | 0.55 | tCK | |
| Clock low level width | | $t_{CL}$ | 0.45 | 0.55 | tCK | |
| DQ Output data access time from CK / $\overline{CK}$ | CL=2 | $t_{AC}$ | 2 | 8 | ns | 4 |
| | CL=3 | | 2 | 5 | | |
| DQS Output data access time from CK / $\overline{CK}$ | CL=2 | $t_{DQSCK}$ | 2 | 8 | ns | |
| | CL=3 | | 2 | 5 | | |
| Data strobe edge to output data edge | | $t_{DQSQ}$ | | 0.4 | ns | |
| Read Preamble | CL=2 | $t_{RPRE}$ | 0.5 | 1.1 | tCK | |
| | CL=3 | | 0.9 | 1.1 | | |
| Read Postamble | | $t_{RPST}$ | 0.4 | 0.6 | tCK | |
| CK to valid DQS-in | | $t_{DQSS}$ | 0.75 | 1.25 | tCK | |
| DQS-in setup time | | $t_{WPRES}$ | 0 | | ns | 5 |
| DQS-in hold time | | $t_{WPREH}$ | 0.25 | | tCK | |
| DQS-in high level width | | $t_{DQSH}$ | 0.4 | 0.6 | tCK | |
| DQS-in low level width | | $t_{DQSL}$ | 0.4 | 0.6 | tCK | |
| DQS falling edge to CK setup time | | $t_{DSS}$ | 0.2 | | tCK | |
| DQS falling edge hold time from CK | | $t_{DSH}$ | 0.2 | | tCK | |
| DQS-in cycle time | | $t_{DSC}$ | 0.9 | 1.1 | tCK | |
| Address and Control Input setup time | fast slew rate | $t_{IS}$ | 0.9 | | ns | 7 |
| | slow slew rate | | 1.1 | | | 8 |
| Address and Control Input hold time | fast slew rate | $t_{IH}$ | 0.9 | | ns | 7 |
| | slow slew rate | | 1.1 | | | 8 |
| Address & Control input pulse width | | $t_{IPW}$ | 2.2 | | | |
| DQ & DM setup time to DQS | fast slew rate | $t_{DS}$ | 0.48 | | ns | 6,7 |
| | slow slew rate | | 0.58 | | | 6,8 |
| DQ & DM hold time to DQS | fast slew rate | $t_{DH}$ | 0.48 | | ns | 6,7 |
| | slow slew rate | | 0.58 | | | 6,8 |
| DQ & DM input pulse width | | $t_{DIPW}$ | 1.2 | | ns | |
| DQ & DQS low-impedence time from CK / $\overline{CK}$ | | $t_{LZ}$ | 1.0 | | ns | |
| DQ & DQS high-impedence time from CK / $\overline{CK}$ | | $t_{HZ}$ | | 5 | ns | |
| DQS write postamble time | | $t_{WPST}$ | 0.4 | 0.6 | tCK | |

| Parameter | Symbol | DDR400 | | Unit | Note |
|---|---|---|---|---|---|
| | | Min | Max | | |
| DQS write preamble time | $t_{WPRE}$ | 0.25 | | tCK | |
| Refresh interval time | $t_{REF}$ | | 64 | ms | |
| Mode register set cycle time | $t_{MRD}$ | 2 | | tCK | |
| Power down exit time | $t_{PDEX}$ | 2 | | tCK | |
| CKE min. pulse width (high and low pulse width) | $t_{CKE}$ | 2 | | tCK | |
| Auto refresh cycle time | $t_{RFC}$ | 120 | | ns | 9 |
| Exit self refresh to active command | $t_{XSR}$ | 120 | | ns | |
| Data hold from DQS to earliest DQ edge | $t_{QH}$ | $t_{HP}$min - $t_{QHS}$ | | ns | |
| Data hold skew factor | $t_{QHS}$ | | 0.5 | ns | |
| Clock half period | $t_{HP}$ | $t_{CL}$min or $t_{CH}$min | | ns | |
| Clock half period | $t_{HP}$ | $t_{CL}$min or $t_{CH}$min | | ns | |
| Minimum Deep Power Down Time | $t_{DPD}$ | 500 | | us | |

**NOTE :**

1) $t_{CK}$ (max) value is measured at 100ns.

2) The only time that the clock Frequency is allowed to be changed is during clock stop, power-down, self-refresh modes.

3) In case of below 33MHz ($t_{CK}$=30ns) condition, SEC could support $t_{DAL}$ (=2*tCK).
$t_{DAL}$ =($t_{WR}$/$t_{CK}$) + ($t_{RP}$/$t_{CK}$)

4) $t_{AC}$ (min) value is measured at the high VDD (1.95V) and cold temperature (-25°C).
$t_{AC}$ (max) value is measured at the low VDD (1.7V) and hot temperature (85°C).
$t_{AC}$ is measured in the device with half driver strength and under the AC output load condition (Fig.6 in next Page).

5) The specific requirement is that DQS be valid (High or Low) on or before this CK edge. The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on $t_{DQSS}$.

6) I/O Delta Rise/Fall Rate(1/slew-rate) Derating

| Data Rise/Fall Rate | ΔtDS | ΔtDH |
|---|---|---|
| (ns/V) | (ps) | (ps) |
| 0 | 0 | 0 |
| ±0.25 | +50 | +50 |
| ±0.5 | +100 | +100 |

This derating table is used to increase $t_{DS}$/$t_{DH}$ in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calculated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 1.0V/ns and slew rate 2 =0.8V/ns, then the Delta Rise/Fall Rate =-0.25ns/V.

7) Input slew rate 1.0 V/ ns.

8) Input slew rate 0.5V/ns and < 1.0V/ns.

9) Maximum burst refresh cycle : 8

# 14.0 AC OPERATING TEST CONDITIONS (VDD = 1.7V to 1.95V, TC = -25°C to 85°C)

| Parameter | Value | Unit |
|---|---|---|
| AC input levels (Vih/Vil) | 0.8 x VDDQ / 0.2 x VDDQ | V |
| Input timing measurement reference level | 0.5 x VDDQ | V |
| Input signal minimum slew rate | 1.0 | V/ns |
| Output timing measurement reference level | 0.5 x VDDQ | V |
| Output load condition | See Figure 6 | |

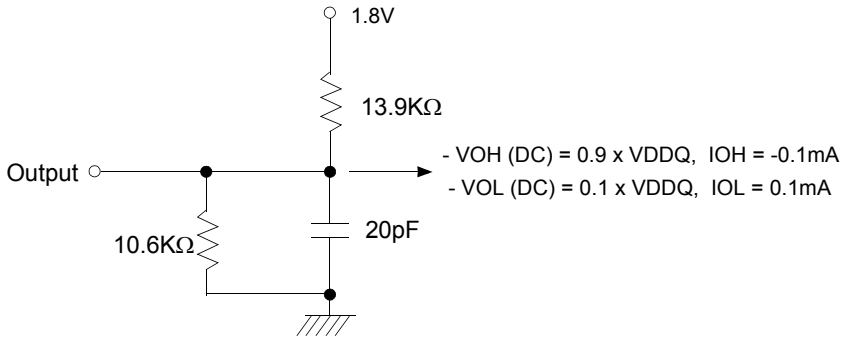



**Figure 5. DC Output Load Circuit**

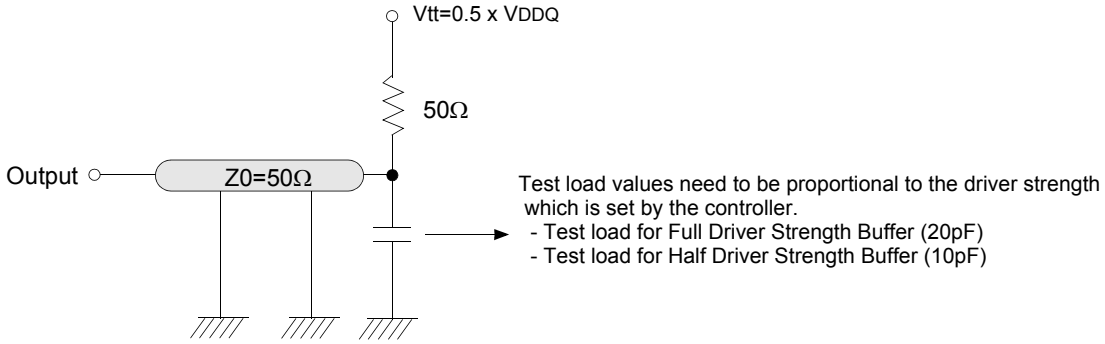



**Figure 6. AC Output Load Circuit [1), 2)]**

**NOTE :**

1) The circuit shown above represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half driver strength with a nominal 10pF load parameters $t_{AC}$ and $t_{QH}$ are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design / characterization. Use of IBIS or other simulation tools for system design validation is suggested.

2) Based on nominal impedance at 0.5 x VDDQ.
The impedence for Half(1/2) Driver Strength is designed 55ohm. And for other Driver Strength, it is designed proportionally.

# 15.0 INPUT/OUTPUT CAPACITANCE (VDD=1.8, VDDQ=1.8V, TC = 25°C, f=100MHz)

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input capacitance<br>(A0 ~ A13, BA0 ~ BA1, CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$) | CIN1 | 1.5 | 3.0 | pF |
| Input capacitance (CK, $\overline{CK}$) | CIN2 | 1.5 | 3.5 | pF |
| Data & DQS input / output capacitance | COUT | 2.0 | 4.5 | pF |
| Input capacitance (DM) | CIN3 | 2.0 | 4.5 | pF |

# 16.0 AC OVERSHOOT/UNDERSHOOT SPECIFICATION FOR ADDRESS & CONTROL PINS

| Parameter | Specification |
|---|---|
| Maximum peak Amplitude allowed for overshoot area | 0.9V |
| Maximum peak Amplitude allowed for undershoot area | 0.9V |
| Maximum overshoot area above VDD | 3V-ns |
| Maximum undershoot area below VSS | 3V-ns |

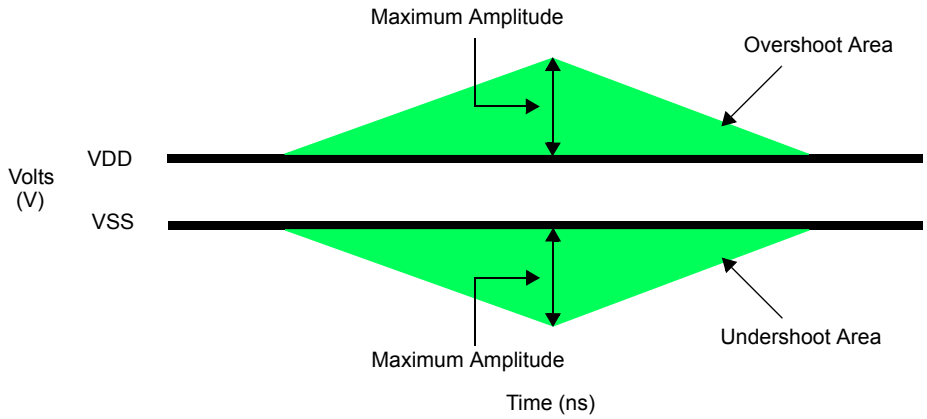



**Figure 7. AC Overshoot and Undershoot Definition for Address and Control Pins**

# 17.0 AC OVERSHOOT/UNDERSHOOT SPECIFICATION FOR CK, DQ, DQS AND DM PINS

| Parameter | Specification |
|---|---|
| Maximum peak Amplitude allowed for overshoot area | 0.9V |
| Maximum peak Amplitude allowed for undershoot area | 0.9V |
| Maximum overshoot area above VDDQ | 3V-ns |
| Maximum undershoot area below VSSQ | 3V-ns |

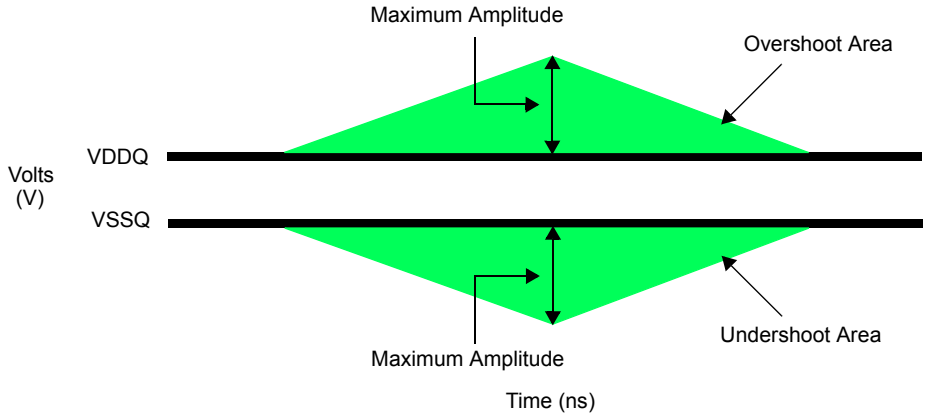



**Figure 8. AC Overshoot and Undershoot Definition for CK, DQ, DQS and DM Pins**

# 18.0 COMMAND TRUTH TABLE

| Command | | | CKEn-1 | CKEn | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | BA0,1 | A10/AP | A13~11, A9~A0 | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Register | Mode Register Set | | H | X | L | L | L | L | OP CODE | | | 1, 2 |
| Refresh | Auto Refresh | | H | H | L | L | L | H | X | | | 3 |
| | Self Refresh | Entry | | L | | | | | | | | 3 |
| | | Exit | L | H | L | H | H | H | X | | | 3 |
| | | | | | H | X | X | X | | | | 3 |
| Bank Active & Row Addr. | | | H | X | L | L | H | H | V | Row Address | | |
| Read & Column Address | Auto Precharge Disable | | H | X | L | H | L | H | V | L | Column Address (A0~A9) | 4 |
| | Auto Precharge Enable | | | | | | | | | H | | 4 |
| Write & Column Address | Auto Precharge Disable | | H | X | L | H | L | L | V | L | Column Address (A0~A9) | 4 |
| | Auto Precharge Enable | | | | | | | | | H | | 4, 6 |
| Deep Power Down | | Entry | H | L | L | H | H | L | X | | | |
| | | Exit | L | H | H | X | X | X | | | | |
| Burst Stop | | | H | X | L | H | H | L | X | | | 7 |
| Precharge | Bank Selection | | H | X | L | L | H | L | V | L | X | |
| | All Banks | | | | | | | | X | H | | 5 |
| Active Power Down | | Entry | H | L | H | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | |
| | | Exit | L | H | X | X | X | X | | | | |
| Precharge Power Down | | Entry | H | L | H | X | X | X | X | | | |
| | | | | | L | H | H | H | | | | |
| | | Exit | L | H | H | X | X | X | | | | |
| | | | | | L | H | H | H | | | | |
| DM | | | H | X | | | | | X | | | 8 |
| No operation (NOP) : Not defined | | | H | X | H | X | X | X | X | | | 9 |
| | | | | | L | H | H | H | | | | 9 |

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

**NOTE :**
1) OP Code : Operand Code. A0 ~ A13 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)
2) EMRS / MRS can be issued only at all banks precharge state.
   A new command can be issued 2 clock cycles after EMRS or MRS.
3) Auto refresh functions are same as the CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4) BA0 ~ BA1 : Bank select addresses.
5) If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
6) During burst write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at $t_{RP}$ after the end of burst.
7) Burst stop command is valid at every burst length.
8) DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
9) This combination is not defined for any function, which means "No Operation(NOP)" in Mobile DDR SDRAM.

# 19.0 FUNCTIONAL TRUTH TABLE

| Current State | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| PRECHARGE STANDBY | L | H | H | L | X | Burst Stop | ILLEGAL [2] |
| | L | H | L | X | BA, CA, A10 | READ/WRITE | ILLEGAL [2] |
| | L | L | H | H | BA, RA | Active | Bank Active, Latch RA |
| | L | L | H | L | BA, A10 | PRE/PREA | ILLEGAL [4] |
| | L | L | L | H | X | Refresh | AUTO-Refresh [5] |
| | L | L | L | L | Op-Code, Mode-Add | MRS | Mode Register Set [5] |
| ACTIVE STANDBY | L | H | H | L | X | Burst Stop | NOP |
| | L | H | L | H | BA, CA, A10 | READ/READA | Begin Read, Latch CA, Determine Auto-Precharge |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEA | Begin Write, Latch CA, Determine Auto-Precharge |
| | L | L | H | H | BA, RA | Active | Bank Active/ILLEGAL [2] |
| | L | L | H | L | BA, A10 | PRE/PREA | Precharge/Precharge All |
| | L | L | L | H | X | Refresh | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| READ | L | H | H | L | X | Burst Stop | Terminate Burst |
| | L | H | L | H | BA, CA, A10 | READ/READA | Terminate Burst, Latch CA, Begin New Read, Determine Auto-Precharge [3] |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEA | ILLEGAL |
| | L | L | H | H | BA, RA | Active | Bank Active/ILLEGAL [2] |
| | L | L | H | L | BA, A10 | PRE/PREA | Terminate Burst, Precharge [10] |
| | L | L | L | H | X | Refresh | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| WRITE | L | H | H | L | X | Burst Stop | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READA | Terminate Burst With DM=High, Latch CA, Begin Read, Determine Auto-Precharge [3] |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEA | Terminate Burst, Latch CA, Begin new Write, Determine Auto-Precharge [3] |
| | L | L | H | H | BA, RA | Active | Bank Active/ILLEGAL [2] |
| | L | L | H | L | BA, A10 | PRE/PREA | Terminate Burst With DM=High, Precharge [10] |
| | L | L | L | H | X | Refresh | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| READ with AUTO PRECHARGE[6] (READA) | L | H | H | L | X | Burst Stop | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READA | NOTE6 |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEA | ILLEGAL |
| | L | L | H | H | BA, RA | Active | NOTE6 |
| | L | L | H | L | BA, A10 | PRE/PREA | NOTE6 |
| | L | L | L | H | X | Refresh | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

| Current State | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Address | Command | Action |
|---|---|---|---|---|---|---|---|
| WRITE with AUTO RECHARGE[7] (WRITEA) | L | H | H | L | X | Burst Stop | ILLEGAL |
| | L | H | L | H | BA, CA, A10 | READ/READA | NOTE7 |
| | L | H | L | L | BA, CA, A10 | WRITE/WRITEA | NOTE7 |
| | L | L | H | H | BA, RA | Active | NOTE7 |
| | L | L | H | L | BA, A10 | PRE/PREA | NOTE7 |
| | L | L | L | H | X | Refresh | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| PRECHARGING (DURING $t_{RP}$) | L | H | H | L | X | Burst Stop | ILLEGAL [2] |
| | L | H | L | X | BA, CA, A10 | READ/WRITE | ILLEGAL [2] |
| | L | L | H | H | BA, RA | Active | ILLEGAL [2] |
| | L | L | H | L | BA, A10 | PRE/PREA | NOP [4] (Idle after $t_{RP}$) |
| | L | L | L | H | X | Refresh | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| ROW ACTIVATING (FROM ROW ACTIVE TO $t_{RCD}$) | L | H | H | L | X | Burst Stop | ILLEGAL [2] |
| | L | H | L | X | BA, CA, A10 | READ/WRITE | ILLEGAL [2] |
| | L | L | H | H | BA, RA | Active | ILLEGAL [2] |
| | L | L | H | L | BA, A10 | PRE/PREA | ILLEGAL [2] |
| | L | L | L | H | X | Refresh | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| WRITE RECOVERING (DURING $t_{WR}$ OR $t_{CDLR}$) | L | H | H | L | X | Burst Stop | ILLEGAL [2] |
| | L | H | L | H | BA, CA, A10 | READ | ILLEGAL [2] |
| | L | H | L | L | BA, CA, A10 | WRITE | WRITE |
| | L | L | H | H | BA, RA | Active | ILLEGAL [2] |
| | L | L | H | L | BA, A10 | PRE/PREA | ILLEGAL [2] |
| | L | L | L | H | X | Refresh | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| RE-FRESHING | L | H | H | L | X | Burst Stop | ILLEGAL |
| | L | H | L | X | BA, CA, A10 | READ/WRITE | ILLEGAL |
| | L | L | H | H | BA, RA | Active | ILLEGAL |
| | L | L | H | L | BA, A10 | PRE/PREA | ILLEGAL |
| | L | L | L | H | X | Refresh | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |
| MODE REGISTER SETTING | L | H | H | L | X | Burst Stop | ILLEGAL |
| | L | H | L | X | BA, CA, A10 | READ/WRITE | ILLEGAL |
| | L | L | H | H | BA, RA | Active | ILLEGAL |
| | L | L | H | L | BA, A10 | PRE/PREA | ILLEGAL |
| | L | L | L | H | X | Refresh | ILLEGAL |
| | L | L | L | L | Op-Code, Mode-Add | MRS | ILLEGAL |

| Current State | CKE n-1 | CKE n | $\overline{CS}$ | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Add | Action |
|---|---|---|---|---|---|---|---|---|
| SELF-REFRESHING [8] | L | H | H | X | X | X | X | Exit Self-Refresh |
| | L | H | L | H | H | H | X | Exit Self-Refresh |
| | L | H | L | H | H | L | X | ILLEGAL |
| | L | H | L | H | L | X | X | ILLEGAL |
| | L | H | L | L | X | X | X | ILLEGAL |
| | L | L | X | X | X | X | X | NOP (Maintain Self-Refresh) |
| POWER DOWN | L | H | X | X | X | X | X | Exit Power Down (Idle after $t_{PDEX}$) |
| | L | L | X | X | X | X | X | NOP (Maintain Power Down) |
| DEEP POWER DOWN | L | H | H | X | X | X | X | Exit Deep Power Down [10] |
| | L | L | X | X | X | X | X | NOP (Maintain Deep Power Down) |
| ALL BANKS IDLE [9] | H | H | X | X | X | X | X | Refer to Function Truth Table |
| | H | L | L | L | L | H | X | Enter Self-Refresh |
| | H | L | H | X | X | X | X | Enter Power Down |
| | H | L | L | H | H | H | X | Enter Power Down |
| | H | L | L | H | H | L | X | Enter Deep Power Down |
| | H | L | L | H | H | L | X | ILLEGAL |
| | H | L | L | H | L | X | X | ILLEGAL |
| | H | L | L | L | X | X | X | ILLEGAL |
| | L | X | X | X | X | X | X | Refer to Current State = Power Down |

(H=High Level, L=Low level, X=Don't Care)

**NOTE :**
1) All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2) ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
(ILLEGAL = Device operation and/or data integrity are not guaranteed.)
3) Must satisfy bus contention, bus turn around and write recovery requirements.
4) NOP to bank precharging or in idle sate. May precharge bank indicated by BA.
5) ILLEGAL if any bank is not idle.
6) Refer to "Read with Auto Precharge Timing Diagram" for detailed information.
7) Refer to "Write with Auto Precharge Timing Diagram" for detailed information.
8) CKE Low to High transition will re-enable CK, $\overline{CK}$ and other inputs asynchronously.
A minimum setup time must be satisfied before issuing any command other than EXIT.
9) Power-Down, Self-Refresh and Deep Power Down Mode can be entered only from All Bank Idle state.
10) The Deep Power Down Mode is exited by asserting CKE high and full initialization is required after exiting Deep Power Down Mode.