

LDOs

CONNECTORS / SWITCHES

DIGITAL IC


ANALOG / MIXED IC

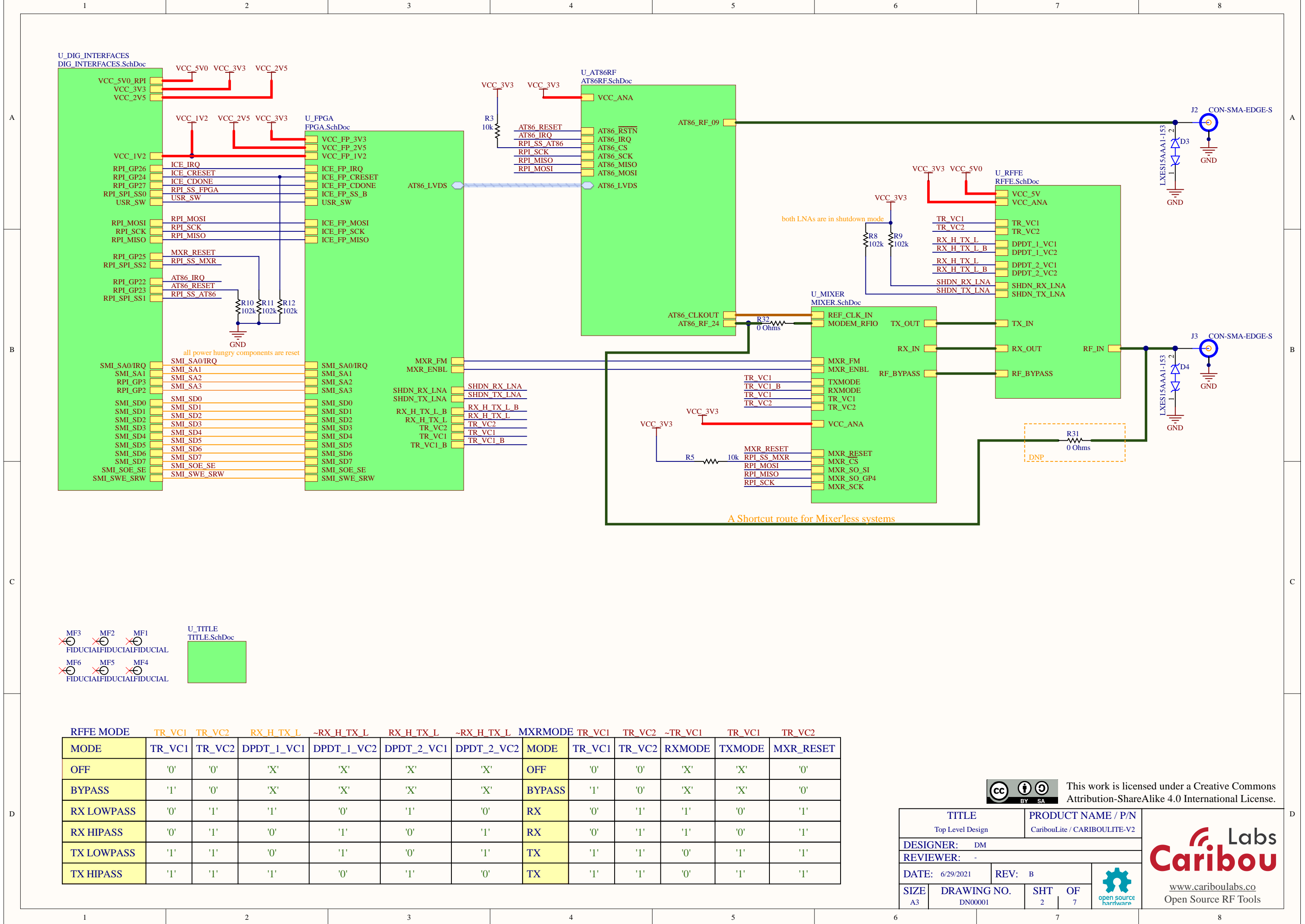
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TITLE Block Diagrams		PRODUCT NAME / P/N CaribouLite / CARIBOULITE-V2		<div> <a href="http://www.cariboulabs.co">www.cariboulabs.co</a> Open Source RF Tools</div>
DESIGNER: DM				
REVIEWER: -				
DATE: 6/27/2021		REV: B		
SIZE A3	DRAWING NO. DN00001	SHT 1	OF 7	



## A



## B




## C

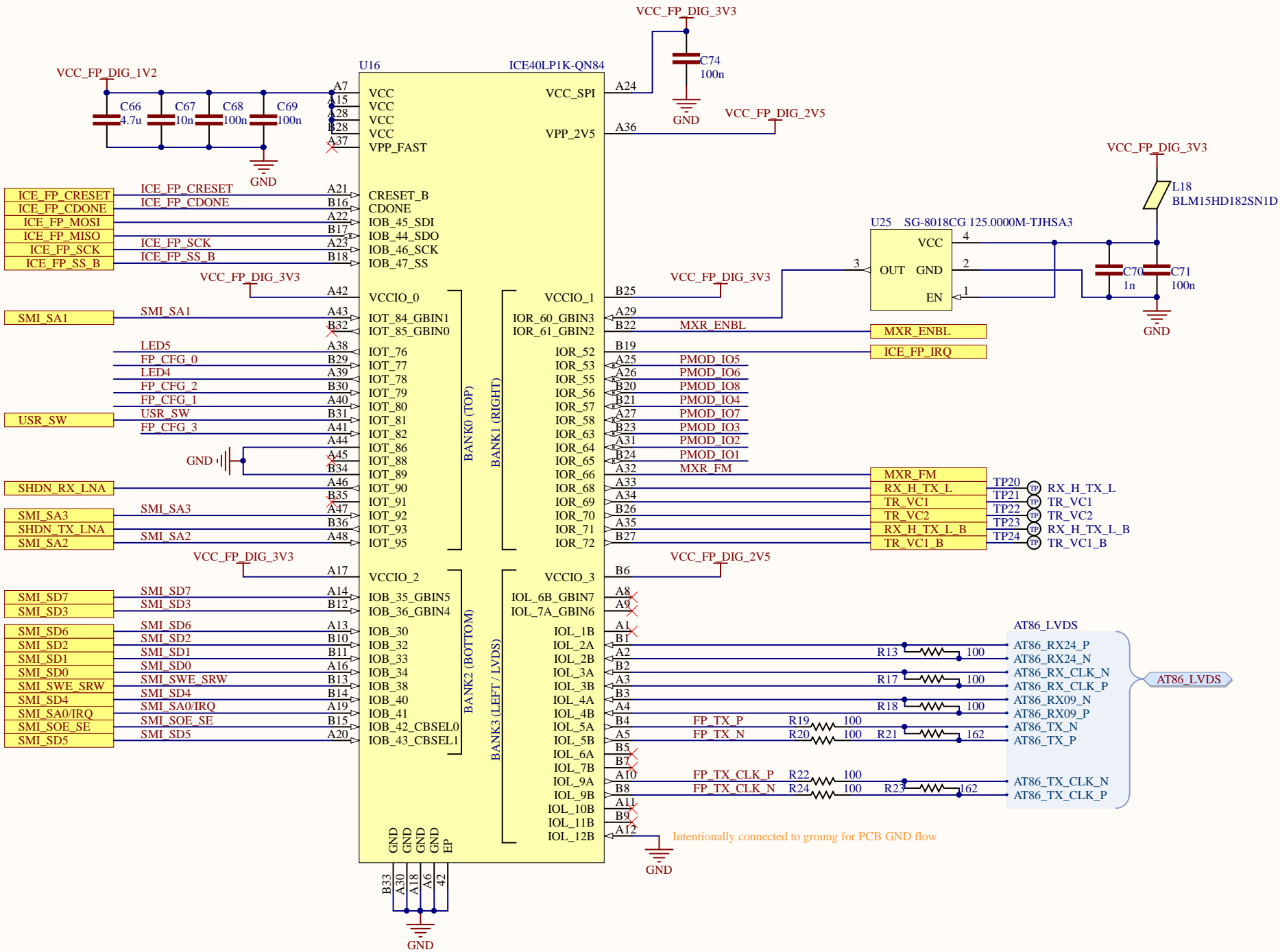


## C



TITLE Connectors and Power		PRODUCT NAME / P/N CaribouLite / CARIBOULITE-V2		 <a href="http://www.cariboulabs.co">www.cariboulabs.co</a> Open Source RF Tools
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FPGA



LVDS Negated Pairs

AT86\_TX  
AT86\_RX09  
AT86\_TX\_CLK

The other two are direct logic.

PROGRAMMING

POR=> Check SS  
1. if SS='1' => if NVCM programmed, use NVCM, otherwise use external flash (SPI MASTER).  
2. if SS='0', wait to be configured from external controller through SPI

RESET - restarts the configuration  
CDONE - before configuration finished is '0', When done turns '1'

Calculation of differential lines

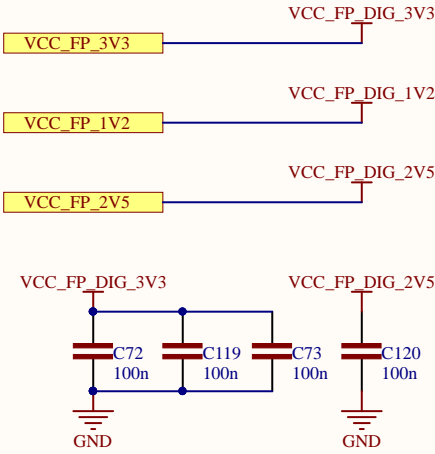
VCCIO = 2.5V  
VOD = 0.5V (this is the differential swing nominal)  
Rouput = 30 Ohms (given by ICE40 Specs)

The parallel output resistor:  
 $VCCIO = 2.5V \Rightarrow R_p = 2 * (50 * 2.5 / (2.5 - (2 * 0.5))) = 250 / 1.5 = 166 \text{ Ohms} \Rightarrow R_p / 2 = 83.3 \text{ Ohms}$   
The series output resistors:  
 $VCCIO = 2.5V \Rightarrow R_s = (50 * 83.3) / (83.3 - 50) - 30 = 4165 / 33.3 - 30 = 95 \text{ Ohms}$

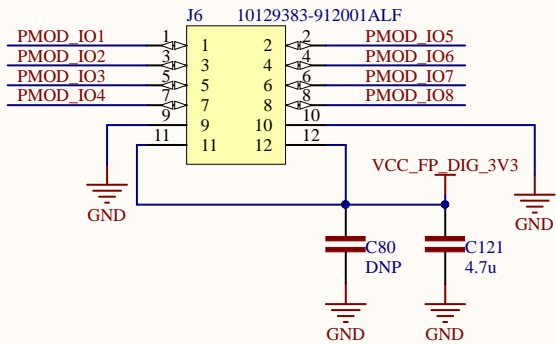
But, we want to make Rs a 100 Ohms to minimize BOM =>  
 $R_s = 100 \Rightarrow R_p = 162.5 \text{ Ohms} \Rightarrow V_{od} = 0.48 \text{ Vdiff} \Rightarrow \text{Looks good enough!}$

Connect the positive or true polarity side of the differential pair to the DPxxA input and the negative or complementary side of the pair to the DPxxB input.  
==== If it is easier to route the differential pair, the input pins can be swapped, which produces an inverted input value. ====  
====The inverted input value can subsequently be inverted by logic within the FPGA. ====

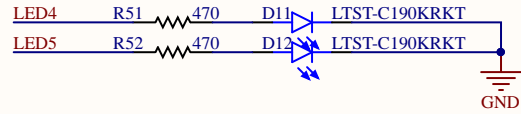
POWER TERMINALS



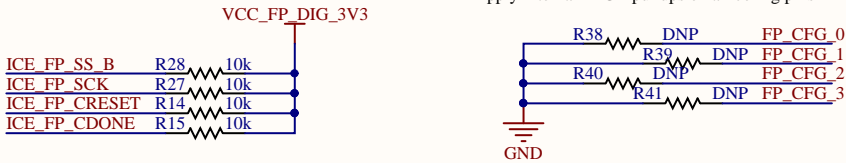
PMOD





LEDS



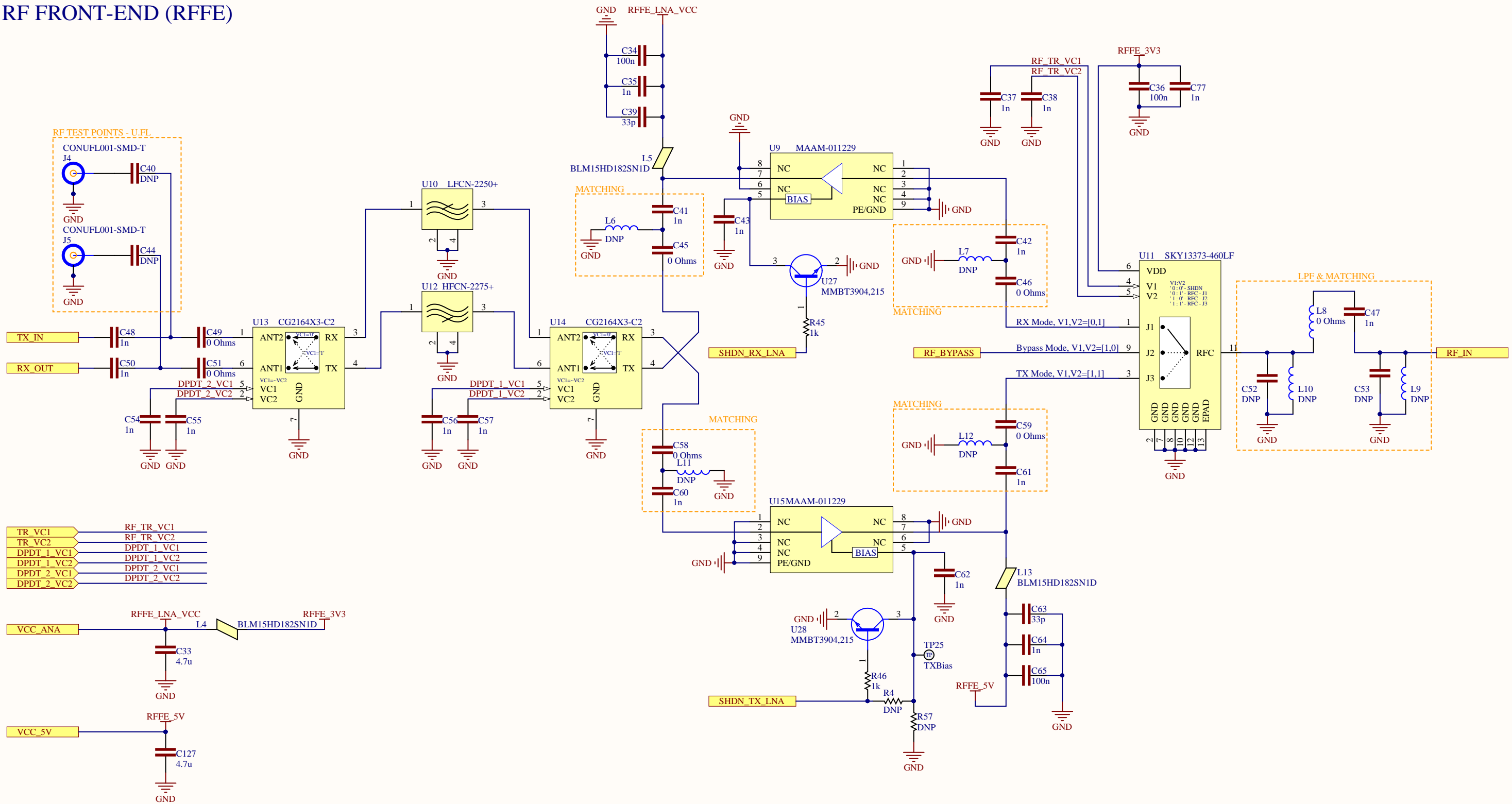
Configuration Resistors - Place 10k for pulldown as needed  
Apply internal FPGA pullups on all config pins



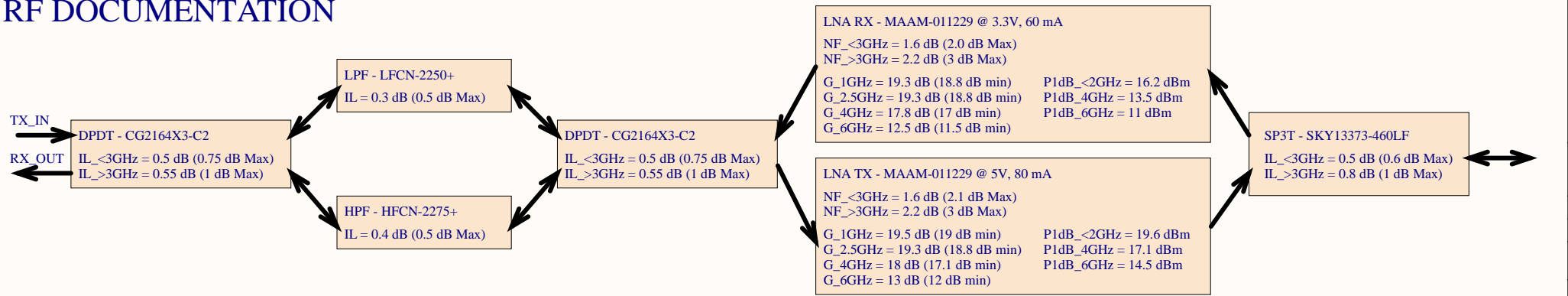
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RF FRONT-END (RFFE)



RF DOCUMENTATION



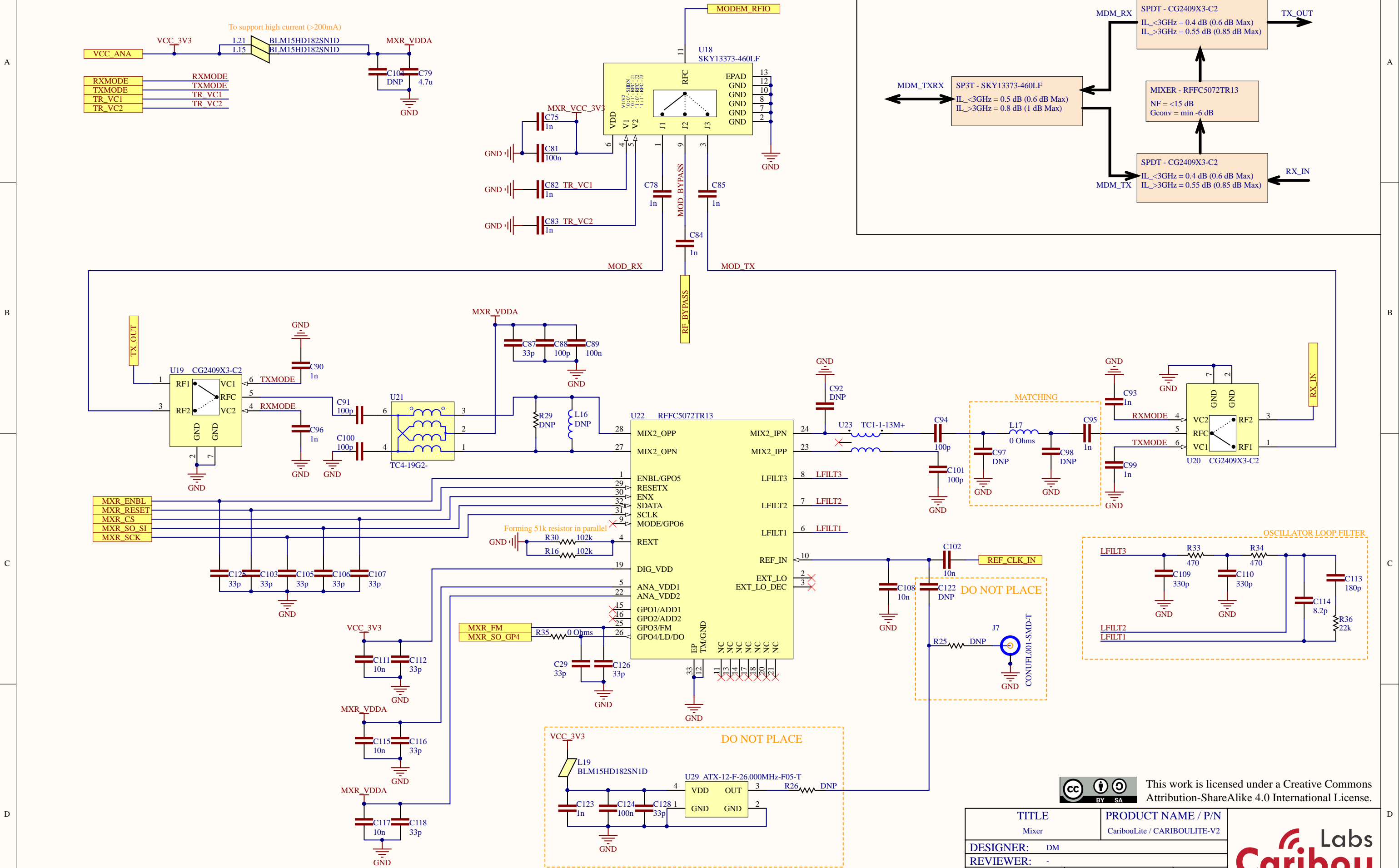
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RF Front-End		CaribouLite / CARIBOULITE-V2	
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REVIEWER:		-	
DATE:		6/27/2021	REV: B
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MIXER - QORVO RFFC5072


RF DOCUMENTATION





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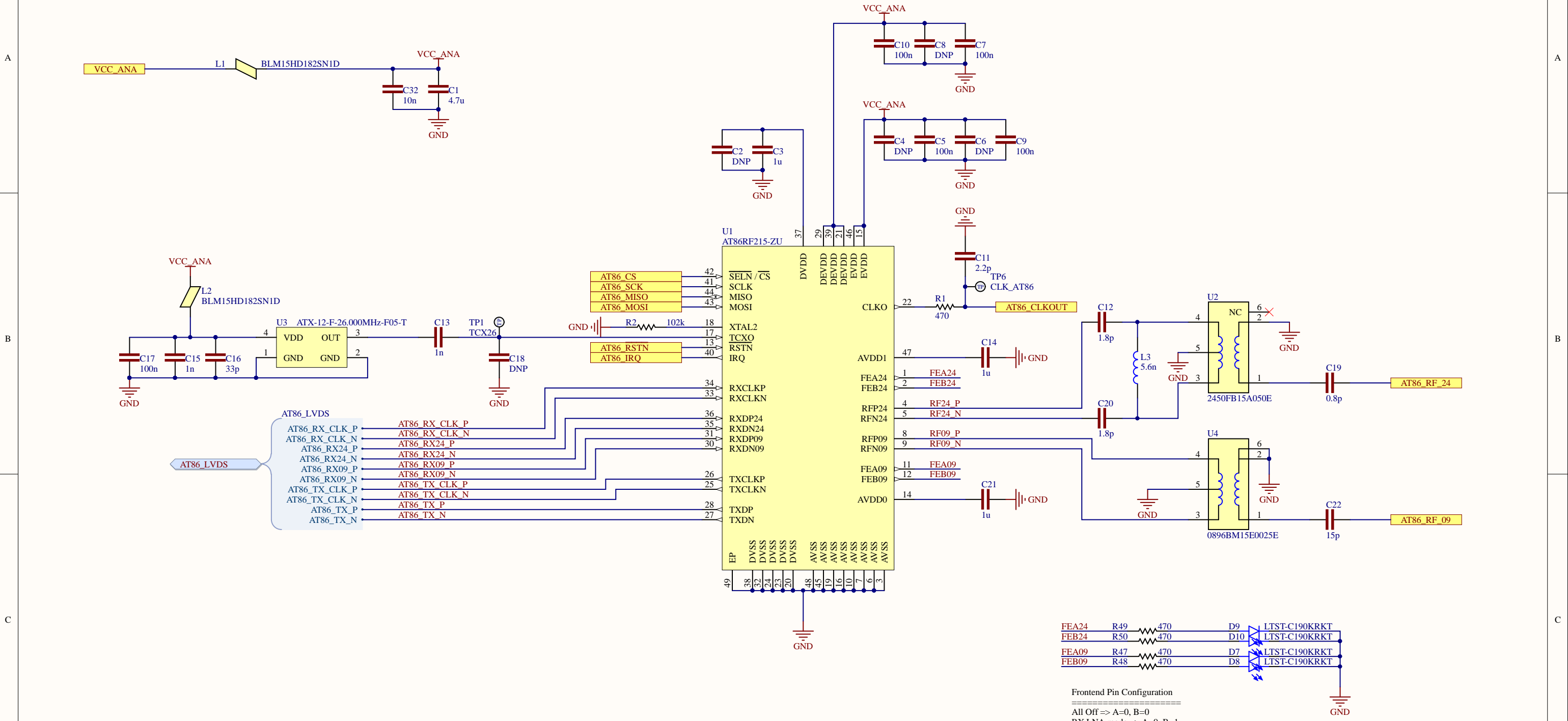
TITLE		PRODUCT NAME / P/N	
Mixer		CaribouLite / CARIBOULITE-V2	
DESIGNER: DM			
REVIEWER: -			
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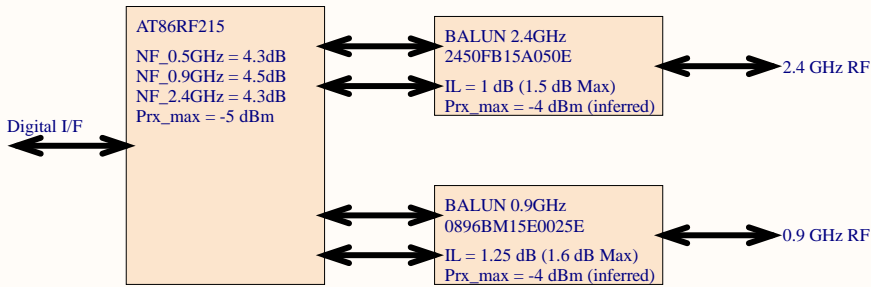
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MODEM - AT86RF215



RF DOCUMENTATION





FEA24 R49 470 D9 LTST-C190KRKT  
FEB24 R50 470 D10 LTST-C190KRKT  
FEA09 R47 470 D7 LTST-C190KRKT  
FEB09 R48 470 D8 LTST-C190KRKT

Frontend Pin Configuration  
=====

All Off => A=0, B=0  
RX LNA mode => A=0, B=1  
TX mode => A=1, B=0  
RX Bypass => A=1, B=1

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TITLE Modem and TCXO		PRODUCT NAME / P/N CaribouLite / CARIBOULITE-V2		<div><p>www.cariboulabs.co Open Source RF Tools</p></div>
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