

U_DIG_INTERFACES
DIG_INTERFACES.SchDoc

VCC_5V0_RPI
VCC_3V3
VCC_2V5

VCC_5V0 VCC_3V3 VCC_2V5

VCC_1V2 VCC_2V5 VCC_3V3

RPI_GP26
RPI_GP27
RPI_SPL_SS0
USR_SW

ICE_CRESET
ICE_CDONE
RPI_SS_FPGA
USR_SW

VCC_FP_3V3
VCC_FP_2V5
VCC_FP_1V2

ICE_FP_CRESET
ICE_FP_CDONE
ICE_FP_SS_B
USR_SW

RPI_MOSI
RPI_SCK
RPI_MISO

ICE_FP_MOSI
ICE_FP_SCK
ICE_FP_MISO

RPI_GP5
RPI_SPL_SS2

MXR_RESET
RPI_SS_MXR

RPI_GP22
RPI_GP23
RPI_SPL_SS1

AT86_IRQ
AT86_RESET
RPI_SS_AT86

R10
R11
R12
102k 102k 102k

all power hungry components are reset

RPI_GP24
RPI_GP25
SML_SA1
RPI_GP3
RPI_GP2

SML_READ_REQ
SML_WRITE_REQ
SML_SA1
SML_SA2
SML_SA3

SML_SD0
SML_SD1
SML_SD2
SML_SD3
SML_SD4
SML_SD5
SML_SD6
SML_SD7
SML_SOE_SE
SML_SWE_SRW

SML_SD0
SML_SD1
SML_SD2
SML_SD3
SML_SD4
SML_SD5
SML_SD6
SML_SD7
SML_SOE_SE
SML_SWE_SRW

MXR_FM

MXR_ENBL

SHDN_RX_LNA

SHDN_TX_LNA

RX_H_TX_L_B

RX_H_TX_L

TR_VC2

TR_VC1

TR_VC1_B

SHDN_RX_LNA

SHDN_TX_LNA

RX_H_TX_L_B

RX_H_TX_L

TR_VC2

TR_VC1

TR_VC1_B

U_AT86RF
AT86RF.SchDoc

VCC_ANA

VCC_3V3
R3
10k

AT86_RESET
AT86_IRQ
RPI_SS_AT86
RPI_SCK
RPI_MISO
RPI_MOSI

AT86_RSTN
AT86_IRQ
AT86_CS
AT86_SCK
AT86_MISO
AT86_MOSI

AT86_LVDS

AT86_RF_09

AT86_CLKOUT

AT86_RF_24

both LNAs are in shutdown mode

VCC_3V3
R8
R9
102k 102k

TR_VC1
TR_VC2

RX_H_TX_L

RX_H_TX_L_B

RX_H_TX_L

RX_H_TX_L_B

SHDN_RX_LNA

SHDN_TX_LNA

U_MIXER
MIXER.SchDoc

REF_CLK_IN

MODEM_RFIO

TX_OUT

RX_IN

RF_BYPASS

MXR_FM

MXR_ENBL

TR_VC1

TR_VC1_B

TR_VC1

TR_VC2

VCC_ANA

VCC_3V3

R5
10k

MXR_RESET
RPI_SS_MXR
RPI_MOSI
RPI_MISO
RPI_SCK

MXR_RESET
MXR_CS
MXR_SO_SI
MXR_SO_GP4
MXR_SCK

A Shortcut route for Mixer'less systems

U_RFFE
RFFE.SchDoc

VCC_5V

VCC_ANA

TR_VC1

TR_VC2

DPDT_1_VC1

DPDT_1_VC2

DPDT_2_VC1

DPDT_2_VC2

SHDN_RX_LNA

SHDN_TX_LNA

TX_IN

RX_OUT

RF_IN

RF_BYPASS

R31
0 Ohms
DNP

J2 CON-SMA-EDGE-S
LXES15AAA1-153
D3
GND

J3 CON-SMA-EDGE-S
LXES15AAA1-153
D4
GND


MF3 MF2 MF1
FIDUCIAL FIDUCIAL FIDUCIAL
MF6 MF5 MF4
FIDUCIAL FIDUCIAL FIDUCIAL

U_TITLE
TITLE.SchDoc

RFFE MODE	TR_VC1	TR_VC2	RX_H_TX_L	~RX_H_TX_L	RX_H_TX_L	~RX_H_TX_L	MXRMODE	TR_VC1	TR_VC2	~TR_VC1	TR_VC1	TR_VC2
MODE	TR_VC1	TR_VC2	DPDT_1_VC1	DPDT_1_VC2	DPDT_2_VC1	DPDT_2_VC2	MODE	TR_VC1	TR_VC2	RXMODE	TXMODE	MXR_RESET
OFF	'0'	'0'	'X'	'X'	'X'	'X'	OFF	'0'	'0'	'X'	'X'	'0'
BYPASS	'1'	'0'	'X'	'X'	'X'	'X'	BYPASS	'1'	'0'	'X'	'X'	'0'
RX LOWPASS	'0'	'1'	'1'	'0'	'1'	'0'	RX	'0'	'1'	'1'	'0'	'1'
RX HIPASS	'0'	'1'	'0'	'1'	'0'	'1'	RX	'0'	'1'	'1'	'0'	'1'
TX LOWPASS	'1'	'1'	'0'	'1'	'0'	'1'	TX	'1'	'1'	'0'	'1'	'1'
TX HIPASS	'1'	'1'	'1'	'0'	'1'	'0'	TX	'1'	'1'	'0'	'1'	'1'



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TITLE		PRODUCT NAME / P/N	
Top Level Design		CaribouLite / CARIBOULITE-V2	
DESIGNER: DM		REVIEWER: -	
DATE: 6/30/2021		REV: B	
SIZE A3	DRAWING NO. DN00001	SHT 2	OF 7
		 open source hardware	
		www.cariboulabs.co Open Source RF Tools	

A



B



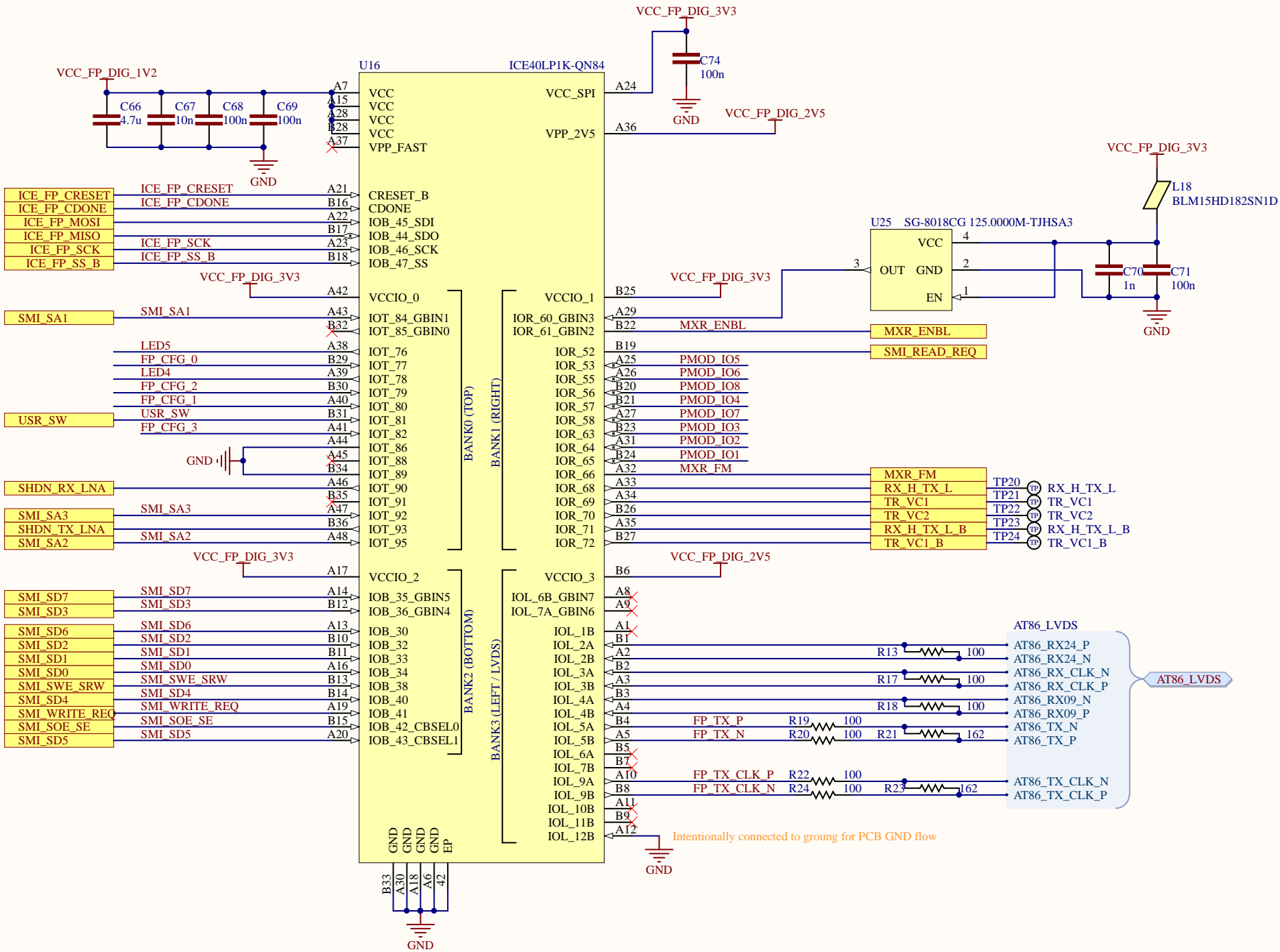
D



C



FPGA



LVDS Negated Pairs

AT86_TX
AT86_RX09
AT86_TX_CLK

The other two are direct logic.

PROGRAMMING

POR=> Check SS
1. if SS='1' => if NVCM programmed, use NVCM, otherwise use external flash (SPI MASTER).
2. if SS='0', wait to be configured from external controller through SPI

RESET - restarts the configuration
CDONE - before configuration finished is '0', When done turns '1'

Calculation of differential lines

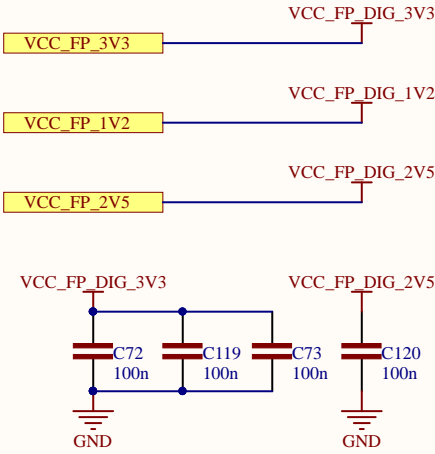
VCCIO = 2.5V
VOD = 0.5V (this is the differential swing nominal)
Rouput = 30 Ohms (given by ICE40 Specs)

The parallel output resistor:
 $VCCIO = 2.5V \Rightarrow R_p = 2 * (50 * 2.5 / (2.5 - (2 * 0.5))) = 250 / 1.5 = 166 \text{ Ohms} \Rightarrow R_p / 2 = 83.3 \text{ Ohms}$
The series output resistors:
 $VCCIO = 2.5V \Rightarrow R_s = (50 * 83.3) / (83.3 - 50) - 30 = 4165 / 33.3 - 30 = 95 \text{ Ohms}$

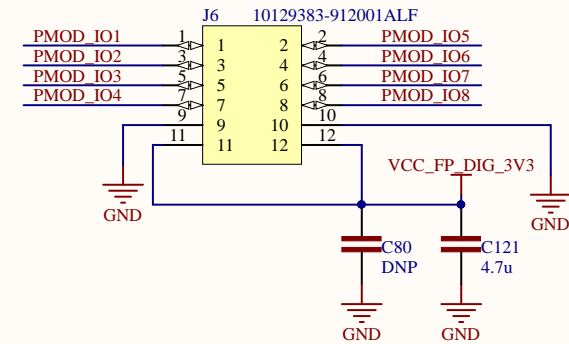
But, we want to make Rs a 100 Ohms to minimize BOM =>
 $R_s = 100 \Rightarrow R_p = 162.5 \text{ Ohms} \Rightarrow V_{od} = 0.48 \text{ Vdiff} \Rightarrow \text{Looks good enough!}$

Connect the positive or true polarity side of the differential pair to the DPxxA input and the negative or complementary side of the pair to the DPxxB input.
==== If it is easier to route the differential pair, the input pins can be swapped, which produces an inverted input value. =====
====The inverted input value can subsequently be inverted by logic within the FPGA. =====

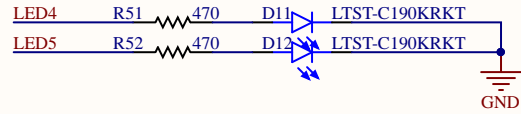
POWER TERMINALS



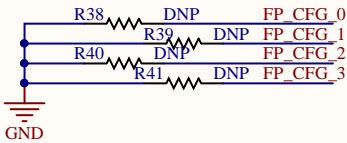
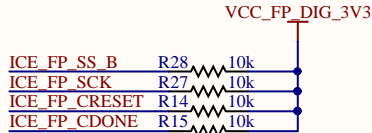
PMOD





LEDS



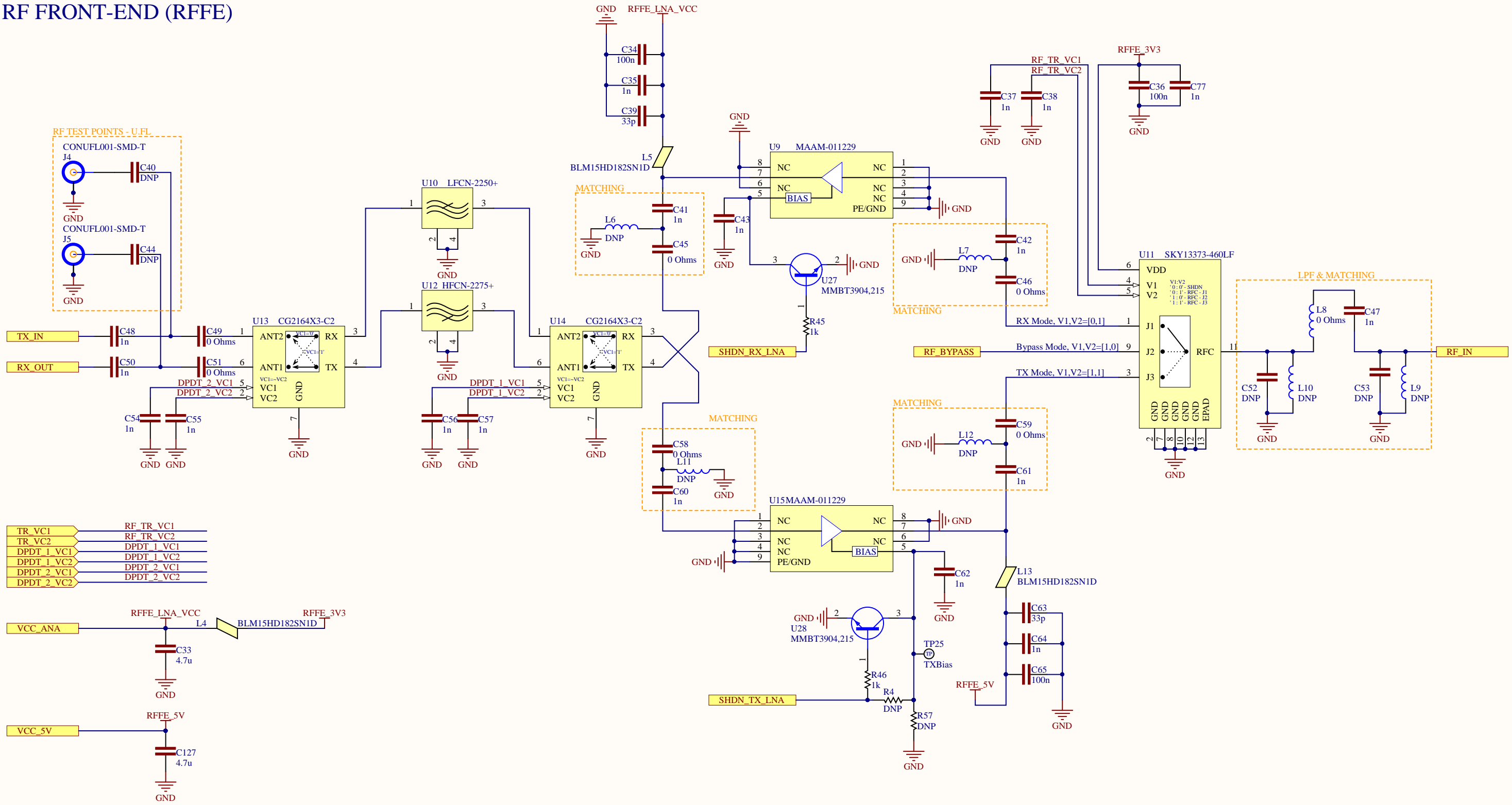
Configuration Resistors - Place 10k for pulldown as needed
Apply internal FPGA pullups on all config pins



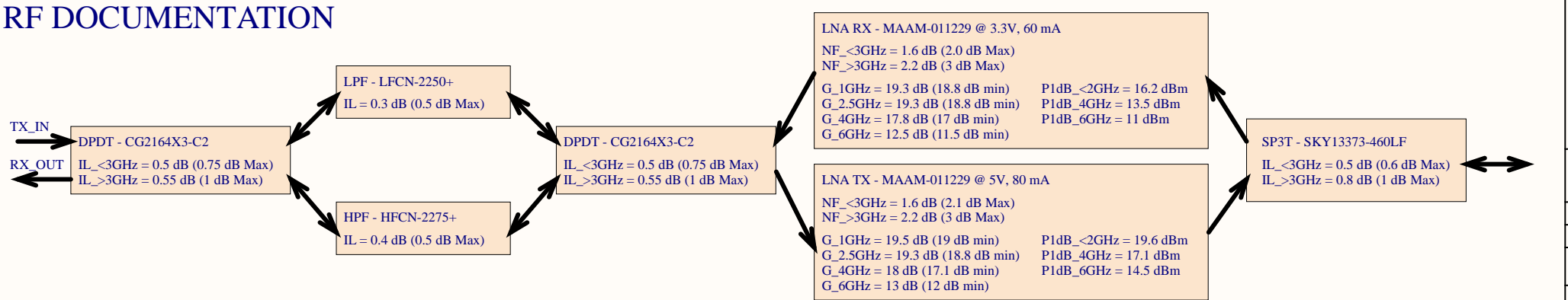
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TITLE FPGA ICE40LP		PRODUCT NAME / P/N CaribouLite / CARIBOULITE-V2		<div> www.cariboulabs.co Open Source RF Tools</div>
DESIGNER: DM				
REVIEWER: -				
DATE: 7/7/2021		REV: B		
SIZE A3	DRAWING NO. DN00001	SHT 4	OF 7	
<div> open source hardware</div>				

RF FRONT-END (RFFE)



RF DOCUMENTATION



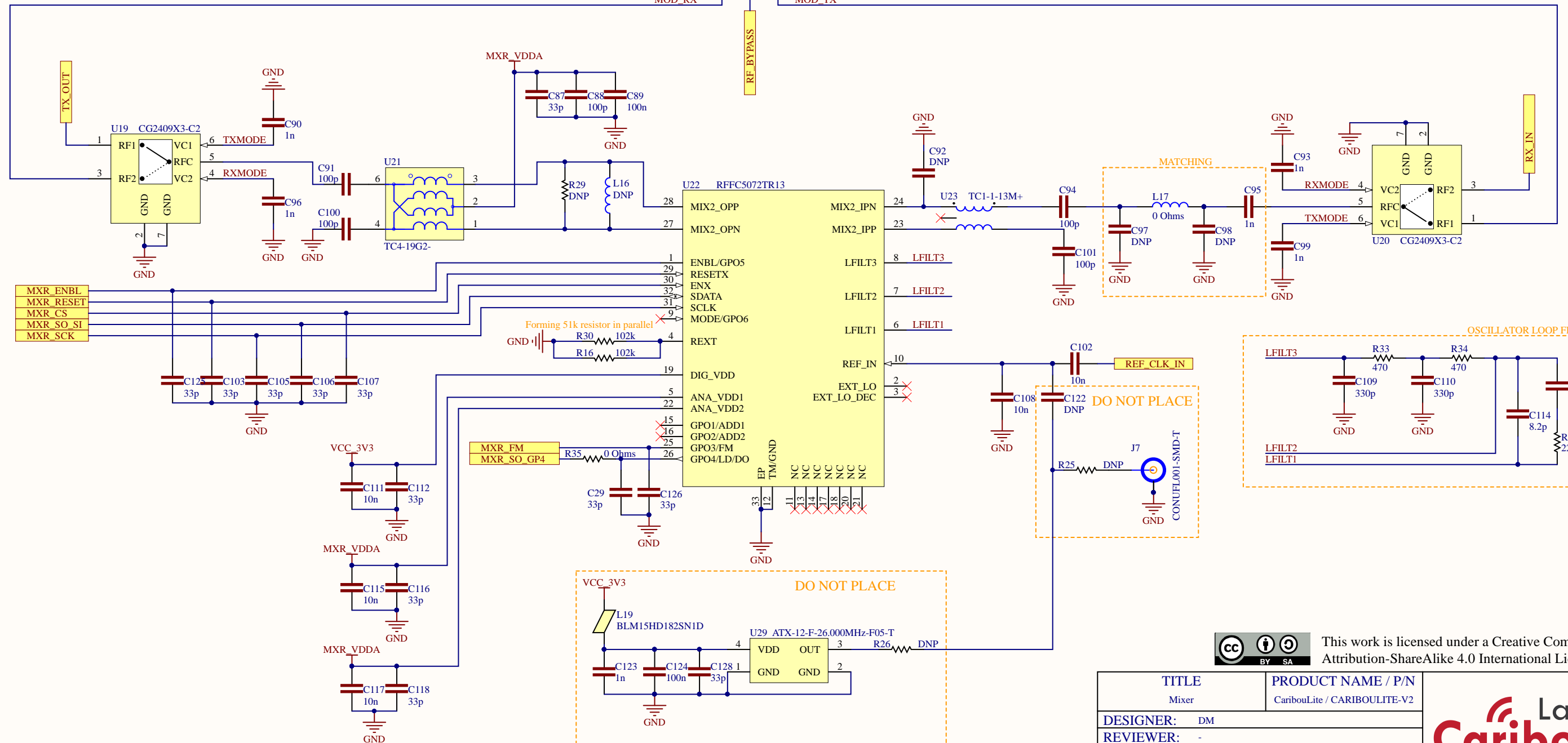
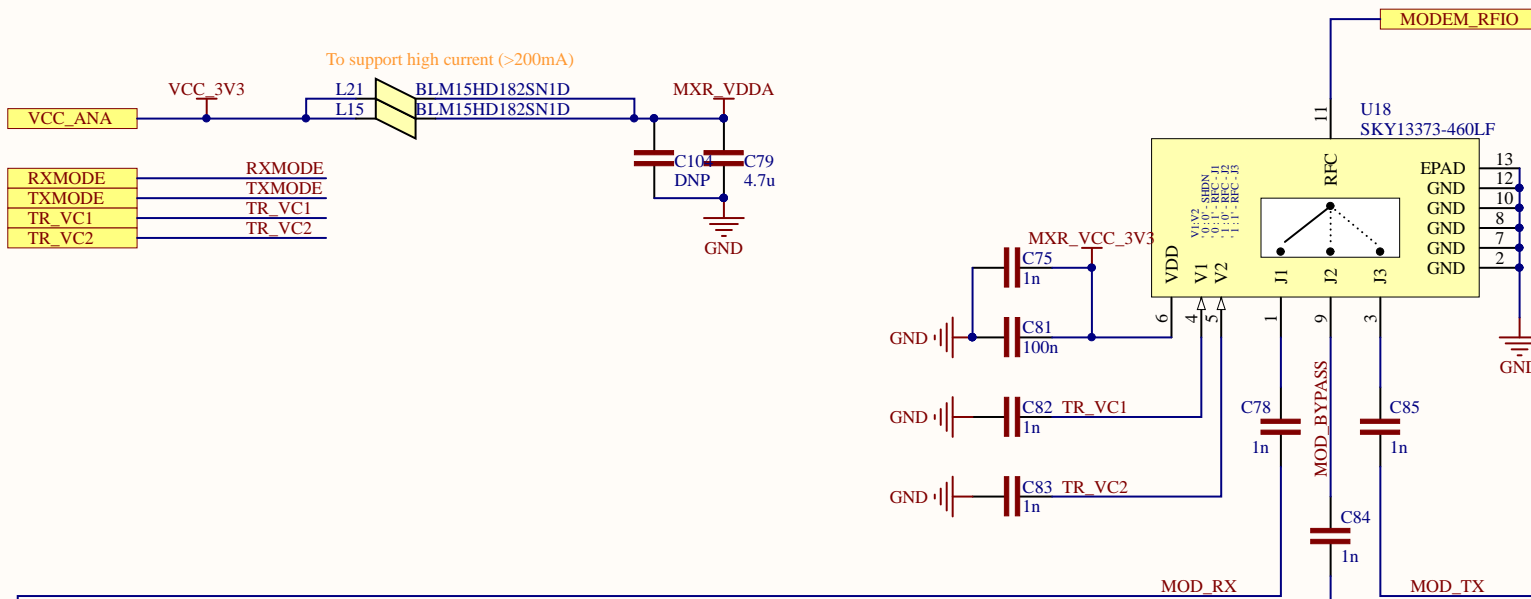
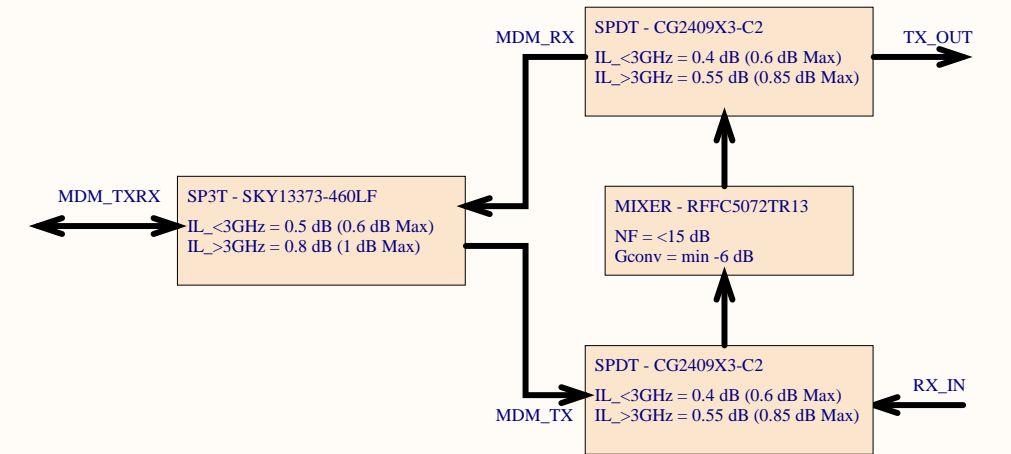
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TITLE		PRODUCT NAME / P/N	
RF Front-End		CaribouLite / CARIBOULITE-V2	
DESIGNER:		DM	
REVIEWER:		-	
DATE:		6/27/2021	REV: B
SIZE	DRAWING NO.	SHT	OF
A3	DN00001	5	7




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Open Source RF Tools

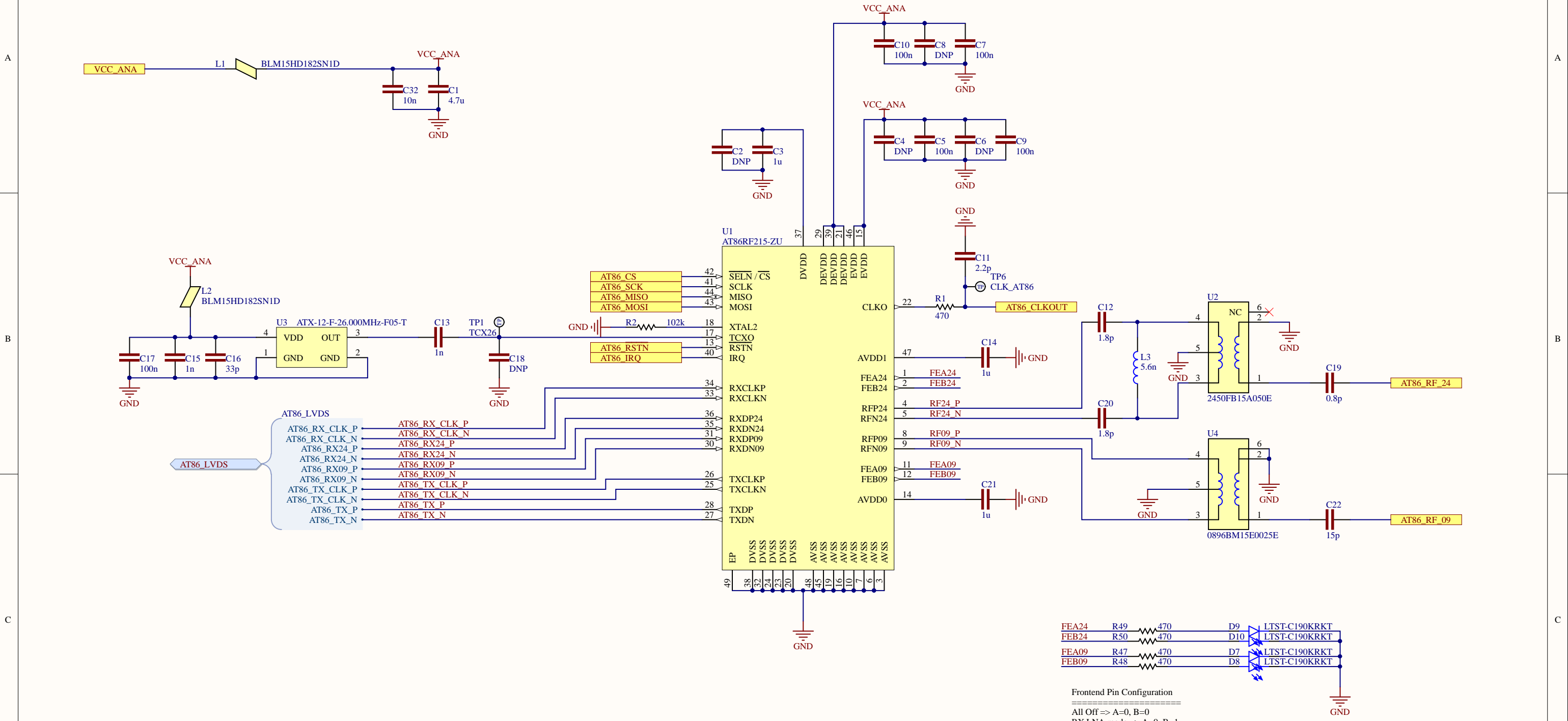
MIXER - QORVO RFFC5072



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TITLE Mixer		PRODUCT NAME / P/N CaribouLite / CARIBOULITE-V2		 www.cariboulabs.co Open Source RF Tools
DESIGNER: DM				
REVIEWER: -				
DATE: 6/28/2021		REV: B		
SIZE A3	DRAWING NO. DN00001	SHT 6	OF 7	

MODEM - AT86RF215



RF DOCUMENTATION

