

LDOs / DC-DCs


CONNECTORS / SWITCHES


DIGITAL IC

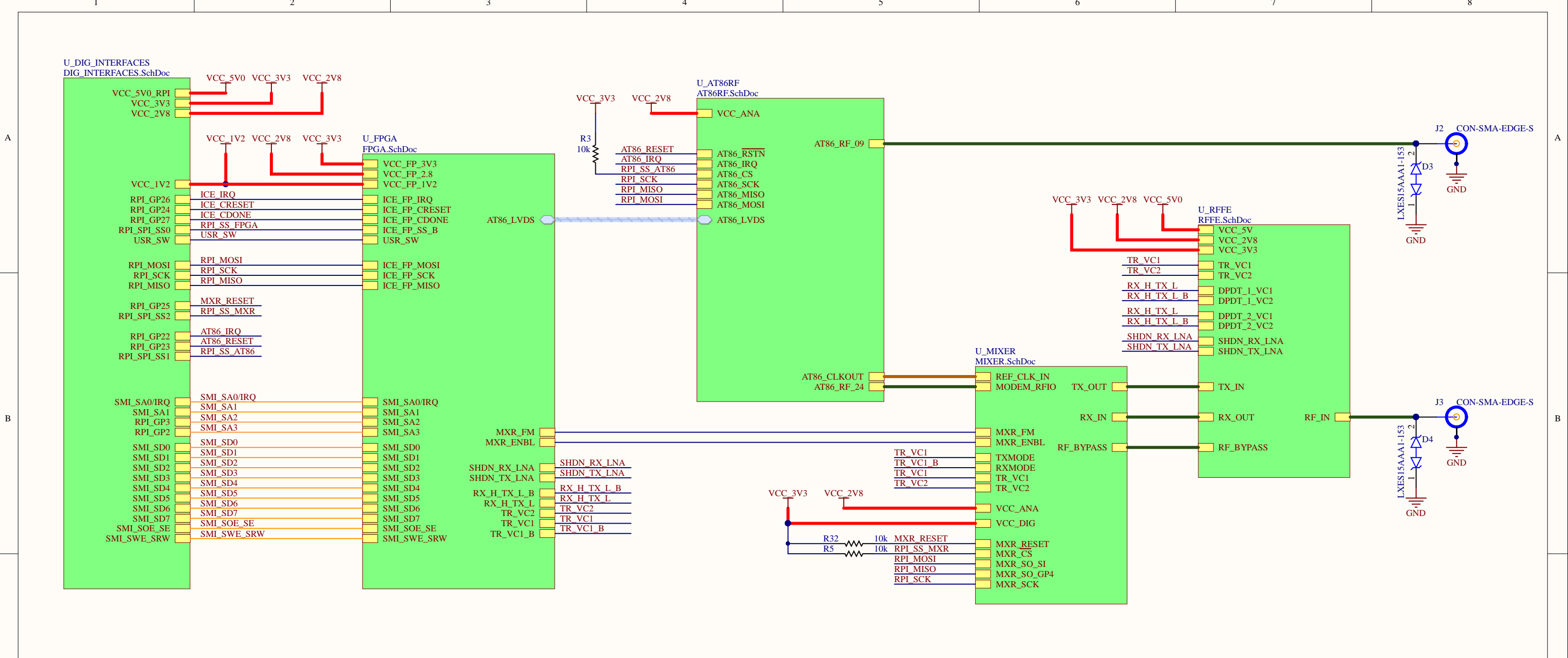
ANALOG / MIXED IC



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TITLE Block Diagrams		PRODUCT NAME / P/N CaribouLite / CARIBOULITE-V2		<div> <a href="http://www.cariboulabs.co">www.cariboulabs.co</a> Open Source RF Tools</div>
DESIGNER: DM				
REVIEWER: -				
DATE: 6/18/2021		REV: B		
SIZE A3	DRAWING NO. DN00001	SHT 1	OF 7	

  
open source hardware



MF3

MF2

MF1

FIDUCIALFIDUCIALFIDUCIAL

MF6

MF5

MF4

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U\_TITLE

TITLE.SchDoc

RFFE MODE	TR_VC1	TR_VC2	RX_H_TX_L	~RX_H_TX_L	RX_H_TX_L	~RX_H_TX_L	MXRMODE	TR_VC1	TR_VC2	~TR_VC1	TR_VC1	TR_VC2
MODE	TR_VC1	TR_VC2	DPDT_1_VC1	DPDT_1_VC2	DPDT_2_VC1	DPDT_2_VC2	MODE	TR_VC1	TR_VC2	RXMODE	TXMODE	MXR_RESET
OFF	'0'	'0'	'X'	'X'	'X'	'X'	OFF	'0'	'0'	'X'	'X'	'0'
BYPASS	'1'	'0'	'X'	'X'	'X'	'X'	BYPASS	'1'	'0'	'X'	'X'	'0'
RX LOWPASS	'0'	'1'	'1'	'0'	'1'	'0'	RX	'0'	'1'	'1'	'0'	'1'
RX HIPASS	'0'	'1'	'0'	'1'	'0'	'1'	RX	'0'	'1'	'1'	'0'	'1'
TX LOWPASS	'1'	'1'	'0'	'1'	'0'	'1'	TX	'1'	'1'	'0'	'1'	'1'
TX HIPASS	'1'	'1'	'1'	'0'	'1'	'0'	TX	'1'	'1'	'0'	'1'	'1'

CHANGE LOG

[06/04/2021] added C125, C126 for ASM (33pF I/O filters)

[06/04/2021] changed C25, C127 to 10V alternative 4.7uF

[28/04/2021] EN\_2V8 signal moved to pin B32@U16 (FPGA) - 3.3V Bank

[09/05/2021] connected A44, B34 @ FPGA to GND for flow

[02/06/2021] EN\_2V8 signal was cancelled and the LDO always on

[02/06/2021] FPGA config flash removed together with all res / caps

[02/06/2021] reversed MISO / MOSI on FPGA as should be

[02/06/2021] Mixer - removed PLL Lock on GPO4, connected to MISO

[02/06/2021] Mixer - separated VCC\_ANA and VDD\_DIG (3.3V vs 2.8V)

[02/06/2021] Removed external clock secondary for FPGA

[02/06/2021] FPGA added additional output for IRQ

CC

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TITLE

Top Level Design

PRODUCT NAME / P/N

CaribouLite / CARIBOULITE-V2

DESIGNER: DM

REVIEWER: -

DATE: 6/18/2021

REV: B

SIZE A3

DRAWING NO. DN00001

SHT 2

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## A



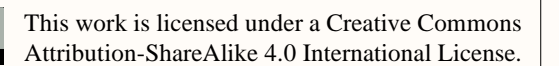
## B



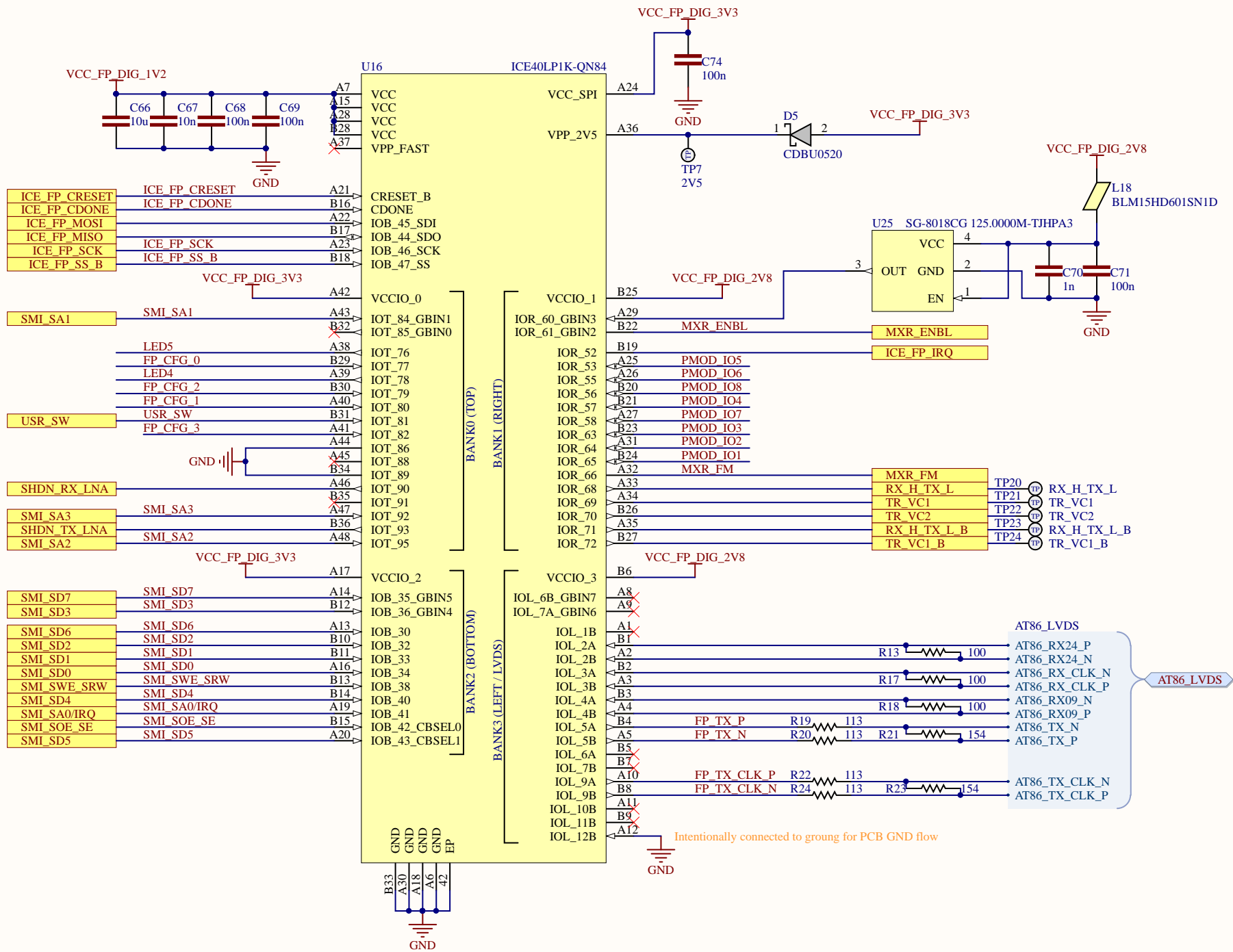
NOTE: Dual function - WP for HAT EEPROM



## C

D

FPGA



LVDS Negated Pairs

AT86\_TX  
AT86\_RX09  
AT86\_TX\_CLK

The other two are direct logic.

PROGRAMMING

POR=> Check SS  
1. if SS='1' => if NVCM programmed, use NVCM, otherwise use external flash (SPI MASTER).  
2. if SS='0', wait to be configured from external controller through SPI

RESET - restarts the configuration  
CDONE - before configuration finished is '0', When done turns '1'

Calculation of differential lines

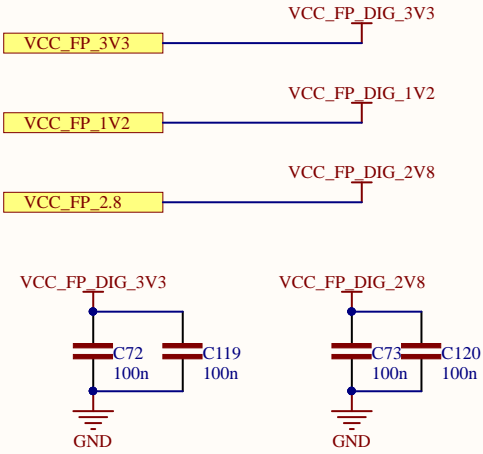
VCCIO = 2.8V  
VOD = 0.5V (this is the differential swing nominal)  
Rouput = 30 Ohms (given by ICE40 Specs)

The parallel output resistor:  
 $R_p = 2 * (50 * 2.8 / (2.8 - (2 * 0.5))) = 280 / 1.8 = 155 \text{ Ohms}$

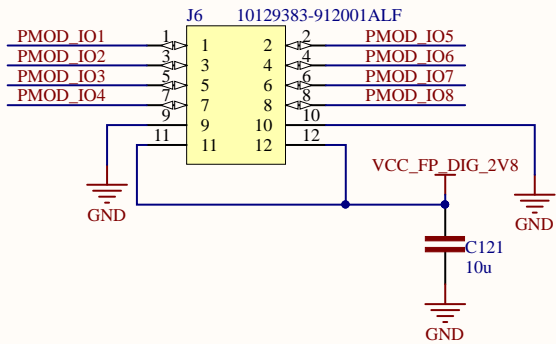
The series output resistors:  
 $R_s = (50 * 77) / (77 - 50) - 30 = 112 \text{ Ohms}$

Connect the positive or true polarity side of the differential pair to the DPxxA input and the negative or complementary side of the pair to the DPxxB input.  
==== If it is easier to route the differential pair, the input pins can be swapped, which produces an inverted input value. =====  
====The inverted input value can subsequently be inverted by logic within the FPGA. =====

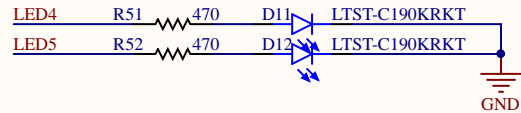
POWER TERMINALS



PMOD




LEDS



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TITLE FPGA ICE40LP		PRODUCT NAME / P/N CaribouLite / CARIBOULITE-V2	
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DATE: 6/18/2021		REV:    B	
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## A

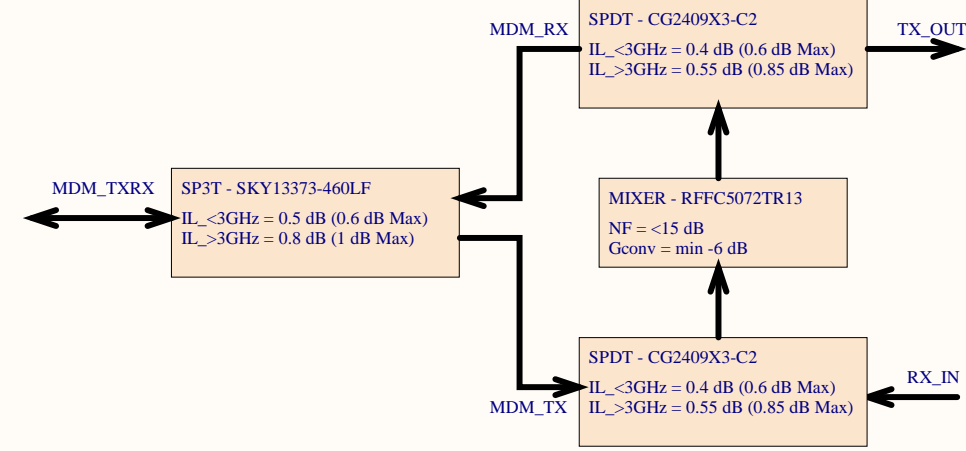
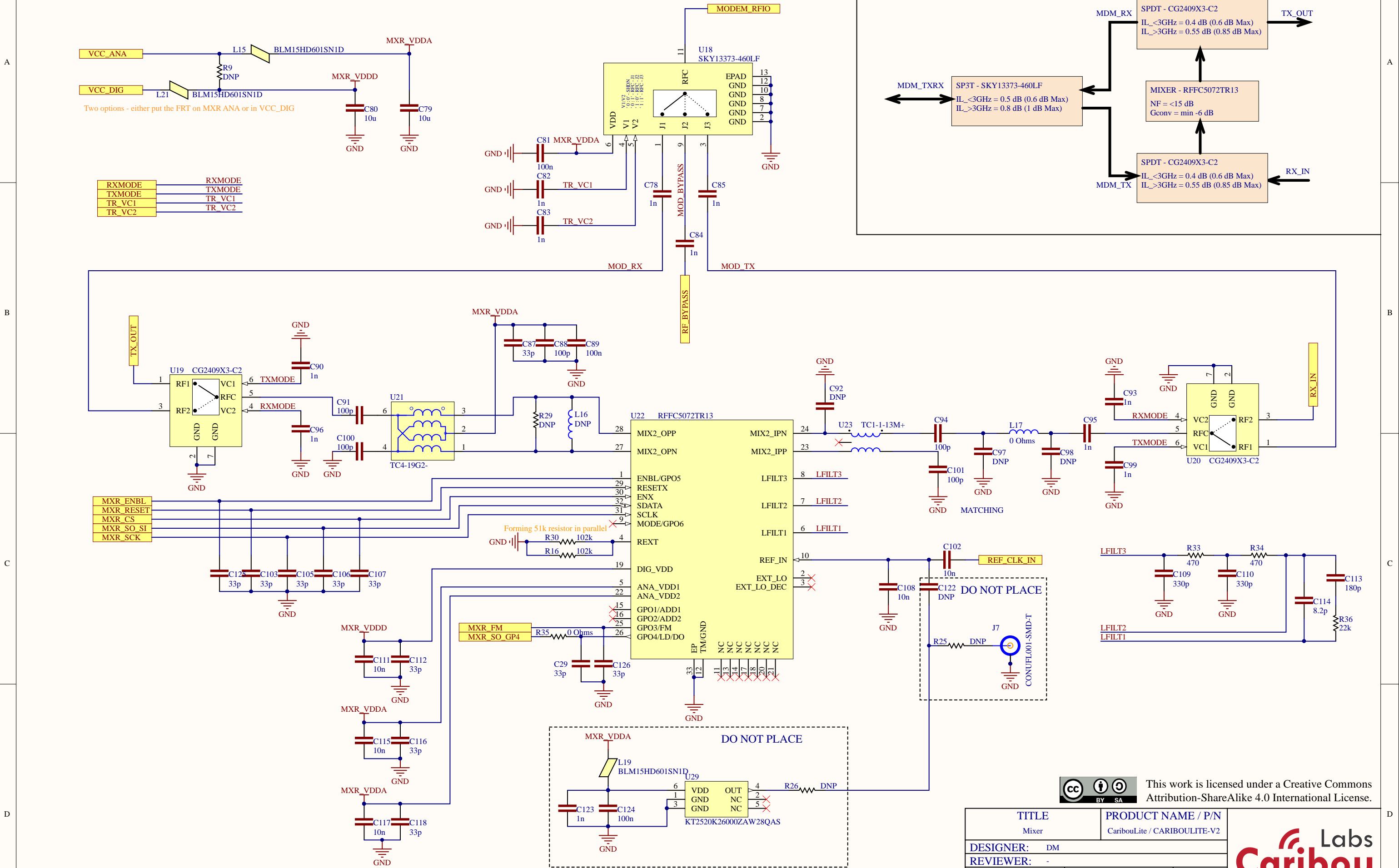


## D




MIXER - QORVO RFFC5072

RF DOCUMENTATION



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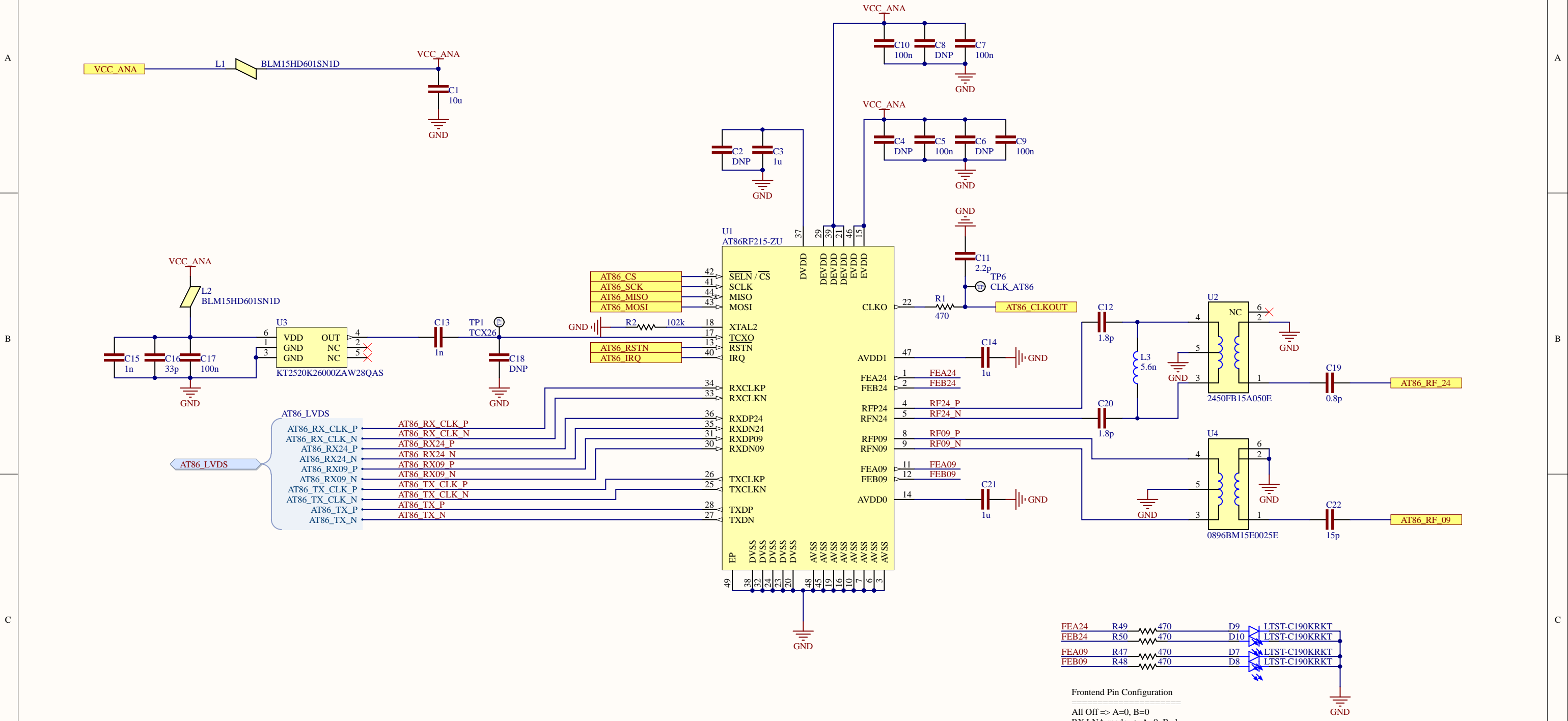
TITLE		PRODUCT NAME / P/N	
Mixer		CaribouLite / CARIBOULITE-V2	
DESIGNER:		DM	
REVIEWER:		-	
DATE: 6/18/2021		REV: B	
SIZE A3	DRAWING NO. DN00001	SHT 6	OF 7



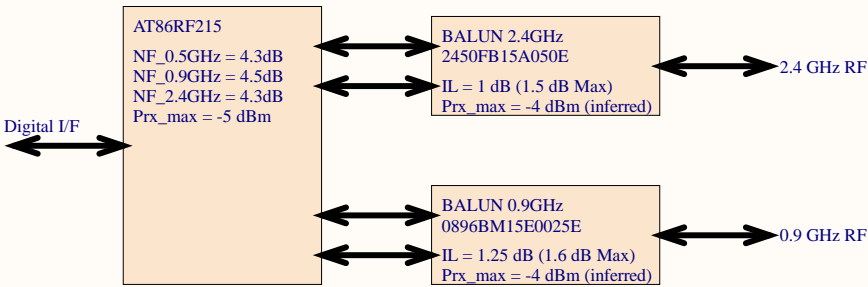
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MODEM - AT86RF215



RF DOCUMENTATION





FEA24 R49 470 D9 LTST-C190KRKT  
FEB24 R50 470 D10 LTST-C190KRKT  
FEA09 R47 470 D7 LTST-C190KRKT  
FEB09 R48 470 D8 LTST-C190KRKT

Frontend Pin Configuration  
=====

All Off => A=0, B=0  
RX LNA mode => A=0, B=1  
TX mode => A=1, B=0  
RX Bypass => A=1, B=1



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TITLE Modem and TCXO		PRODUCT NAME / P/N CaribouLite / CARIBOULITE-V2		<div> <a href="http://www.cariboulabs.co">www.cariboulabs.co</a> Open Source RF Tools</div>
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