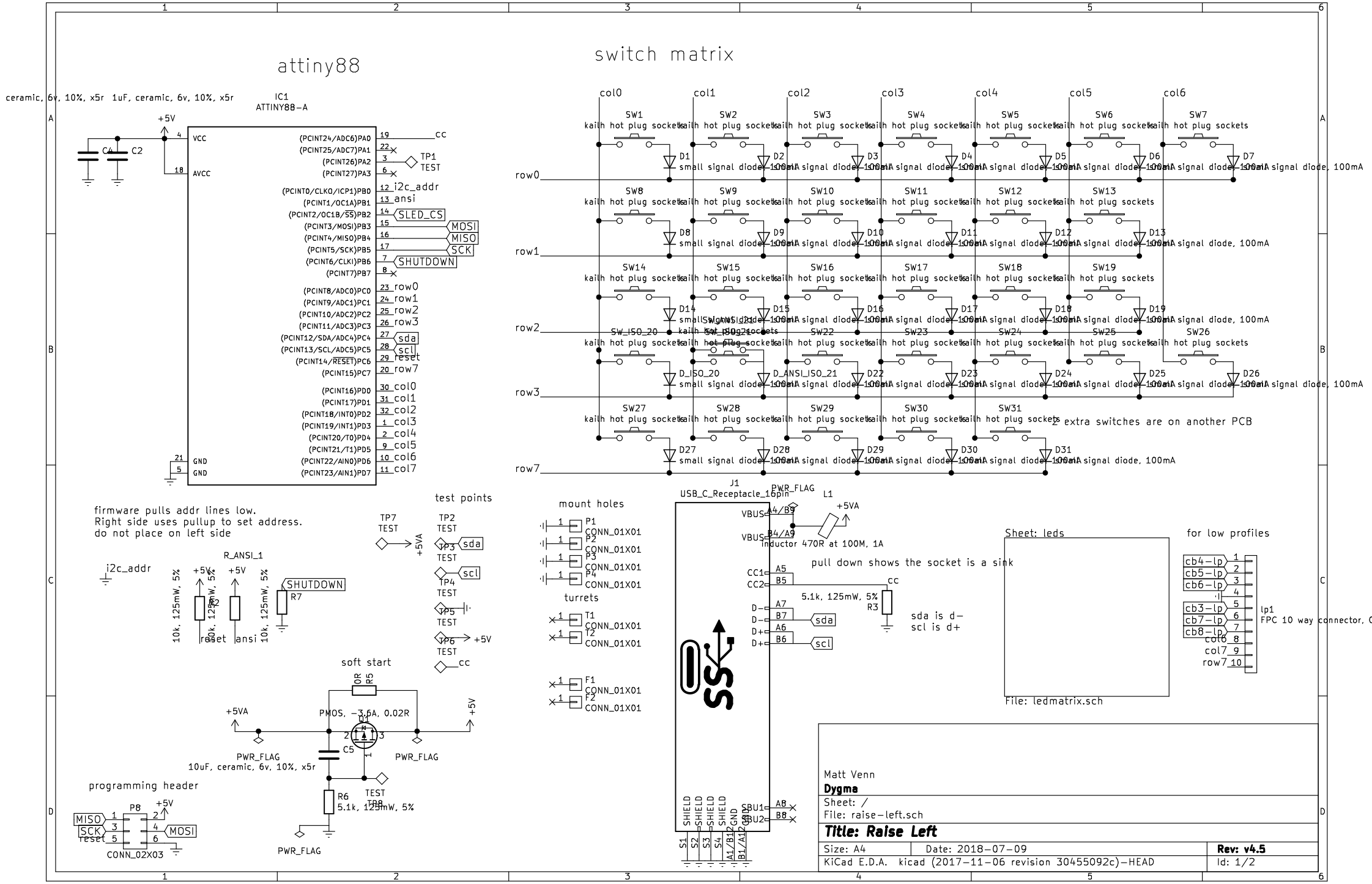
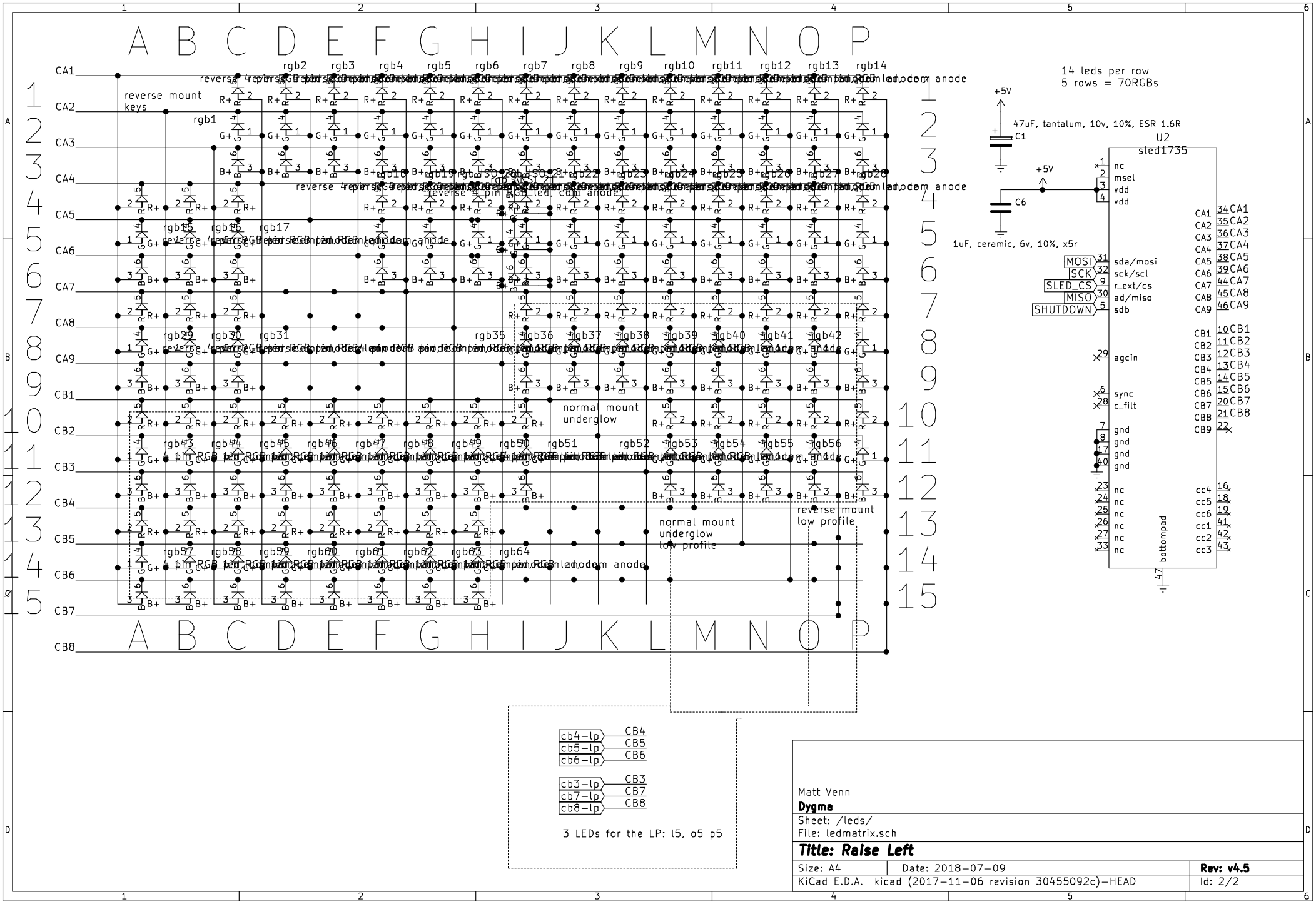

attiny88
switch matrix
IC1
ATTINY88-A
ceramic, 6v, 10%, x5r
1uF, ceramic, 6v, 10%, x5r
+5V
C4
C2
VCC
AVCC
GND
(PCINT24/ADC6)PA0
(PCINT25/ADC7)PA1
(PCINT26)PA2
(PCINT27)PA3
(PCINT0/CLKO/ICP1)PB0
(PCINT1/OC1A)PB1
(PCINT2/OC1B/SS)PB2
(PCINT3/MOSI)PB3
(PCINT4/MISO)PB4
(PCINT5/SCK)PB5
(PCINT6/CLKI)PB6
(PCINT7)PB7
(PCINT8/ADC0)PC0
(PCINT9/ADC1)PC1
(PCINT10/ADC2)PC2
(PCINT11/ADC3)PC3
(PCINT12/SDA/ADC4)PC4
(PCINT13/SCL/ADC5)PC5
(PCINT14/RESET)PC6
(PCINT15)PC7
(PCINT16)PD0
(PCINT17)PD1
(PCINT18/INT0)PD2
(PCINT19/INT1)PD3
(PCINT20/T0)PD4
(PCINT21/T1)PD5
(PCINT22/AIN0)PD6
(PCINT23/AIN1)PD7
cc
TP1
TEST
i2c_addr
ansi
SLED_CS
MOSI
MISO
SCK
SHUTDOWN
row0
row1
row2
row3
sda
scl
reset
row7
col0
col1
col2
col3
col4
col5
col6
col7
firmware pulls addr lines low.
Right side uses pullup to set address.
do not place on left side
test points
TP7
TEST
+5VA
TP2
TP3
TP4
TP5
TP6
R_ANSI_1
R2
R7
10k, 125mW, 5%
soft start
OR
R5
PMOS, -3.6A, 0.02R
Q1
C5
10uF, ceramic, 6v, 10%, x5r
PWR_FLAG
R6
5.1k, 125mW, 5%
TP8
programming header
P8
CONN_02X03
mount holes
P1
P2
P3
P4
CONN_01X01
turrets
T1
T2
F1
F2
J1
USB_C_Receptacle_16pin
VBUS
CC1
CC2
D-
D+
SHIELD
GND
SBU1
SBU2
S1
S2
S3
S4
A1/B12
B1/A12
L1
inductor 470R at 100M, 1A
pull down shows the socket is a sink
5.1k, 125mW, 5%
R3
sda is d-
scl is d+
Sheet: leds
File: ledmatrix.sch
for low profiles
cb4-lp
cb5-lp
cb6-lp
cb3-lp
cb7-lp
cb8-lp
lp1
FPC 10 way connector, 0
Matt Venn
Dygma
Sheet: /
File: raise-left.sch
Title: Raise Left
Size: A4
Date: 2018-07-09
Rev: v4.5
KiCad E.D.A. kicad (2017-11-06 revision 30455092c)-HEAD
Id: 1/2

common anode type 3 matrix