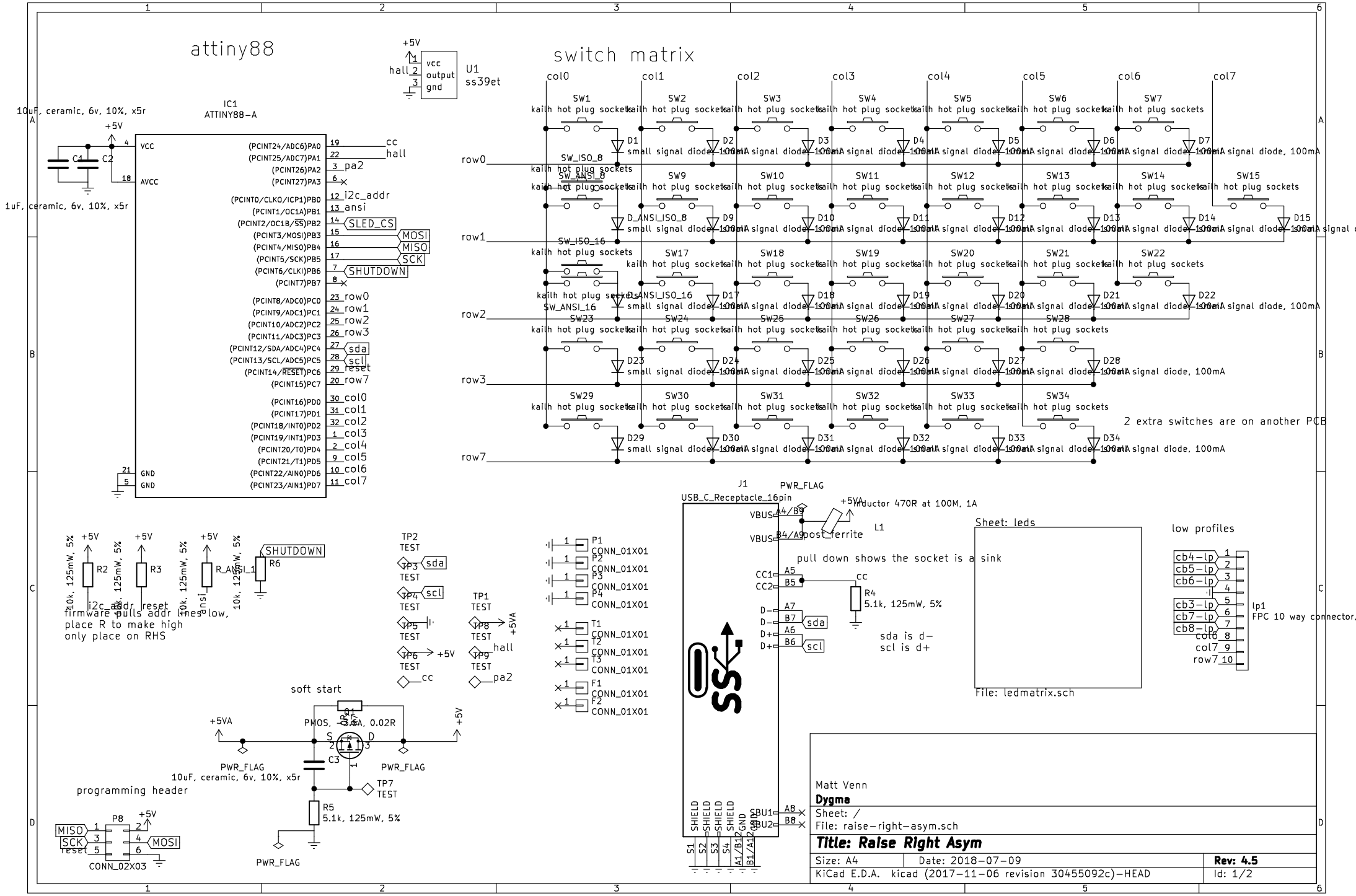
attiny88
IC1
ATTINY88-A
10uF, ceramic, 6v, 10%, x5r
1uF, ceramic, 6v, 10%, x5r
C1
C2
+5V
VCC
AVCC
GND
(PCINT24/ADC6)PA0
(PCINT25/ADC7)PA1
(PCINT26)PA2
(PCINT27)PA3
(PCINT0/CLKO/ICP1)PB0
(PCINT1/OC1A)PB1
(PCINT2/OC1B/SS)PB2
(PCINT3/MOSI)PB3
(PCINT4/MISO)PB4
(PCINT5/SCK)PB5
(PCINT6/CLKI)PB6
(PCINT7)PB7
(PCINT8/ADC0)PC0
(PCINT9/ADC1)PC1
(PCINT10/ADC2)PC2
(PCINT11/ADC3)PC3
(PCINT12/SDA/ADC4)PC4
(PCINT13/SCL/ADC5)PC5
(PCINT14/RESET)PC6
(PCINT15)PC7
(PCINT16)PD0
(PCINT17)PD1
(PCINT18/INT0)PD2
(PCINT19/INT1)PD3
(PCINT20/T0)PD4
(PCINT21/T1)PD5
(PCINT22/AIN0)PD6
(PCINT23/AIN1)PD7
cc
hall
pa2
i2c_addr
ansi
SLED_CS
MOSI
MISO
SCK
SHUTDOWN
row0
row1
row2
row3
sda
scl
reset
row7
col0
col1
col2
col3
col4
col5
col6
col7
U1
ss39et
vcc
output
gnd
switch matrix
kailh hot plug sockets
small signal diode, 100mA
SW_ISO_8
SW_ANSI_8
D_ANSI_ISO_8
SW_ISO_16
SW_ANSI_16
D_ANSI_ISO_16
2 extra switches are on another PCB
R2
R3
R_ANSI_1
R6
10k, 125mW, 5%
firmware pulls addr lines low,
place R to make high
only place on RHS
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TP9
TEST
P1
P2
P3
P4
T1
T2
T3
F1
F2
CONN_01X01
soft start
PMOS, 3.6A, 0.02R
Q1
+5VA
PWR_FLAG
C3
R5
5.1k, 125mW, 5%
programming header
P8
CONN_02X03
J1
USB_C_Receptacle_16pin
VBUS
CC1
CC2
D-
D+
SBU1
SBU2
SHIELD
GND
R4
5.1k, 125mW, 5%
pull down shows the socket is a sink
sda is d-
scl is d+
L1
Inductor 470R at 100M, 1A
post ferrite
Sheet: leds
File: ledmatrix.sch
low profiles
cb4-lp
cb5-lp
cb6-lp
cb3-lp
cb7-lp
cb8-lp
col6
col7
row7
lp1
FPC 10 way connector, 0.5
Matt Venn
Dygma
Sheet: /
File: raise-right-asym.sch
Title: Raise Right Asym
Size: A4
Date: 2018-07-09
Rev: 4.5
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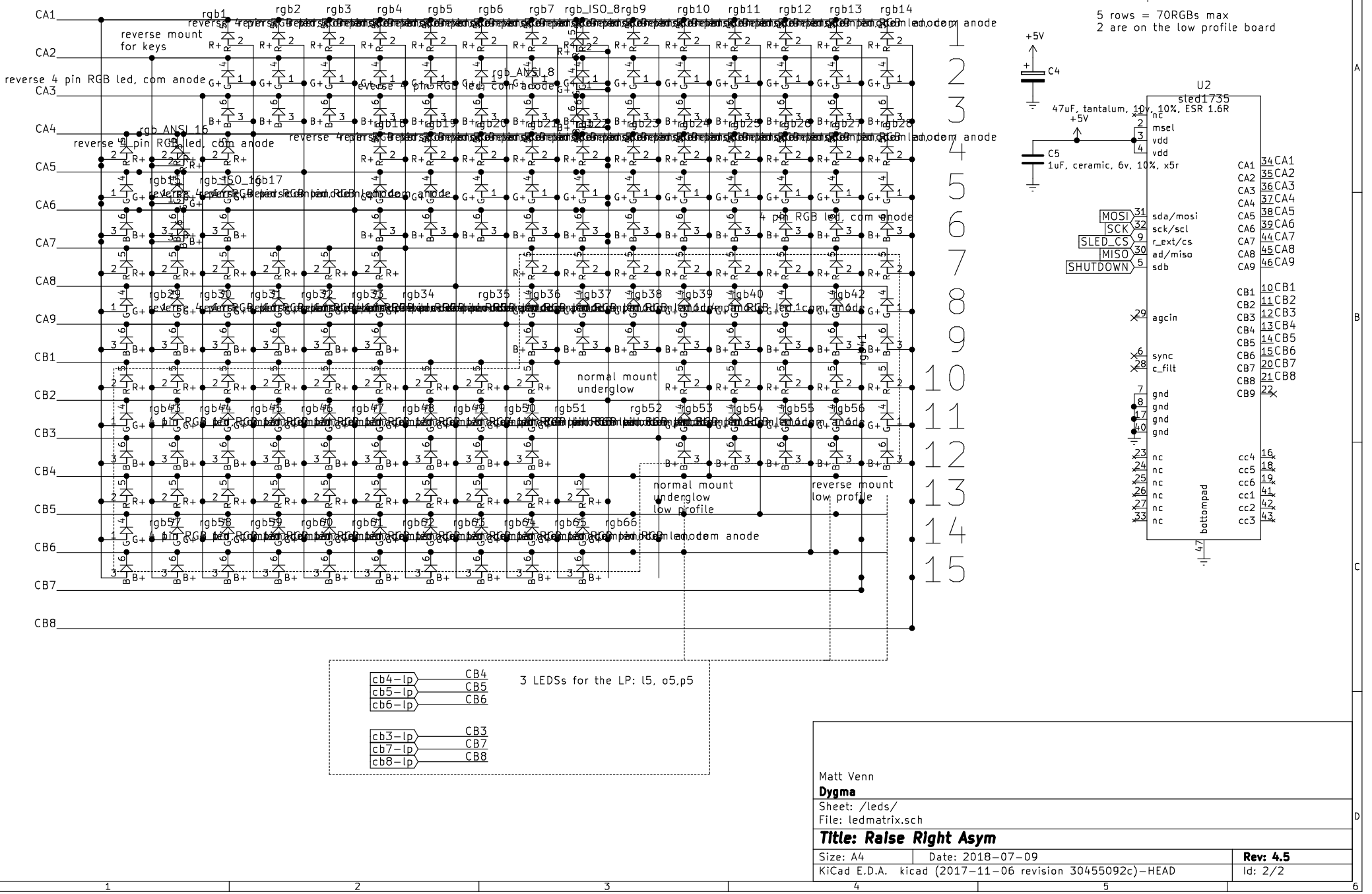
common anode type 3 matrix



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Dygma

Sheet: /leds/

File: ledmatrix.sch

Title: Raise Right Asym

Size: A4	Date: 2018-07-09	**Rev: 4.5**
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