DAC0830/DAC0832 8-Bit µP Compatible, Double-Buffered D to A Converters

Check for Samples: DAC0830, DAC0832

FEATURES

- **Double-Buffered, Single-Buffered or Flow-Through Digital Data Inputs**
- **Easy Interchange and Pin-Compatible with 12-bit DAC1230 Series**
- **Direct Interface to All Popular Microprocessors**
- **Linearity Specified with Zero and Full Scale Adjust Only—NOT BEST STRAIGHT LINE FIT.**
- **Works with ±10V Reference-Full 4-Quadrant Multiplication**
- **Can Be Used in the Voltage Switching Mode**
- **Logic Inputs Which Meet TTL Voltage Level Specs (1.4V Logic Threshold)**
- **Operates "STAND ALONE" (without µP) if Desired**
- **Available in 20-Pin SOIC or PLCC Package**

KEY SPECIFICATIONS

- **Current Settling Time: 1 µs**
- **Resolution: 8 bits**
- **Linearity: 8, 9, or 10 bits (Ensured Over Temp.)**
- **Gain Tempco: 0.0002% FS/°C**
- **Low Power Dissipation: 20 mW**
- **Single Power Supply: 5 to 15 V_{DC}**

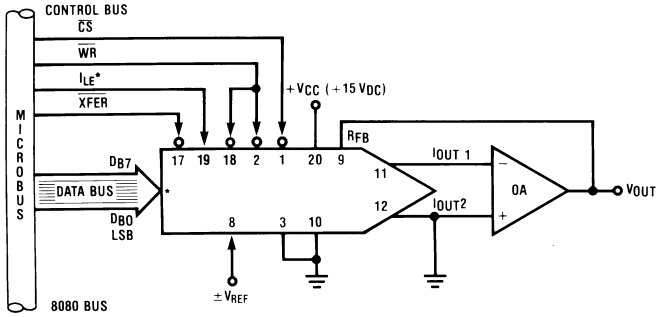
DESCRIPTION

The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z80®, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.

Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.

The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DACs (MICRO-DAC).

Typical Application



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Connection Diagrams

(Top Views)

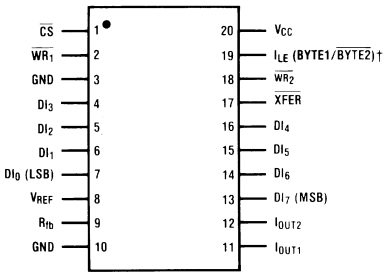


Figure 1. PDIP, CDIP, and SOIC Packages

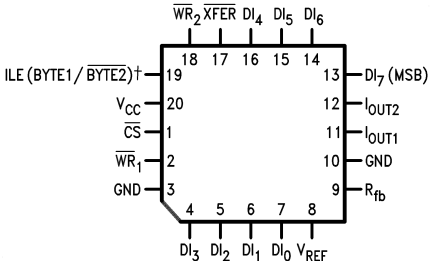


Figure 2. PLCC Package

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)(3)

Supply Voltage (V_{CC})			17 V_{DC}	
Voltage at Any Digital Input			V_{CC} to GND	
Voltage at V_{REF} Input			±25V	
Storage Temperature Range		−65°C to +150°C	Package Dissipation at T_A=25°C(4)	500 mW
			DC Voltage Applied to I_{OUT1} or I_{OUT2}(5)	−100 mV to V_{CC}
ESD Susceptability(5)(6)			800V	
Lead Temperature (Soldering, 10 sec.)	PDIP Package (plastic)		260°C	
	CDIP Package (ceramic)		300°C	
	SOIC Package	Vapor Phase (60 sec.)	215°C	
		Infrared (15 sec.)	220°C	

(1) All voltages are measured with respect to GND, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{JMAX} = 125°C (plastic) or 150°C (ceramic), and the typical junction-to-ambient thermal resistance of the J package when board mounted is 80°C/W. For the NFH package, this number increases to 100°C/W and for the FN package this number is 120°C/W.
(5) For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if V_{REF} = 10V then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.
(6) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Operating Conditions

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	Part numbers with "LCN" suffix	0°C to +70°C
		Part numbers with "LCWM" suffix	0°C to +70°C
		Part numbers with "LCV" suffix	0°C to +70°C
		Part numbers with "LCJ" suffix	−40°C to +85°C
		Part numbers with "LJ" suffix	−55°C to +125°C
		Voltage at Any Digital Input	V_{CC} to GND

Electrical Characteristics

V_{REF}=10.000 V_{DC} unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** (1) For all other limits T_A=25°C.

Parameter	Conditions		See Note	V_{CC} = 4.75 V_{DC} V_{CC} = 15.75 V_{DC}		V_{CC} = 5 V_{DC} ±5% V_{CC} = 12 V_{DC} ±5% to 15 V_{DC} ±5%	Limit Units (2)
				Typ (3)	Tested Limit (4)	Design Limit (5)	
CONVERTER CHARACTERISTICS							
Resolution				8	8	**8**	bits
Linearity Error Max	Zero and full scale adjusted $-10V \le V_{REF} \le +10V$		See (6) and (2)				
DAC0830LJ & LCJ					**0.05**	**0.05**	% FSR
DAC0832LJ & LCJ					**0.2**	**0.2**	% FSR
DAC0830LCN, LCWM & LCV					0.05	**0.05**	% FSR
DAC0831LCN					0.1	**0.1**	% FSR
DAC0832LCN, LCWM & LCV					0.2	**0.2**	% FSR
Differential Nonlinearity Max	Zero and full scale adjusted $-10V \le V_{REF} \le +10V$		See (6) and (2)				
DAC0830LJ & LCJ					**0.1**	**0.1**	% FSR
DAC0832LJ & LCJ					**0.4**	**0.4**	% FSR
DAC0830LCN, LCWM & LCV					0.1	**0.1**	% FSR
DAC0831LCN					0.2	**0.2**	% FSR
DAC0832LCN, LCWM & LCV					0.4	**0.4**	% FSR
Monotonicity	$-10V \le V_{REF} \le +10V$	LJ & LCJ	See (6)		**8**	**8**	bits
		LCN, LCWM & LCV			8	**8**	bits
Gain Error Max	Using Internal R_{fb} $-10V \le V_{REF} \le +10V$		See (7)	±0.2	±1	**±1**	% FS
Gain Error Tempco Max	Using internal R_{fb}			**0.0002**		**0.0006**	% FS/°C

(1) **Boldface** tested limits apply to the LJ and LCJ suffix parts only.
(2) The unit "FSR" stands for "Full Scale Range." "Linearity Error" and "Power Supply Rejection" specs are based on this unit to eliminate dependence on a particular V_{REF} value and to indicate the true performance of the part. The "Linearity Error" specification of the DAC0830 is "0.05% of FSR (MAX)". This ensures that after performing a zero and full scale adjustment (see sections Zero Adjustment and Full-Scale Adjustment), the plot of the 256 analog voltage outputs will each be within 0.05%×V_{REF} of a straight line which passes through zero and full scale.
(3) Typicals are at 25°C and represent most likely parametric norm.
(4) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(5) Ensured, but not 100% production tested. These limits are not used to calculate outgoing quality levels.
(6) For current switching applications, both I_{OUT1} and I_{OUT2} must go to ground or the "Virtual Ground" of an operational amplifier. The linearity error is degraded by approximately $V_{OS} \div V_{REF}$. For example, if V_{REF} = 10V then a 1 mV offset, V_{OS}, on I_{OUT1} or I_{OUT2} will introduce an additional 0.01% linearity error.
(7) Specified at V_{REF}=±10 V_{DC} and V_{REF}=±1 V_{DC}.

Electrical Characteristics (continued)

V_{REF}=10.000 V_{DC} unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.**(1) For all other limits T_A=25°C.

Parameter		Conditions		See Note	V_{CC} = 4.75 V_{DC} V_{CC} = 15.75 V_{DC}		V_{CC} = 5 V_{DC} ±5% V_{CC} = 12 V_{DC} ±5% to 15 V_{DC} ±5%	Limit Units(2)
					Typ(3)	Tested Limit(4)	Design Limit(5)	
Power Supply Rejection		All digital inputs latched high						
		V_{CC}=14.5V to 15.5V			0.0002	0.0025		%
		11.5V to 12.5V			0.0006			FSR/V
		4.5V to 5.5V			0.013	0.015		
Reference Input	Max				**15**	**20**	**20**	kΩ
	Min				**15**	**10**	**10**	kΩ
Output Feedthrough Error		V_{REF}=20 Vp-p, f=100 kHz All data inputs latched low			3			mVp-p
Output Leakage Current Max(8)	I_{OUT1}	All data inputs latched low	LJ & LCJ	See(8)		**100**	**100**	nA
			LCN, LCWM & LCV			50	**100**	
	I_{OUT2}	All data inputs latched high	LJ & LCJ			**100**	**100**	nA
			LCN, LCWM & LCV			50	**100**	
Output Capacitance	I_{OUT1} I_{OUT2}	All data inputs latched low			45 115			pF
	I_{OUT1} I_{OUT2}	All data inputs latched high			130 30			pF
DIGITAL AND DC CHARACTERISTICS								
Digital Input Voltages	Max	Logic Low	LJ: 4.75V			**0.6**		V_{DC}
			LJ: 15.75V			**0.8**		
			LCJ: 4.75V			**0.7**		
			LCJ: 15.75V			**0.8**		
			LCN, LCWM, LCV			0.95	**0.8**	
	Min	Logic High	LJ & LCJ			**2.0**	**2.0**	V_{DC}
			LCN, LCWM, LCV			1.9	**2.0**	
Digital Input Currents	Max	Digital inputs <0.8V	LJ & LCJ		−50	**−200**	**−200**	µA
			LCN, LCWM, LCV			−160	**−200**	µA
		Digital inputs>2.0V	LJ & LCJ		0.1	**+10**	**+10**	µA
			LCN, LCWM, LCV			+8	**+10**	
Supply Current Drain	Max		LJ & LCJ		1.2	**3.5**	**3.5**	mA
			LCN, LCWM, LCV			1.7	**2.0**	

(8) A 100nA leakage current with R_{fb}=20k and V_{REF}=10V corresponds to a zero error of $(100\times10^{-9}\times20\times10^{3})\times100/10$ which is 0.02% of FS.

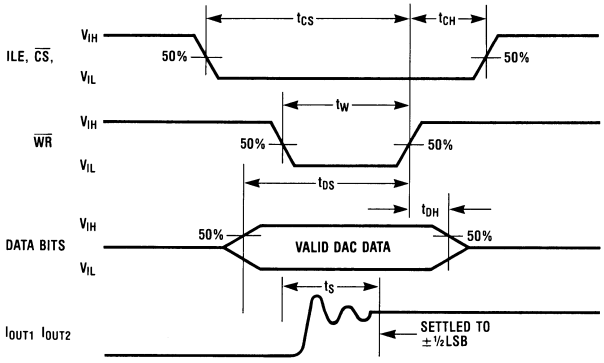
Electrical Characteristics

V_{REF}=10.000 V_{DC} unless otherwise noted. **Boldface limits apply over temperature, $T_{MIN} \le T_A \le T_{MAX}$.** (1) For all other limits T_A=25°C.

Symbol	Parameter	Conditions	See Note	V_{CC}=15.75 V_{DC}		V_{CC}=12 V_{DC}±5% to 15 V_{DC} ±5%	V_{CC}=4.75 V_{DC}		V_{CC}=5 V_{DC}±5%	Limit Units
				Typ (2)	Tested Limit (3)	Design Limit (4)	Typ (2)	Tested Limit (3)	Design Limit (4)	
AC CHARACTERISTICS (5)										
t_s	Current Setting Time	V_{IL}=0V, V_{IH}=5V		1.0			1.0			µs
t_W	Write and XFER Pulse Width Min	V_{IL}=0V, V_{IH}=5V	See (5) See (1)	100	250 **320**	**320**	375	600 **900**	**900**	
t_{DS}	Data Setup Time Min	V_{IL}=0V, V_{IH}=5V	See (1)	100	250 **320**	**320**	375	600 **900**	**900**	
t_{DH}	Data Hold Time Min	V_{IL}=0V, V_{IH}=5V	See (1)		30 **30**			50 **50**		ns
t_{CS}	Control Setup Time Min	V_{IL}=0V, V_{IH}=5V	See (1)	110	250 **320**	**320**	600	900 **1100**	**1100**	
t_{CH}	Control Hold Time Min	V_{IL}=0V, V_{IH}=5V	See (1)	0	0 **0**	**10**	0	0 **0**		

(1) **Boldface** tested limits apply to the LJ and LCJ suffix parts only.
(2) Typicals are at 25°C and represent most likely parametric norm.
(3) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(4) Ensured, but not 100% production tested. These limits are not used to calculate outgoing quality levels.
(5) The entire write pulse must occur within the valid data interval for the specified t_W, t_{DS}, t_{DH}, and t_S to apply.

Switching Waveform



Definition of Package Pinouts

Control Signals

(All control signals level actuated)

$\overline{CS}$: **Chip Select** (active low). The $\overline{CS}$ in combination with ILE will enable $\overline{WR_1}$.

ILE: **Input Latch Enable** (active high). The ILE in combination with $\overline{CS}$ enables $\overline{WR_1}$.

$\overline{WR_1}$: **Write 1.** The active low $\overline{WR_1}$ is used to load the digital input data bits (DI) into the input latch. The data in the input latch is latched when $\overline{WR_1}$ is high. To update the input latch–$\overline{CS}$ and $\overline{WR_1}$ must be low while ILE

is high.

$\overline{WR_2}$: Write 2 (active low). This signal, in combination with $\overline{XFER}$, causes the 8-bit data which is available in the input latch to transfer to the DAC register.

$\overline{XFER}$: Transfer control signal (active low). The $\overline{XFER}$ will enable $\overline{WR_2}$.

Other Pin Functions

DI_0-DI_7: Digital Inputs. DI_0 is the least significant bit (LSB) and DI_7 is the most significant bit (MSB).

I_{OUT1}: DAC Current Output 1. I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in DAC register.

I_{OUT2}: DAC Current Output 2. I_{OUT2} is a constant minus I_{OUT1} , or $I_{OUT1} + I_{OUT2}$ = constant (I full scale for a fixed reference voltage).

R_{fb}: Feedback Resistor. The feedback resistor is provided on the IC chip for use as the shunt feedback resistor for the external op amp which is used to provide an output voltage for the DAC. This on-chip resistor should always be used (not an external resistor) since it matches the resistors which are used in the on-chip R-2R ladder and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input. This input connects an external precision voltage source to the internal R-2R ladder. V_{REF} can be selected over the range of +10 to −10V. This is also the analog voltage input for a 4-quadrant multiplying DAC application.

V_{CC}: Digital Supply Voltage. This is the power supply pin for the part. V_{CC} can be from +5 to $+15V_{DC}$. Operation is optimum for $+15V_{DC}$

GND: The pin 10 voltage must be at the same ground potential as I_{OUT1} and I_{OUT2} for current switching applications. Any difference of potential (V_{OS} pin 10) will result in a linearity change of :

$$\frac{V_{OS} \text{ pin } 10}{3V_{REF}} \quad (1)$$

For example, if V_{REF} = 10V and pin 10 is 9mV offset from I_{OUT1} and I_{OUT2} the linearity change will be 0.03%.

Pin 3 can be offset ±100mV with no linearity change, but the logic input threshold will shift.

Linearity Error

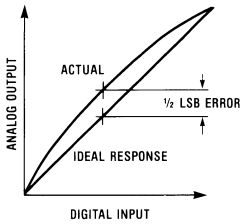


Figure 3. a) End Point Test After Zero and fs adj.

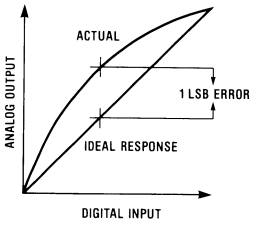


Figure 4. b) Best Straight Line

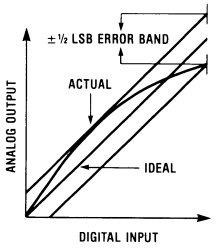


Figure 5. c) Shifting fs adj. to Pass Best Straight Line Test

Definition of Terms

Resolution: Resolution is directly related to the number of switches or bits within the DAC. For example, the DAC0830 has 2^8 or 256 steps and therefore has 8-bit resolution.

Linearity Error: Linearity Error is the maximum deviation from a *straight line passing through the endpoints of the DAC transfer characteristic*. It is measured after adjusting for zero and full-scale. Linearity error is a parameter intrinsic to the device and cannot be externally adjusted.

TI's linearity “end point test” (a) and the “best straight line” test (b,c) used by other suppliers are illustrated above. The “end point test'' greatly simplifies the adjustment procedure by eliminating the need for multiple iterations of checking the linearity and then adjusting full scale until the linearity is met. The “end point test'' ensures that linearity is met after a single full scale adjust. (One adjustment vs. multiple iterations of the adjustment.) The “end point test'' uses a standard zero and F.S. adjustment procedure and is a much more stringent test for DAC linearity.

Power Supply Sensitivity: Power supply sensitivity is a measure of the effect of power supply changes on the DAC full-scale output.

Settling Time: Settling time is the time required from a code transition until the DAC output reaches within ±½LSB of the final output value. Full-scale settling time requires a zero to full-scale or full-scale to zero output change.

Full Scale Error: Full scale error is a measure of the output error between an ideal DAC and the actual device output. Ideally, for the DAC0830 series, full scale is V_{REF} −1LSB. For V_{REF} = 10V and unipolar operation, $V_{FULL-SCALE}$ = 10,0000V–39mV 9.961V. Full-scale error is adjustable to zero.

Differential Nonlinearity: The difference between any two consecutive codes in the transfer curve from the theoretical 1 LSB to differential nonlinearity.

Monotonic: If the output of a DAC increases for increasing digital input code, then the DAC is monotonic. An 8-bit DAC which is monotonic to 8 bits simply means that increasing digital input codes will produce an increasing analog output.

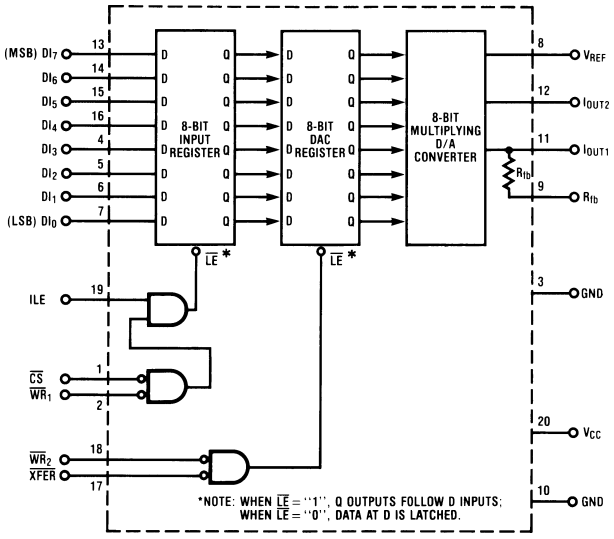


Figure 6. DAC0830 Functional Diagram

Typical Performance Characteristics

Digital Input Threshold vs. Temperature

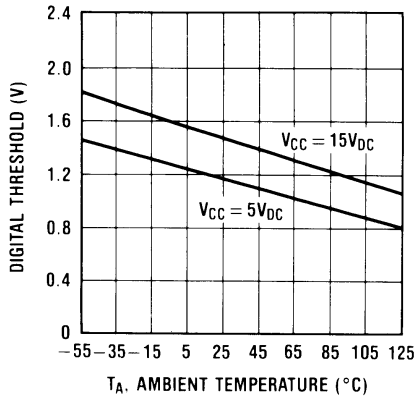


Figure 7.

Digital Input Threshold vs. V_{CC}

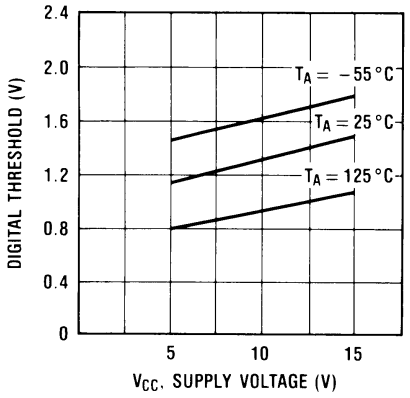


Figure 8.

Gain and Linearity Error Variation vs. Temperature

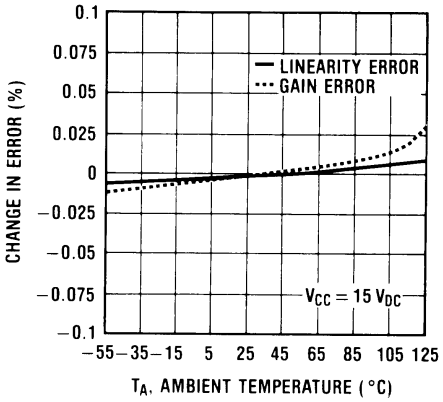


Figure 9.

Gain and Linearity Error Variation vs. Supply Voltage

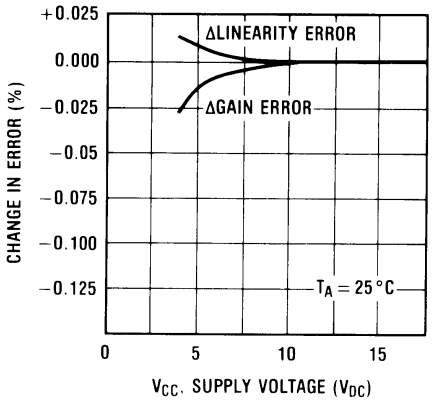


Figure 10.

Write Pulse Width

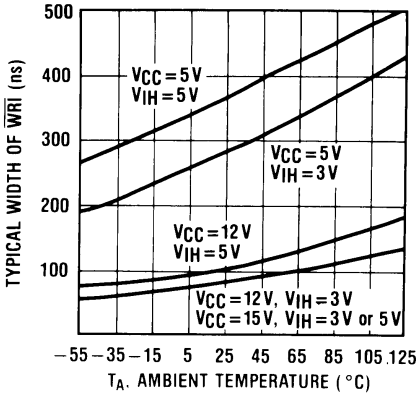


Figure 11.

Data Hold Time

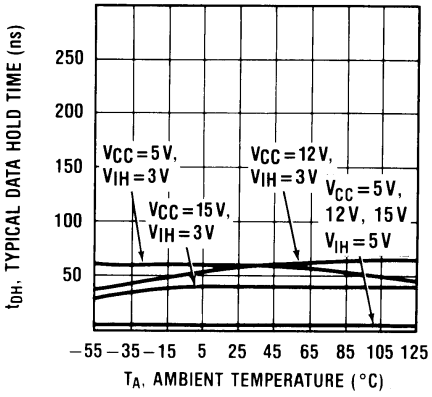


Figure 12.

DAC0830 SERIES APPLICATION HINTS

These DAC's are the industry's first microprocessor compatible, double-buffered 8-bit multiplying D to A converters. Double-buffering allows the utmost application flexibility from a digital control point of view. This 20-pin device is also pin for pin compatible (with one exception) with the DAC1230, a 12-bit MICRO-DAC. In the event that a system's analog output resolution and accuracy must be upgraded, substituting the DAC1230 can be easily accomplished. By tying address bit A_0 to the ILE pin, a two-byte µP write instruction (double precision) which automatically increments the address for the second byte write (starting with A_0="1") can be used. This allows either an 8-bit or the 12-bit part to be used with no hardware or software changes. For the simplest 8-bit application, this pin should be tied to V_{CC} (also see other uses in Double-Buffered Operation).

Analog signal control versatility is provided by a precision R-2R ladder network which allows full 4-quadrant multiplication of a wide range bipolar reference voltage by an applied digital word.

DIGITAL CONSIDERATIONS

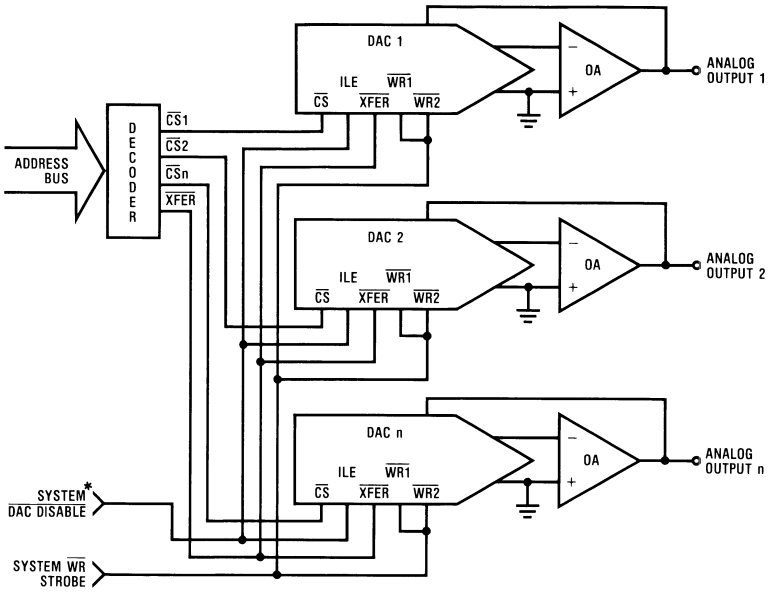
A most unique characteristic of these DAC's is that the 8-bit digital input byte is double-buffered. This means that the data must transfer through two independently controlled 8-bit latching registers before being applied to the R-2R ladder network to change the analog output. The addition of a second register allows two useful control features. First, any DAC in a system can simultaneously hold the current DAC data in one register (DAC register) and the next data word in the second register (input register) to allow fast updating of the DAC output on demand. Second, and probably more important, double-buffering allows any number of DAC's in a system to be updated to their new analog output levels simultaneously via a common strobe signal.

The timing requirements and logic level convention of the register control signals have been designed to minimize or eliminate external interfacing logic when applied to most popular microprocessors and development systems. It is easy to think of these converters as 8-bit "write-only" memory locations that provide an analog output quantity. All inputs to these DAC's meet TTL voltage level specs and can also be driven directly with high voltage CMOS logic in non-microprocessor based systems. To prevent damage to the chip from static discharge, all unused digital inputs should be tied to V_{CC} or ground. If any of the digital inputs are inadvertantly left floating, the DAC interprets the pin as a logic "1".

Double-Buffered Operation

Updating the analog output of these DAC's in a double-buffered manner is basically a two step or double write operation. In a microprocessor system two unique system addresses must be decoded, one for the input latch controlled by the $\overline{CS}$ pin and a second for the DAC latch which is controlled by the $\overline{XFER}$ line. If more than one DAC is being driven, Figure 13, the $\overline{CS}$ line of each DAC would typically be decoded individually, but all of the converters could share a common $\overline{XFER}$ address to allow simultaneous updating of any number of DAC's. The timing for this operation is shown, Figure 14.

It is important to note that the analog outputs that will change after a simultaneous transfer are those from the DAC's whose input register had been modified prior to the $\overline{XFER}$ command.



*TIE TO LOGIC 1 IF NOT NEEDED (SEE Double-Buffered Operation).

Figure 13. Controlling Mutiple DACs

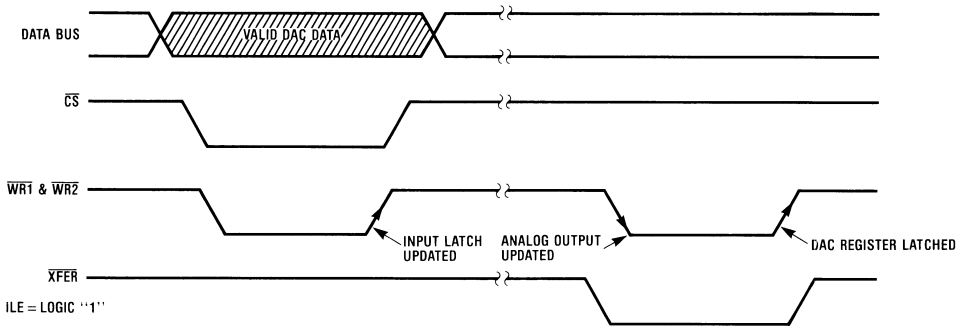
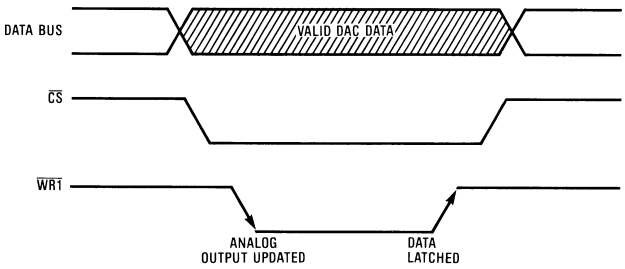


Figure 14.

The ILE pin is an active high chip select which can be decoded from the address bus as a qualifier for the normal $\overline{CS}$ signal generated during a write operation. This can be used to provide a higher degree of decoding unique control signals for a particular DAC, and thereby create a more efficient addressing scheme.

Another useful application of the ILE pin of each DAC in a multiple DAC system is to tie these inputs together and use this as a control line that can effectively "freeze" the outputs of all the DAC's at their present value. Pulling this line low latches the input register and prevents new data from being written to the DAC. This can be particularly useful in multiprocessing systems to allow a processor other than the one controlling the DAC's to take over control of the data bus and control lines. If this second system were to use the same addresses as those decoded for DAC control (but for a different purpose) the ILE function would prevent the DAC's from being erroneously altered.

In a "Stand-Alone" system the control signals are generated by discrete logic. In this case double-buffering can be controlled by simply taking $\overline{CS}$ and $\overline{XFER}$ to a logic "0", ILE to a logic "1" and pulling $\overline{WR_1}$ low to load data to the input latch. Pulling $\overline{WR_2}$ low will then update the analog output. A logic "1" on either of these lines will prevent the changing of the analog output.



ILE=LOGIC "1"; $\overline{WR2}$ and $\overline{XFER}$ GROUNDED

Figure 15.

Single-Buffered Operation

In a microprocessor controlled system where maximum data throughput to the DAC is of primary concern, or when only one DAC of several needs to be updated at a time, a single-buffered configuration can be used. One of the two internal registers allows the data to flow through and the other register will serve as the data latch.

Digital signal feedthrough (see Section Digital Signal Feedthrough) is minimized if the input register is used as the data latch. Timing for this mode is shown in Figure 15.

Single-buffering in a "stand-alone" system is achieved by strobing $\overline{WR}_1$ low to update the DAC with $\overline{CS}$, $\overline{WR}_2$ and $\overline{XFER}$ grounded and ILE tied high.

Flow-Through Operation

Though primarily designed to provide microprocessor interface compatibility, the MICRO-DAC's can easily be configured to allow the analog output to continuously reflect the state of an applied digital input. This is most useful in applications where the DAC is used in a continuous feedback control loop and is driven by a binary up-down counter, or in function generation circuits where a ROM is continuously providing DAC data.

Simply grounding $\overline{CS}$, $\overline{WR}_1$, $\overline{WR}_2$, and $\overline{XFER}$ and tying ILE high allows both internal registers to follow the applied digital inputs (flow-through) and directly affect the DAC analog output.

Control Signal Timing

When interfacing these MICRO-DAC to any microprocessor, there are two important time relationships that must be considered to insure proper operation. The first is the minimum $\overline{WR}$ strobe pulse width which is specified as 900 ns for all valid operating conditions of supply voltage and ambient temperature, but typically a pulse width of only 180ns is adequate if V_{CC}=15V_{DC}. A second consideration is that the specified minimum data hold time of 50ns should be met or erroneous data can be latched. This hold time is defined as the length of time data must be held valid on the digital inputs *after* a qualified (via $\overline{CS}$) $\overline{WR}$ strobe makes a low to high transition to latch the applied data.

If the controlling device or system does not inherently meet these timing specs the DAC can be treated as a slow memory or peripheral and utilize a technique to extend the write strobe. A simple extension of the write time, by adding a wait state, can simultaneously hold the write strobe active and data valid on the bus to satisfy the minimum $\overline{WR}$ pulsewidth. If this does not provide a sufficient data hold time at the end of the write cycle, a negative edge triggered one-shot can be included between the system write strobe and the $\overline{WR}$ pin of the DAC. This is illustrated in Figure 16 for an exemplary system which provides a 250ns $\overline{WR}$ strobe time with a data hold time of less than 10ns.

The proper data set-up time prior to the latching edge (LO to HI transition) of the $\overline{WR}$ strobe, is insured if the $\overline{WR}$ pulsewidth is within spec and the data is valid on the bus for the duration of the DAC $\overline{WR}$ strobe.

Digital Signal Feedthrough

When data is latched in the internal registers, but the digital inputs are changing state, a narrow spike of current may flow out of the current output terminals. This spike is caused by the rapid switching of internal logic gates that are responding to the input changes.

There are several recommendations to minimize this effect. When latching data in the DAC, always use the input register as the latch. Second, reducing the V_{CC} supply for the DAC from +15V to +5V offers a factor of 5 improvement in the magnitude of the feedthrough, but at the expense of internal logic switching speed. Finally, increasing C_C (Figure 19) to a value consistent with the actual circuit bandwidth requirements can provide a substantial damping effect on any output spikes.

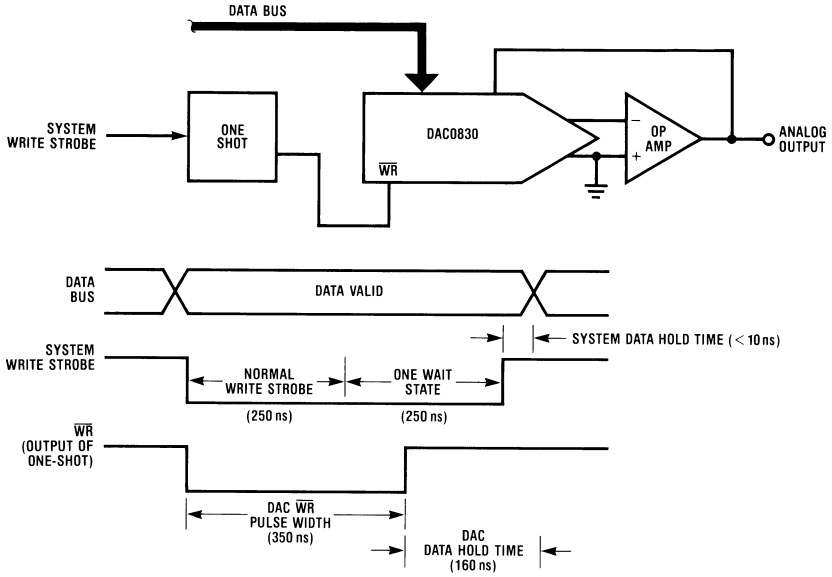


Figure 16. Accommodating a High Speed System

ANALOG CONSIDERATIONS

The fundamental purpose of any D to A converter is to provide an accurate analog output quantity which is representative of the applied digital word. In the case of the DAC0830, the output, I_{OUT1}, is a current directly proportional to the product of the applied reference voltage and the digital input word. For application versatility, a second output, I_{OUT2}, is provided as a current directly proportional to the complement of the digital input. Basically:

$$I_{OUT1} = \frac{V_{REF}}{15\ k\Omega} \times \frac{\text{Digital Input}}{256};$$

$$I_{OUT2} = \frac{V_{REF}}{15\ k\Omega} \times \frac{255 - \text{Digital Input}}{256}$$

where the digital input is the decimal (base 10) equivalent of the applied 8-bit binary word (0 to 255), V_{REF} is the voltage at pin 8 and 15 kΩ is the nominal value of the internal resistance, R, of the R-2R ladder network (discussed in Section The Current Switching R-2R Ladder).

Several factors external to the DAC itself must be considered to maintain analog accuracy and are covered in subsequent sections.

The Current Switching R-2R Ladder

The analog circuitry, Figure 17, consists of a silicon-chromium (SiCr or Si-chrome) thin film R-2R ladder which is deposited on the surface oxide of the monolithic chip. As a result, there are no parasitic diode problems with the ladder (as there may be with diffused resistors) so the reference voltage, V_{REF}, can range −10V to +10V even if V_{CC} for the device is $5V_{DC}$.

The digital input code to the DAC simply controls the position of the SPDT current switches and steers the available ladder current to either I_{OUT1} or I_{OUT2} as determined by the logic input level (“1” or “0”) respectively, as shown in Figure 17. The MOS switches operate in the current mode with a small voltage drop across them and can therefore switch currents of either polarity. This is the basis for the 4-quadrant multiplying feature of this DAC.

Basic Unipolar Output Voltage

To maintain linearity of output current with changes in the applied digital code, it is important that the voltages at both of the current output pins be as near ground potential ($0V_{DC}$) as possible. With V_{REF}=+10V every millivolt appearing at either I_{OUT1} or I_{OUT2} will cause a 0.01% linearity error. In most applications this output current is converted to a voltage by using an op amp as shown in Figure 18.

The inverting input of the op amp is a “virtual ground” created by the feedback from its output through the internal 15 kΩ resistor, R_{fb}. All of the output current (determined by the digital input and the reference voltage) will flow through R_{fb} to the output of the amplifier. Two-quadrant operation can be obtained by reversing the polarity of V_{REF} thus causing I_{OUT1} to flow into the DAC and be sourced from the output of the amplifier. The output voltage, in either case, is always equal to $I_{OUT1} \times R_{fb}$ and is the opposite polarity of the reference voltage.

The reference can be either a stable DC voltage source or an AC signal anywhere in the range from −10V to +10V. The DAC can be thought of as a digitally controlled attenuator: the output voltage is always less than or equal to the applied reference voltage. The V_{REF} terminal of the device presents a nominal impedance of 15 kΩ to ground to external circuitry.

Always use the internal R_{fb} resistor to create an output voltage since this resistor matches (and tracks with temperature) the value of the resistors used to generate the output current (I_{OUT1}).

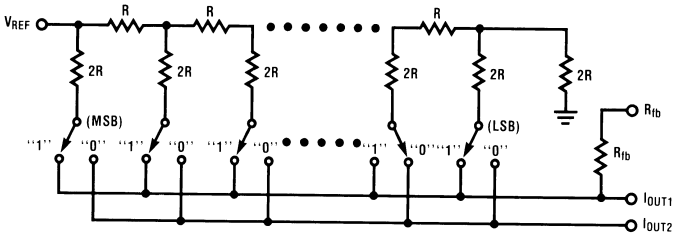


Figure 17.

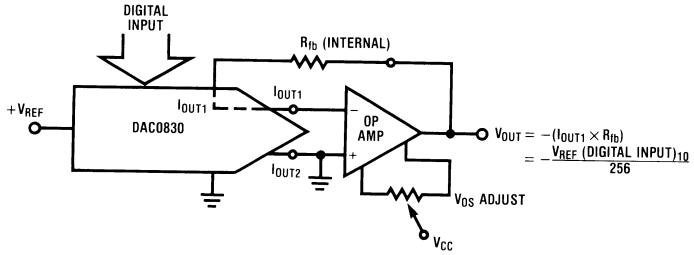


Figure 18.

Op Amp Considerations

The op amp used in Figure 18 should have offset voltage nulling capability (See Section Zero Adjustment).

The selected op amp should have as low a value of input bias current as possible. The product of the bias current times the feedback resistance creates an output voltage error which can be significant in low reference voltage applications. BI-FET™ op amps are highly recommended for use with these DACs because of their very low input current.

Transient response and settling time of the op amp are important in fast data throughput applications. The largest stability problem is the feedback pole created by the feedback resistance, R_{fb}, and the output capacitance of the DAC. This appears from the op amp output to the (−) input and includes the stray capacitance at this node. Addition of a lead capacitance, C_C in Figure 19, greatly reduces overshoot and ringing at the output for a step change in DAC output current.

Finally, the output voltage swing of the amplifier must be greater than V_{REF} to allow reaching the full scale output voltage. Depending on the loading on the output of the amplifier and the available op amp supply voltages (only ±12 volts in many development systems), a reference voltage less than 10 volts may be necessary to obtain the full analog output voltage range.

Bipolar Output Voltage with a Fixed Reference

The addition of a second op amp to the previous circuitry can be used to generate a bipolar output voltage from a fixed reference voltage. This, in effect, gives sign significance to the MSB of the digital input word and allows two-quadrant multiplication of the reference voltage. The polarity of the reference can also be reversed to realize full 4-quadrant multiplication: $\pm V_{REF} \times \pm$Digital Code$= \pm V_{OUT}$. This circuit is shown in Figure 20.

This configuration features several improvements over existing circuits for bipolar outputs with other multiplying DACs. Only the offset voltage of amplifier 1 has to be nulled to preserve linearity of the DAC. The offset voltage error of the second op amp (although a constant output voltage error) has no effect on linearity. It should be nulled only if absolute output accuracy is required. Finally, the values of the resistors around the second amplifier do not have to match the internal DAC resistors, they need only to match and temperature track each other. A thin film 4-resistor network available from Beckman Instruments, Inc. (part no. 694-3-R10K-D) is ideally suited for this application. These resistors are matched to 0.1% and exhibit only 5 ppm/°C resistance tracking temperature coefficient. Two of the four available 10 kΩ resistors can be paralleled to form R in Figure 20 and the other two can be used independently as the resistances labeled 2R.

Zero Adjustment

For accurate conversions, the input offset voltage of the output amplifier must always be nulled. Amplifier offset errors create an overall degradation of DAC linearity.

The fundamental purpose of zeroing is to make the voltage appearing at the DAC outputs as near $0V_{DC}$ as possible. This is accomplished for the typical DAC — op amp connection (Figure 18) by shorting out R_{fb}, the amplifier feedback resistor, and adjusting the V_{OS} nulling potentiometer of the op amp until the output reads zero volts. This is done, of course, with an applied digital code of all zeros if I_{OUT1} is driving the op amp (all one's for I_{OUT2}). The short around R_{fb} is then removed and the converter is zero adjusted.

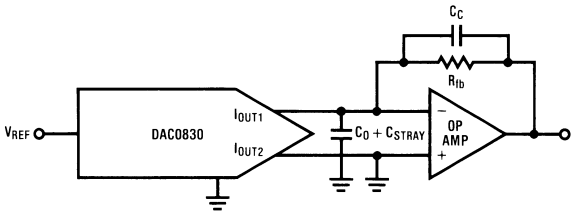
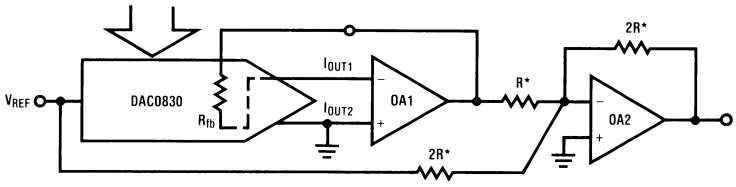


Figure 19.

		t_s
OP Amp	**C_C**	**(O to Full Scale)**
LF356	22 pF	4 µs
LF351	22 pF	5 µs
LF357 (1)	10 pF	2 µs

(1) 2.4 kΩ RESISTOR ADDED FROM−INPUT TO GROUND TO INSURE STABILITY



*THESE RESISTORS ARE AVAILABLE FROM BECKMAN INSTRUMENTS, INC. AS THEIR PART NO. 694-3-R10K-D

Figure 20.

$$V_{OUT} = V_{REF} \frac{(\text{DIGITAL CODE} - 128)}{128}$$

$$1\ \text{LSB} = \frac{|V_{REF}|}{128}$$

Input Code								IDEAL V_{OUT}	
MSB							LSB	$+V_{REF}$	$-V_{REF}$
1	1	1	1	1	1	1	1	$V_{REF} - 1$ LSB	$-\lvert V_{REF}\rvert + 1$ LSB
1	1	0	0	0	0	0	0	$V_{REF}/2$	$-\lvert V_{REF}\rvert/2$
1	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	-1 LSB	$+1$ LSB
0	0	1	1	1	1	1	1	$-\frac{\lvert V_{REF}\rvert}{2} - 1$ LSB	$\frac{\lvert V_{REF}\rvert}{2} + 1$ LSB
0	0	0	0	0	0	0	0	$-\lvert V_{REF}\rvert$	$+\lvert V_{REF}\rvert$

Full-Scale Adjustment

In the case where the matching of R_{fb} to the R value of the R-2R ladder (typically ±0.2%) is insufficient for full-scale accuracy in a particular application, the V_{REF} voltage can be adjusted or an external resistor and potentiometer can be added as shown in Figure 21 to provide a full-scale adjustment.

The temperature coefficients of the resistors used for this adjustment are of an important concern. To prevent degradation of the gain error temperature coefficient by the external resistors, their temperature coefficients ideally would have to match that of the internal DAC resistors, which is a highly impractical constraint. For the values shown in Figure 21, if the resistor and the potentiometer each had a temperature coefficient of ±100 ppm/°C maximum, the overall gain error temperature coefficent would be degraded a maximum of 0.0025%/°C for an adjustment pot setting of less than 3% of R_{fb}.

Using the DAC0830 in a Voltage Switching Configuration

The R-2R ladder can also be operated as a voltage switching network. In this mode the ladder is used in an inverted manner from the standard current switching configuration. The reference voltage is connected to one of the current output terminals (I_{OUT1} for true binary digital control, I_{OUT2} is for complementary binary) and the output voltage is taken from the normal V_{REF} pin. The converter output is now a voltage in the range from 0V to 255/256 V_{REF} as a function of the applied digital code as shown in Figure 22.

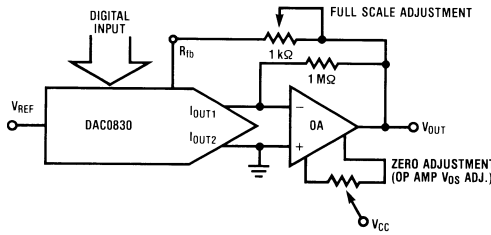


Figure 21. Adding Full-Scale Adjustment

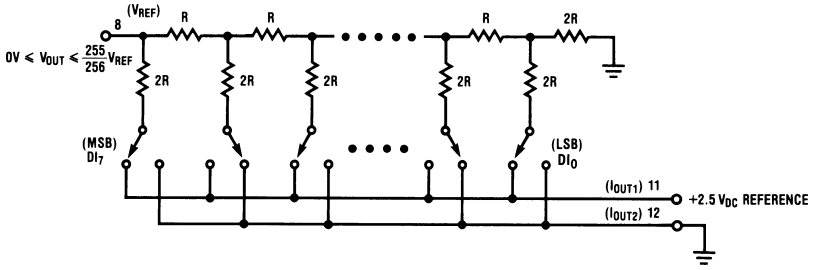
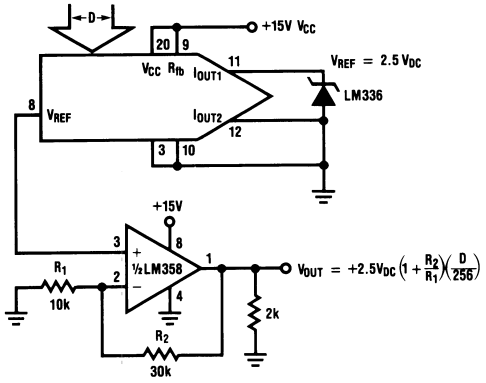


Figure 22. Voltage Mode Switching

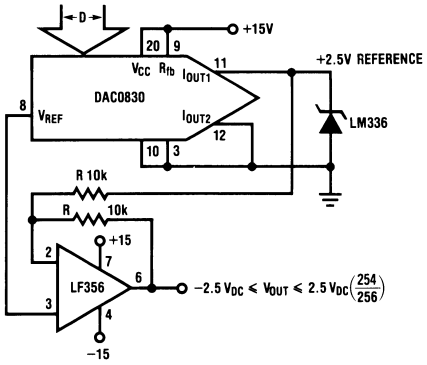
This configuration offers several useful application advantages. Since the output is a voltage, an external op amp is not necessarily required but the output impedance of the DAC is fairly high (equal to the specified reference input resistance of 10 kΩ to 20 kΩ) so an op amp may be used for buffering purposes. Some of the advantages of this mode are illustrated in Figure 23, Figure 24, Figure 25, and Figure 26.

There are two important things to keep in mind when using this DAC in the voltage switching mode. The applied reference voltage must be positive since there are internal parasitic diodes from ground to the I_{OUT1} and I_{OUT2} terminals which would turn on if the applied reference went negative. There is also a dependence of conversion linearity and gain error on the voltage difference between V_{CC} and the voltage applied to the normal current output terminals. This is a result of the voltage drive requirements of the ladder switches. To ensure that all 8 switches turn on sufficiently (so as not to add significant resistance to any leg of the ladder and thereby introduce additional linearity and gain errors) it is recommended that the applied reference voltage be kept less than $+5V_{DC}$ and V_{CC} be at least 9V more positive than V_{REF}. These restrictions ensure less than 0.1% linearity and gain error change. Figure 27, Figure 28, and Figure 29 characterize the effects of bringing V_{REF} and V_{CC} closer together as well as typical temperature performance of this voltage switching configuration.



- Voltage switching mode eliminates output signal inversion and therefore a need for a negative power supply.
- Zero code output voltage is limited by the low level output saturation voltage of the op amp. The 2 kΩ pull-down resistor helps to reduce this voltage.
- V_{OS} of the op amp has no effect on DAC linearity.

Figure 23. Single Supply DAC



- $V_{OUT} = 2.5V \left(\frac{D}{128} - 1\right)$
- Slewing and settling time for a full scale output change is ≈ 1.8 μs

Figure 24. Obtaining a Bipolar Output from a Fixed Reference with a Single Op Amp

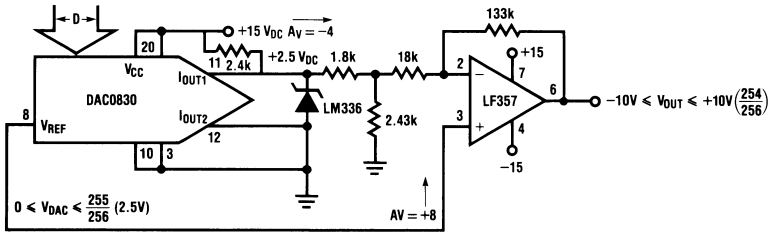
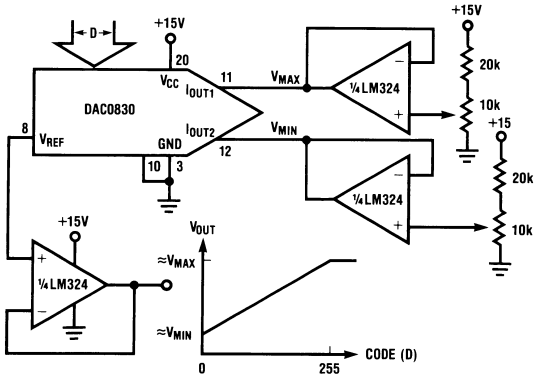


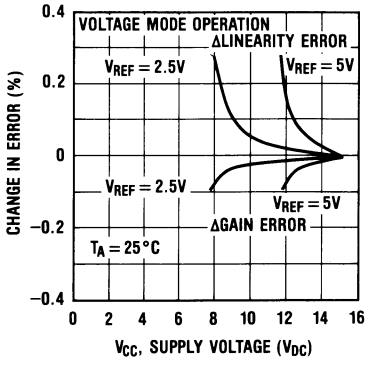
Figure 25. Bipolar Output with Increased Output Voltage Swing



- Only a single +15V supply required
- Non-interactive full-scale and zero code output adjustments
- V_{MAX} and V_{MIN} must be $\leq$ +5VDC and $\geq$ 0V.
- Incremental Output Step $= \frac{1}{256}(V_{MAX} - V_{MIN})$.
- $V_{OUT} = \frac{D}{256}(V_{MAX} - V_{MIN}) + \frac{255}{256}V_{MIN}$

Figure 26. Single Supply DAC with Level Shift and Span- Adjustable Output

Gain and Linearity Error Variation vs. Supply Voltage



Note: For these curves, V_{REF} is the voltage applied to pin 11 (I_{OUT1}) with pin 12 (I_{OUT2}) grounded.

Figure 27.

Gain and Linearity Error Variation vs. Reference Voltage

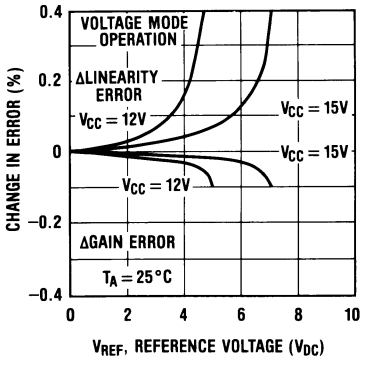


Figure 28.

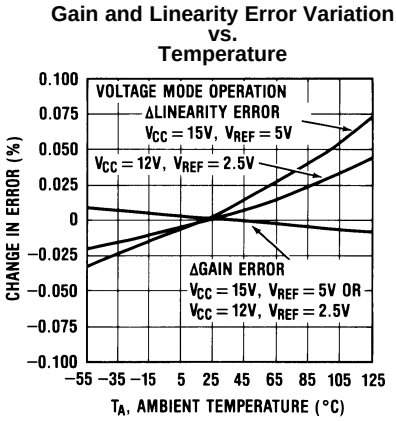


Figure 29.

Miscellaneous Application Hints

These converters are CMOS products and reasonable care should be exercised in handling them to prevent catastrophic failures due to static discharge.

Conversion accuracy is only as good as the applied reference voltage so providing a stable source over time and temperature changes is an important factor to consider.

A “good” ground is most desirable. A single point ground distribution technique for analog signals and supply returns keeps other devices in a system from affecting the output of the DACs.

During power-up supply voltage sequencing, the −15V (or −12V) supply of the op amp may appear first. This will cause the output of the op amp to bias near the negative supply potential. No harm is done to the DAC, however, as the on-chip 15 kΩ feedback resistor sufficiently limits the current flow from I_{OUT1} when this lead is internally clamped to one diode drop below ground.

Careful circuit construction with minimization of lead lengths around the analog circuitry, is a primary concern. Good high frequency supply decoupling will aid in preventing inadvertant noise from appearing on the analog output.

Overall noise reduction and reference stability is of particular concern when using the higher accuracy versions, the DAC0830 and DAC0831, or their advantages are wasted.

GENERAL APPLICATION IDEAS

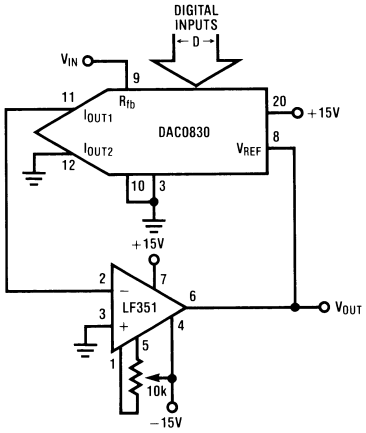
The connections for the control pins of the digital input registers are purposely omitted. Any of the control formats discussed in Digital Considerations of the accompanying text will work with any of the circuits shown. The method used depends on the overall system provisions and requirements.

The digital input code is referred to as D and represents the decimal equivalent value of the 8-bit binary input, for example:

Binary Input								D
Pin 13						Pin 7		Decimal
MSB						LSB		Equivalent
1	1	1	1	1	1	1	1	255
1	0	0	0	0	0	0	0	128
0	0	0	1	0	0	0	0	16
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	0	0

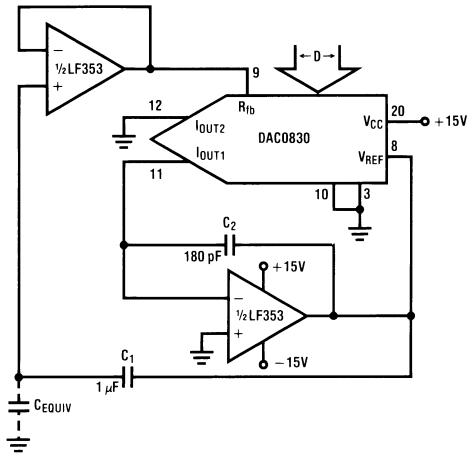
Applications

Figure 30. DAC Controlled Amplifier (Volume Control)



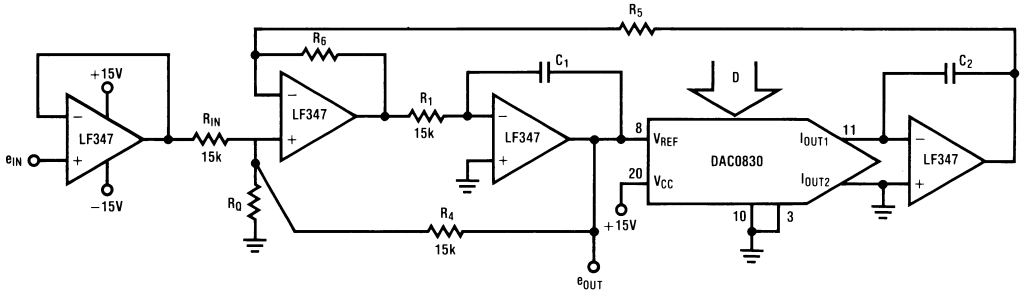
- $V_{OUT} = \frac{-V_{IN}\,(256)}{D}$
- When D=0, the amplifier will go open loop and the output will saturate.
- Feedback impedance from the −input to the output varies from 15 kΩ to ∞ as the input code changes from full−scale to zero.

Figure 31. Capacitance Multiplier



- $C_{EQUIV} = C_1 \left(1 + \frac{256}{D}\right)$
- Maximum voltage across the equivalent capacitance is limited to $\frac{V_{O\,MAX}\,(\text{op amp})}{1 + \frac{256}{D}}$
- C_2 is used to improve settling time of op amp.

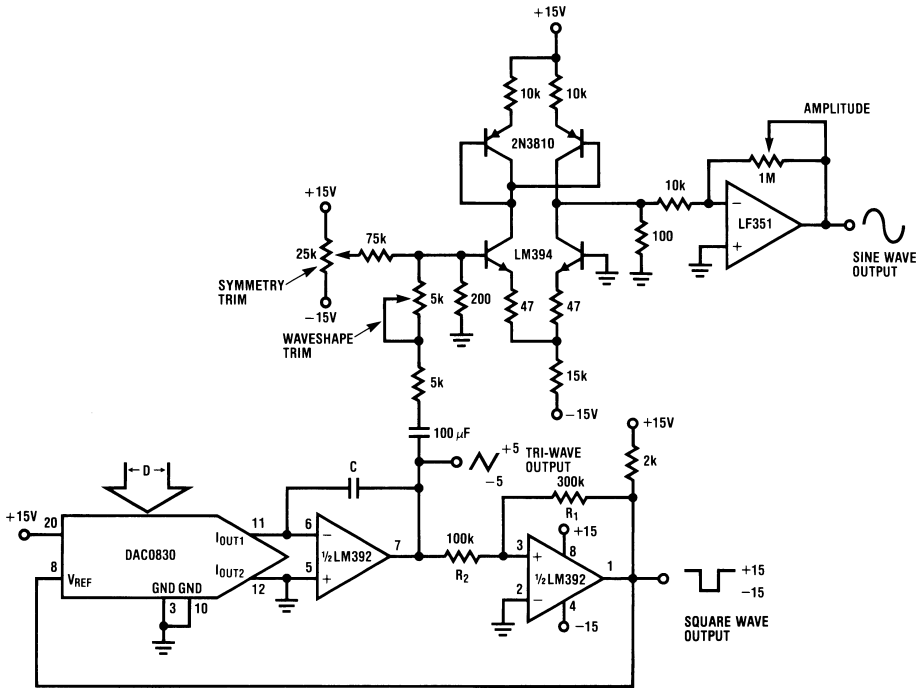
Figure 32. Variable f_O, Variable Q_O, Constant BW Bandpass Filter



- $f_O = \frac{\sqrt{\frac{KD}{256}}}{2\pi R_1 C}$; $Q_O = \sqrt{\frac{KD}{256}} \frac{(2R_Q + R_1)}{R_Q(K+1)}$; $3dbBW = \frac{R_Q(K+1)}{2\pi R_1 C(2R_Q + R_1)}$

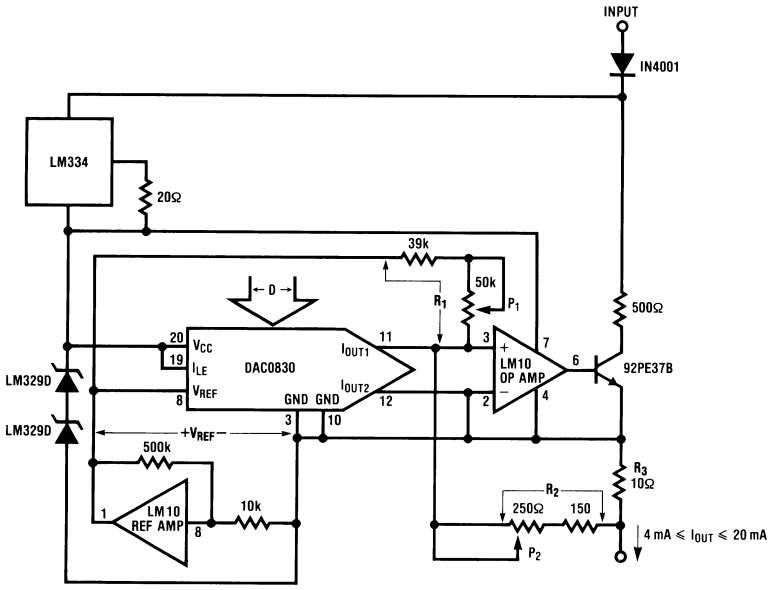
  where $C_1 = C_2 = C$; $K = \frac{R_6}{R_5}$ and R_1 = R of DAC = 15k
- H_O = 1 for $R_{IN} = R_4 = R_1$
- Range of f_O and Q is ≈16 to 1 for circuit shown. The range can be extended to 255 to 1 by replacing R_1 with a second DAC0830 driven by the same digital input word.
- Maximum f_O x Q product should be ≤ 200 kHz.

Figure 33. DAC Controlled Function Generator



- DAC controls the frequency of sine, square, and triangle outputs.
- $f = \frac{D}{256(20k)C}$ for $V_{OMAX} = V_{0MIN}$ of square wave output and $R_1 = 3\ R_2$.
- 255 to 1 linear frequency range; oscillator stops with D = 0
- Trim symmetry and wave−shape for minimum sine wave distortion.

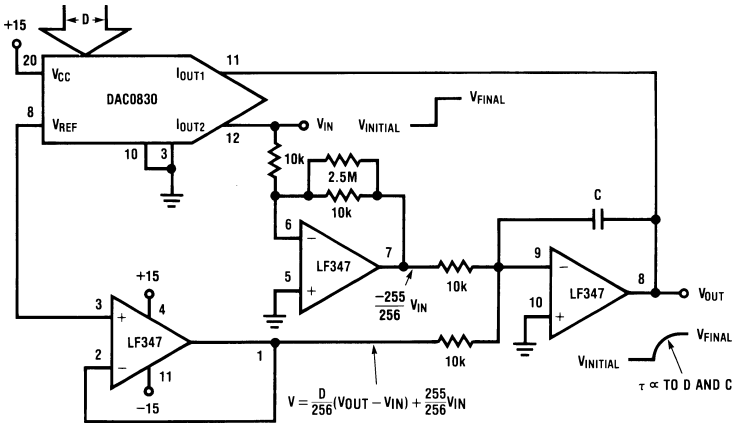
Figure 34. Two Terminal Floating 4 to 20 mA Current Loop Controller



$$I_{OUT} = V_{REF}\left[\frac{1}{R_1} + \frac{D}{256\,R_{fb}}\right]\left[1 + \frac{R_2}{R_3}\right]$$

- DAC0830 linearly controls the current flow from the input terminal to the output terminal to be 4 mA (for D=0) to 19.94 mA (for D=255).
- Circuit operates with a terminal voltage differential of 16V to 55V.
- P_2 adjusts the magnitude of the output current and P_1 adjusts the zero to full scale range of output current.
- Digital inputs can be supplied from a processor using opto isolators on each input or the DAC latches can flow-through (connect control lines to pins 3 and 10 of the DAC) and the input data can be set by SPST toggle switches to ground (pins 3 and 10).

Figure 35. DAC Controlled Exponential Time Response



- Output responds exponentially to input changes and automatically stops when $V_{OUT}=V_{IN}$
- Output time constant is directly proportional to the DAC input code and capacitor C
- Input voltage must be positive (See Using the DAC0830 in a Voltage Switching Configuration

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC0830LCN	NRND	PDIP	NFH	20	18	TBD	Call TI	Call TI	0 to 70	DAC0830LCN	
DAC0830LCN/NOPB	ACTIVE	PDIP	NFH	20	18	Pb-Free (RoHS)	CU SN	Level-1-NA-UNLIM	0 to 70	DAC0830LCN	Samples
DAC0832LCN	NRND	PDIP	NFH	20	18	TBD	Call TI	Call TI	0 to 70	DAC0832LCN	
DAC0832LCN/NOPB	ACTIVE	PDIP	NFH	20	18	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	DAC0832LCN	Samples
DAC0832LCWM	NRND	SOIC	DW	20	36	TBD	Call TI	Call TI	0 to 70	DAC0832 LCWM	
DAC0832LCWM/NOPB	ACTIVE	SOIC	DW	20	36	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	DAC0832 LCWM	Samples
DAC0832LCWMX	NRND	SOIC	DW	20	1000	TBD	Call TI	Call TI	0 to 70	DAC0832 LCWM	
DAC0832LCWMX/NOPB	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 70	DAC0832 LCWM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

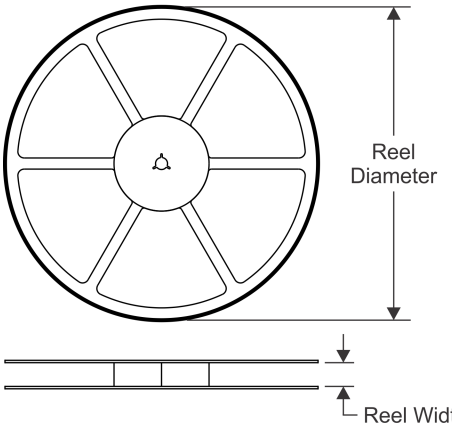
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

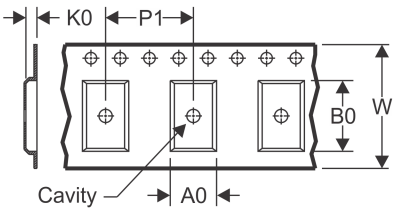
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

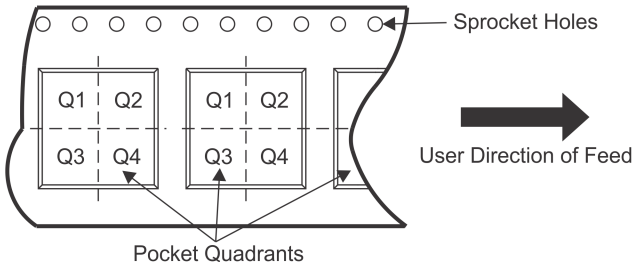


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

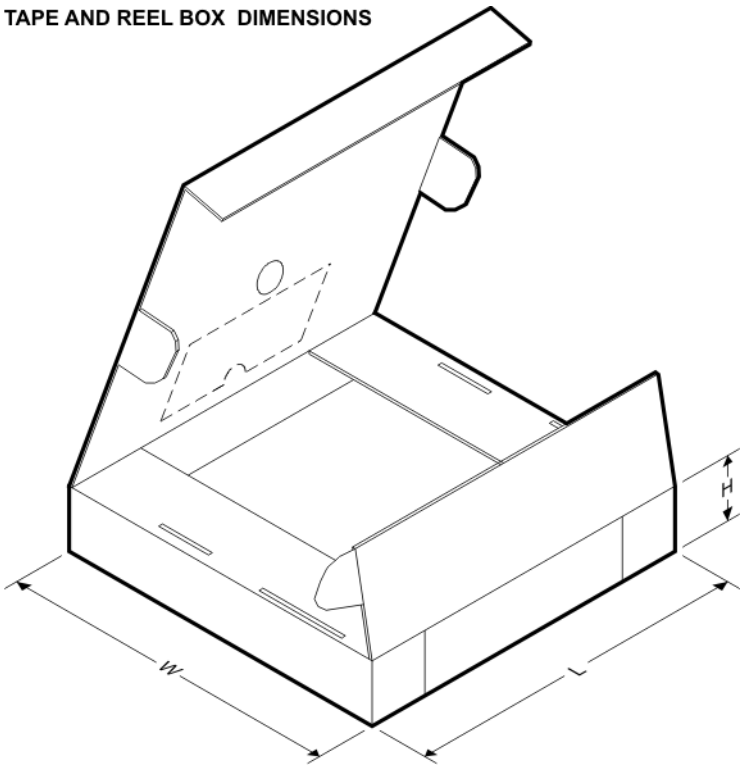
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC0832LCWMX	SOIC	DW	20	1000	330.0	24.4	10.9	13.3	3.25	12.0	24.0	Q1
DAC0832LCWMX/NOPB	SOIC	DW	20	1000	330.0	24.4	10.9	13.3	3.25	12.0	24.0	Q1

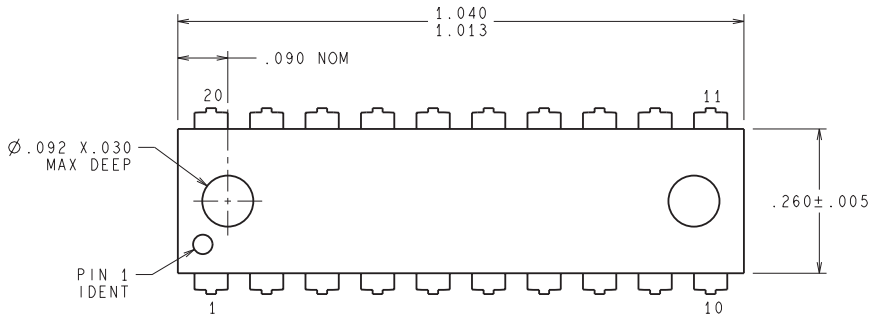
TAPE AND REEL BOX DIMENSIONS



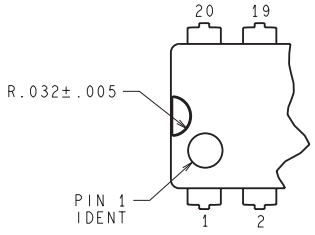
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC0832LCWMX	SOIC	DW	20	1000	367.0	367.0	45.0
DAC0832LCWMX/NOPB	SOIC	DW	20	1000	367.0	367.0	45.0

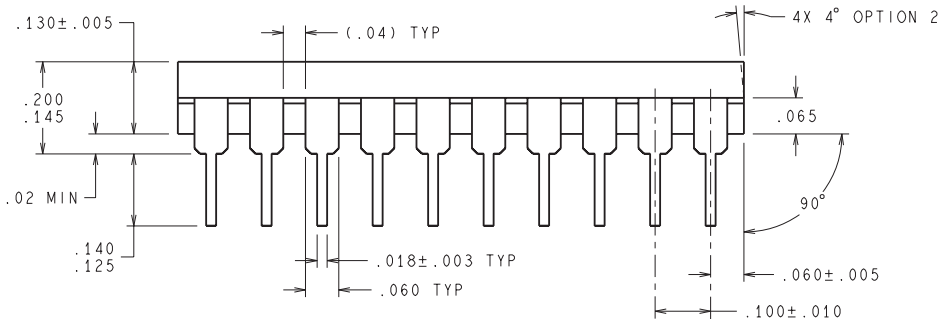
NFH0020A

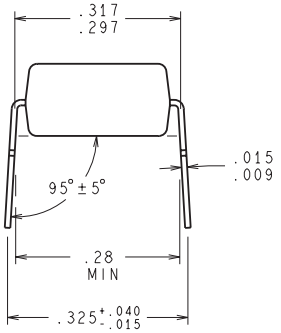


OPTION 1

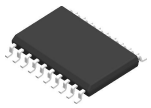


OPTION 2





N20A (Rev G)

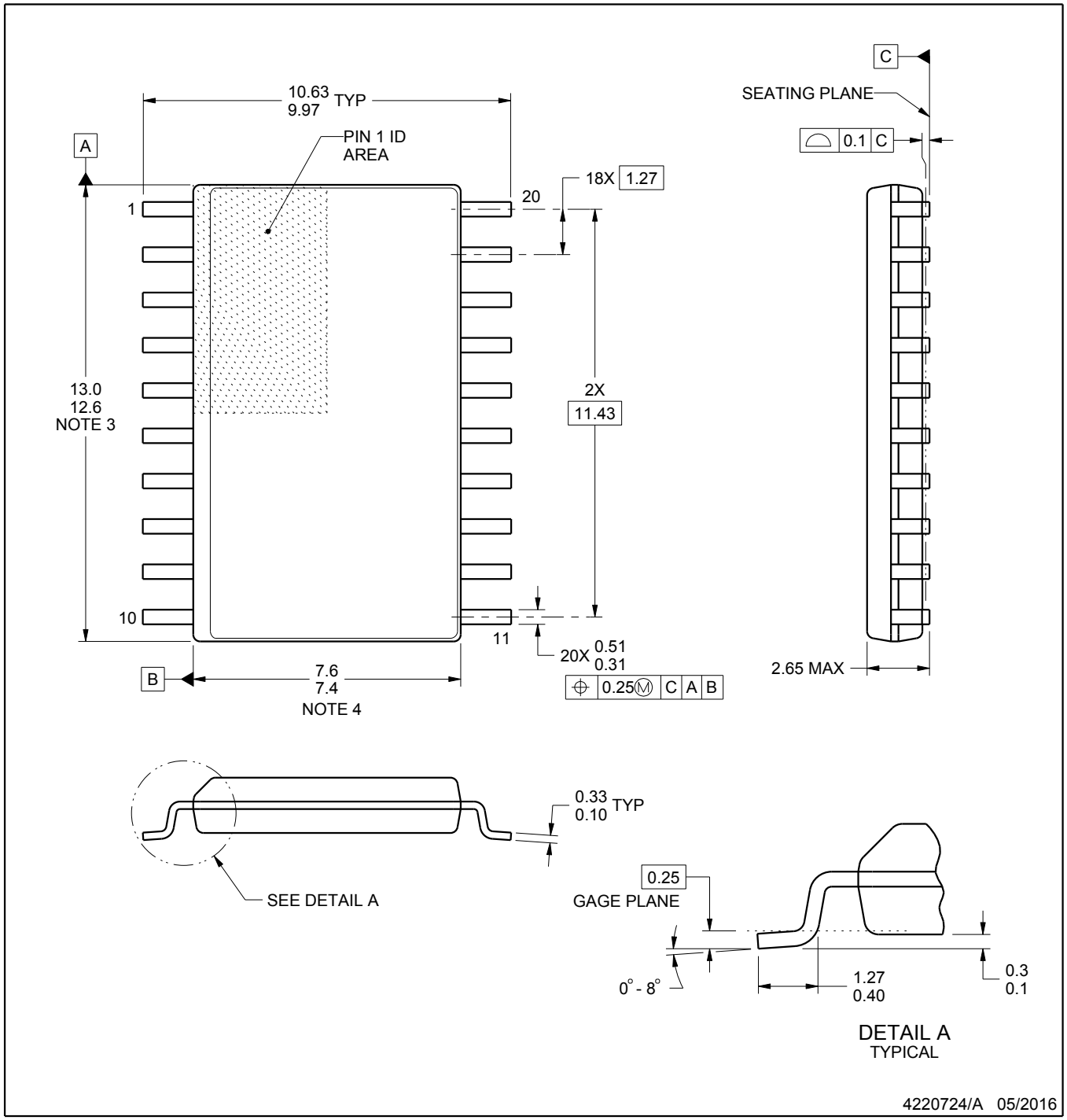


PACKAGE OUTLINE

DW0020A

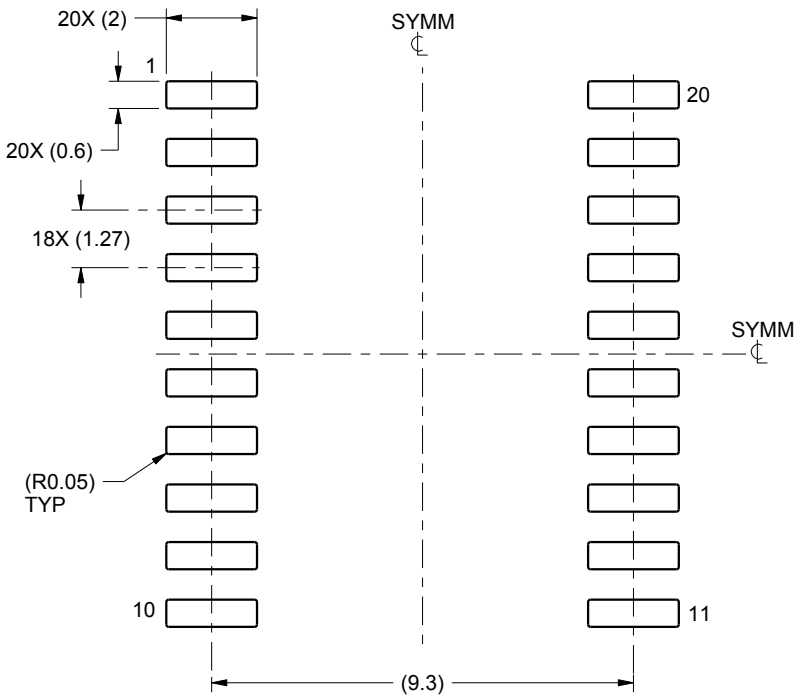
SOIC - 2.65 mm max height

SOIC

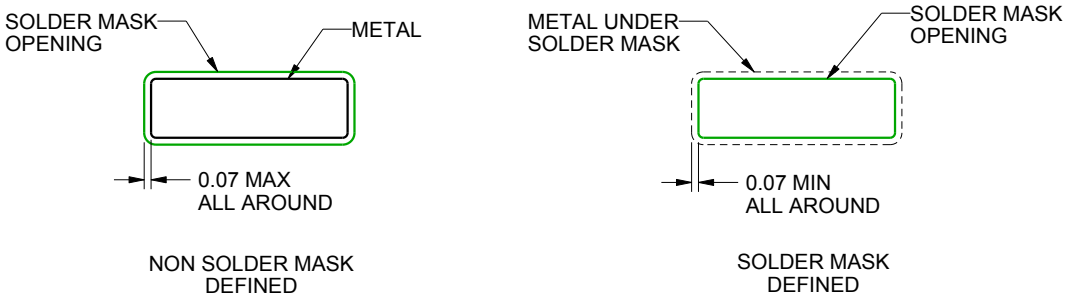


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

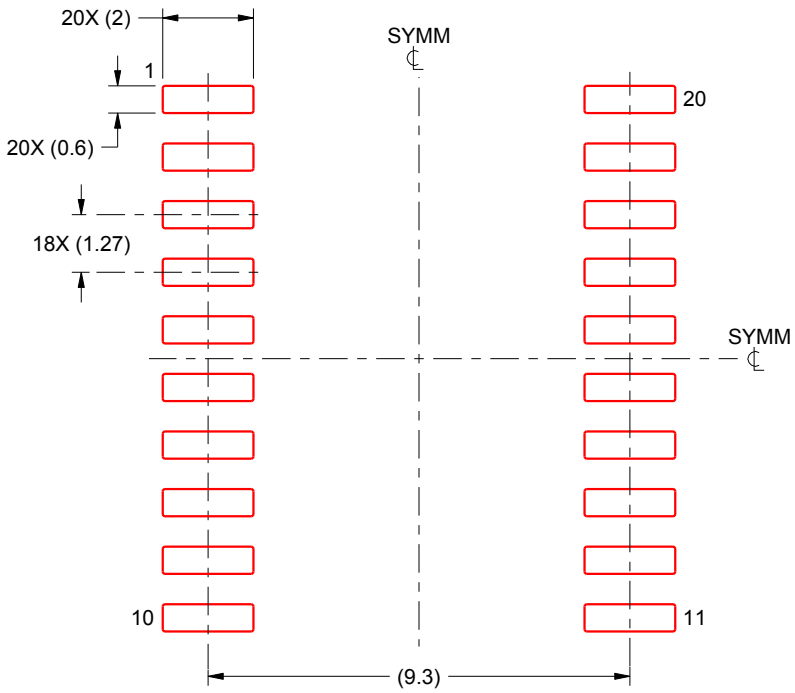


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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