

Final Exam

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CDA3203

1 I. Answer the below.

1. What is sequential logic design and give its examples.

Answer: Sequential logic design is a type of circuit design where the output is not solely determined by the inputs but also the previous states of the inputs (memory). Compared to combination logic design, where the output is derived from the current inputs only.

Examples: Flipflops, latches, and counters.

2. Differentiate Latches and Flipflops with valid points.

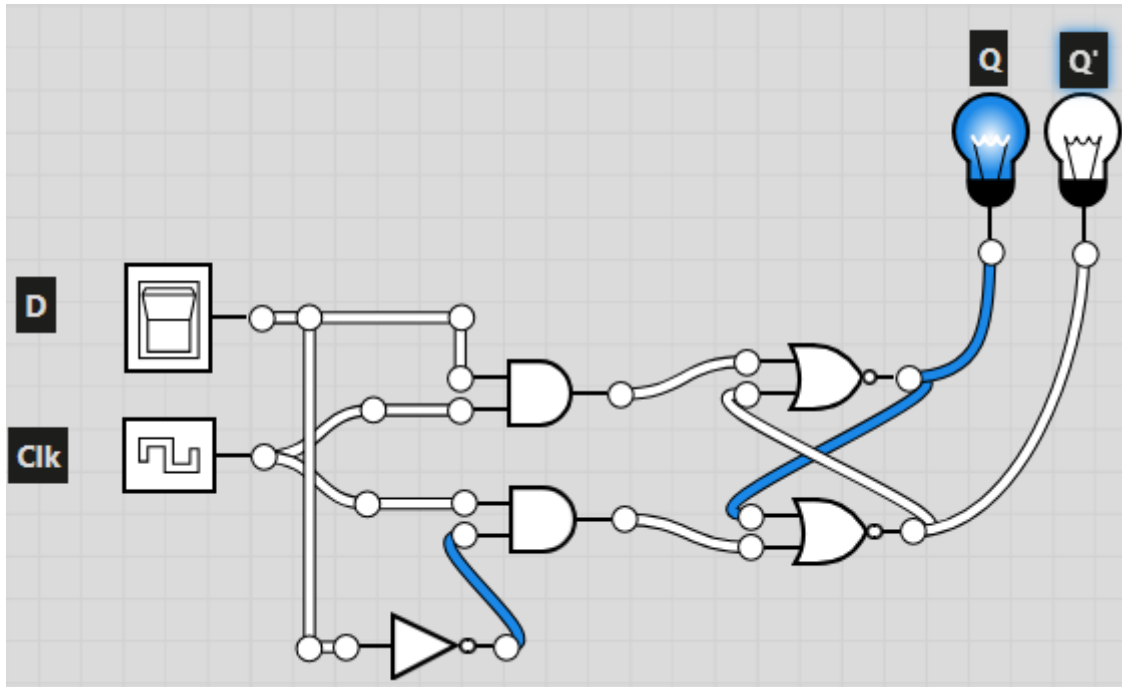
Answer: Flipflops are edge sensitive, while latches are level sensitive.

3. What is clock gating and give an example with D-Latch.

Answer: Clock gating is a power management technique, the clock signal is disabled to the parts of the circuit not in use to prevent unnecessary switching.

Example: The gated clock is connected to the D-latch at the enable input, when the clock is high the signal passes to the latch and the latch works as normal. When the clock is low, the signal is blocked, this prevents the latch from switching.

4. Draw the logic diagram for the D-flipflop.



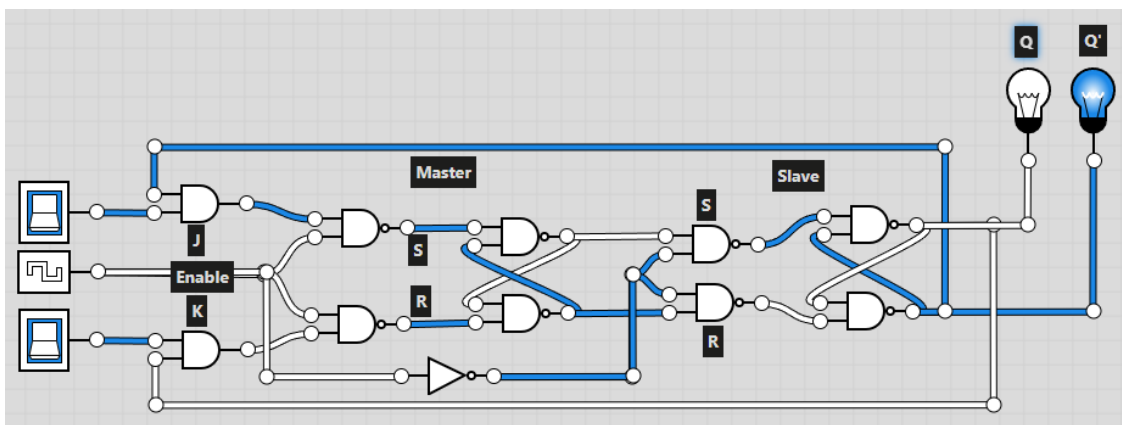
5. Draw the state diagram for SR flipflop.

S	R	Q+
0	0	Q
0	1	0
1	0	1
1	1	x

2 II Answer the below.

1. Explain JK Flipflop. Draw the JK flipflop logic structure with equivalent symbol

Answer: A JK Flipflop is a type of flipflop that can handle both inputs at high, the SR flipflop for example can not do this, but for the jk flipflop this puts it in toggle mode.

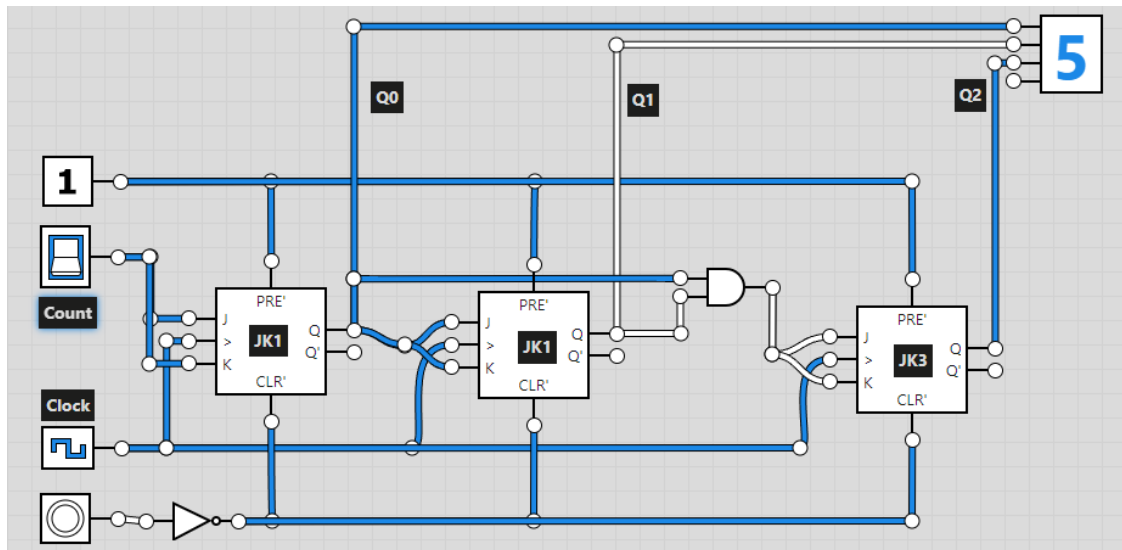


Design a 3-bit synchronous binary counter using j-k flip-flops.

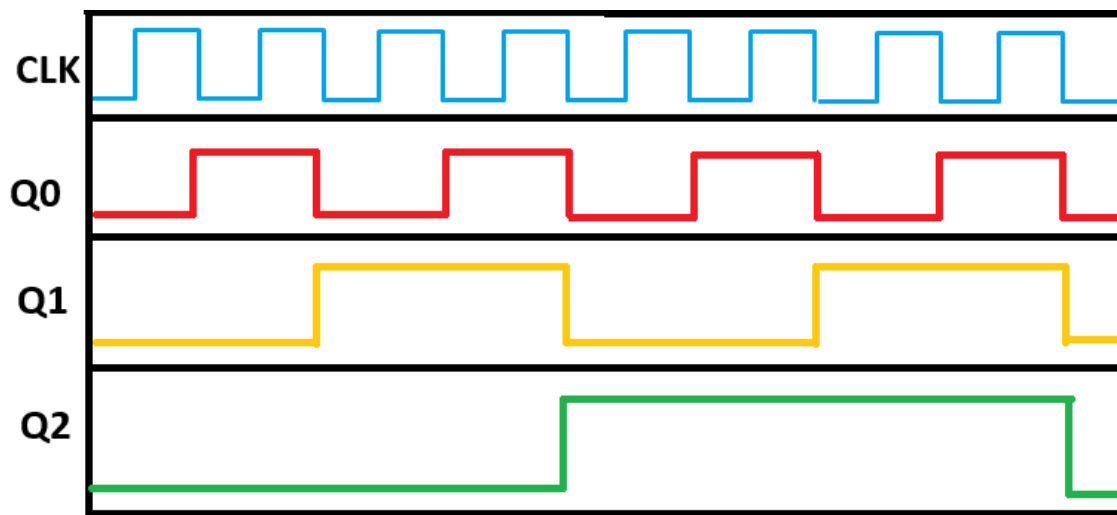
Step (1) – Determine the number of flip-flops required

Answer: 3

Step (2) – Draw the Logic diagram (with flipflop Symbols)



Step (3) – Draw timing diagram



Step (4) – Obtain the Binary state sequence for JK flipflops used in the design.

