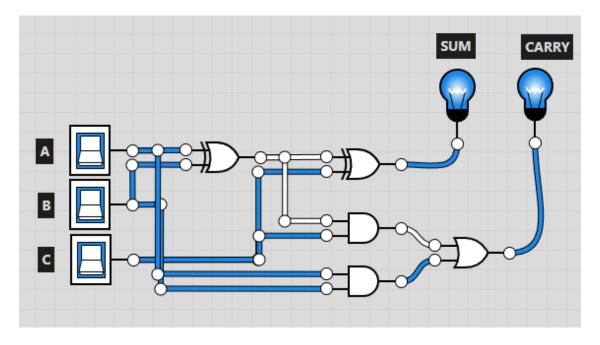
Grade Compensation

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1 Give the logical structure of a 1-bit Full Adder with its functional description and truth table. Write the VHDL code of a 1-bit Full Adder.

Logical Structure:



Functional Description:

$$SUM = (A \oplus B) \oplus C$$

$$Carry = ((A \oplus B)C) + (AB)$$

Truth Table:

Α	В	С	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

VHDL Code:

Design:

```
[]: library IEEE;
     use IEEE.std_logic_1164.all;
     -- ENTITY
     entity FullAdder is
     port(
         A, B, C: in std_logic;
         Sum, Carry: out std_logic);
     end FullAdder;
     -- ARCHITECTURE
     architecture dataflow of FullAdder is
     signal xor1, xor2, and1, and2, or1: std_logic;
     begin
         xor1 <= A xor B;</pre>
         xor2 <= xor1 xor C;</pre>
         and1 <= xor1 and C;</pre>
         and2 <= A and B;
         or1 <= and1 or and2;</pre>
         Sum <= xor2;</pre>
         Carry <= or1;</pre>
     end dataflow;
```

Test Bench:

```
[]: library IEEE;
use IEEE.std_logic_1164.all;

-- TESTBENCH ENTITY
entity testbench is
--empty
end testbench;
```

```
architecture tb of testbench is
-- DUT COMPONENT
component FullAdder is
port(
    A, B, C: in std_logic;
    Sum, Carry: out std_logic);
end component;
signal A_IN, B_IN, C_IN, SUM_OUT, CARRY_OUT : std_logic;
begin
-- CONNECT DUT
DUT: FullAdder port map(A_IN, B_IN, C_IN, SUM_OUT, CARRY_OUT);
        process
          begin
            A_IN <= '0';
        B_IN <= '0';
                 C_IN <= '0';</pre>
        wait for 1 ns;
              A_IN <= '1';
              B_IN <= '0';
                C_IN <= '0';
              wait for 1 ns;
        A_IN <= 'O';
              B_IN <= '1';
                C_IN <= 'O';
               wait for 1 ns;
        A_IN <= 'O';
              B_IN <= '0';
                 C_IN <= '1';
              wait for 1 ns;
        A_IN <= '1';
              B_IN <= '1';
                C_IN<='1';
              wait for 1 ns;
               -- CLEAR INPUTS
              A_IN <= 'O';
               B_IN <= '0';
                 C_IN <= '0';</pre>
               wait;
```

end process;

end tb;

2 Simplify the following functional description using the algebraic method and mention the Boolean rule at each step.

Z(A,B,C,D) = ABCD + ABCD + ABCD + ABCD + ABCD + BCD + BCD

- 1. Demorgan: ABCD + A(B'+C') + A(B'+C'+D') + A'B'CD' + A'BCD + BC
- 2. Absorption: A(B'+C')D + A(B'+C'+D') + (A'+B)CD + BC
- 3. Distributive: ADB' + ADC' + AB' + AC' + AD' + (A'+B)CD + BC
- 4. Absorption: AB' + AC' + AD' + (A'+B')CD + BC
- 5. Distributive: AB' + AC' + D'(CA'+A) + CD'B' + BC
- 6. Absorption: A'B + AC' + D'(C+A) + CD'B' + BC
- 7. Distributive: AB' + AC' + D'(C+A) + C(D'B'+B)
- 8. Absorption: AB' + AC' + D'(C+A) + C(D'+B)
- 9. Distributive: AB' + AC' + D'C + D'A + CD' + CB
- 10. Idempotent: AB' + AC' + D'C + D'A + CB
- 11. Consensus: AB' + AC' + D'C + CB

Simplified Expression: AB' + AC' + D'C + CB

3 Simplify the following functional description using the algebraic method and mention the Boolean rule at each step.

V(X,Y,Z) = X YZ + XY + XZ

- 1. Distributive: Y(X'Z + X) + XZ
- 2. Absorption: Y(Z + X) + XZ
- 3. Distribute: YZ + YX + XZ

Simplified Expression: YZ + YX + XZ