Computer Logic Design (CDA 3203)

Assignment-3

Design the below combinational logic design using VHDL and simulate the same in EDA Playground, submit the output for any 4 test cases in EPWave.

- `HalfAdder`
- `FullAdder`
- `4:2 Encoder`
- `2:4 Decoder`

Assignment 3-Submission Guidelines

- Complete Project-2 with given guidelines
- Make a single report in pdf with the below contents:
  - VHDL design
  - VHDL testbench
  - Simulated results in EDA playground
  - Brief observations

Good Luck!!!

Reference:

VHDL Basic-

https://www.youtube.com/watch?v=fhZAWZ4PEvs&list=PLJ1g6uqLp358rFx54WUUPLi3HxcDLSO_m

How to Write a Basic Testbench using VHDL

https://fpgatutorial.com/how-to-write-a-basic-testbench-using-vhdl/

EDA Playground Repo-

https://www.edaplayground.com/home

https://github.com/edaplayground/eda-playground/tree/master/docs