Class Activity 4: Designing Sequential Circuits with JK Flip-Flops

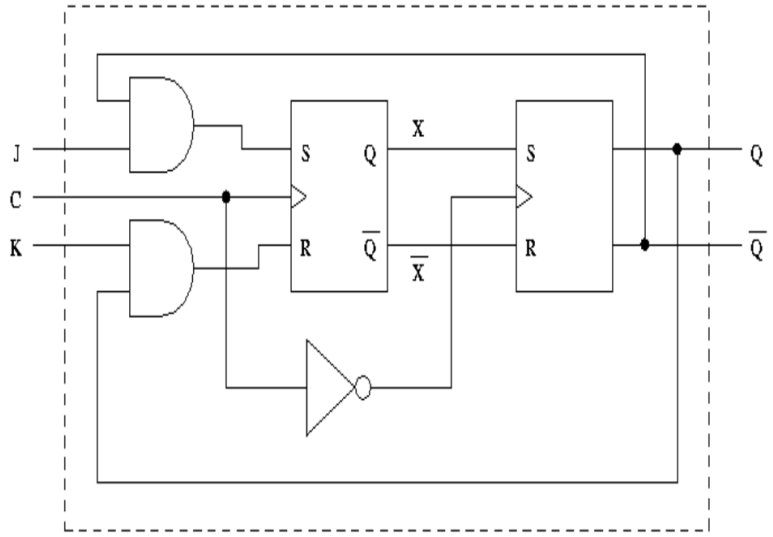

Figure. JK Flip-Flop

Task 1: Design the Sequential Circuit

1. **State Diagram Analysis:**
    - Draw and analyze the state diagram for the JK Flip Flop.
2. **State Table:**
    - Create the state table based on the state diagram.
3. **Circuit Diagram:**
    - Draw the complete circuit diagram including the JK flip-flops and combinational logic.

Task 2: Simulate the Circuit

1. **VHDL Code:**
    - Write the VHDL code for the designed sequential circuit.
    - Include the JK flip-flop components and the combinational logic.
2. **Testbench:**
    - Create a testbench to simulate the circuit.
    - Include test cases that cover all state transitions.
3. **Simulation:**
    - Use EDA Playground to simulate the VHDL code.

Materials Needed:

- EDA Playground access
- VHDL code templates
- Printed handouts of the state diagram and state table

Hints:

1. Refer to the JK flip-flop excitation table to determine the J and K inputs.
2. Use EDA Playground to write, simulate, and verify your VHDL code.