Class Activity 4

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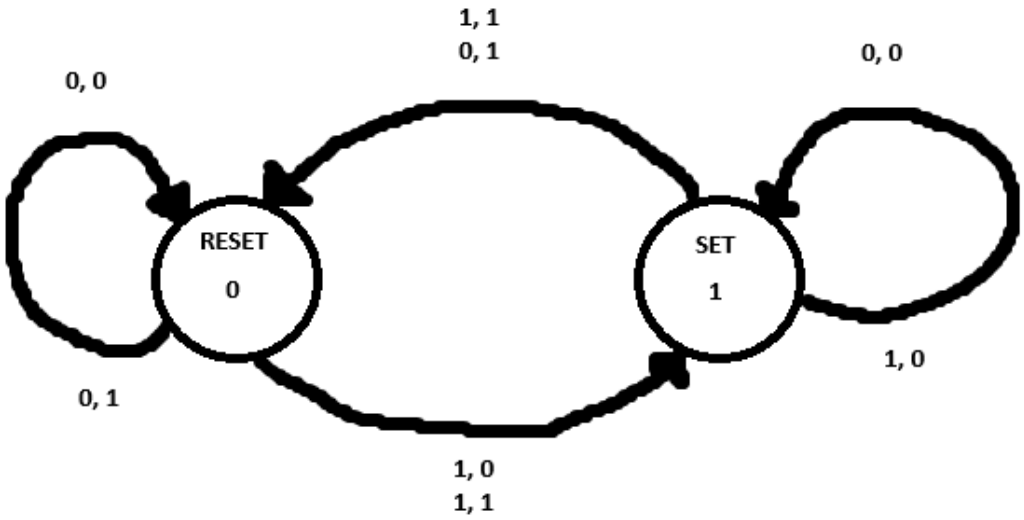
1 Task: Design The Sequential Circuit

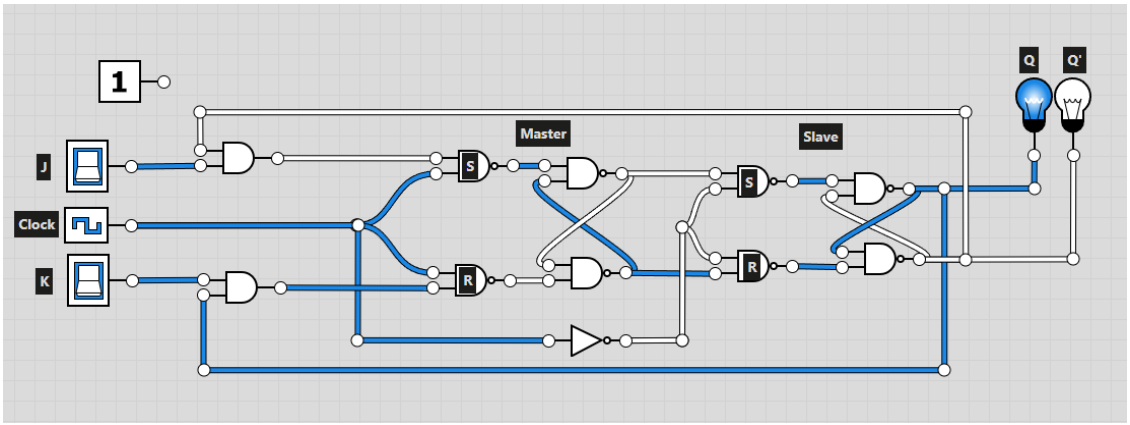
1. State Diagram Analysis:



2. State Table:

J	K	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

3. Circuit Diagram:



2 Task: Simulate The Circuit

1. VHDL Code:

[ ]:
```
library IEEE;
use IEEE.std_logic_1164.all;

entity JKFlipFlop is
    port (
        J, K, CLOCK : in std_logic;
        Q, Qbar : out std_logic
    );
end JKFlipFlop;

architecture Behavioral of JKFlipFlop is
    signal Q_internal : std_logic := '0';
begin

    process (CLOCK)
    begin
        if rising_edge(CLOCK) then
            if (J = '0' and K = '0') then
                Q_internal <= Q_internal; -- No change
            elsif (J = '0' and K = '1') then
                Q_internal <= '0'; -- Reset
            elsif (J = '1' and K = '0') then
                Q_internal <= '1'; -- Set
            elsif (J = '1' and K = '1') then
                Q_internal <= not Q_internal; -- Toggle
            end if;
        end if;
    end process;

    Q <= Q_internal;
```

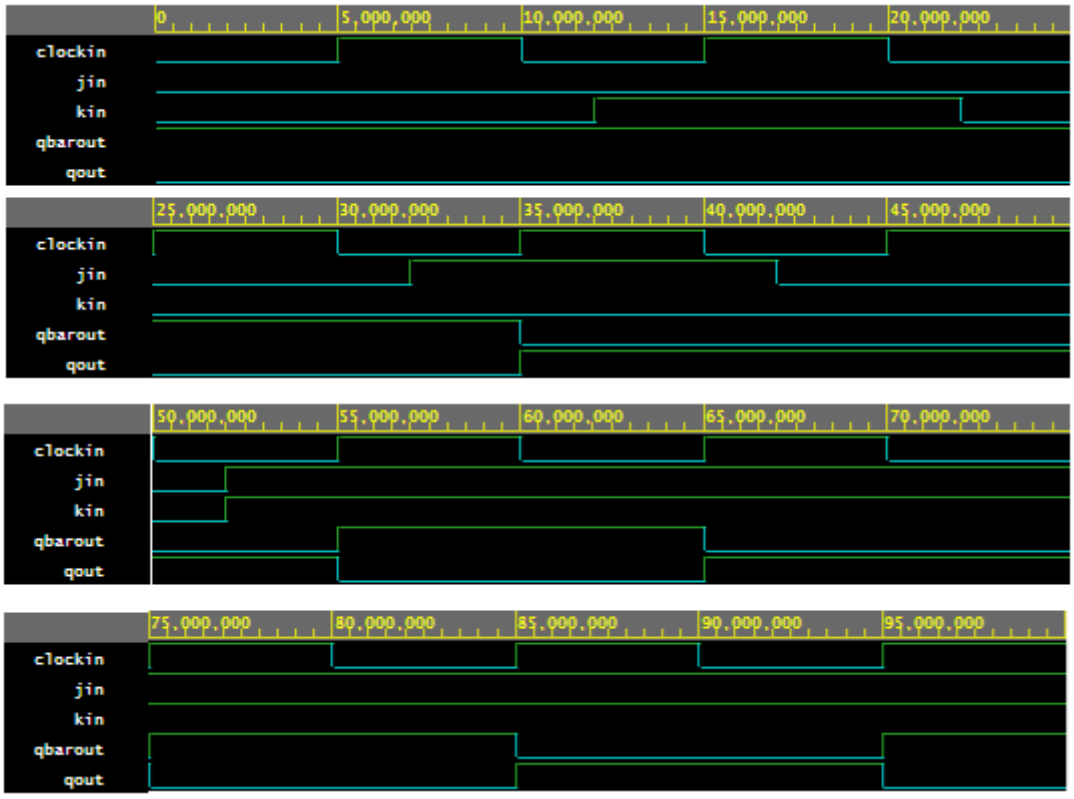
```
    Qbar <= not Q_internal;

end Behavioral;
```

2. Test Bench:

[ ]:
```
library IEEE;
use IEEE.std_logic_1164.all;

-- TESTBENCH ENTITY
entity testbench is
--empty
end testbench;

architecture tb of testbench is
-- DUT COMPONENT
component JKFlipFlop is
port(
    J, K, CLOCK: in std_logic;
    Q, Qbar: out std_logic);
end component;

signal Jin, Kin, CLOCKin: std_logic := '0';
signal Qout, QBARout: std_logic;

constant clk_period : time := 10 ns;

begin

-- CONNECT DUT
DUT: JKFlipFlop port map(Jin, Kin, CLOCKin, Qout, QBARout);

    clk_process: process
    begin
        while now < 100 ns loop
            CLOCKin <= '0';
            wait for clk_period/2;
            CLOCKin <= '1';
            wait for clk_period/2;
        end loop;
        wait;
    end process;

    stim_proc: process
    begin
        wait for 2 ns;
```

```
        Jin <= '0';
        Kin <= '0';
        wait for clk_period;

        Jin <= '0';
        Kin <= '1';
        wait for clk_period;

        Jin <= '0';
        Kin <= '0';
        wait for clk_period;

        Jin <= '1';
        Kin <= '0';
        wait for clk_period;

        Jin <= '0';
        Kin <= '0';
        wait for clk_period;

        Jin <= '1';
        Kin <= '1';
        wait for clk_period;

        wait;
    end process;
end tb;
```

3. Simulation:


0
5,000,000
10,000,000
15,000,000
20,000,000
clockin
jin
kin
qbarout
qout
25,000,000
30,000,000
35,000,000
40,000,000
45,000,000
clockin
jin
kin
qbarout
qout
50,000,000
55,000,000
60,000,000
65,000,000
70,000,000
clockin
jin
kin
qbarout
qout
75,000,000
80,000,000
85,000,000
90,000,000
95,000,000
clockin
jin
kin
qbarout
qout