

ELEN 120 HW 5 | Dylan Thornburg

1.

Screenshot (results bottom right in decimal):

The screenshot displays the uVision IDE interface with the following components:

- Registers Window:**

Register	Value
R0	0x0000220
R1	0xA5A5A5A5
R2	0x0000230
R3	0x0000003
R4	0x0000220
R5	0x0000001
R6	0x0000000
R7	0x0000001
R8	0x0000000
R9	0x0000000
R10	0x0000000
R11	0x0000000
R12	0x0000000
R13 (SP)	0x10001500
R14 (LR)	0xFFFFFFFF
R15 (PC)	0x000001F0
xPSR	0x61000000
- Disassembly Window:**

```

29: bne start
0x000001EE D1F0 BNE 0x000001D2
30: endless b endless
31:
32: ENDP
33:
34: onecount PROC
35:
36: loop cmp r5, #1

```
- Memory Window:**

Address	Hex	Dec	Hex	Dec
0x0000020C	0000059377	0305419896	-1091567891	
0x00000218	1431655765	-1515870811	0000000000	
0x00000224	0000000005	0000000019	0000000000	
0x00000230	0000000003	00000000544	00000000544	
0x0000023C	0000000000	0000000000	0000000000	
0x00000248	0000000000	0000000000	0000000000	
0x00000254	0000000000	0000000000	0000000000	
0x00000260	0000000000	0000000000	0000000000	

Code:

```

***** (C) Andrew Wolfe *****
;
; @file HW4 Problem 3
; @author Andrew Wolfe

```

; @date Aug. 13, 2023

,*****

AREA main, CODE, READONLY
EXPORT __main
ENTRY

__main PROC
ldr r0, =samplelist
ldr r4, =eol1
ldr r2, =resultlist
mov r8, #0 ;count
start ldr r1, [r0]
ldr r3, [r2]
ldr r5, =0xc0000000; mask
b onecount
return add r0,r0,#4
add r2,r2,#4
mov r3, r8
str r3, [r2]
mov r8, #0
cmp r0,r4
bne start
endless b endless

ENDP

onecount PROC

loop cmp r5, #1
beq return
and r7, r1, r5
cmp r7, r5
beq addcount
lsl r5, #1
b loop
addcount add r8, #1
lsl r5, #1
b loop
ENDP

```
samplelist dcd 0x12345678, 0xbeeffeed, 0x55555555, 0xa5a5a5a5
eol1
resultlist dcd 0x0,0x0,0x0,0x0
eol2
```

END

2.

RCC_AHB2ENR: offset 0x4C

RCC_BASE = 0x40021000.

Therefore RCC_AHB2ENR: $0x40021000 + 0x4c = 0x4002104c$

GPIOB_OSPEEDR (GPIO_OSPEEDR for GPIO B): offset 0x08

GPIOB_BASE = 0x48000400

Therefore GPIOB_OSPEEDR = $0x48000400 + 0x08 = 0x48000408$

TIM_CR1 for Timer 2: offset 0x0

Timer 2 base: 0x40000000

Therefore: TIM_CR1 = $0x40000000 + 0x0 = 0x40000000$

LCD control register (LCD_CR): offset 0x0

Base: 0x40002400

Therefore: LCD_CR = $0x40002400 + 0x0 = 0x40002400$

Resources used:

STM32L476VGT6 Datasheets.pdf

Keil software and lab 3 files

STM32L47xxx, STM32L48xxx, STM32L49xxx and STM32L4Axxx advanced Arm®-based 32-bit MCUs - Reference manual