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SANTA CLARA UNIVERSITY	ECEN 122 Winter 2024	Hoeseok Yang

Homework #8: Memory Hierarchy and Caches

Answer the following problems and upload your answers to Camino in pdf format.

Posted: March 7, 2024, Due by: 9pm on March 13, 2024

1. [2.0 pts] For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache:

Tag	Index	Offset
31-16	15 - 6	5 - 0

A. (0.3 pts) What is the cache block size (in bytes)?

5-0=6, 2^6 bytes (64bytes)

B. (0.3 pts) How many entries (blocks) does this cache have?

15-6=10, 2^{10} = 1024 entries

C. (0.5 pts) What is the ratio of the total bits required for such a cache implementation to the data bits? (Hint: The total bits include all "valid", "tag", and "data" fields.)

data bits $8*1024*64 = 524288$
tag bits $16*1024 = 16384$
valid bits $1*1024 = 1024$

524288+16384+1024 / 524288 = 1.0332
total bits / data bits

D. (0.6 pts) Since reset, the following byte-address cache references are observed. How many cache misses have been observed? (Answer by filling in the table)

First time seeing a specific index results in miss.
If index matches and tag matches, hit. If index matches but tag doesn't, it's a miss w/ replacement

order	Addr (hex)	Tag (bin)	Index (bin)	Offset (bin)	Hit/Miss?
1	deadbeef	1101111010101101	1011111011	101111	miss
2	00c0ffee	0000000011000000	1111111111	101110	miss
3	deadbef6	1101111010101101	1011111011	110110	hit
4	00c07fae	0000000011000000	0111111110	101110	miss
5	00c0ffe0	0000000011000000	1111111111	100000	hit
6	deafbee0	1101111010101111	1011111011	100000	miss
7	00c07fae	0000000011000000	0111111110	101110	miss
8	deafbee4	1101111010101111	1011111011	100100	hit

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1st time hit rate: 33%

E. (0.3 pts) Within the above sequence, how many cache blocks are replaced?

2 cache blocks

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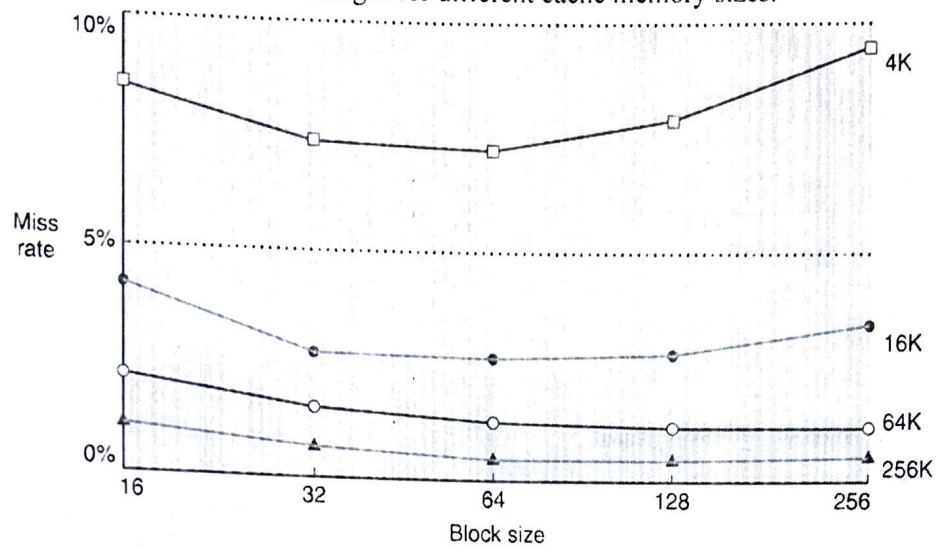
2. [1.0 pts] Below is a chart showing how the cache miss rate of the cache changes as the cache block size changes for different cache memory sizes.



A. (0.5 pts) Briefly explain why the cache miss rate decreases (for all memory sizes) when the block size is changed from 16B to 32B.

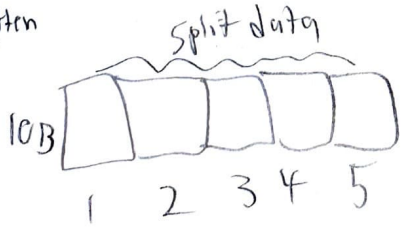
Up to a point, larger block sizes will reduce miss rate b/c they exploit spatial locality more. If the block size starts to become a significant fraction of the cache size however, it will start to increase the miss rate.

B. (0.5 pts) Briefly explain why the cache miss rate increases (for most memory sizes) when the block size is changed from 128B to 256B.

It increases b/c the block size becomes too large relative to the cache size. This is also why the larger cache sizes (64K and 256K) don't increase as much as 16K and 4K.

Ex If any data is changed the whole block has to be rewritten

Whereas here data can be changed and only one block needs to be rewritten which lowers miss rate



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