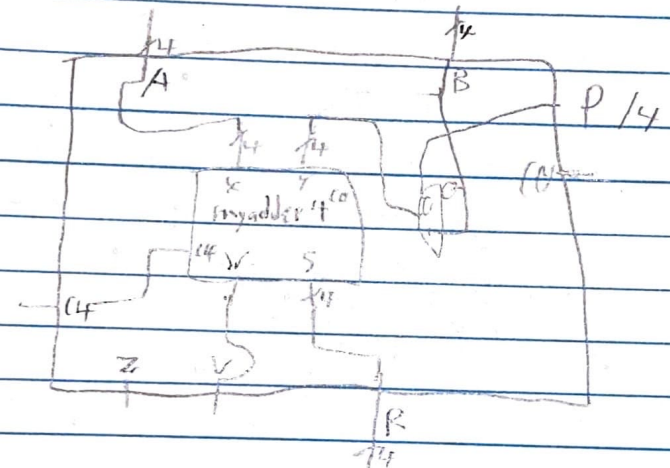


xor: ⊕

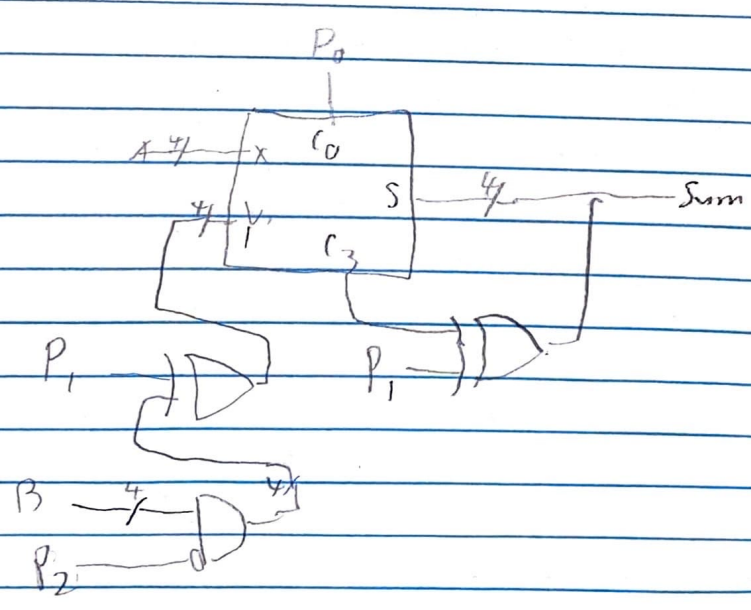
Rylan Thanning

- | | | | | | | | | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|---------|-------|-----------------------------|
| p^3 | p^2 | p^1 | p^0 | a^3 | a^2 | a^1 | a^0 | b^3 | b^2 | b^1 | b^0 | (-in op | notes | |
| 0 | 0 | 0 | 0 | | | | | 0 | 3 | 2 | 1 | 0 | 0 | $R = A + B$ add |
| 0 | 0 | 0 | 1 | | | | | 0 | 3 | 2 | 1 | 0 | 1 | $R = A + B + 1$ odd and inc |
| 0 | 0 | 1 | 0 | | | | | 0 | 3 | 2 | 1 | 0 | 0 | $R = A - B - 1$ sub and dec |
| 0 | 0 | 1 | 1 | | | | | 0 | 3 | 2 | 1 | 0 | 1 | $R = A - B$ sub |

2.



3.



5. p0 controls carry-in, p1 controls sign of B, and p2 controls if B is used at all

4.

```
module alu(p, A, B, CO, R, C4, V, Z);  
    input [3:0] P, A, B;  
    output [4, V, Z];  
    input CO;  
    output [3:0] R;  
    always @(*)  
    if
```

6. Step one! write out code in verilog

Step two! simulate

Step three! upload and test the 8 different possible combos

Step four! finish