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Lab 2 Report

Introduction/Procedure:

We worked on creating a circuit that turns a light on when a switch is pressed or motion is detected. It also has a disable switch which turns off the light when only motion is detected but still allows for it to be turned on with the switch. Lastly, when motion is detected and the light switch is on, an alarm is sounded. Both of our Pre-Lab's contained the same circuit schematic and same truth tables. We started off by setting up Quartus and then by creating our schematic in the software. Next, we had to examine the waveforms and simulate them. Once the simulation was done and there were no errors, we uploaded our circuit to the FPGA. From there we demo-ed our circuit on the FPGA working in real time.

Questions:

In Lab 1, what would you have had to change to use three motion detectors such that any of three different motion detectors could turn on the light and could also turn on the buzzer if the light were already on because the manual switch S was on? Specifically consider the component changes or additions, the wiring changes, and the testing.

Compare that to the changes you would need to make for the Intel FPGA implementation of a logic circuit using three motion detector inputs.

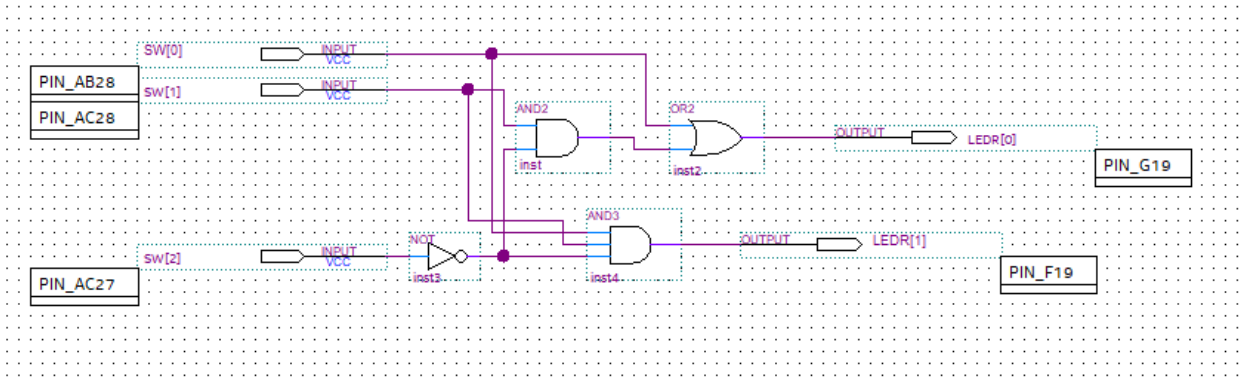
We simply would've had to add an "or" gate and wires connecting the three motion detectors to that "or" gate which would replace SW[1] seen in our circuit schematics. The schematic of the circuit and logic stays the same besides that. For the Intel FPGA, we only have to change the simulation and no physical components which is nice and more efficient.

Conclusion

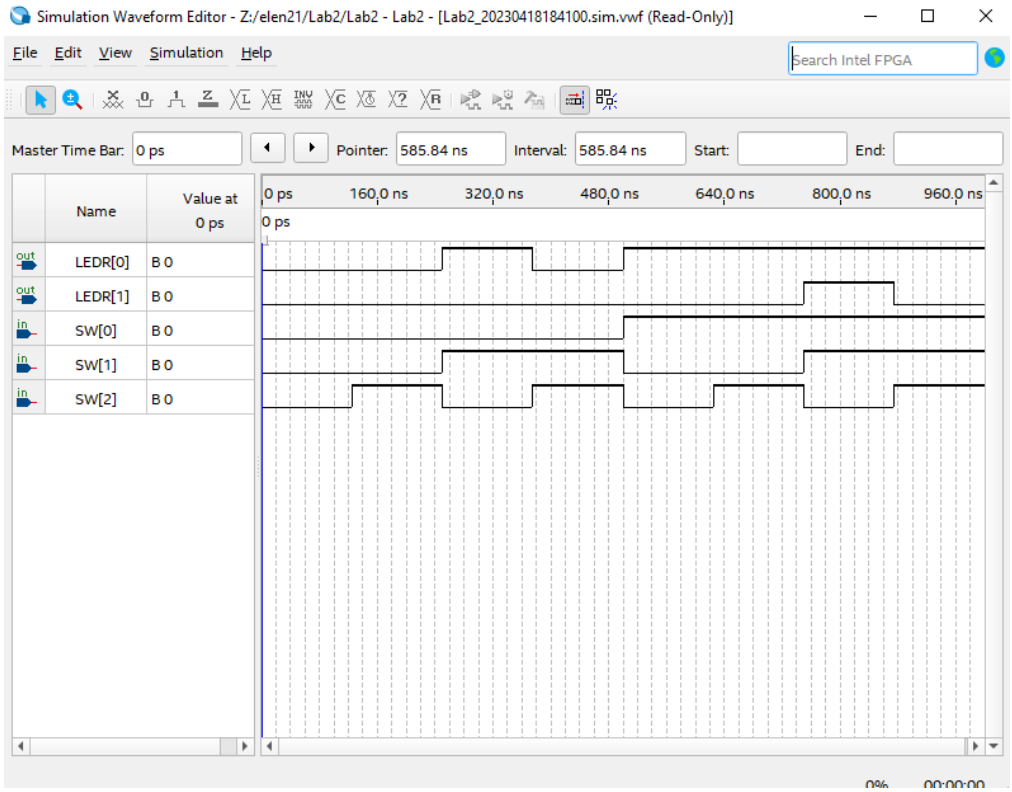
This lab was helpful to get an introduction into using the Quartus software since it was not too intricate. It was also interesting to see how logic circuits can be easily created using software and uploaded onto a chip that works in real life. Lastly, it introduced us to a powerful piece of technology; an FPGA.

Dylan's:

Circuit Schematic (Figure 1)

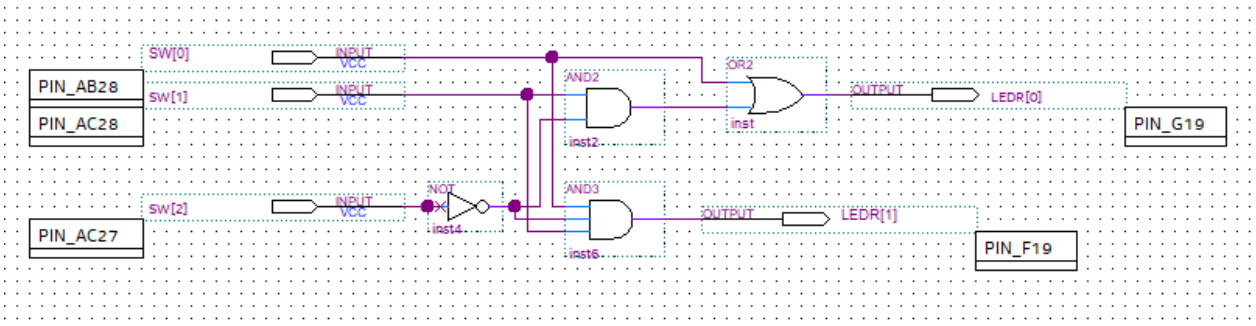


Waveform (Figure 2)

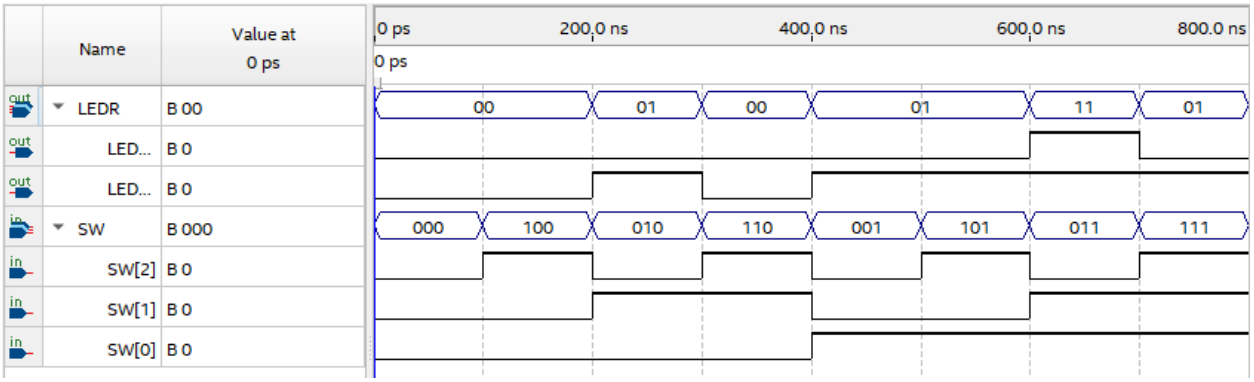


Alan’s:

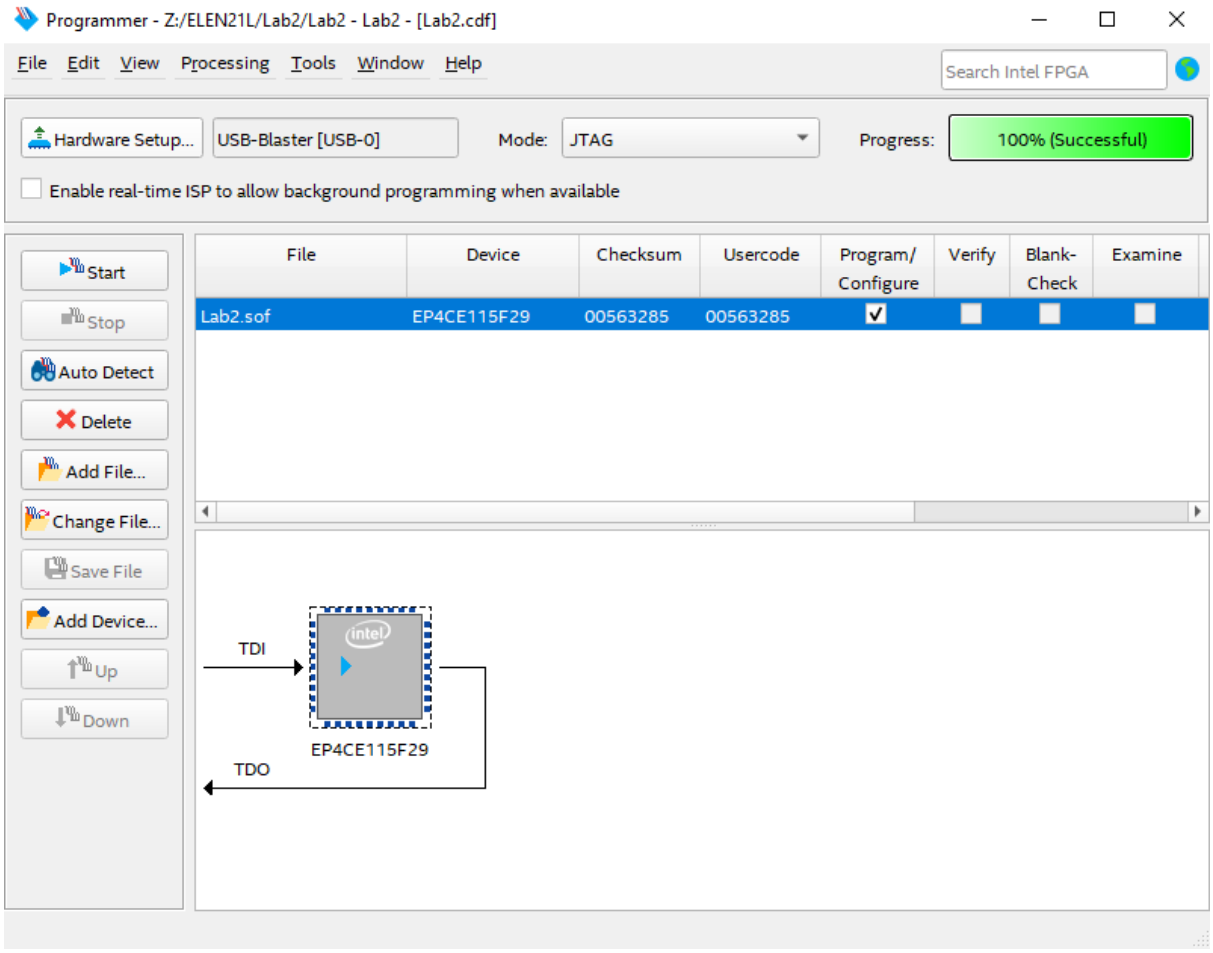
Circuit Schematic (Figure 3)



Waveform (Figure 4)



Successful Download to FPGA (Figure 5)



FPGA Working (Figure 6 and 7)